Plastic Encapsulated Microcircuit (PEM) Guidelines for Screening and Qualification for Space Applications

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PLASTIC ENCAPSULATED MICROCIRCUITS (PEMS)
QUALIFICATION AND SCREENING GUIDELINES

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Applicable Documents

Government Documents

MIL-PRF-38535 : Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883 : Test Methods and Procedures for Microelectronics

Non-Government Publications

Electronic Industries Association (EIA)

JEDEC-22-A101 : Temperature Humidity Bias (THB) Test Method
JEDEC-22-A102 : Autoclave Test Method
JEDEC-22-A104 : Temperature Cycling (TC) Test Method
JEDEC-22-A105 : Power Temperature Cycling (PTC) Test Method
JEDEC-22-A113 : Preconditioning

American Society for Testing and Materials

ASTM, E595 : Test Method for Outgassing
ASTM, F1192 : Test Method for Radiation Hardness for Single Event Effects (SEE)
ASTM, F1269 : Test Methods for Destructive Shear Testing of Ball Bonds

The Institute for Interconnecting and Packaging Electronic Circuits

IPC-SM-786 : Recommended Procedures for Handling of Moisture Sensitive Plastic IC Packages

1. BACKGROUND

Plastic Encapsulated Microcircuits (PEMs) offer advantages of size, weight, cost, and availability. The traditional barrier to their use in highly reliable systems has been their perceived lower reliability in space and aerospace applications. In spite of this perception, the space and aerospace electronics industries have begun to reconsider the use of PEMs due to 1) improvements in reliability of PEMs, as evidenced by their use in the automotive industry; 2) improved methods of accelerated testing and deterministic reliability prediction; 3) awareness that factors other than "part reliability" are more important than previously thought; and 4) concerns that many hermetic part types may not be available for future designs of space systems.

For high-reliability applications, PEMs cannot be implemented in product designs and parts lists simply by replacing military part numbers with their commercial counterparts. The entire system of parts specifications, qualification, screening, and control needs to be modified to accommodate the unique features of PEMs.

2. OBJECTIVE

The objective of these Qualification and Screening Guidelines is to ensure that the PEM devices are procured and tested appropriately to assure reliable performance in space applications.

3. PART SELECTION

Plastic Encapsulated Microcircuits (PEMs) shall be selected for the applicable test level in accordance with the priority order shown in Table 1.This table also indicates screening and qualification testing required for each part designation for different test levels. These part designations are discussed below:

(1) Class N. This part designation includes PEMs procured as "Class N", which have been subjected to and passed all applicable requirements of MIL-PRF-38535 specifications, including qualification testing, screening testing, and TCI/QCI inspections, and are listed in Part I or Part II of QML-38535.

(2) Source Control Drawing (SCD). This part designation includes PEMs which are not available to the other acceptable procurement methods listed for a specific level, and must be procured to a user controlled specification. The SCD shall include the screening and qualification requirements specified in Tables 2, 3 and 4. The testing required by the SCD does not have to be performed by the user.

(3) High Reliability (Hi-Rel). This part designation includes PEMs which are available only to a manufacturer controlled test program as described in the manufacturer's catalog. These parts are controlled only by the manufacturer, who assigns them a special part number and provides a certificate of compliance that they have been tested as advertised. It is the responsibility of the user to assure that the parts meet or

exceed the testing requirements in Tables 2, 3 and 4. If the manufacturer's program does not meet these requirements, then appropriate testing must be performed. There are no approved vendors for Hi-Rel PEMs at this time for space applications.

(4) Commercial Parts. This part designation represents all PEMs which do not conform to any of the part designation categories (1) through (3) above.

4. SCREENING

Defects in PEMs are often attributable to lack of control in material quality and manufacturing processes, and the presence of contamination. Besides product defects due to poor material quality, defects can be different from one manufacturer to another, and from one process to another.

The critical decision of whether or not to screen is influenced by the program test level, quality test level (AOQL), the device category (for example analog or digital devices) and the intended application. Certain screens, for example, static burn-in, are more applicable to analog devices than digital, due to susceptibility of analog circuits to parametric shifts that affect their performance.

Commercial parts do not receive 100% screening or lot acceptance tests as part of the standard flow, except for new products or high-density devices. Instead of 100% screening, suppliers generally use continuous improvement and statistical methods to control quality.

For parts not designated "use as is" in Table 1, screening tests shall be performed on 100% of the flight parts in accordance with Tables 2 and 3. The user is responsible for specifying device unique requirements not specified in Tables 2 and 3. The following MIL-STD-883 tests shall not be performed since die and wire bonds are protected by an epoxy molding compound, and these devices do not have a cavity:

- Seal (Method#1014)
- Constant Acceleration (Method#2001)
- Internal Visual (Method# 2010)
- PIND (Method#2020)

5. QUALIFICATION

The most effective qualification procedure is one which can be used to estimate the reliability of a given part for a variety of different applications. Qualification shall be accomplished by history, similarity, existing test data, or by qualification testing for different part test levels, as indicated in Table 4 and as discussed below. When testing is required, it is indicated in Table 4 by a quantity (accept number) or LTPD, and shall always be lot specific. MIL-STD-883 shall be followed to

the maximum extent possible. The following MIL-STD-883 tests are not applicable to PEMs for space application:

- Salt Atmosphere (Method#1009)
- Internal Water Vapor Content (Method#1018)

5.1 Qualification by History

A part type can be considered qualified if it has previously been successfully used in: (a) applications identical to those proposed, or (b) applications different from those proposed, if the applications, including derating and environmental conditions, are fully documented and are more severe than the proposed application. The part must be similar to those previously used, as defined in section 5.2. The part must have been used in two or more missions consisting of three years minimum operating time in orbit. The part must have been built by the same manufacturer in the same facility to an equivalent specification. It is the responsibility of the user to have such evidence and to present it to the approving activity upon request.

5.2 Qualification by Similarity

A part can be considered qualified if it is similar to a part for which detailed qualification test (QCI) data exist, and these test data (a) satisfy the requirements specified herein for the part test level, and (b) are less than 1 year old. In order to be considered similar, the parts shall be made by the same manufacturer, with the same technology, belong to the same die family as defined in Appendix A of MIL-I-38535, and made on the same manufacturing line, or on a line with only minor differences which are understood, documented, and shown to represent no increased reliability risk. In addition, a part meeting these criteria can only be qualified by similarity to a part with a more complex mask set, such as more gates or transistors.

Similarity criteria for Package Qualification

A device package may be qualified by similarity to one that was formerly tested and qualified provided that all of the following conditions apply:

(1) Both parts are supplied by the same manufacturer,

(2) Both parts are supplied in the same package type (e.g., SO, SOL, PLCC, DIP) and have the same pin count. Devices with differing pin counts may be qualified by similarity provided that either (a) for small pin-count packages such as DIP, SOIC and PLCC, the difference in the packages' top surface areas must be no greater than 25%, or (b) for large packages such as PQFP, the difference in die area must be no greater than 40%,

(3) Both parts are produced using the same fabrication process, where a fabrication process is defined as a specific device technology, such as ACMOS, HCMOS, and Schottky,

(4) The plastic molding compound used for both devices is the same,

(5) Both parts have the same basic lead frame and material design,

(6) Both parts have the same passivation, die coating, and external lead finish.

5.3 Qualification by Existing Test Data

Parts can be considered qualified by existing test data of the following types:

(a) Lot Specific Data : Lot specific data imply that the flight parts have the same lot date code as the qualification samples. Lot specific data are always acceptable in place of qualification testing when it meets the requirements specified in Table 4.

(b) Generic Data : Generic data should be based on the same device type, manufactured by the same process, and should include all characteristics of the device. Sources of generic data should come from supplier-certified test labs, and can include internal supplier's qualifications, user-specific qualifications and supplier's in-process monitors. The generic data to be submitted must meet or exceed the test conditions specified in Table 4. End-point test temperatures must meet the worst case temperature extremes and designed product life for the application of the user requesting the qualification on at least one lot. The user(s) will be the final authority on the acceptance of generic data in lieu of test data.

(c) Catalog Data : Catalog data are defined as test data that are controlled only by the part manufacturer, or other test data not controlled by the user. Generally, any generic test data not conforming to the above can be considered catalog data. For a test level 1 or test level 2 program, use of catalog data is not allowed. For test level 3 programs, the user is responsible for assuring that the data represent the true assessment of the reliability of the proposed part, and that no process changes which may adversely affect the reliability of the parts have occurred between the time the data were obtained and the time the proposed parts were processed.

5.4 Qualification Testing

A part is considered to be qualified if it passes the appropriate qualification tests specified in Table 4, either by performing the test (acceptance of zero failures using the specified minimum sample size) or by demonstrating acceptable generic data. Any unique reliability tests, or conditions requested by the user and not specified in this document, shall be negotiated between the supplier and user requesting the test. Passing the acceptance criteria of all the tests and conditions of Table 4 constitutes qualification to the appropriate test level. When the number of failures for any given test in Table 4 exceeds the acceptance criteria, the device shall not be qualified until the root

cause of the failure is determined and the corrective and preventive actions are confirmed to be effective. New samples or data may be requested to verify the above.

5.4.1 **Qualification of Die**

Tests defined in Table 4 with letter D shall be performed.

5.4.2 Qualification of Packaging

Tests defined in Table 4 with letter P shall be performed.

5.4.3 Qualification of a New Device

The test requirements and conditions for a new part qualification are listed in Table 4. For each qualification, the supplier must present data for all of these tests, whether the data are from actual flight lot tests or are acceptable generic data. Justification for the use of generic data, whenever they are used, must be demonstrated by the supplier and approved by the user and, ultimately, the NASA acquiring activity. A review should be made of other parts in the same generic family to ensure that there are no common failure mechanisms in that family.

5.4.4 Test Samples

Test samples shall consist of representative devices from the qualification family. Where multiple lot testing is required, test samples as indicated in Table 4 must consist of approximately equal numbers from three non-consecutive wafer lots, assembled in three non-consecutive molding lots.

Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 4. If the supplier elects to submit generic data for qualification, the specific test conditions and results must be reported.

All parts to be qualified shall be produced by the same tooling and processes at the same manufacturing site that will supply part deliveries at the projected production volumes.

5.4.5 Alternative Testing Requirements

Any deviation from the test requirements and conditions listed in Table 4 must be approved by the user by presenting supporting data from the supplier, demonstrating equivalency. These deviations shall be clearly reported when the results of the qualification are submitted to the NASA acquiring activity for approval.

5.4.6 Qualification of Molding Compound (Optional)

Qualification of the molding compound is provided in Table 5 as an option, since those typical values and/or limits depend on the user's unique intended application. Only test level 1 and test level 2 parts are subjected to this qualification.

5.5 Requalification

Requalification of a device will be required when the supplier makes a change to the product and/or process that impacts the form, fit, function, quality and/or reliability of the device.

In the event that a manufacturer implements a major change in a part (as identified in Tables 6 and 7), a requalification shall be performed. The specific test shall be performed if the designation "Yes" is indicated. The use of equivalent manufacturer data is an acceptable method to meet the die qualification requirement.

All devices using the same process and materials are to be categorized in the same qualification family for that process and are qualified by association when one family member successfully completes qualification, with the exception of part-specific requirements.

5.5.1 Changes Requiring Requalification

As a minimum, any change to the product requires performing the tests listed in Tables 6 and 7 as applicable. Tables 6 and 7 shall be used as guides for determining which tests need to be performed, or whether equivalent generic data can be submitted for that test. An agreement between the supplier and the user, including justifications for performing or not performing any recommended tests shall be made before a requalification plan is implemented.

5.6 Test Failure Criteria

Test failures are defined as devices not meeting the individual device specification, criteria specific to the test, or the specifications in the supplier's data sheet. Any device that shows external physical damage attributable to the environmental test is also considered a failed device. If the cause of failure is agreed to be due to mishandling or ESD, the failure shall be discounted, but reported as part of the data submission.

5.7 Subsequent Device Qualification Selection Criteria

Prior qualification data obtained from a part in a specific family may be extended to the qualification of subsequent devices in that family if the following requirements are met.

5.7.1 Fabrication (Fab) Process

Each process technology (e.g., CMOS, NMOS, Bipolar, etc.) must be considered and qualified separately. No matter how similar, processes data from one fundamental fab technology cannot be used for the other. For BiCMOS devices, data must be taken from the appropriate technology based on the device under consideration.

Family requalification with the appropriate tests is required when one or more processing steps or materials are changed. The important attributes defining a qualification family are listed below:

a) Wafer Fab Technology (e.g., CMOS, NMOS, Bipolar, etc.)

b) Wafer Fab Process - consisting of the elements listed below:
   - Circuit element feature size (e.g., layout design rules, die shrinks, contact gates, isolations)
   - Substrate (e.g., orientation, doping, epi, wafer size)

- Number of masks
- Lithographic process (e.g., contact vs. projection, E-beam vs. X-ray, photoresist polarity)
- Doping process (e.g., diffusion vs. ion implantation)
- Gate structure, material and process (e.g., polysilicon, metal, silicide, wet vs. dry etch)
- Polysilicon material, thickness range and number of levels
- Oxidation process and thickness range (for gate and filed oxides)
- Interlayer dielectric material and thickness range
- Metallization material, thickness range and number of levels
- Passivation material and thickness range
- Die backside preparation process and metallization.

c) Wafer Fab Site

5.7.2 Assembly Process

The processes for each PEM package technologies must be considered and qualified separately. For devices to be categorized in a qualification family, they all must share the same major process and material elements as defined below. Family requalification, with the appropriate tests, are required when the process or a material is changed. The supplier must submit technical justification to support the acceptance of generic data with pin counts, die sizes, paddle sizes and die aspect ratios different than the device to be qualified.

The important attributes defining a qualification family are listed below:

a) Package Type (e.g., DIP, SOIC, PLCC, QFP, PGA)
   - Same cross-sectional dimensions (width x height).
   - Range of paddle (flag) size (maximum and minimum dimensions) qualified for the die size/aspect ratio under consideration.

b) Assembly Process consists of the attributes listed below:
   - Leadframe base material
   - Leadframe plating (internal and external to the package)
   - Die attach material
   - Wire bond material, wire diameter, and process
   - Plastic mold compound or ceramic package material

c) Assembly site

6. GUIDANCE FOR SELECTION AND APPLICATION OF PEMS

6.1 Characteristics of PEMs

1) PEMs are not suitable in certain applications. Every application should be analyzed prior to using PEMs. Particular PEM environmental concerns are the following:

   a) Outgassing
      - Outgassing materials can degrade sensors
      - NASA specifications for outgassing:
        - Maximum Total Mass Loss (TML) of 1 %
        - Maximum Collected Volatile Condensable Materials (CVCM) of 0.1 %
      - Use NASA published data base; NASA reference publication 1124, revision 3, "Outgassing Data for Selecting Spacecraft Materials"
      - Epoxy novalacs, as a group, typically meet the NASA outgassing requirements, but various molding compound formulations contain proprietary additives, and should be checked.

   b) Temperature limits
      - PEMs typically have a narrower operating temperature range (0°C to 70°C for commercial devices). Temperature limits in operation or storage can be a problem.
      - When military temperature range (-55°C to 125°C) parts are not available, then select industrial temperature range (-40°C to 85°C) parts, as most suppliers offer parts in this range.
      - Use suppliers' data or actual test data to establish capability of parts to meet performance parameters at extended temperatures, beyond the specified operating temperature range by the manufacturer .

   c) Thermal cycling
      - Thermal cycling induces cyclic mechanical stress eventually leading to delaminations and cracking of the molding compound. Pathways for rapid moisture and chemical ingress are thereby created.

   d) Radiation
      - Cosmic and trapped radiation
      - When preconditioned in certain environments (such as burn-in), the non-hermetic characteristic of PEMs may lead to a different radiation response from that of hermetic devices.
      - Commercial suppliers generally do not understand the effects of space radiation and have not characterized their processes regarding the test level of tolerance to either total ionizing dose or single event effects. Process changes are made frequently (every three to four years). and sometimes even less than one year, depending on the advances in technology. Process changes made to improve yield may have negative effects on radiation tolerance and single event susceptibility. Smaller feature size, higher density and lower logic levels all work against radiation tolerance.

   e) Moisture absorption and chemical ingress

- Popcorning during reflow surface-mount soldering can be managed with proper precautions. (See IPC-SM-786)
- Larger and thinner packages are more susceptible to popcorning, because the capacity of the molding compound to withstand stresses developed due to CTE mismatches and vaporizing moisture is reduced. These packages require special handling. Mechanical stresses, such as vibration and mechanical shock can also cause damage to such devices.

2) Plastic has higher thermal impedance, therefore, PEMs require stricter time and temperature control during soldering, and cannot withstand prolonged, high temperatures >230°C. Check material properties to ensure consistency with application, e.g., T_g>175°C for high-temperature applications.

3) PEMs should not be used in long-term high-humidity environments, or harsh chemical environments, especially where high voltages or high temperatures are encountered.

4) Do not use aggressive-halide-base fluxes during PEM soldering/assembly/repair.

5) MIL-HDBK-217 cannot be used for reliability modeling of PEMs because:
   - Reliability models are based on activation energies, not failure mechanisms.
   - It does not adequately assess feature size and element density.
   - It assigns "points" for adding screening tests, i.e. the more the screening tests, the lower the failure rate.

   The Quality Factor (PIQ) of 10 assigned to PEMs in MIL-HDBK-217 is subjective and there is no data to substantiate it.

6) Utilize the manufacturers' published data to establish FIT rate. Millions of device hours are accumulated during internal qualifications and outgoing reliability audit testing. Data is published in quarterly reports and is available directly from the manufacturer.

7) Do not use high stress-mold compounds with large chips (>250 mils/side).

8) In microcircuits, the exposed and corrodable aluminum present at the bonding pads represents over 95 percent of the aluminum present on the chip. In a PEM, this corrodable aluminum is only protected by the moisture-permeable plastic. As microcircuits become denser and operate at higher frequencies, moisture and corrosion becomes more of an issue. Some plastic-encapsulated high-frequency clock chips are not stable until they have been powered up for as much as two weeks. This frequency instability is due to moisture being driven from the encapsulating plastic. When the system powers down, the plastic reabsorbs the moisture. This is the big concern for long-term dormant storage which can be more severe than many forms of laboratory life testing at elevated temperatures.

6.2 Suppliers/Distributors

1) Commercial PEM suppliers have a tiered level of service tied to sales volume of individual customers; i.e., the bigger the buyer, the more attention you get. Smaller volume requirements are serviced through distributors and the level of support varies, depending on distributors. Most spacecraft builders are small volume buyers; hence, they will have to use distributors.

2) Distribution should be evaluated for ESD precaution, handling, storage and shipping. Distributors can play a vital role in after-sale service and in obtaining reliability information. Users can benefit in several ways by buying from distributors:
    - cost effective for small volume buyers
    - warranty and technical support

6.3 Packing and Storage Conditions

1) PEMs require dry-bag packing with desiccant, and special controlled storage conditions (moisture barrier bags). Bake-out moisture-sensitive PEMs and seal them in moisture-proof bags. Assemble devices before critical levels of moisture are exceeded per industry specification (IPC-SM-786 and JEDEC-STD-113). Rebake and reseal in bags with fresh desiccant if necessary and always store in nitrogen cabinets.
2) Surface mount devices should be stored at Temperature <30°C and Relative Humidity < 55%.
3) The chemical components of epoxy molding compounds (EMCs) are subject to the laws of chemistry. The chemical components react to their manufacturing and use environment and also degrade with time. EMC life degradation is accelerated in uncontrolled environments, or long-term dormant storage (Refer to IPC-SM-786 guidelines for storage).
4) Special attention is needed for the long-term storage of PEMs so far as concerns solderability, vulnerability to corrosion and delamination.

6.4 Shipping and Handling

1) Shipping exposes the parts to moisture and temperature changes. Humidity cards, desiccants, moisture barrier bags, dry packs, rough handling packing systems should be specified in order to prevent moisture ingress during shipping and handling.

7. DESTRUCTIVE PHYSICAL ANALYSIS PROCEDURE FOR PEMS

7.1 External Visual Examination.

Inspect each sample at 3X to 10X magnification. One photograph of one typical device showing all marking shall be taken. Failure criteria of MIL-STD-883D, Method 2009, “External visual” are applicable except paragraphs 3.3.1.b, 3.3.2.a, 3.3.3, 3.3.4, 3.3.5.e, 3.3.5.g, 3.3.6.b, 3.3.7, 3.3.8. Additionally, look for the following defects:

- package nonplanarity, warping, or bowing,
- foreign inclusions in the package, voids and cracks in the plastic encapsulant
- deformed leads.

7.2 X-ray Examination

The purpose of this examination is to find the die and wire placement for future decapsulation and to detect internal defects of the package. Look for the following defects:

- foreign objects, voids, and filler conglomerates in the encapsulant,
- voids in the die attach material,
- misaligned leads,
- burrs on lead frame (inside the package),
- poor wire bond geometry (wires that deviate from a straight line from bond to external lead or have no arc and make a straight line run from die bonding pad to lead),
- swept or broken wires,
- improper die placement.

Radiographs shall be taken of each device in two views 90 degrees apart (top and side views). MIL-STD-883D, Method 2012, "Radiography" is applicable; using an X-ray inspection system "TORREX 150D", the regimen 125 kV at current 3 mA and 30 seconds of exposure gives good results in the most cases.

7.3 Acoustic Microscopy

All samples shall be subjected to the acoustic micro imaging analysis. The purpose of this examination is to nondestructively detect the following defects:

- delamination of the molding compound from the lead frame, die, or paddle;
- voids and cracks in molding compound;
- unbonded regions and voids in the die-attach material (if possible).

The apparatus and materials for this test shall include:

1. An ultrasonic imaging equipment based on reflection (pulse echo) technology in which a single focused acoustic lens mechanically scans a tiny dot of ultrasound (in frequency range of 10 to 150 MHz) through the sample. A reflection is generated at each interface and returned to the sending transducer for processing and image generating. Signal processing shall allow information to be gathered from multiple levels within the sample. A C-Mode Scanning Acoustic Microscope (C-SAM) can be used for this purpose.
2. Deionized water shall be used as a medium fluid to provide acoustic coupling between the sample and the transducer.

7.3.1 Examination Sites

Examination of the package for voids, cracks, and delaminations shall be performed on each sample at six areas:

1. interface between the die and molding compound;
2. interface between the lead frame and molding compound (top view);
3. interface between the paddle periphery and molding compound (top view);
4. die-to-paddle attachment interface (if possible);

5. interface between the paddle and molding compound (back view);
6. interface between the lead frame and molding compound (back view).

NOTE

- Combined C-mode scans can be performed to investigate more than one area during one scanning run.
- Die-attach inspection shall be performed per MIL-STD 883D, Method 2030, "Ultrasonic inspection of die attach" for the parts with the die mounted onto a substrate or heat sink. This standard can also be applicable for other package types provided the resolution is adequate to detect voids in the attachment material.

Procedure

Package surface roughness, mold marks, labels and surface defects create additional ultrasonic wave reflections and hinder analysis results. Packages with nonflat shapes may require milling or grinding before analysis.

- Remove labels from the area to be scanned. Note all mold marks or defects, which may have affected the scan results. Flatten the surface using a grinding/polishing and wet the surface with alcohol if necessary.
- Place sample in the holder in deionized water with the upper surface parallel to the scanning plane of the acoustic transducer. Sweep air bubbles away from the unit surface and from the bottom of the transducer head.
- Set the focus by maximizing the amplitude of the reflection from the die-molding compound interface and perform acoustic scanning.
- If the lead frame-molding compound interface was not in focus, reset the focus and perform scanning of this interface.
- Refocus the transducer to the periphery of the paddle-molding compound interface and perform acoustic scanning.
- Refocus the transducer to the die attachment (if possible) and perform acoustic scanning. If the image is not sharp enough, try to view the area from the back side of the part.
- Turn the part over, sweep air bubbles away from the unit, focus the transducer to the back side of the die paddle, and perform acoustic scanning.
- Refocus the transducer to the lead frame-molding compound interface and perform acoustic scanning.

7.3.2 Evaluation criteria

In the device examination, the following aspects shall be considered as unacceptable and devices which exhibit any of the following defects shall be rejected:

1. Cracks in plastic package intersecting bond wires.
2. Internal cracks extending from any lead finger to any other internal feature (lead finger, chip, die attach paddle) if crack length is more than a half of the corresponding distance.
3. Any crack in the package breaking the surface.
4. Any void in molding compound crossing wire bond.
5. Any measurable amount of delamination between plastic and die.
6. Delamination of more than half of the backside or top peripheral area of the interface between the paddle and plastic.

7. Complete leadfinger delamination from the plastic (either top or backside).
8. Delamination of the top tie bar area for more than half of its length.

NOTE
If rejectable internal cracks or delaminations are suspected, a polished cross section may be required to verify the suspected site.

7.4 Die Penetrant/Cross-Sectioning Test.

Two devices, or 40% of the DPA samples, whichever is larger, shall be subjected to this examination. The purposes of this test are as follows:

- to inspect wire bonding (to the die and lead frame);
- to examine die attachment for voiding and cracks;
- to characterize integrity of molding compound;
- to ensure that there is no direct way (along the leads) for moisture and contamination to reach the die.

7.4.1 Procedure

Die penetrant test shall be performed per MIL-STD-883D, Method 1034, with the following deviations:

1. Any appropriate microscope with ultraviolet illumination can be used.
2. All samples shall be examined under ultraviolet illumination after the die penetrant hardening before cross-sectioning using low power microscope (10X - 40X). Look for external cracks in sites other than the lead-plastic interface where some separation between the lead and the package is possible.
3. Half of the samples shall be sectioned along one side and half along the other side of the package in three planes (minimum). The planes shall cross the package along the leads (approximately in the middle) in vicinity of the paddle edge, approximately in the middle of the die, and in vicinity of the other paddle edge. Parts with the paddle tie bars shall be sectioned along the bars. At least three planes shall cross the wire bond to the die and to the lead. If suitable, a sample can be sawed in two parts before potting.

7.4.2 Evaluation Criteria

The following defects shall be rejected.

1. Package cracks and delaminations;
   - any evidence of die penetration to the die or the paddle;
   - any evidence of external cracks other than between the lead and plastic;
   - any evidence of die penetration of more than 2/3 of the lead length;
   - any evidence of die penetration of more than half of the tie bar length.
2. Bonding:
   - lifted and shifted bonds;
   - intermetallic compound formation in areas of reliability concern.
3. Die attach: voiding of more than 50%.
4. Molding compound:
   - foreign intrusions;

- voids in vicinity of bonding wires.

7.5 Decapsulation

The purpose of this section is to provide guidelines for possible decapsulation methods for failure analysis (FA) and destructive physical analysis (DPA) of plastic encapsulated semiconductor devices. It is also intended to characterize advantages and disadvantages, and indicate possible pitfalls.

7.5.1 Preliminary Steps

X-ray analysis should be performed before decapsulation to learn die shape, placement and size; and to determine the height of the bond wires. This information will assist in choosing the correct mask or gasket and/or depth of the trench to be milled in the package surface.

The samples should be baked before wet decapsulation. This step is intended to remove all moisture from the package so that damage will not occur due to acidic corrosion of the metallization.

CAUTIONS

- Results of subsequent examinations depend heavily on decapsulation quality. Detailed records about decapsulation process irregularities and possible artifacts should be maintained.
- Do not expose wire bonds at the lead frame when using wet etching techniques. These bonds are frequently made to silver plated areas and chemical etchants will quickly degrade them.

7.5.2 Milling

This step is not necessary but is often useful for Manual Wet etching and Plasma etching. Milling prevents the leads from breaking off by ensuring that the chip surface is exposed before the lead frame, and reduces the time required for etching.

Any suitable milling machine is acceptable; use of a dental drill to create a small impression is possible but not preferable because a flat surface would not result. The procedure is as follows;

1. Using X-ray data, calculate the depth of the trench to be milled.
2. Install the part into the fixture of a milling machine. The surface being worked should be parallel with the milling plane.
3. Start milling, moving the mill tip down to the calculated depth. Mill the trench slightly longer and wider than the die.

To ensure that the bond wires remain intact during milling, it is recommended that approximately 0.2 mm of plastic be allowed to remain covering them.

7.5.3 Suggested Techniques

7.5.3.1 Manual Wet Etching

Advantage: A quick result is possible with readily available equipment. Disadvantage: Removal of contamination from the surface of the die preventing chemical analysis; the method requires very careful attention to safety.

Apparatus and materials

- A heating plate, metal block, beaker, aluminum weighing dish, and disposable dropper.
- Red fuming nitric or sulfuric acid can be used as etchants. Acetone, isopropanol, or methanol can be used for rinsing.

Notices

- Red fuming nitric acid can be used in most cases. Sulfuric acid can be used as a solvent specific to anhydride epoxies.
- Red fuming nitric acid has little effect on plastic at room temperature, but elevating the temperature to approximately 100°C will cause it to decapsulate a device in few minutes. Higher temperatures will only decompose the acid. When heated in an open beaker, the acid will evaporate NO_2 and absorb moisture with time, thus becoming diluted and converted into yellow nitric acid. Dilute (yellow) nitric acid is not suitable for decapsulation purposes because it reacts with the metal in the devices.
- To have an effect on epoxy, sulfuric acid must be heated to about 150°C. Use deionized water for rinsing.

Procedure

1. Mill a trench or create a small impression, according to section 7.5.2.
2. Make a mask using aluminum foil adhesive tape shielding the specific areas not to be etched.
3. Install the part on a metal (copper or aluminum) block to provide heat directly to the bottom of the device. Then place it in an aluminum weighing dish on a plate heated to approximately 90°C and wait several minutes to allow the package to heat up.
4. Pour a small quantity of red fuming nitric acid into a beaker and apply several drops to the device with the dropper.
5. Cleanup: rinse with cold nitric acid for a few seconds, rinse in a spray of acetone, then in isopropanol or ultrasonically clean in methanol. Blow with dry air.
6. Repeat steps 3-5 until the die is exposed.
7. If necessary, perform a plasma cleanup with a 10:1 mixture of 0_2:CF_4 in a barrel plasma (50W, 30-60 min.).

Cautions

- It is very important to keep the part hot and the exposure time very short for reaction with acid.
- There are safety hazards with this process. All safety procedures should be invoked.

7.5.3.2 Wet Chemical Jet Etching

This method eliminates some safety problems inherent to Method I and provides quick, clean, and localized removal of encapsulant in the die area, usually with no damage to the part.

Apparatus and materials

- Jet etcher (e.g., B&G decapsulator, model 250).
- Red fuming nitric or sulfuric acid, acetone, isopropanol.

Notices

- Red fuming nitric acid can be used in most cases. Sulfuric acid can be used as a solvent specific to anhydride epoxies.
- Red fuming nitric acid has little effect on plastic at room temperature, but elevating the temperature to approximately 100°C will cause it to decapsulate a device in few minutes. Higher temperatures will only decompose the acid. When heated in an open beaker, the acid will evaporate NO_2 and absorb moisture with time, thus becoming diluted and converted into yellow nitric acid. Dilute (yellow) nitric acid is not suitable for decapsulation purposes because it reacts with the metal in the devices.
- To have an effect on epoxy, sulfuric acid must be heated to about 150°C. Use deionized water for rinsing.
- Decapsulation of the first part may require from 3 to 6 steps followed by low power optical examination. After the process regimen is readjusted, decapsulation can be done in one - two steps (three - five minutes).

Procedure

1. Choose a gasket according to the die size, calculated by X-ray data.
2. Adjust the part and the gasket onto the fixture.
3. Set parameters of the process (etching temperature, etching time, and volume of etching acid) using manufacturer's data and experience and perform decapsulation.
4. Rinse the part in acetone and then in isopropanol after each step of etching. Blow with dry air.
5. If necessary, perform a plasma cleanup with a 10:1 mixture of 0_2:CF_4 in a barrel plasma (50W, 30-60 min.)

Caution

Decapsulation of thick packages with relatively small surface areas (like DIP-8) may result in a cavity wall depression which halts the etching process. To avoid this, use gaskets of a lesser size.

7.5.3.3 Plasma etching

Plasma etching has very high selectivity (the technique minimizes etching of the die metals and lead frame). Safety and contamination problems of wet chemical processes are avoided. Plasma treatment is a gentle process compared to wet etching and sometimes makes it possible to expose bonds at both ends of the wires. The disadvantage is that significantly more time is required.

Apparatus and materials

- A non reactive ion etching mode plasma system should be used, for example, Plasma GIGA-ETCH 100-E system (Technics Plasma GmbH). In this system the plastic molding compound is removed from the device automatically and up to 12 devices can be treated simultaneously. The filler material (quartz powder) is automatically blown from the surface with brief blasts of compressed air in time intervals of several minutes.
- Deprocessing is performed at approximately 0.5 - 1 mbar pressure of the gas mixture O_2:CF_4 (80:20).

Note
The process time varies typically between 5 and 15 hours depending upon the type of the device and the trench depth.

Procedure
1. Mill a trench according to section 7.5.2.
2. If necessary, cover the package with an aluminum foil mask so only the area to be etched is exposed to the plasma.
3. Adjust and secure samples under the blow nozzles and start the process.

Caution
Oxygen/freon plasma (mostly used for deprocessing) does not affect Al and Au, but can attack other metals and glassivation (especially Si_3N_4).

7.6 Internal Visual Inspection

All decapsulated samples shall be subjected to this examination.

The purpose of this test is to verify that the quality of the performed decapsulation is adequate for further analysis, to examine decapsulated device for visual defects, and to identify those damaged by decapsulation.

The device shall be examined microscopically first at a low power (30X to 60X) magnification and then at a high power magnification (75X to 200X) to determine the existence of defects as described in 7.6.1 and 7.6.2. All failures from 7.6.1 should be analyzed to confirm that the failure mechanism occurrence is due to the decapsulation technique.

7.6.1 Verification of the decapsulation quality

a. Confirm acceptance of the specimen for further bonding examination. At least 25%, or 3 wire bonds, whichever is more, should meet the following criteria: be clean, have no damage, and be exposed more than approximately 2/3 of their length.
b. Confirm acceptance of the specimen for further glassivation integrity and SEM examinations. At least 75% of the die area should be clean and have no damage caused by deprocessing.
c. Record any artifacts which may have affected the DPA results.

7.6.2 Criteria

Evaluation criteria per MIL-STD-883D, Method 2013, "Internal visual inspection for DPA" are applicable. Additionally, no device shall be acceptable that exhibits the following defects:

- Foreign intrusions in exposed plastic material.
- Glassivation pinholes, peeling or cracks (in particular those specific to filler particle-induced damage).
- Metallization voids, corrosion, peeling, or lifting.

7.7 Glassivation Layer Integrity

One sample, or 20% of the lot, whichever is larger, which met the requirements per 7.6.1.b. shall be subjected to a glassivation layer integrity test.

This examination shall be performed per MIL-STD-883D, Method 2021, "Glassivation layer integrity.

7.8 Bond Pull Test

Each sample which met the requirements per 7.6.1.a. shall be subjected to a destructive bond pull test.

The wire bonds shall be pulled to destruction according to MIL-STD-883, Method 2011, "Bond strength (destructive bond pull test)", Condition D.

Note

- According to the procedure of MIL-STD-883, Method 2011, the pull is applied by inserting a hook under the wire approximately in the center of the loop. Normally, decapsulation exposes approximately 75% of the loop (exposure of the wire-to-lead bond would weaken the bond strength due to chemical attack). The wire tension in which the pull force is not applied in the middle of the loop and part of the loop is buried in plastic may differ (up to two times) from the case described in MIL-STD-883. This means that the rejection criteria per MIL-STD-883, Method 2011 may be not applicable.
- Typically, the ball neck is the weakest site of a wire bond (in particular, because it has been annealed during ball formation). If another site of the wire bond is found to be broken, the site could indicate a problem (especially in the case of the ball-lift).
- A wire bond strength test may be greatly influenced by the history of the sample. Thermocycling or storage of the sample under high temperature and humidity environments can cause deterioration of the wire bond strength. Enhanced degradation of the intermetallic region of the gold wire-aluminum bonding pad interface occurs in the presence of some flame retardants in epoxy molding compounds (such as those containing bromine or antimony). In some cases, to ensure an adequate quality of the part and its long term reliability, different types of accelerated tests are recommended before the sample is subjected to the wire pull test.

Data records. Results of the bond pull test shall be recorded in the DPA history records.

7.9 Scanning Electron Microscope (SEM) Examination

All samples, except those which were subjected to glassivation integrity examination, which met the requirements per 7.6.1.b. shall be subjected to this test.

In most cases the PEM manufacturer does not use military specifications in the wafer or die fabrication. Thus, this examination should be regarded as a major test for die compliance to high reliability requirements.

The purpose of this examination is to evaluate quality of the wire bonding, glassivation integrity, and acceptability of the die interconnect metallization.
Half of the samples shall undergo SEM inspection for bonding, glassivation and metallization quality. The other shall be subjected to a SEM examination followed by cross-sectioning.

1. Samples intended for wire bonding and glassivation integrity evaluation shall be covered with a thin (approximately 100Å) gold film for the following SEM examination.
2. Glassivation shall be examined for delamination, pinholes, and cracks.
3. Wire-to-die bonding shall be examined for the following defects:
   - cratering of the bond pad on the die*;
   - bond liftoff*;
   - wirebonds which are sheared from the die pads*;
   - intermetallic compounds visible more than 0.1 mil beyond the ball attachment periphery.

   * only wires which were not subjected to the bond pull test.

4. Cross-sectioning. Samples intended for cross-sectioning shall be separated from the plastic package.
5. Die separation. The die can be removed from the package in two ways:
   - by etching away the paddle;
   - by removing most of the molding compound around the paddle followed by heating the part to a temperature above the eutectic, or solder melting point.
6. The subsequent examination shall be performed in accordance with MIL-STD-883, Method 2018.

It is important to remove all polymer residues from the die before cross sectioning. Otherwise, the acid absorbed in the polymer remnants would mix with deionized water (during polishing) and cause corrosion of the aluminum metallization.

Evaluation criteria

No device with defects mentioned above shall be accepted. The acceptability of the die interconnect metallization shall be evaluated in accordance with MIL-STD-883, Method 2018.

Table 1. Plastic Encapsulated Microcircuit Requirements

(Note: ✓ indicates the tests to be performed)

Part Designation / Requirements	Test Level 1		Test Level 2			Test Level 3		
	Class N	**SCD**	**Class N**	**HI-REL 6/**	**Commercial**	**Class N**	**HI-REL 6/**	**Commercial**
USE AS IF								
1/ Screening data is	on file	on file	on file	on file	on file	on file	on file	on file
or 2/ AOQL failure rate is	≤ 0.05%	≤ 0.05%	≤ 0.1%	≤ 0.1%	≤ 0.1%	N/A	N/A	N/A
and 3/ QCI data is	Lot specific	Lot specific	N/A	N/A	Lot specific	N/A	N/A	Catalog
SCREEN TEST 1/, 2/, 4/	✓	✓	✓	✓	✓	✓	✓	✓
QUALIFICATION TEST 3/, 5/	✓	✓	✓	✓	✓	✓	✓	✓

1/ The attributes data for the screening tests performed by the compliant part manufacturer may be purchased by the user and kept on file at the user's site for NASA's review. In the absence of such data, the user shall perform the screening tests required per Table 2, herein.

2/ If the part meets AOQL (Average Outgoing Quality Lot) limits, screening may not be required per Table 2 but must have a certificate of assurance signed by a recognized company (supplier) officer. AOQL is the average value of lot quality that would be obtained over a long sequence of lots from a process with a given population fraction defective.

3/ The QCI data should include data on all tests included in Table 4, as applicable to different levels. This data shall be available for NASA's review.

4/ If the part manufacturer has performed any of the specific tests required by Tables 2, 3, and 4 as part of his processing flow, those tests need not be repeated if lot specific data is on file at the manufacturer's facility.

5/ Only radiation hardness and outgassing test shall be performed prior to part acceptance for test level 2 and test level 3. These two tests are very critical for PEMs, and it is possiible that many PEMs (Class N, SCD, HI-REL, and Commercial) may not meet the projects requirement for these two tests. Therefore users are advised to perform Look-Ahead radiation hardness and outgassing tests before procuring the flight lot for detailed testing. If the parts pass the two tests during the Look-Ahead testing, only then the flight lot should be procured and subjected to the detailed qualification testing per Table 4. The Look-Ahead testing increases the likelihood that flight lot would be acceptable.

6/ No HI-REL parts are available at this time for the space application users.

Table 2. Screening Requirements for PEM Integrated Circuits

Inspection/Test	Methods/Conditions	Test level 1		Test level 2			Test level 3		
		Class N	SCD	Class N	HI-REL	Commercial	Class N	HI-REL	Commercial
1. DPA 1/	section 7.0 herein.	✓	✓	✓	✓	✓			
2. Temperature Cycling 2/	MIL-STD-883,TM1010 /B	✓	✓	✓	✓	✓			
3. Initial Electrical Measurements	per Table 3 herein and applicable device specification	✓ Read/Record	✓ Read/Record	✓ Read only	✓ Read only	✓ Read only			✓
4. Burn-in 3/	per Table 3 herein and applicable device specification Duration (hours)	✓ 48/160	✓ 48/160	✓	✓	✓			
5. Final Electrical Measurements 4/	per Table 3 herein and applicable device specification	✓ Read/Record	✓ Read/Record	✓ Read only	✓ Read only	✓ Read only			
6. Calculate Delta 5/	per Table 3 herein and applicable device spec.	✓ Record	✓ Record	✓	✓	✓			
7. Calculate PDA 6/		3%	3%	5%	5%	5%			
8. External Visual	MIL-STD-883,TM2009 / (modified)	✓	✓	✓	✓	✓	✓	✓	✓

1/ If parts fail DPA, consult with parts engineer for the lot may have to be rejected or additional screens imposed.

2/ Cycle between maximum and minimum storage temperature of device for 10 cycles, no power applied during test.

3/ See Table 3. The burn-in duration is indicated as "Static/Dynamic". For example, burn-in duration 72/160 requires 72 hours of static burn-in (if applicable) and 160 hours of dynamic burn-in (if applicable). If more than 1 burn-in type is required per Table 3, the delta parameters shall be measured after each required burn-in step for test level 1 only. Also, the Delta and PDA calculations shall be made after each burn-in step for test level 1. Table 3 specifies an ambient of 125 °C. This temperature shall only be used if the manufacturers specified max. junction temperature for the plastic device is not violated. Otherwise, choose a temperature commensurate with the max. junction temperature taking into account joule heating for device under test. The duration hours at a lower burn-in temperature must be extended to yield an equivalent hours duration at 125 °C. These calculations generally require an activation energy for the Arrhenius equation associated with specific failure mechanisms.

4/ For field programmable (nonerasable) devices, such as fuse-linked PROMS, PALs and FPGAs, steps 4 through 5 shall be performed after the programming, even if they were performed earlier on the blank devices.

5/ If record is not required, delta criteria may be applied “go/nogo”. This implies that delta parameters should be calculated from the pre and post electrical measurements. However no record is needed for the attribute data except recording whether the parts met the delta criteria or not as specified here.

6/ PDA applies to cumulative failures during all burn-in steps. For test level 1, cumulative catastrophic functional and parametric failures shall be less than 3% in order for the lot to be accepted. For other levels, PDA applies to the functional failures only.

Table 3. Burn-in and Electrical Measurement Requirements for PEMs

IC Type	Required Burn-In		Delta Parameters Limits 2/	Electrical Measurement 1/, 2/, 3/
	Static (Cond. A, B)	Dynamic (Cond. D)		
Digital **TTL, DTL, ECL** Logic (Gates, Buffers, Flip-Flops, Registers and Counters), RAM FIFOs ROM, PROM, PLA Microprocessors, Interface, Peripherals, ASICs 6/	Not Required	T_A = 125°C. V_{CC} = Max. Op. V_{CC} Vout = $V_{CC/2}$ through Load Resistors or V_{CC} through Pull-Up Resistors for Open Collector Outputs. Bidirectional pins are treated as output pins. Vin = Square wave, 50% Duty Cycle, F = 100 KHz to 1 MHz. Apply input signals to have all possible outputs to switch on and off. For memories, apply input signals to read all addresses.	$\Delta I_{CC}(I_{EE}) \leq \pm$ 10% of Limit $\Delta I_{IL} \leq \pm$ 10% of Limit $\Delta I_{IH} \leq \pm$ 10% of Limit $\Delta I_{OZL} \leq \pm$ 10% of Limit (if applicable) $\Delta I_{OZH} \leq \pm$ 10% of Limit (if applicable)	**DC**: V_{IC}, V_{OH}, V_{OL}, $I_{CC}(I_{EE})$, I_{IL}, I_{IH}, I_{OZL}, I_{OZH}, I_{OS} (if applicable) **AC:** T_{PLH}, T_{PHL}, T_{TLH}, T_{THL}, (if applicable) T_{PZH}, T_{PHZ}, T_{PLZ}, T_{PZL}, Access Time (T_A), Set-up Time (T_S), Hold Time (T_H) **Functional Test:** Verify Truth Table. 5/

Notes at the end of Table 3

Table 3. Burn-in and Electrical Measurement Requirements for PEMs

IC Type	Required Burn-In		Delta Parameters Limits 2/	Electrical Measurement 1/, 2/, 3/
	Static (Cond. A, B)	Dynamic (Cond. D)		
Digital **CMOS, PMOS, NMOS, Bi-CMOS** Logic (Gates, Buffers, Flip-Flops, Registers and Counters), RAM FIFOs ROM, PROM, PLA Microprocessors, Interface, Peripherals, ASICs 6/	T_A = 125°C. V_{DD} = Max. Op. V_{DD} Vin = GND (Static 1) Vin = V_{DD} (Static 2) Vout = V_{DD}/2 through Load Resistor. 4/	T_A = 125°C. V_{DD} = Max. Op. V_{DD} Vout = V_{DD}/2 through Load Resistors. Bi-directional pins are treated as output pins. Vin = Square wave, 50% Duty Cycle, F = 100 KHz to 1 MHz. Apply input signals to have all possible outputs to switch on and off. For memories, apply input signals to read all addresses.	$\Delta I_{DD} \leq \pm$ 10% of Limit $\Delta I_{IL} \leq \pm$ 10% of Limit $\Delta I_{IH} \leq \pm$ 10% of Limit $\Delta I_{OZH} \leq \pm$ 10% of Limit (if applicable) $\Delta I_{OZL} \leq \pm$ 10% of Limit (if applicable)	**DC**: V_{OH}, V_{OL}, I_{DD}, I_{IL}, I_{IH}, I_{OZL}, I_{OZH}, I_{OS} (if applicable) **AC:** T_{PLH}, T_{PHL}, T_{TLH}, T_{THL}, (if applicable) T_{PZH}, T_{PHZ}, T_{PLZ}, T_{PZL}, Access Time (T_A), Set-up Time (T_S), Hold Time (T_H) **Functional Test:** Verify Truth Table.

Notes at the end of Table 3

Table 3. Burn-in and Electrical Measurement Requirements for PEMs

IC Type	Required Burn-In		Delta Parameters Limits	Electrical Measurement 1/, 2/, 3/
	Static (Cond. A, B)	Dynamic (Cond. D)		
Linear Amplifiers (Op-Amps, Instrument Amps, Sample and Holds) Comparators,	Not Required	T_A = 125°C. Supply = ±Max. VCC, VEE Open Loop or Gain = -1. V_{IS} = Vpk, Sine wave 7/, F < 60Hz. Choose Vpk not to exceed T_J max. Vout = GND through Load Resistors (R_L). Choose R_L not to exceed T_J max.	$\Delta I_{IB} \leq \pm$ 50% of Limit $\Delta I_{IO} \leq \pm$ 50% of Limit $\Delta V_{IO} \leq \pm$ 50% of Limit	**DC:** I_{CC}, I_{EE}, I_{IB}, I_{IO}, V_{IO}, V_{OPP} A_V, CMRR, PSRR, **AC:** Slew Rate
Linear Voltage References, Regulators.	T_A = 125°C. Input =Vin. Output = GND through R_L. Choose Vin and R_L not to exceed T_J Max.	Not Required	$\Delta V_{OUT} \leq \pm$ 1/2 x (Max. Limit - Min. Limit)	**DC:** I_{CC}, V_{OUT}, I_{OS}, Line Regulation, Load Regulation

Notes at the end of Table 3

Table 3. Burn-in and Electrical Measurement Requirements for PEMs

IC Type	Required Burn-In		Delta Parameters Limits	Electrical Measurement 1/, 2/, 3/
	Static (Cond. A, B)	Dynamic (Cond. D)		
Linear Line Drivers/Receivers	**MOS Devices Only** T_A = 125°C. V_{DD} = Max. Op. V_{DD} V_{SS} = Max. Op. V_{SS} For Drivers 4/ Vin = GND (Static 1) Vin = V_{DD} (Static 2) For Receivers Vin = V_{ID} Max. Vout = $V_{DD}/2$ through Load Resistor.	T_A = 125°C. Supply = ±Max. Op. VCC V_{IS} = Square Wave, F = 100 KHz, 50% duty cycle, Vpk = $\pm V_{ID}$ (Receiver), Vpk = 0 to 5V (Drivers). Vout = V_{CC} through Load Resistors.	$\Delta I_{CC} \leq \pm$ 10% of Limit $\Delta I_{IH} \leq \pm$ 10% of Limit $\Delta I_{OZH} \leq \pm$ 10% of Limit (if applicable) $\Delta I_{OZL} \leq \pm$ 10% of Limit (if applicable)	**DC**: V_{OH}, V_{OL}, $\pm I_{CC}$, I_{IL}, I_{IH}, I_{OS} I_{OZL}, I_{OZH}, (if applicable) **AC:** T_{PLH}, T_{PHL}, T_{TLH}, T_{THL}, **Functional Test:** Verify Truth Table.
Linear Analog Multiplexer / Switches	**MOS Devices Only** T_A = 125°C. V_{DD} = Max. Op. V_{DD} V_{SS} = Max. Op. V_{SS} All Channels OFF. Apply $+V_{DD}$ across half of the channels, and $-V_{SS}$ across the other half of the channels.	T_A = 125°C. $\pm V_{CC}$ = ±Max. Op. V_{CC} Vout = $V_{CC/2}$ through Load Resistors or V_{CC} through Pull-Up Resistors for Open Collector Outputs. Vin = Square wave, 50% Duty Cycle, F = 100 KHz to 1 MHz.	$\Delta I_{CC} \leq \pm$ 10% of Limit $\Delta I_{D(OFF)} \leq \pm$ 100% of Limit $\Delta I_{S(OFF)} \leq \pm$ 100% of Limit $\Delta R_{(ON)} \leq \pm$ 10% of Limit	**DC**: $\pm I_{CC}$, $I_{D(ON)}$, $R_{(ON)}$, $I_{D(OFF)}$, $I_{S(ON)}$, $I_{S(OFF)}$, **AC:** $T_{(ON)}$, $T_{(OFF)}$, Break Before Make Time.

Notes at the end of Table 3

Table 3. Burn-in and Electrical Measurement Requirements for PEMs

IC Type	Required Burn-In		Delta Parameters Limits	Electrical Measurement 1/, 2/, 3/
	Static (Cond. A, B)	Dynamic (Cond. D)		
Linear Pulse Width Modulators (PWM)	T_A = 125°C. V_{in} = Max. Op. V_{in} Outputs = GND through Load Resistors (R_L). Choose R_L not to exceed T_J max.	Not Required	$\Delta V_{REF} \leq \pm$ 10% of Limit $\Delta I_{IO} \leq \pm$ 50% of Limit $\Delta I_{IB} \leq \pm$ 50% of Limit $\Delta I_{IN} \leq \pm$ 10% of Limit	**DC:** V_{REF}, I_{IB}, I_{IO}, I_{OS}, V_{IO}, V_{OL}, V_{OH}, A_V, CMRR, PSRR, **AC:** Rise Time, Fall Time, f_{OSC}
Linear Timer	T_A = 125°C. V_{CC} = Max. Op. V_{CC} Output = V_{CC} through Load Resistors (R_L).	Not Required	$\Delta I_{CEX} \leq \pm$ 50% of Limit $\Delta V_{OL} \leq \pm$ 10% of Limit $\Delta V_{OH} \leq \pm$ 10% of Limit	**DC:** V_{TRIG}, V_{TH}, V_R, V_{OL}, V_{OH}, V_{SAT}, I_{CC}, I_{TRIG}, I_{TH}, I_R, I_{CEX}. **AC:** T_{TLH}, T_{THL}.
Linear Active Filters	Not Required	T_A = 125°C. Supply = ±Max. Op. VCC V_{IN} = Sine wave, F < f_O. Vout = GND through Load Resistors.	$\Delta V_{OS} \leq \pm$ 100% of Limit $\Delta I_{CC} \leq \pm$ 10% of Limit	**DC:** I_{CC}, I_{SS}, V_{OS}, **AC:** f_O, Q, Input Frequency Range.

Notes at the end of Table 3

Table 3. Burn-in and Electrical Measurement Requirements for PEMs

IC Type	Required Burn-In		Delta Parameters Limits	Electrical Measurement 1/, 2/, 3/
	Static (Cond. A, B)	Dynamic (Cond. D)		
Mixed Signal Analog to Digital (A/D) Converters.	**MOS Devices Only** T_A = 125°C. V_{DD} = Max. Op. V_{DD} Vin = GND (Static 1) Vin = V_{DD} (Static 2) Vout = $V_{DD}/2$ through Load Resistor. 4/	T_A = 125°C. $\pm V_{CC}$ = ±Max. Op. V_{CC} Vout = $V_{CC}/2$ through Load Resistors. Vin = Triangular Wave to have all codes outputted. Apply control signals accordingly.	$\Delta I_{CC} \leq \pm$ 10% of Limit $\Delta I_{EE} \leq \pm$ 10% of Limit $\Delta I_{IH} \leq \pm$ 10% of Limit $\Delta I_{IL} \leq \pm$ 10% of Limit $\Delta I_{OZH} \leq \pm$ 10% of Limit $\Delta I_{OZL} \leq \pm$ 10% of Limit	**DC**: V_{REF}, V_{OH}, V_{OL}, V_{IO}, I_{CC}, I_{EE}, I_{IL}, I_{IH}, I_{OZL}, I_{OZH}, I_{OS}, Zero Error, Gain Error, Linearity Error. PSRR **AC:** Conversion Time (T_C), Set-up Time (T_S), Hold Time (T_H) **Functional Test:** Verify All Codes, Look For Missing Codes.
Mixed Signal Digital to Analog (D/A) Converters.	**MOS Devices Only** T_A = 125°C. V_{DD} = Max. Op. V_{DD} Vin = GND (Static 1) Vin = V_{DD} (Static 2) Vout = VDD (or GND) through Load Resistor. 4/	T_A = 125°C. $\pm V_{CC}$ = ±Max. Op. V_{CC} Vout = GND through Load Resistor. Vin = Output of n bit counter n= # of resolution bits of the D/A) to input all codes. Apply control signals accordingly.	$\Delta I_{CC} \leq \pm$ 10% of Limit $\Delta I_{EE} \leq \pm$ 10% of Limit $\Delta I_{IH} \leq \pm$ 10% of Limit $\Delta I_{IL} \leq \pm$ 10% of Limit	**DC**: I_{CC}, I_{EE}, I_{IL}, I_{IH}, I_{OZL}, I_{OZH}, I_{OS}, Zero Error, Gain Error, Linearity Error. PSRR **AC:** Conversion Time (T_C), Set-up Time (T_S), Hold Time (T_H) **Functional Test:** Verify All Codes, Look For Missing Codes.

Notes at the end of Table 3

Notes:

1/ See MIL-STD-1331 for symbol definitions. The burn-in conditions provided in the Required Burn-in columns are for typical configuration of a given device type and should be modified for specific devices.

2/ Minimum required parameters are specified. Other device or application critical parameters shall also be measured.

3/ All DC parameters shall be tested at 25°C, at minimum operating temperatures and at maximum operating temperature. All AC parametric measurements are required to be made at 25°C only.

4/ Static 1 burn-in shall be performed for half of the required static burn-in duration per Table 2. Static 2 burn-in shall be performed for the other half of the required duration. Delta calculations shall be made after each static burn-in.

5/ The functional test for RAMs shall include writing and reading the following patterns as a minimum: 1) Zeros and Ones, 2) Checker Board and Inverse Checker Board, 3) March (March Zero and March One), and 4) GAL-PAT. For complex "State Machine" devices, such as microprocessors, and custom ASIC devices, for which 100% testing of all states are not possible, test vectors which have 95% fault coverage as a minimum shall be developed and used as the functional test.

6/ For user programmable (Non-Erasable) devices such as fuse (anti-fuse) linked PROMS, PALs and FPGAs, the burn-in shall be performed after programming. If the manufacturer performs the burn-in on unprogrammed devices only, the user is responsible for the post programming burn-in. The post programming burn-in shall include the following as a minimum. 1) room temperature DC parametric measurement and verification of the "fuse map" followed by 2) a dynamic burn-in for 160 hours and 3) room temperature DC parametric measurements, delta calculation, and verification of the "fuse map". This is part of the screening requirements for these device types.

7/ Square Wave, 50% duty cycle for Sample and Hold, and Comparators.

Table 4. Qualification Test Requirements for PEM Integrated Circuits

Inspection/Tests	Method/Condition	Die or Pack-age	Test level 1		Test level 2			Test level 3			Sample size per lot (Accept on # failed)
			Class N	SCD	Class N	Hi-Rel	Commercial	Class N	Hi-Rel	Commercial	
Subgroup 1 1/											
a. Physical Dimensions 2/	MIL-STD-883, TM2016	P	✓	✓			✓			✓	4 devices (0)
b. Resistance to Solvents 3/	MIL-STD-883, TM2015	P	✓	✓			✓				3 devices (0)
b. Solderability 4/	MIL-STD-883, TM2003	P	✓	✓			✓			✓	22 leads, min 3 devices (0)
c. Lead Integrity	MIL-STD-883, TM2004	P	✓	✓			✓				45 leads, min. 3 devices (0)
d. Bond Pull 5/	MIL-STD-883, TM2011/	P	✓	✓			✓				30 bonds, min. 5 devices (0)
OR	C or D										
Bond Shear	ASTM, F1269	P	✓	✓			✓				30 bonds, min. 5 devices (0)
Subgroup 2											
a. Pre/Post Electrical Test 6/	User or Supplier Specification		✓	✓	✓	✓	✓	✓	✓	✓	
b. Radiation Hardness :		D, P									
Total dose tolerance 7/	MIL-STD-883, TM1019		✓	✓	✓	✓	✓	✓	✓	✓	8 devices (0)
Single event effects (SEE) 8/	ASTM F1192-90		✓	✓	✓	✓	✓	✓	✓	✓	4 devices (0)
Subgroup 3											
a. Pre/Post Electrical Test 6/	User or Supplier Specification		✓	✓			✓				77 devices (0)
b. High-Temp Operating Life 9/	MIL-STD-883, TM1016	D, P	✓	✓			✓				
Subgroup 4											
a. Pre/Post Electrical Test 6/	User or Supplier Specification		✓	✓			✓				77 devices (0)
b. Temperature Cycling (TC) 10/	MIL-STD-883, TM-1010 or	P	✓	✓			✓				77 devices (0)
OR	JEDEC-22-A104										
Power Temp Cycling (PTC) 11/	JEDEC-22-A105	D, P	✓	✓			✓				
Subgroup 5											
a. Pre/Post Electrical Test 6/	User or Supplier Specification		✓	✓			✓			✓	77 devices (0)
b. Preconditioning 12/	JEDEC-22-A113	P	✓	✓			✓			✓	77 devices (0)
c. Temp Humidity Bias (THB) 13/	JEDEC-22-A101	D, P	✓	✓			✓			✓	77 devices (0)
OR											
Autoclave (AC) 14/	JEDEC-22-A102	D, P	✓	✓			✓			✓	77 devices (0)
d. DPA 15/	Section 7.0 herein	D, P	✓	✓			✓			✓	3 - 5 devices (0)
Subgroup 6 1/											
a. Outgassing 16/	ASTM E595	P	✓	✓	✓	✓	✓	✓	✓	✓	1 device (0)

1/ Electrical rejects may be used.
2/ Performed for initial and requalification only.
3/ Resistance to solvents only required on devices using inks or paint.
4/ If burn-in screening is performed on the device, samples for solderability must first undergo burn-in. Perform 1 hour steam aging prior to testing for gold-plated leads.
5/ Unless otherwise specified, the sample size number of bond pulls selected from a minimum number of 5 devices.
6/ Read and record shall be adapted according to levels listed in Table 2.
7/ Some of the tests (such as burn-in) included in the screening requiements of PEMs may significantally reduce their totat dose radiation tolerance. Users are advised to perform radiation tests on parts that have passed the screening tests. For more information , refer to S.D.Clark , et al., *Plastic Packaging and Burn-in Effects on Ionizing Dose Response in CMOS Microcircuits* , IEEE Transactions on Nuclear Science, vol.42, pp.1607-1614, December 1995.
8/ SEE testing may be waived if the parts have been adequately characterized previously, and it can be ascertained that the manufacturing has not made significant process changes since the previous characterization of the parts.
9/ Typically, 125 °C for 1000 hours. (Junction temperature not to exceed maximum at which DC and AC parametrics are guaranteed by the mfr.. Static or dynamic bias shall be applied as specified in Table 3. Test before and after at room temperature. If device specifications limit the junction temperature such that 125 °C ambient cannot be achieved, than hours must be extended in accordance with the governing reliability model. These calculation will require the use of Arrhenius equation with an appropriate activation energy. Actual duration of Life Test at lower temperature should be equivalent to 1000 hours at 125 °C ambient.
10 Minimum to maximum storage temperature for 250 cycles for test level 1 and 2.
11/ Test is performed only on devices with maximum rated power ≥ 1 watt and $\Delta T_j \geq 40°C$, -40°C to +125°C, 1000 cycles. Max. ambient temperature shall not exceed supplier's spec. Test before and after PTC at room and high temperature or as per maximum rating of power device.
12/ Performed on surface mount devices only. Preconditioning should be performed before THB, AC and TC tests. Test before and after at room temperature.
13/ 85°C/85% RH/1000 hours or 130°C/85% RH/50 hours (HAST). Test before and after THB at room and high temperatures. Any downward revision in temperature due to limit fore device specs. will require an adjustment in duration based on the governing reliability model. In every instance, the equivalent for 85 °C/85% RH/1000 hours or 130°C/85% RH/50 hours shall be achieved.
14/ 121°C/2 ATM. PSIG/100% RH/96 hours. This test should be biased. Test before and after AC at room temperature. Any revisions to temperature or pressure due to limits in device specs. will require an adjustment in duration based on the governing reliability model. The equivalent for 121 °C/2 ATM. PSIG/100% RH/96 hours shall be achieved.
15/ DPA shall be performed on parts exposed to temperature humidity bias or autoclave.
16/ CVCM<0.1%, TML<1.0%. This test requires analytical measurement.

Table 5. Molding Compound Qualification (Optional)

Molding Compound Properties	Test level 1		Test level 2		
	Class N	SCD	Class N	Hi-Rel	Commercial
1. Check PH	$4 \leq ph \leq 9$				
2. Glass Transition Temperature	≥ 150 °C				
3. Coefficient of Thermal Expansion	Typically 16 X 10^{-6} $°C^{-1}$				
4. Water Extract					
Conductivity	20 umhos/cm max				
Chlorine	25 ppm max				
Sodium	25 ppm max				
Potassium	10 ppm max				
5. Hydrolyzable Chlorine	50 ppm max				
6. Total Bromine	0.6 -0.9 %				
7. Total Antimony	1.0 - 2.5 %				
8. Water Absorption for 48 hrs @ 85/85	0.9 %				

Table 6. Package Requalification Criteria

Major Change Description	Temperature Humidity Bias or Autoclave	Temp Cycle Test	Solderability Test
Package Material	Yes	Yes	No
Passivation or Die Coating	Yes	Yes	No
Lead Frame/Material & Design	Yes	Yes	Yes
External Lead Finish and/or Material	No	No	Yes

Table 7. Die Requalification Criteria

Major Change Description
Die Redesign
Major die fabrication change. Examples of changes that would typically require requalification are included in and defined in MIL-PRF-38535. 1. Metallization changes 2. Die structure topology changes (double-diffused, epitaxial, isolation) 3. Mask changes that alter active elements