Electrical Operation of 6H-SiC MESFET at 500 °C for 500 Hours in Air Ambient

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Abstract

A high temperature n-channel 6H-SiC metal semiconductor field effect transistor (MESFET) was fabricated, packaged, and electrically operated continuously at 500 °C for over 500 hours in an air ambient with less than 10% change in operational transistor parameters. To the best of our knowledge, this is the first report of a semiconductor transistor operating in this harsh environment with excellent stability over an extended period of time. The fabrication process that enabled such stability in air atmosphere featured multiple levels of high temperature metal and dielectric passivation to prevent contamination (particularly oxygen) from reaching electrically sensitive interfaces. A thick-film metallization based ceramic package with conductive die attach material and Au wire bonds facilitated long-term testing under electrical bias at 500 °C. Over the course of the 500 hour operational test in air, the only observed degradation of transistor characteristics was increased leakage of the gate-channel diode as anneal time increased. This demonstration of 500 °C transistor durability represents an important step toward significantly expanding the operational envelope of sensor signal processing electronics for harsh combustion-engine environments.

Introduction

As the reliable operating temperature envelope of integrated silicon electronics has been expanded from 125 °C to temperatures above 200 °C, these electronics have found beneficial use in aerospace, automotive, industrial, and energy production systems [1,2]. Further extension of the reliable operational envelope of semiconductor electronics above 300 °C is also expected to offer additional benefits to these industries, particularly in aerospace combustion engine applications where temperatures can approach 600 °C [1,3]. The emergence of wide bandgap semiconductors, including silicon carbide (SiC), diamond, and gallium nitride (GaN), has enabled short-term electrical device demonstrations at ambient temperatures from 500 °C to 650 °C [4-6]. However, these devices have previously not demonstrated sufficient long-term durability when electronically operated at these high temperatures to be considered viable for most envisioned applications.

In order to begin meeting the needs of most applications, a wide bandgap transistor technology must first demonstrate that it can achieve stable, long-term operation under electrical bias at temperature without significant changes in electrical operating parameters. This paper reports on the processing, testing, and numerical modeling of a 6H-SiC transistor (MESFET) that achieved over 500 hours of electrical operation in 500 °C air ambient with less than 10% change in operational transistor parameters. To the best of our knowledge, this is the first report of a semiconductor transistor electrically operating in 500 °C harsh environment with excellent stability over an extended period of time.

Experimental Procedures

Fabrication

The cross-sectional schematic of the MESFET is shown in Fig. 1. The MESFET was fabricated on a commercially purchased off-axis Si-face 6H-SiC epitaxial wafer [7]. Epilayer doping and thicknesses were verified independently by secondary ion mass spectroscopy (SIMS) on a sliver sawed off the edge of the wafer. The transistor had originally been intended to be a junction field effect transistor (JFET), but the top p-type epitaxial layer was inadvertently lost in device processing. A scanning electron microscope (SEM) image of the device can be seen in Fig. 2. The intended JFET gate pattern and n-type channel were separately patterned with metal masks and etched in an inductively coupled plasma (ICP) reactive ion etcher (RIE). The ICP-RIE allows controlled etch rates with nearly vertical sidewalls. The metal masks were stripped in a piranha mixture. A thin blanket and a thicker patterned layer of Si

were applied as a mask for elevated temperature nitrogen ion implant. The source/drain nitrogen ion implant had dosages of ~10^{14} cm^{-2} through a range of energies to create a box-like profile.

After ion implantation, the Si mask was stripped. The wafer was then annealed in an inert atmosphere for less than an hour in order to activate the implant. Unexpectedly, this removed most of the p-layer of the intended JFET gate. The rest of the gate was probably consumed during the next step of thermal oxidation. Loss of the gate epitaxial layer was confirmed by SIMS, which also showed thinning of the channel not under the gate. The lower energy implants were thereby believed lost, but the highest energy implants of the box-like profile remained. The surface was thermally oxidized in steam [8]. Gate, source and drain contact vias were patterned with a BOE 6:1 wet etch. After stripping the photoresist the sample was cleaned in a piranha mixture.

The device was baked-out in vacuum for 1 hour to drive water out of any micro-pipes and metalized with Ti/$TaSi_2$/Pt without breaking vacuum [9]. The metallization was magnetron sputtered with argon as the backfill gas. The metal was patterned with photoresist and dry etched in a parallel plate RIE, following which the photoresist was removed. A backside Ti/$TaSi_2$/Pt contact was deposited, and both metallizations annealed in nitrogen at 600 °C for 30 minutes.

For passivation, Si_3N_4 was deposited onto the wafer. The Si_3N_4 was then patterned with photoresist and etched in a parallel plate RIE. Then the Ti/$TaSi_2$/Pt metallization and the Si_3N_4 depositions were repeated two more times in order to insure excellent passivation. The sample was briefly annealed at 600 °C after each metallization was patterned in order to insure good adhesion with the next Si_3N_4 layer. The metal gate finger was only one metal layer thick and did not completely cover the channel (see Fig. 2b), since the gate finger was designed to be a JFET instead of a MESFET.

Simulation

Commercial device modeling software was employed to carry out two-dimensional simulations of the Fig. 1 device cross-section [10]. Table 1 summarizes the 6H-SiC material and MESFET device parameters used in the simulations. Band parameters not listed in Table 1 were taken from [11]. A single-energy-level approximation was used to model nitrogen freeze-out [12]. Refinements in simulation device parameters, such as doping compensation, channel etch depths, etc., were arrived at by iterative fitting of simulated results to measured data. However, all device parameters listed in Table 1 fall within expected uncertainties of the experimental

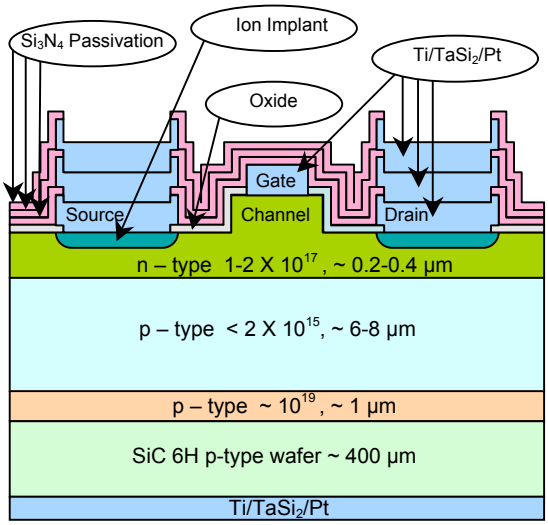

Fig. 1: Schematic drawing of the structure of the MESFET.

device fabrication process across the wafer. The channel region not covered by the gate finger (Fig. 2b) was accounted for in the simulation. The approximate resistance of this parasitic leakage path was calculated from the slope of the measured below-threshold drain I-V characteristic.

Packaging and Interconnection

An Al_2O_3 substrate and Au thick-film metallization [13] were used as the packaging framework. The SiC die was attached to the metallized packaging substrate using an in-house developed Pt-based electrically conductive die-attach

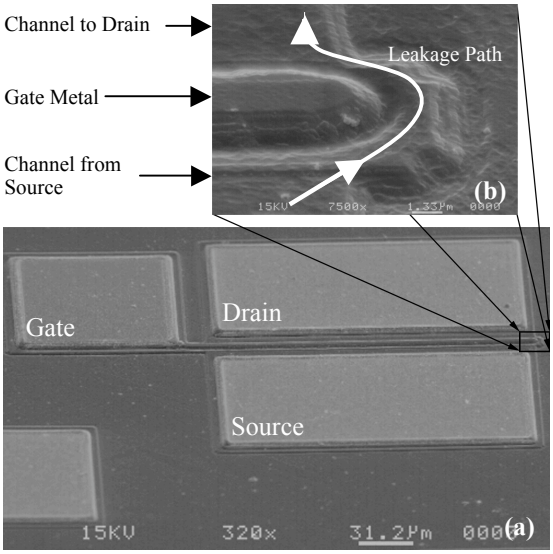

Fig. 2: (a) SEM of the complete MESFET. **(b)** SEM of incomplete coverage of the channel by the gate.

Table 1: 6H-SiC MESFET Simulation Parameters

Parameter	Symbol (Unit)	Value
Gate width/length	(μm)	190/6
n-Channel Doping	(cm^{-3})	$1.1x10^{17}$
n-Channel Thickness Below Gate Source/Drain Region	 (μm) (μm)	 0.37 0.22
p-Buffer Layer Doping Acceptor Compensating Donor	 (cm^{-3}) (cm^{-3})	 $7x10^{14}$ $2x10^{14}$
Contact Resistivity	□ (ohm cm^2)	10^{-4}
Gate Metal Work Function	□ (eV)	5.0
Negative Oxide-Semiconductor Interface Trap Charge	N_{trap} (cm^{-2})	$1.8x10^{12}$
Electron Affinity	□ (eV)	2.7
300 K Density of States	N_c (cm^{-3}) N_v (cm^{-3})	$6.59x10^{18}$ $1.68x10^{18}$
Dopant Ionization Energies	E_d (eV) E_a (eV)	0.09 0.30
Richardson Constant for Electrons	$A_{Rich,n}$ ($A/cm^2/K^2$)	146
Caughey-Thomas Model Electron Mobility Parameters (See [10,11])	□1,n ($cm^2/V/s$) □1,p ($cm^2/V/s$) □2,n ($cm^2/V/s$) □2,p ($cm^2/V/s$) □n ,□p □n ,□p □h, □p □h ,□p $N_{crit,n}$ (cm^{-3}) $N_{crit,p}$ (cm^{-3})	10 20 415 99 □3.0 □1.8 0.6, 0.5 0.0 $1.3x10^{18}$ $1.0x10^{19}$
Electron Saturation Velocity	$V_{sat,n}$ (cm/s)	$1.9x10^7$
Field-Dependent Electron Mobility Parameter ([10,11])	□n'	1.2

material, which was specifically designed for the Pt thin-film capped ohmic contact metallization formula on the backside of the SiC chip. This die attach material provides a low curing temperature of 500°C so the device was not exposed to any higher temperatures beyond the testing/operation environment in the packaging process. Heavily doped 1 mil (diameter) Au wires were used to electrically interconnect the device to the metallization traces on the alumina substrate using thermo-sonic bonding. 10 mil diameter Au wires were used to provide the second level electrical interconnections from the packaging substrate to room temperature terminals for measuring instruments. These Au wires directly extend to the outside of the oven in which the thermal-electrical testing of the device was conducted.

Electrical Characterization

The packaged chip was placed into a temperature-controlled oven and connected to a digitizing curve tracer [14]. Electrical testing commenced following an unbiased overnight heat soak at 500 °C. All tests were carried out in air atmosphere, in darkness, with the curve tracer continuously sweeping families of drain current (I_D) versus drain voltage (V_D) curves (i.e., "drain characteristics") at a drain sweep frequency of 60 Hz. The parameters used for these bias and measurement sweeps are as shown in Fig. 3, with V_D sweeping from zero to ~ 30 V, and then back for each gate voltage (V_G) step. V_G stepped from 0 V to –20 V in -2V increments, and the source voltage (V_S) was always tied to the instrument ground. The substrate bias voltage (V_{Sub}) was either 0 V (ground) or –20 V at various times during the testing. The substrate bias and temperature test schedule are summarized in Table 2. For I-V characterization of the gate-to-channel diode of the MESFET, the gate terminal was biased while drain, source, and substrate terminals were grounded. Similarly, channel-to-substrate diode I-V characteristics were measured by biasing the substrate while grounding the other three device terminals. The oven heat-up and cool-down times are not counted as part of the device's cumulative electrical operating time at 500 °C (t_{500C}).

Table 2: Temperature and Substrate Bias Test

Clock Time (hours)	t_{500C} (hours)	Temperature Profile	Substrate Bias
0-117	0-117	500 °C	-20 V
117-126.5	117-126.5	500 °C	-20 V*
126.5-140	-	Cool to 27 °C	-20 V
140-146	-	27 °C	0 V
146-148	-	Heat to 500 °C	-20 V
148-163.5	126.5-142	500 °C	-20 V
163.5-170.5	142-149	500 °C	0 V*
170.5-402	149-380.5	500 °C	0 V
402-570	380.5-548.5	500 °C	-20 V
570-579.5	548.5-558	500 °C	0 V*

*** With few-minute bias excursions to 0 V or –20 V.**

Results

Fig. 3 compares (a) 27 °C and (b) 500 °C measured (near the beginning of the test) and simulated transistor drain characteristics (I_D vs V_D curves) for a grounded substrate. The section of channel not covered by the gate finger (Fig. 2b) forms a parasitic parallel resistor, which prevents the drain current from being fully cutoff for voltages below threshold ($V_G < V_T$). The approximate resistance of this parasitic leakage path can be

extracted from the slope of the below-threshold drain I-V characteristic. The threshold voltage (V_T) for cutting off the measured source-to-drain current flow in the gate-covered region is –11.3 V at 27 °C and –10.5 V at 500 °C. The leakage path prevents measurement of useful transistor subthreshold slope properties [15, 16]. The nearly 3-fold reduced transistor current at 500 °C compared to 27 °C is consistent with previously reported channel electron mobility degradation due to increased phonon scattering [4, 5]. Fig. 3 shows reasonable agreement between simulated and measured results, especially considering the large difference in temperature. Similar agreement was obtained between simulated and measured results for V_{Sub} = -20 V using identical (i.e., Table 1) device and material simulation parameters.

It is important to note that almost no I-V hysteresis (i.e., looping) was observed between the rising and falling drain voltage sweeps, both of which are shown on 60 Hz curve-tracer measured I-V plots of Fig. 3. In addition, no change in drain I-V properties were observed when the number of gate steps was reduced, or when fast or slow pulsed DC mode [14] was used for measurements at 500 °C. These observations are consistent with highly stable device operation expected from devices free of significant charge trapping effects [17].

The operational durability of the 6H-SiC MESFET observed during 500 °C bias-temperature testing is summarized in Figs. 3-6. Taken together, these figures show the excellent durability and stability of almost every aspect of transistor operation at 500 °C. The only significant transistor degradation mechanism observed over the course of the 500 °C test was the gradual degradation of the MESFET's Schottky barrier gate leakage characteristics under high temperature annealing.

Proper rectification of diode junctions within a MESFET structure is necessary for transistor electrical operation. In particular, both the pn junction formed by the p-substrate to n-channel semiconductor interface (Fig. 1) and the metal-semiconductor Schottky junction formed by the metal gate residing on the n-channel (Fig. 1) must block current flow when subjected to reverse bias from positive drain voltage used in operating n-channel MESFET's [15, 16]. Fig. 4 shows the 500 °C measured I-V properties of the diode junctions in the 6H-SiC MESFET. The substrate-channel pn diode exhibited excellent rectification throughout the 500 °C test with essentially no reverse leakage current.

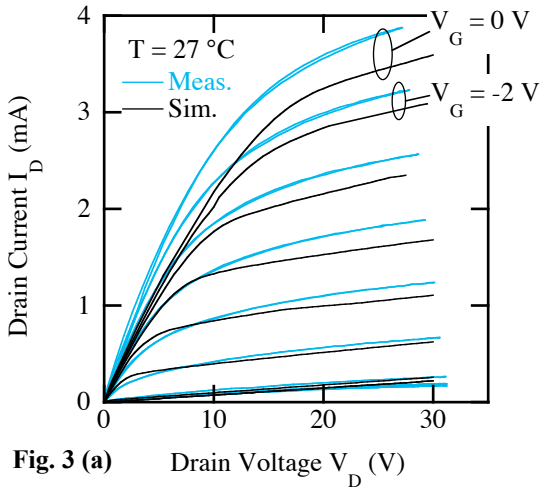

Fig. 3 (a)

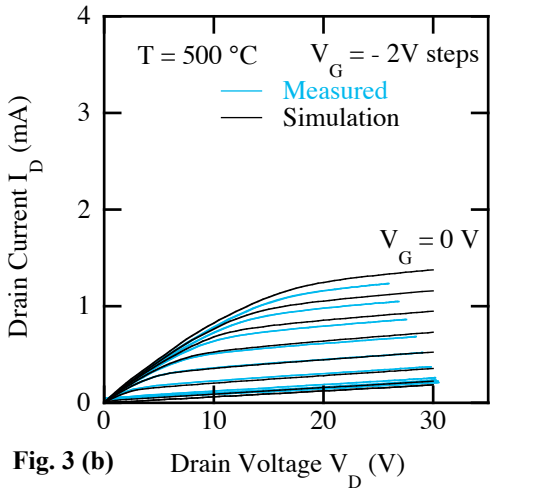

Fig. 3 (b)

Fig. 3: (a) 27°C and **(b)** 500°C measured and simulated transistor drain characteristics for V_{Sub} = 0 V. Note the absence of looping between the rising and falling drain voltage sweeps.

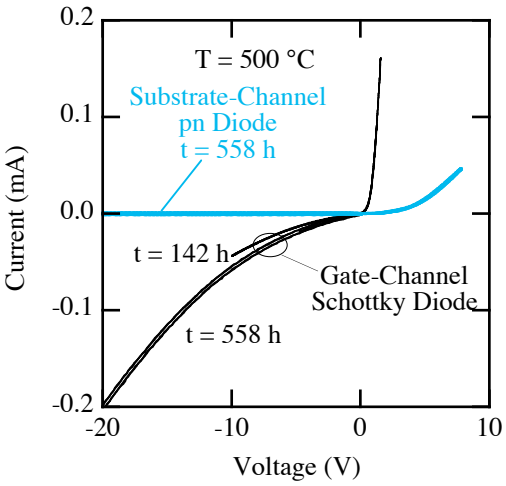

Fig. 4: Measured 500 °C I-V characteristics of the gate-to-channel (metal-semiconductor Schottky) and substrate-channel (pn junction) diodes of the 6H-SiC MESFET.

However, as shown in Fig. 4, the gate-channel Schottky diode exhibited significant 500 °C reverse leakage current that increased with both anneal time and applied voltage. These behaviors appear quite consistent with previous works. Thermally activated Schottky barrier reverse-bias leakage mechanisms exponentially increase with both temperature and applied voltage [15, 18]. The gate metallization, which has previously been demonstrated to be an excellent ohmic contact to degenerately doped n-type 6H-SiC, became more ohmic (i.e., less rectifying) during prolonged "burn-in" at 500 °C [9].

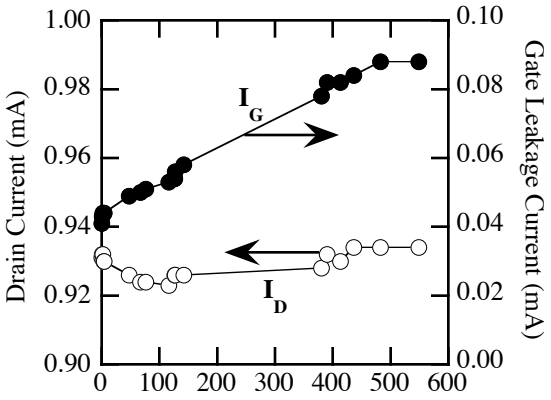

Fig. 5 (a) Operating Time at 500 °C (h)

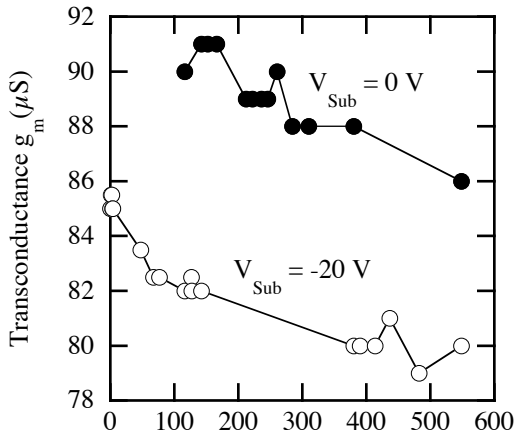

Fig. 5 (b) Operating Time at 500 °C (h)

Fig. 5: Time evolution of selected transistor parameters observed during 500 °C bias-temperature testing. The drain current I_D plotted in **(a)** was recorded at V_D = 20 V, V_G = 0 V, and V_{Sub} = -20 V, while the gate current I_G was measured at V_D = 0 V, V_G = -20 V, and V_{Sub} = -20 V. The large signal transconductance g_m shown in **(b)** was calculated at V_D = 20 V using measured V_G = 0 V and V_G = -2 V current data. The threshold voltage V_T is not plotted because it changed by less than 0.1 V.

Fig. 5 plots selected transistor electrical parameters measured over the duration of the 500 °C testing. The transistor drain current I_D (measured in saturation region at V_D = 20 V) exhibits less than 5% change throughout the course of the test (Fig. 5a). The MESFET large signal transconductance g_m (dI_D/dV_G measured at V_D = 20 V between V_G = 0 and -2 V) also exhibits less than 10% change during the test (Fig. 5b). The change in 500 °C threshold voltage V_T (not shown) was less than 0.1 V. These results indicate that most relevant aspects of transistor structure (i.e., the conductive channel charge, ohmic contacts, dielectric surface passivation, high temperature packaging, etc.) are functionally stable in this harsh environment. To the best of our knowledge, this is the first report of a semiconductor transistor able to operate continuously in this temperature regime for an extended period of time with such minute changes in electrical behavior. The only significant change in transistor properties observed during the bias-temperature test is the more than 2-fold increase in Schottky gate leakage current I_G measured at V_G = -20 V (Fig. 5a).

Fig. 6 compares transistor drain characteristics for V_{sub} = -20 V, which were measured at the beginning and end of the 558 hour 500 °C bias-temperature test. The change in I-V characteristics is

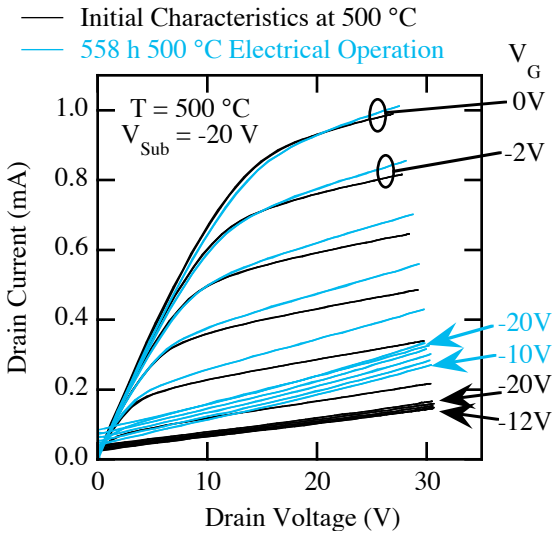

Fig. 6: Comparison of the MESFET drain characteristics measured before and after the 558 hour 500 °C bias-temperature stress. Some of the stepped gate voltages (V_G) are denoted with arrows along the right side of the plot. As discussed in the text, the change in I-V properties over the course of the anneal is due to increased leakage of the gate-channel Schottky contact. All other transistor properties did not significantly degrade during the biased anneal.

attributed to the degraded rectification of the gate-channel Schottky barrier. The change in measured I-V properties is minimal for biases where V_D and V_G differ by less than ~ 20 V (i.e., $|V_G - V_D| = |V_{GD}| <$ 20 V). However, as $|V_{GD}|$ reverse bias increases beyond ~ 20 V, the 558 hour I_D vs. V_D curves clearly exhibit an additional current component due to the increased gate-channel diode leakage, which, after annealing, exceeds the parasitic current flowing through the channel region not spanned by the gate finger. This additional current is more significant for V_G approaching or below $-V_T$ due to the fact that source-to-drain channel current I_{DS} becomes small in comparison with the gate-channel junction leakage. The gate-to-drain junction leakage increases with higher $|V_{GD}|$ reverse bias, which causes the 558 hour baseline off-state current to noticeably increase with drain voltage for the V_G steps between -12 V and -20 V, as shown in Fig. 6.

Discussion

The MESFET transistor reported here demonstrated previously unattained 500 °C transistor electronic durability. The dominant degradation mechanism of this MESFET was due to annealing of the metal-semiconductor gate interface. By implementing a relatively minor correction to the process reported in this paper, the originally intended JFET structure could be implemented. The semiconductor pn junction gate of the JFET should not degrade with 500 °C annealing time in the manner that the metal-semiconductor gate junction of the MESFET degraded. Therefore, we anticipate that a JFET-based structure would exhibit even better long-term durability than the MESFET transistor of this paper. Furthermore, the intended JFET p^+ gate would have completely covered the width of the transistor channel, thereby enabling complete turn-off of the transistor. Therefore, it should be possible to rapidly build upon the results of this paper to realize even more durable capable 500-600 °C capable 6H-SiC transistors.

Aside from the gate-related degradation, all other aspects of the transistor appear to demonstrate excellent harsh-environment stability while operating under prolonged electrical bias at 500 °C. It is worth noting some specific transistor process improvements (compared to our previous work [6]) that enabled this increased high temperature device durability. One critical improvement was the use of recently developed ohmic contact technology that demonstrates excellent durability when subjected to unbiased air-anneal treatments at 500 °C and 600 °C [9]. While specific contact resistance durability measurements have not yet been carried out, the initial transistor durability demonstration indicates that the ohmic contacts remain durable even under the prolonged application of modest electrical bias. Further, the prolonged electrical testing of the device was enabled by the recent development of packaging technology including conductive die attach material and electrical interconnections for high temperature operation, as probe-station testing over long time periods at 500 °C is largely impractical.

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Biography

David Spry received his B.S. in Engineering Physics form The Ohio University in 1998. He has spent the last five years working on SiC high temperature electronics and micro electro-mechanical systems (MEMS). Prior research areas include CVD of diamond films, CdTe/CdS solar cells, and organic light emitting diodes (OLEDs).