# HOT SPOT SUSCEPTIBILITY AND TESTING OF PV MODULES

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## ABSTRACT

Localized heating or hot spots in a photovoltaic module can occur by any combination of cell failure, interconnection failure, partial shading, and variation in the photocurrent from cell to cell (mismatch). To probe the sensitivity for hot spot heating of commercial amorphous silicon and crystalline modules, several intrusive and nonintrusive experiments have been performed. In the intrusive experiments each cell in several commercial amorphous silicon modules was evaluated separately and in groups for localized heating effects. Damage in amorphous silicon modules occurred under reverse-bias conditions in the dark above a 5-20 $mAcm^{-2}$ cell current density at the interconnection between cells. Shading can cause a larger temperature rise than current mismatch. For the monolithic amorphous silicon modules investigated the current mismatch between each cell was substantial, but the temperature rise was negligible because of the rather low shunt resistance.

## INTRODUCTION

Localized heating (hot spot) of photovoltaic modules has been documented since the early spacecraft days (1). It was argued that cell failure, interconnection failure, or partial shading by parts of the spacecraft could cause cells to heat up and possibly damage. In 1979, damage due to hot spot heating was observed at test sites at Mead, Nebraska and Arlington, Texas (2). At Mead, a hail storm caused cells to crack, which in turn, caused some cells to become reverse biased and heat up. At Arlington, hot spot heating occurred after the modules, each with a bypass diode, were short-circuited for washing and inspection.

In the past years, several tests have been developed to test the ability of a photovoltaic (PV) module to withstand hot spot heating. When bypass diodes are used to limit the reverse bias voltage across a module to less than 1 V hot spot heating is minimized. Standards have been developed to determine the degree of hot spot heating when bypass diodes are properly installed in a module. The Jet Propulsion Laboratory (JPL) (3) and Underwriters Laboratory (4) developed an intrusive test, in which individual cells are reverse biased in the dark or under reduced illumination. The Joint Research Center in Ispra, Italy under the auspices of the Commission of the European Communities developed a nonintrusive test under a simulator, in which cells in the modules are shaded (5). Various national and international standards organizations are developing module qualification procedures involving hot spot susceptibility. Because current hot spot tests were developed specifically for crystalline silicon modules, these tests should be reevaluated for use in evaluating amorphous silicon and other thin-film material systems. The first goal was to investigate and compare the behavior of amorphous silicon (a–Si) and crystalline silicon (c–Si) modules under reverse biasing. This study addressed the basic question of what is hot spot heating, what causes it and how can it be simulated? The experiments done on the a-Si and c-Si modules show that the procedures for the different hot spot tests have problems as far as cell selection and determination of the test conditions are concerned.

### What is Hot Spot Heating?

Hot spot heating occurs when a cell in a string of series connected cells is negatively biased and dissipates power in the form of heat instead of producing electrical power. This happens when the current produced by a given cell is lower than the string current. This can occur when the cell is shaded, damaged, or simply generates less current than the module. One example of mismatch is given in Figure 1, which shows a thermal image of a short-circuited crystalline module. The temperature of the mismatched cell is about 80°C versus 50°C of the rest of the module. When a single cell in a series string generates less current than the module, localized heating will occur because the current flowing through each cell in the string must be equal.

Figure 2 shows a module operating under standard test conditions with a voltage at maximum power of $V_{mp}$ and current at maximum power of $I_{mp}$ with a single shaded cell in the series string. Because of Kirchoff's voltage and current laws the shaded cell will operate at a voltage of $-V'$ and current of $I_{mp}$, causing power to be dissipated in the cell



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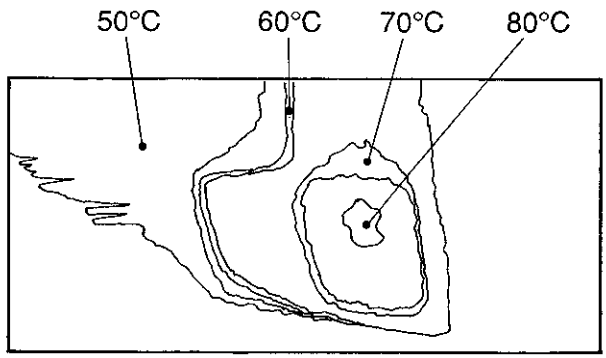


Figure 1. Thermogram of a mismatched mono-Si cell in a short-circuited module.

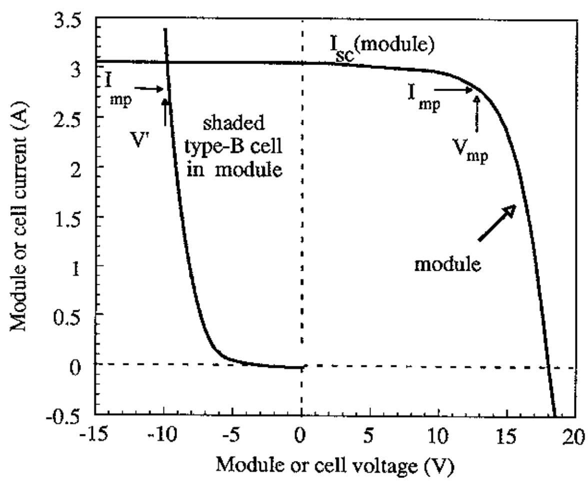


Figure 2. Reverse I-V curve of a partially shaded or mismatched type-B cell and I-V curve of the module.

equal to $V'^{*} I_{mp}$. A cell is considered to be type-A if the cell voltage in the dark at $-V'$ is greater than the illuminated module voltage at the maximum power point ($V_{mp}$) with a current equal to $I_{mp}$. A cell is also type-A if the cell voltage in the dark is at $-V_{mp}$ and the current is less than $I_{mp}$. The reverse characteristics of a type-A cell are voltage limited. A cell is considered to be type-B if $-V'$ is less than $V_{mp}$. The reverse characteristics of a type-B cell are current limited. A type-B cell often has a low shunt resistance or has been damaged. Two typical examples of reverse current-voltage (I-V) curves for commercial crystalline and amorphous silicon modules are given in Figure 3.

The power dissipation for any given faulty or shaded cell depends on series-parallel configuration of cells in a module (6). In general, increasing the number of cells in series increases the power dissipation and increasing the number of cells in parallel decreases the power dissipation of the faulty cell.

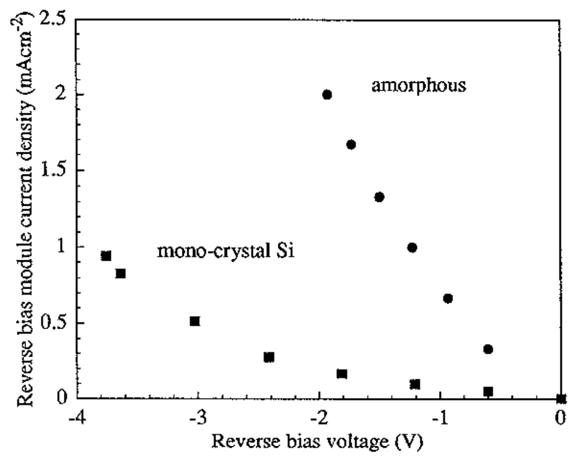


Figure 3. Reverse bias I-V curves of a "typical" commercial crystalline and an amorphous silicon module.

Based upon the results of this study the worst possible condition of hot spot heating is to completely shade a single cell. To minimize these effects the array should be mounted to avoid dust or snow collection on the module, and shadows from objects in the foreground should not obscure a single cell. The term current mismatch refers to any mechanism that can cause a reduction in the short-circuit current of a cell compared to other cells in the series string. Manufacturers of crystalline silicon cells and modules sort their cells by current at a fixed voltage in order to minimize hot spot heating and optimize module power production. If a cell degrades because of a crack or other intrinsic mechanisms, the current mismatch may be severe enough to damage the encapsulation.

## AMORPHOUS SILICON UNDER REVERSE BIASING

The behavior of crystalline silicon modules under reverse biasing (7,8) has been well studied, but little information has been published on amorphous silicon (9). The intrusive hot spot test in wide use was developed by JPL (3). In this, test wires are attached to individual cells. The advantage of this method is that the I-V characteristics of each cell can be known for positive as well as negative voltages under varying degrees of illumination. As can be seen from Figure 3, amorphous silicon behaves differently from crystalline silicon under reverse biasing. For the six amorphous silicon modules from three manufacturers when the number of cells in series exceed 15, the cells can all be considered to be type-B (9). This is not surprising because of the relatively low shunt resistances of the a-Si modules. Most amorphous silicon modules are fabricated by depositing amorphous silicon on tin oxide coated glass. The individual cells are defined by a scribing process. In the intrusive hot spot test, electrical contacts are made to each test cell, and a negative voltage is applied in the dark or under reduced illumination, depending on whether it is a type-B or a type-A cell. However, the individual cells in many thin-film technologies like amorphous silicon are very difficult to contact without damaging.

For the commercial amorphous silicon modules evaluated, electrical contact to the individual cells was made to the back of the cells. Because the aluminum back contact thickness is approximately 1 μm and a single scratch would destroy the cell, great caution was required. Two wires, one at each end, were attached to the back of every cell with silver epoxy that cured at room temperature. Localized heating because of current crowding was measurable but small because the cell length was 10 cm and the use of two wires, one at each end, minimized these effects.

By reverse biasing individual cells in the dark, it was found that the voltage never exceeded the value of -7 to -8 V. At this voltage, only the current still rises. The current level at which damage occurred varied widely, from 0.5 $I_{SC}$ to 2 $I_{SC}$ or 50-200 mA (for 1 by 10 cm cells). In 24 of the 37 damaged cells from two different manufacturers, damage started at the cell interconnection. Inspection of the damaged region under a microscope showed that the damage developed right next to the third scribe line. Figure 4 shows an example. One possible explanation of this phenomenon is the following: When the third scribe line is made, the laser beam causes the a-Si near the scribe line to crystallize to some extent (10). Because c-Si has a much higher dark conductivity than a-Si, these parts may act as shunt paths and break down earlier because of the high current density. Another possible reason that damage occurs at the interconnection is that the particular shape of the interconnection causes the current to concentrate at the edge. This would mean that other thin-film solar cells that are made in the same way might have the same problem.

In case the damage did not start at the cell interconnection, usually pinholes develop (small light spots with a diameter of less than a millimeter). During reverse biasing, sometimes small light emitting spots were observed, which could lead to the formation of pinholes. In the case of crystalline silicon, this has been associated with avalanche breakdown (7).

As is evident from the temperature profile of a reverse biased cell, the power dissipation is very nonuniform. Reverse biasing of a module with 30 cells in series clearly shows this nonuniformity (see Figure 5). Because temperature is the important factor that determines whether the module will be damaged or not, it is interesting to know how much the local temperature rise will be at a given current level. Therefore, several cells and modules were reverse biased and their maximum temperature as a function of the current was measured. The advantage of reverse biasing whole modules is that 30 cells are probed at a time, so that there is a reasonable chance that all possible cell qualities are represented. The disadvantage is that the whole module is heated instead of one cell, but because the heating is localized, the hot spot temperature will probably not be influenced very much by the other cells.

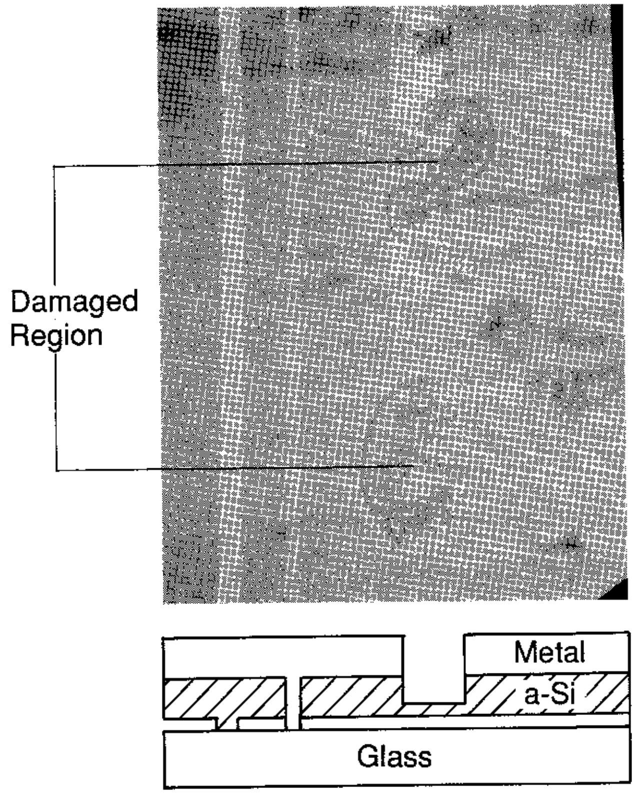


Figure 4. Scribe lines viewed from the aluminum back, 25X.

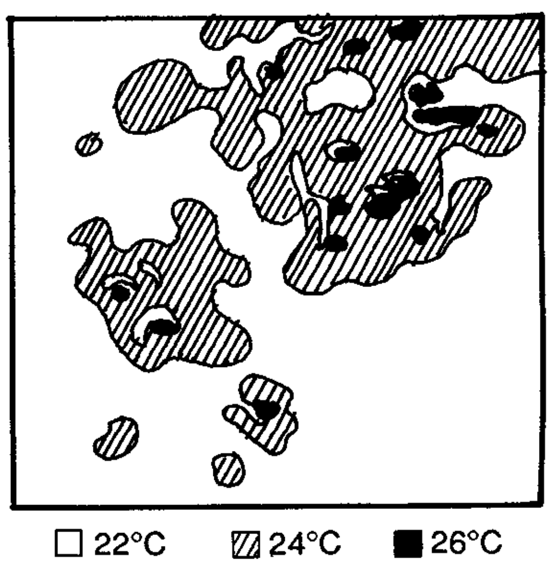


Figure 5. Thermal image of a reverse biased amorphous silicon module in the dark showing hot spots.

The maximum temperature as a function of the current is depicted in Figure 6 for commercial 1-$ft^2$ amorphous silicon on glass modules from three different manufactures. Figure 6 shows that for modules of manufacturers A and B, the temperature rise is moderate, even at the short-circuit current level, which is about 350 mA. In the module of manufacturer A, several pinholes developed. The range of temperatures fell within the range given in the literature earlier (9). A much greater temperature rise was observed for the module from manufacturer C. Visible damage was done to several cells, but not to the encapsulation. Measurement of the I-V curve after the damage had occurred showed no anomalies. The fraction of the cell that was damaged was so small that the power reduction was less than the resolution of the measurement system (~1%).

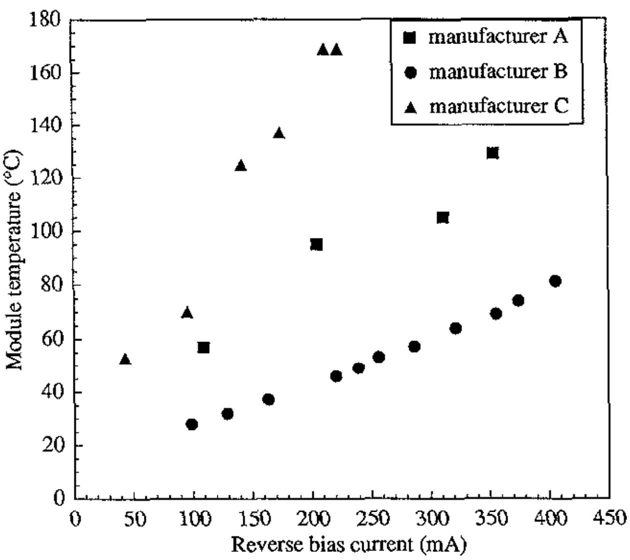


Figure 6. Reverse biasing of three 1-$ft^2$ commercial amorphous silicon modules, at room temperature.

All these experiments were performed in the dark or under shading. Could mismatch of amorphous silicon also lead to a significant temperature rise? Measurement of the short-circuit currents of 20 cells in a submodule (a module without encapsulation) showed that the lowest $I_{SC}$ can be 5% to 8% lower than the module $I_{SC}$. However, short-circuiting a a-Si module does not show cells that are hotter than the rest, as does short-circuiting crystalline silicon modules. This is because the shunt resistance is so low that hardly any power dissipation can take place. It also implies that, in the case of mismatch, when the cell is illuminated, the current distribution is more uniform than under complete shading.

An outdoor hot spot test was also performed on a few modules. For amorphous silicon, three modules of three different manufacturers were placed outside. Cell selection was done by reverse biasing the whole module until temperature differences became visible, as in Figure 7. The cell that gave the highest temperature was selected. One cell in every module was shaded. After one week of outdoor exposure, nothing had happened to the 1-$ft^2$ module of manufacturer B. The 1-$ft^2$ module of manufacturer A showed two small pinholes. The 4 -$ft^2$ module of manufacturer C showed some more damage, at one end as well as in the middle. After two more weeks nothing had changed. Measurement of the I-V curve showed some degradation, probably all due to the Staebler Wronski effect, but no anomalies. The encapsulation, glass on glass as well as glass on polymer, was not damaged. After three more weeks of exposure the result was still the same.

## CRYSTALLINE SILICON UNDER REVERSE BIASING

Crystalline silicon modules from two manufacturers with 30 cells in series were evaluated. A module was illuminated with a filtered Ar-arc (Vortek simulator) to a total irradiance of 1000±40 $Wm^{-2}$, global light. As part of a nonintrusive hot spot test every cell in the module was individually shaded with black tape and the maximum temperature was measured. The maximum temperature that each of the 30 cells achieved when shaded as a function of the reduced current is shown in Figure 7. The reduced current is defined as the short-circuit current of the module after the illumination of one of the cells in the module has been reduced by shading. The module short-circuit current is the module current under uniform illumination. The current at maximum power for the module was 3 A, giving 10 type–A and 20 type–B cells in the module shown in Figure 7. Figure 8 shows the temperature rise for as a function of percentage of the area shaded for one of the type–A cells in the module evaluated in Figure 7. With the uniform shading

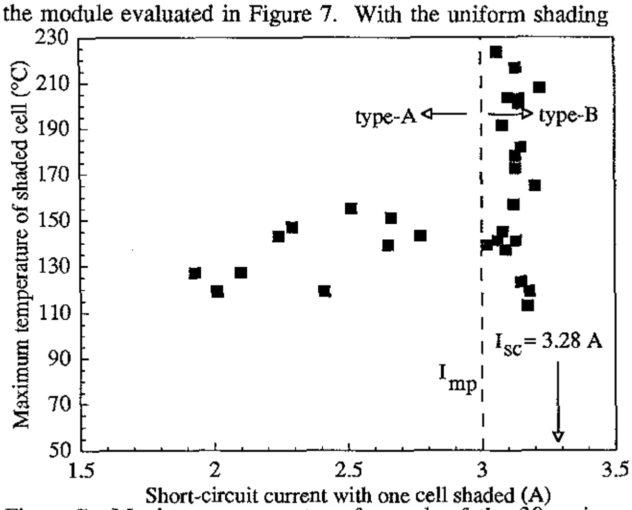


Figure 7. Maximum temperature for each of the 30 series connected c-Si cells shaded individually in a module as a function of reduced short-circuit current.

a translucent cellophane filter was placed over the entire cell while in the case of nonuniform shading the light was completely blocked from part of the cell. Figure 9 compares the results of this experiment for a type–A cell from the module in Figure 8.

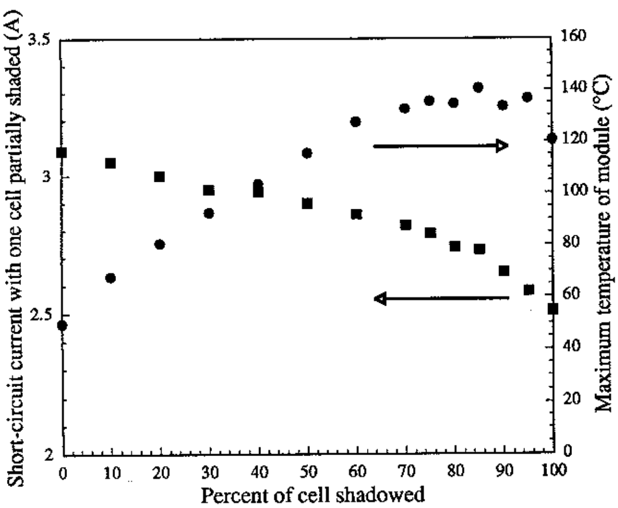


Figure 8. Reduced short-circuit current (■) and maximum localized temperature (●) as a percentage of the cell area that is shaded.

## SUMMARY OF HOT SPOT TESTS

The a-Si modules from manufacturers A and B exhibited neither degradation in the I-V characteristics nor physical damage. In the modules from manufacturer C, some visible pinhole damage occurred with the nonintrusive test but the decrease in performance was insignificant.

Several of the type-B cells in the crystalline-Si module from two different manufacturers showed small cracks and bubbles in the rear encapsulation after continuous one sun illumination; the module shorted and one cell completely shaded. This implies that these modules would fail the nonintrusive hot spot test in reference 4. With proper siting of a PV array, the shading of only one cell in a module should not occur.

The hot spot tests assume that the worst case of heating of type-A cells occurs when the module current is increased to the maximum power current ($I_{mp}$). It is true that the maximum power dissipation for the entire cell is greatest at the maximum power point. However, in the case of partial shading, the power dissipated per unit area is not uniform. In fact, the smaller the illuminated area, the higher power dissipated per unit area in the illuminated region of the cell. The maximum temperature rise in a shaded module is determined by region with the maximum power dissipated per unit area and not the total power dissipated. Figure 9 shows that the temperature rise as a function of the fraction of the total cell area shaded varies from 50 - 140°C.

In the JPL block V procedure (3), type-A cells are tested by applying a voltage equal to the negative of the maximum power voltage ($-V_{mp}$) and adjusting the irradiance level until the current is equal to the current at the maximum power point ($I_{mp}$). This situation for an intrusive test can be translated into a nonintrusive test by applying shading to a cell in a short-circuited, fully illuminated module, until the current is equal to $I_{mp}$. However, in standardized nonintrusive tests such as the one given in reference 4, type-A cells are partially shaded with opaque shading. These two situations are not equivalent, as shown in Figure 9.

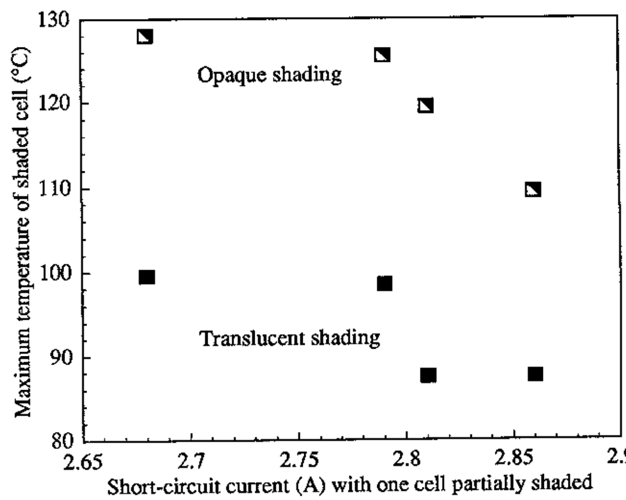


Figure 9. Comparison between partial shading (●) and uniformly reduced illumination (■).

For the c-Si modules investigated, the temperature rise in type-A cells is below the damage threshold, regardless of whether translucent or opaque shading is applied.

For the crystalline and amorphous silicon, PV modules investigated, failures due to hot spot heating are unlikely to occur provided bypass diodes are employed. However, these conclusions are based on the assumption that the reverse bias across a module will not exceed -1 V (a bypass diode is installed). The array design influences the possibility and severity of hot spot heating. Therefore, a hot spot test should take into account this array design by evaluating what could go wrong in a certain design and simulating these circumstances. Some heating due to mismatch can occur in short-circuit conditions. Maybe this could lead to long term degradation. However, the aim of the hot spot test is to detect problems that arise almost immediately.

ACKNOWLEDGEMENTS

This work was supported by the Department of Energy under contract No. DE-AC02-83CH10093.

REFERENCES

1. F.A. Blake and K.L. Hanson, Proc. 4th Intersoc. Eng. Conv. Eng. Conf., Washington, DC, 1969, Am. Inst. Chem. Eng. New York, 575, (1969).
2. S.E. Forman, M.P. Themelis, Proc. 14th IEEE Photvoltaic Specialists' Conf., San Diego, CA, IEEE, New York, 1284, (1980).
3. Block V Solar Cell Module Design and Test Specification for Intermediate Load Applications, JPL internal document 5101-161, Jet Propulsion Laboratory, Pasadena, CA, (February 1981).
4. Qualification Test Procedure for Photovoltaic Modules, Commission of the European Communities standard specification number 502, issue 1, (1984).
5. Standard for Flat-Plate Photovoltaic Modules and Panels, Underwriters Laboratories number UL 1703, August 1, 1986, Underwriters Laboratories Inc., Research Triangle Park, NC (1986).
6. M.M. Alkaisi and N.A. Aldawody, Solar Cells, 28, 11, (1990).
7. J.W. Bishop, Solar Cells, 26, 335, (1989).
8. C. Gonzalez, R.W. Weaver, R.G. Ross, R. Spencer, J.C. Arnett, Proc. 17th IEEE Photovoltaic Specialists' Conf., Kissimmee, FL, IEEE, NY, 1984, 668, (1984).
9. C. Gonzalez and E. Jetter, Proc. 10th IEEE Photovoltaic Specialists Conf., Las Vegas, NV, IEEE, New York, 1041, (1985).
10. S. Yamazaki, K. Itoh, S. Watabe, A. Mose, K. Urata, K. Shibata, and H. Shinohara, Proc. 17th IEEE Photovoltaic Specialists' Conf., Kissimmee, FL, IEEE, New York, 206, (1984).