Summary of TDC issues

A. Hard VME interface Lock-up

Sometimes during power-up the VME interface on a TDC card will not initialize properly. VME reads and writes to a board in this condition will result in VME bus errors. In this state, the VME interface can not be recovered with a sysreset* on the backplane. The only way to clear a board in this state is to power off and on the board preferably via hot extraction/insertion. This problem is only known to occur in crates equipped with CDF power supplies. There is also a requirement that several TDC cards (more than 5-6) must be installed in the crate. In some cases, all of the TDC cards in the crate will be in this state following a power cycle. In other cases, only a small number of the installed TDC cards (as few as one) will be in this state. The cause of this problem is thought to be a known bug in the Cypress VME interface chip (CY7C960). Note that this problem has also been seen in other boards that use this interface chip such as the DCAS board. We are in the process of testing a new version of the VME interface chip (CY7C960A) which should correct this problem.

B. Soft VME interface Lock-up

In some cases when a TDC board is initially installed in a crate, the sequence of VME reads done from the TDC status page of the CDFVME package will cause the VME interface to hang. It is thought but not proven that the rapid series of VME reads of the board performed by this package is responsible for this effect. This idea is somewhat validated by the fact this problem is more easily reproduced in crates with power PC processors than in those with MVME162 processors. In this particular state, the VME interface can be reset with either a sysreset* on the backplane or by pushing the reset button on the front of the TDC card. Studies indicate that the interface does not always hang on the identical read within the sequence but there do seem to be certain places within the sequence where the hang occurs. This effect is almost always seen in boards with the ECO4 modification although there have been some isolated instances of similar behavior in non-modified boards. There is a definite crate slot dependence on this effect. Boards in this state are most often found in slots 8 and 16, although boards in neighboring slots such as 9 and 17 can also go into this state. In order to see this effect, it also seems that a large number of boards must be installed in the crate.

Ron Moore has discovered that there is an unexpected reset of the DSP associated with this type of hang and that these spurious resets are caused by glitches on the sysreset* line. An examination of the board artworks showed that the sysreset* line is routed in parallel with the vme_data(25) line for several inches mostly underneath the P1 connector. Just recently, Ron reported capturing on a scope the correlation between edges on the vme_data(25) line and the spurious resets of the DSP. It appears, therefore, that there is a cross-talk issue between these two lines. Ron has also discovered that this effect does not seem to be as isolated to certain slots within the crate as we first thought. This effect has now been observed in a wide variety of slots within various test crates.

C. Blown Buffer Chips

There are two specific buffer chips on the TDC board which suffer failures on a regular basis and must be replaced. These buffer chips connect the VME data bus to the DSP data bus. An analysis of the failed chips performed by the chip manufacturer indicates these failures are likely due to the chips attempting to drive too much current onto the bus. The most likely set of events that would lead to this scenario would be if multiple chips were attempting to drive the bus at the same time. A number of board modifications have been made to attempt to fix this problem. A small board was fabricated to plug into one of the TDC card diagnostic connector that connects a diode to each data line on the DSP data bus. The addition of this board seemed to slow down the rate of blown buffer chips but was not able to eliminate the problem altogether. The next modification known as ECO3 was to add pull-up resistors to two VME control lines. This modification did not solve the problem either. The final modification was to add a pull-up resistor to the VME control signal cs0*. The evidence that we have collected so far seems to indicate that this last change has been effective. There is a similar slot dependent effect for TDC boards which blow buffer chips to that which is observed in the soft VME interface lock-up condition described above. Boards in slots 8 and 16 seem to blow buffer chips at a greatly increased rate compared to those in other slots. The rate is also increased to a somewhat lesser extent in the slots immediately adjacent to these main two. On the other hand, it should be noted that there have been cases where all boards installed in a crate have experienced blown buffer chips at a single time. In some cases, there is a definite correlation between power cycling or power glitches and buffer chips being blown. It should also be noted, however, that there are examples of buffer chips blowing where no power cycling was known to have occurred.

D. Large Data Input Issue

Readout tests have shown that in some cases where a TDC is forced to process an extremely large number of input pulses, the TDC can hang and give bus errors. In order to recover a TDC from this state, a sysreset* must be issued on the backplane. This problem does not seem to be limited to the TDC readout modes in which VME polling of the boards occurs during DSP processing. In order to deal with this problem during the commissioning run, the COT thresholds had to be raised above a certain level. It was thought that this problem might have disappeared, but Arnd Meyer checked a couple of days ago and was able to reproduce the problem.

E. Local Polling Mode Problem

There is a known glitch that occurs within a programmable PAL on the TDC card that causes some data corruption issues on the TDC board. This effect is seen in the local polling readout mode of the TDC card in which the crate processor continually checks the status registers of the boards while DSP processing is ongoing to determine which board is ready to be read out first. The VME read of the status register causes the DSP to temporarily halt its processing to allow the transaction to occur. The handshake between the DSP and VME interface causes this glitch. The end result of this problem is that the data subsequently read out of the board sometimes contains illegal header words that cause a halt to the run.

F. VME activity Problem

There is another readout mode of the TDC card in which readout of the TDC FIFO for an event takes place while the DSP processing of the next event is taking place. In this case there should be no handshake between the VME interface and DSP because the TDC is designed to allow for readout of the FIFO without any DSP interaction. However, similar data corruption symptoms are seen to those described above for TDC readout in local polling mode.

G. Bunch Counter Errors

Under certain running conditions, the bunch counter value reported in the TDC header word will disagree with the value read out in the rest of the detector on a small fraction of events. For the COT crates this problem only occurs in the local polling mode where the crate processor is continually reading the TDC status registers during DSP processing to determine which card is ready to be read out first. In this run mode, typically one TDC within a crate will output a bunch counter value that is inconsistent with the bunch counter value reported from the other cards in the crate. These types of errors are seen sporadically while running in this mode. When an incorrect bunch counter value is reported, subsequent events read out from the same TDC card have the correct bunch counter values indicating that the board is able to recover automatically. Another place where bunch counter errors are seen is in the CLC crate. The one TDC in this crate sporadically reports bunch counter values that disagree with the rest of the detector readout. For some reason, these disagreements are seen in more than one readout mode (not just local polling mode). The CLC crate is unique in that there is an ADMEM card in this crate that is read out while DSP processing in the TDC card is taking place. The readout code is set up to read out the ADMEM card while TDC DSP processing is underway. This suggests that any VME activity on the backplane during DSP processing may lead to bunch counter errors.

H. Mezzanine Interface Problem

There is a known bug with another programmable PAL on the TDC board that controls VME transactions to/from registers on the trigger mezzanine board. If one attempts to read a register location that does not exist on the installed mezzanine card, a problem inside this PAL can in a small number of cases cause the VME interface on the board to go into a hung state.