SEU Performance of TAG Based Flip Flops

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35-WORD ABSTRACT:

We describe heavy ion test results for two new SEU tolerant latches based on transition nand gates, one for single rail asynchronous and the other for dual rail synchronous designs, implemented in AMI 0.5μprocess.

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INTRODUCTION

The transition and or nand gate, which we call a TAG[1], has the property that the output transitions only when both inputs have transitioned, and is useful for certain types of voting. It can be very simply implemented in CMOS by using series "and" wired FET's on both the high and low side of a gate as shown in Fig. 1.

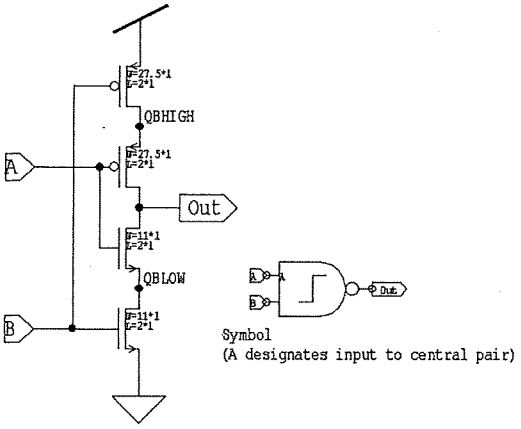

Fig. 1: Schematic diagram of 2-input transition nand gate (TAG). Depends on capacitive loading at node "Out" to retain previous value when inputs do not agree. Note that signals on interior node "A" may be capacitively coupled to the output node. Since this may be important in some circuits, the symbol designates the "A" node.

Whenever two logic signals are available which should agree and errors in the agreement are transient, the TAG may be used to eliminate the transient errors. This may be thought of as a voting circuit in which three things are being voted: the two inputs and the existing output node state. We might expect that a circuit which can suppress transient errors would be useful in mitigating single event upset (SEU) effects. This paper presents two latch designs using TAG's and heavy ion test data on flip flops constructed from those latches.

4-TAG LATCH FOR DUAL RAIL LOGIC

In a dual rail design[2] all logic signals are duplicated. If used with latches which only change state when inputs agree such as the Whitaker cell[3], this eliminates SEU errors. TAG's can also be used to make such a latch. Replacing the first inverter of a latch with a TAG allows the two input signals to be voted when setting the latch, guaranteeing that transient errors are not captured. Replacing the second inverters of a pair of latches with TAG's allows them to be cross coupled and vote each other's internal state, suppressing SEU induced errors occurring in the latch itself. Such a circuit is shown in Fig. 2.

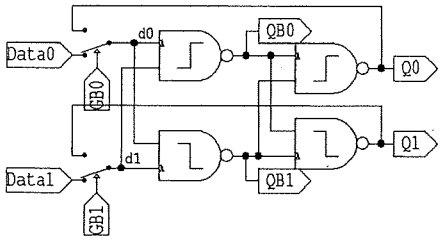

Fig. 2: Schematic diagram of a static self-correcting 4-TAG latch for use with dual rail logic. Data0 and Data1 are the inputs, Q0 and Q1 the outputs, QB0 and QB1 the inverted outputs, and GB0 and GB1 the gate or clock signals.

This circuit is fully static CMOS with no bias currents and no critical transistor sizing.

3-TAG LATCH WITH ASYNCHRONOUS RESET

A well known technique used to harden a latch against SEU effects is a delay in the feedback loop of the latch greater than the expected transient duration, so that the transient error does not reinforce itself and become latched. Methods for accomplishing this include use of passive RC

elements or inverter strings. A minimum length string would be two inverters with FET's sized to provide the required delay given the circuit's loading. This is unsatisfactory because SEU arising in the delay itself may be longer than expected, a result we are planning to publish shortly. The problem can be solved by using a TAG to vote the input and output of the delay, so that no error arising within the delay can ever propagate out. To protect against errors in the TAG, a second TAG must be used, and the outputs of the two TAG's voted with a third TAG. The delay itself then protects against errors arising in the third TAG. This circuit is shown in Fig. 3.

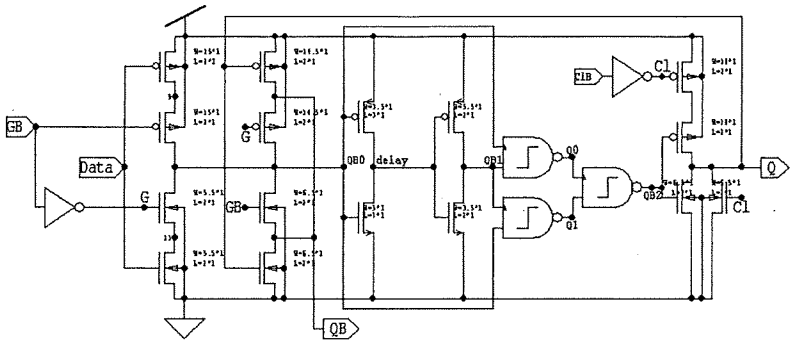

Fig. 3 Schematic of 3-TAG latch with asynchronous reset (clear) input. The delay element consists of inverters between nodes QB0 and QB1.

This latch is usable in ordinary single rail logic with a single clock line, and clock or clear inputs may be generated by other logic, as for example in a ripple counter.

TEST CIRCUITS

Test circuits for unprotected, 3-TAG, and 4-TAG flip flops consisted of two pair of dual 12 bit counters (48 flip flops) driven by a 20 mHz clock. Unprotected and 3-TAG circuits used ripple counters, and the 4-TAG used a synchronous counter with dual rail logic. Each pair of counter bits were exclusive or'd to detect errors. The errors were latched on the rising clock edge, and counted (3 additional flip flops). The test was conducted by monitoring LED's attached to the error counter bits. Fig. 4 shows the 3-TAG test circuit.

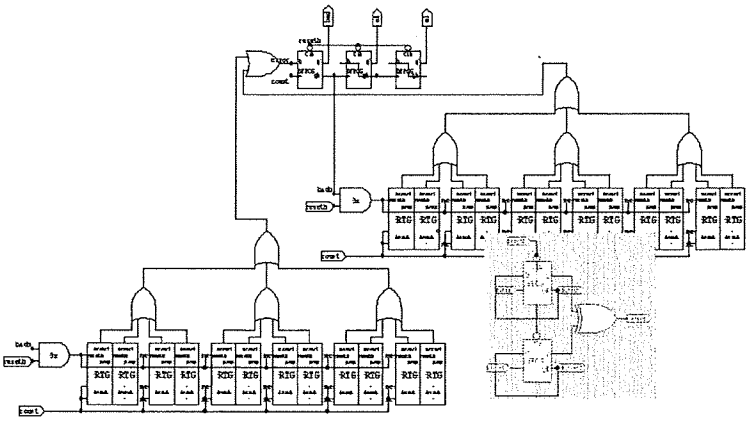

Fig. 4: Test circuit schematic for 3-TAG flip flops. Each d-type flip flop consists of two latches. The unprotected reference flip flops were tested with an identical circuit to this one. The 4-TAG flop flops used synchronous counters and dual rail logic.

The circuits described were fabricated using the AMI 0.5 micron process, and tested with lids removed in the Radiation Effects Facility of the Texas A&M Cyclotron Institute.

TEST PROCEDURE AND DATA

The heavy ion cyclotron test was conducted on April 27, 2005, and required 7 hours of beam time. The ion species, incident angles, effective LETs, and number of errors are presented in Table 1 below. A fluence of 1E6 ions/cm^2 was used for each ion species.

Ion Species	Incident Angle	$LET_{effective}$	Total # errors in 1e6 fluence per 51 flip flops		
			Unprotected	3-TAG	4-TAG
Argon (Ar)	0°	8.8	0	0	0
Copper (Cu)	0°	21	5	0	0
Krypton (Kr)	0°	29	5	0	0
Copper (Cu)	60°	41	20	0	0
Krypton (Kr)	60°	59	25	1	0
Silver (Ag)	60°	88	47	12	0
Gold (Au)	60°	175	80	40	0

Table 1: Test Data

The beam was applied to the test device and the entire fluence was delivered in a single run while the errors accumulated. The device was then rested and the prepared for the next run. The incident angle was either 0 degrees or 60 degrees (in order to achieve a higher LET due to the cosine of the incident angle). After all testing, the error cross sections were derived by dividing the total number of errors at each data point by the total fluence (1E6 ions/cm^2 in every case).

ANALYSIS

The error cross-section data was fit assuming a Weibull distribution for the model cross-section ($\sigma(L)$):

$$\sigma(L) = \sigma_{sat} \left(1.0 - e^{\{-\{(L - L_{th})/W\}s\}} \right)$$

where L is the particle linear energy transfer (LET in MeV cm^2/mg) and the Weibull parameters are σ_{sat} (the saturation cross-section), L_{th} (the LET threshold), W and S (Weibull shape parameters). The resulting Weibull fit parameters are shown in Fig. 5.

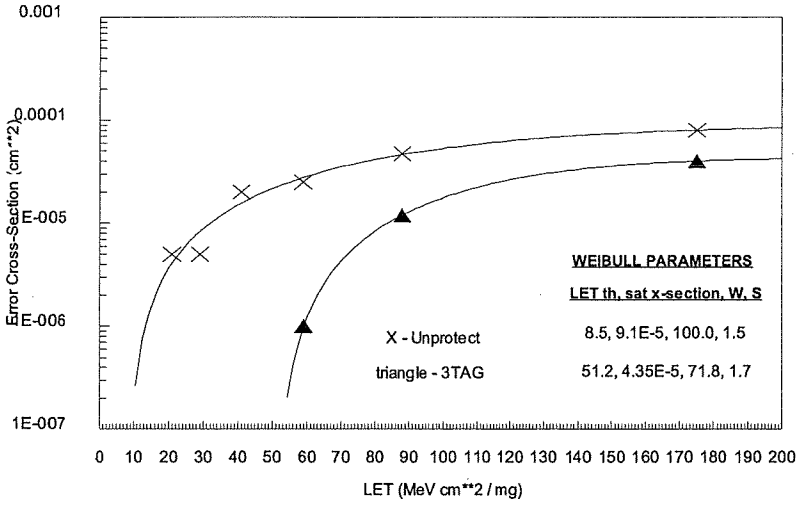

Figure 5: Error cross-section versus LET for parts tested

ON-ORBIT RADIATION ENVIRONMENT

The on-orbit error mean time between failure (MTBF) in years due to heavy ions for the parts tested was determined for both Low Earth Orbit (LEO) and Geosynchronous Earth Orbit (GEO) applications. The Galactic Cosmic Ray flux was modeled with a solar modulation algorithm [4], [5] whose accuracy has been demonstrated over four solar cycles. Orbit average environments were determined for solar minimum conditions with 0.1" thick spherical aluminum shielding for quiet conditions and no earth shadow. Transport and geomagnetic shielding models can be found in [6].

The nominal ionizing radiation environment for LEO errors assumes a 51.6 degree inclination at an altitude of 270 nmi and consists of only Galactic Cosmic Rays. (Note that the error rate provided here for LEO does not include errors due to secondary particles created by protons in the SAA because only heavy ion cross-section data is available for these parts at the time of writing - high energy proton test data is not available).

The nominal ionizing radiation environment for GEO errors assumes an altitude of 22,000 nm and consists of only Galactic Cosmic Rays with no earth magnetic shielding or trapped protons.

An analysis tool called "HiZ" developed at NASA-JSC was used to integrate the test data with the environmental assumptions described above. The tool calculates the expected on-orbit MTBF due only to heavy ions, and the results are listed below in Table 2.

Flip-Flop Device	*Calculated MTBF per 1000 flip flops*	
	LEO	*GEO*
Unprotected	230 years	11.7 years
3-Tag	6920 years	308 years
4-Tag	Indefinite	Indefinite

Table 2: MTBF (in years)

CONCLUSION

We conclude that the data support our claim that the TAG circuit is useful in designing SEU tolerant circuits. The 3-TAG configuration provides a robust general flip flop with asynchronous clear or preset compatible with existing design methods and easily scalable to CMOS processes now in use. For most applications it provides "practical" SEU immunity, with the MTBF being so large that errors from other sources would dominate reliability considerations. The 4-TAG configuration provides complete immunity in a relatively compact design for applications where dual rail logic is acceptable.

REFERENCES:

[1] R. L. Shuler, "Method and Apparatus for Reducing the Vulnerability of Latches to Single Event Upsets," US Patent # 6,492,857, Dec. 2002.

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[4] Badhwar, G. D. and P.M. O'Neill, "Galactic Cosmic Radiation Model and Its Applications," Advances in Space Research, Vol. 17, No. 2, 1996.

[5] Badhwar, G. D. and P.M. O'Neill, "Time Lag of Twenty Two Year Solar Modulation," Proceedings of the International Cosmic Ray Conference, SH 6.21, Calgary, July 19-30, 1993.

[6] Adams Jr., J. H., "Cosmic Ray Effects on Microelectronics, Part IV," Naval Research Laboratory Memorandum Report 5901, December 31, 1986.