Fine pitch grids for an x-ray solar imaging spectrometer fabricated by optical lithography and XeF_2 etching

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ABSTRACT

We have developed fine pitch, sub-collimating X-ray grids for an instrument in the High Energy Solar Spectroscopic Imager[1] (HESSI), a proposed NASA mission. in addition to high-energy X-rays, the instrument requires collimation of photons with energies of less than 4 keV such that free-standing grids are required that have no material between the grid slats. We have fabricated 25 micrometer thick gold grids that can collimate photons from visible light up to 30 keV X-rays. They are 55 millimeters in diameter and have 200 micrometer thick silicon support structures. The fabrication process starts with 200 micrometer thick 3 inch wafers onto which a 50 angstrom chrome, 300 angstrom gold electroplating strike is e-beam evaporated. A 25 micrometer thick optical resist is deposited on the wafers using a low spin rate. The resist is exposed and developed and an oxygen plasma clean is performed to fully strip resist residue from the strike. 25 micrometers of gold is then plated in the resist mold, resulting in a gold grid with photoresist between each gold slat. The wafer is turned over and a 50 micrometer dry resist is patterned such that it has a array of 1 by 4 millimeter openings to the silicon. The silicon is etched through to the chrome/gold strike using a xenon difluoride etching process. Both types of photoresist are removed with acetone followed by a piranha clean and the chrome/gold strike is removed with a hydrochloric acid and hydrogen peroxide chrome etch which also slowly etches gold.

Keywords: x-ray collimators, x-ray grids, thick films, high aspect ratio structures, integrated processes, xenon difluoride, silicon etch, MEMS electroplating

2. INTRODUCTION

Both thick and thin fine-featured grids are required for the High Energy Solar Spectroscopic Imager (HESSI), a proposed NASA mission that will promote the understanding of solar particle acceleration and explosive energy release in the magnetized plasmas at the Sun. These grids have a required minimum pitch that is determined by the expected angular resolution of the imager and have a required minimum and maximum thickness that is governed by the photon energy bandwidth desired for the X-ray imager.

The HESSI mission proposes to perform high resolution imaging and spectroscopy observations in the soft X-ray, hard X-ray, and gamma-ray regimes, with finer angular resolution (nearly 2 arc seconds) and finer energy resolution (approximately 1 keV) then has been previously possible. This combination of imaging and spectroscopy is achieved with a set of Rotating Modulation Collimators placed in front of an array of cooled germanium and silicon

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detectors. A set of 12 bi-grid collimators, each of which consists of a pair 01' widely-separated grids is used to provide the imaging. Each grid consists of a planar array of equally-space, parallel, X-ray opaque, slats separated by X-ray transparent slits. If the slits of each grid are parallel 10 each other, and the pitch is identical for the two grids, then the transmission through the. grid pair depends on the direction of incidence of the incoming X-rays as shown in Fig. 1. For slits and slats of equal width, the transmission varies between zero and 50% depending on whether the shadows of the slats in the top grid fall on the slits or slats of the lower grid. A complete transmission cycle from zero to 50% and back to zero corresponds to a change in source direction that is given by p/f., where *L* is the separation between the grids. The angular resolution is then given by *p/(2L)*.

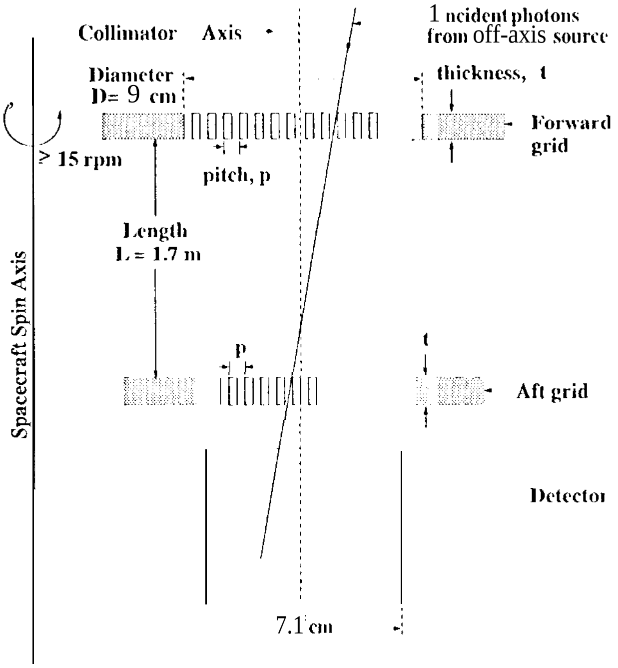

Figure 1 **Schematic of forward and aft grids in the Rotation Modulation Collimator. Note off-axis photon path.**

The finest angular resolution is therefore a function of the smallest pitch of the grids. For a minimum resolution of 2 arc seconds and a grid separation of 1.7 inters, the pitch of the finest grid must be 34 micrometers. Each grid must be almost perfectly identical with the **RMS** pitch of each grid of each pair being within 1 part in 10000. The tolerances for each grid as to slat width, thickness variation, and slat position are much less stringent, being on the order to 5% to 10%. The active grid area of the lower, or aft, grid must have a diameter of 7.1 centimeters and the front grid a diameter' of 8.9 centimeters.

3. GRID REQUIREMENTS AND DESIGN

The thick grids that arc required to collimate high-energy X-rays are fabricated with gold slats with acrylic spacers in between them and while these acrylic pieces are transparent to high energy X-rays, they are opaque to lower energy X-rays. Additional grids must be used that can collimate these lower energy photons. These grids can be thinner than the (hick grids because they only need to collimate the low energy X-rays that cannot be effectively collimated by the grids with the acrylic spacers. For maximum transmission of tbc low energy X-rays, the slots between the gold slats in these grids must not have any material in them. Further, in order to be able to characterize the grids without the. usc of collimated X-rays, a laser measurement system must be used to verify the geometrical

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accuracy of the grids. This also requires that the thin grids have no material in the grid slots or, at worst, a very transparent material.

Except for thickness and overall active area diameter, the requirements for a pair of these thin grids are similar to those for the thicker grids: 34 µm pitch, 17 µm openings between the gold slats, and correspondence between the RMS pitch of each of the grids of the pair to within 1 part in 10000. The thickness of the gold grid must be such that the grid can collimate X-rays with energies from 2 keV up to 30 keV and can be mechanically self-supporting over some small area. The active area or diameter of these grids can be much smaller than the active area of the thick grids because the fluence of the X-rays from the sun increases greatly with decreasing photon energy. Further, the necessary active area for X-rays in the 2 keV range can be several orders of magnitude smaller than that for X-rays in the 30 keV range. This has an important implication; the gold grid can be supported by a substrate that is semi-transparent to X-rays in the 10 keV to 30 keV and has a number of openings in it which allow lower energy X-rays through, This allows a sufficient number of photons through in each energy range.

Serendipitously, the fabrication technology of the gold grid section for the grid-and-substrate configuration described above had already been developed for making X-ray masks for deep etch X-ray lithography or LIGA (Lithographie, Galvanoformung, Abformung), which is being used to fabricate the. thick collimating grids for the HESSI project[2] These masks consist of a gold absorber on a 200 µm thick silicon wafer. The same absorber pattern used for the thick grids can also be used to define the thin grids. The gold absorber pattern for the X-ray mask process is 25 µm thick and grids of this thickness can effectively collimate X-rays up to 30 keV.

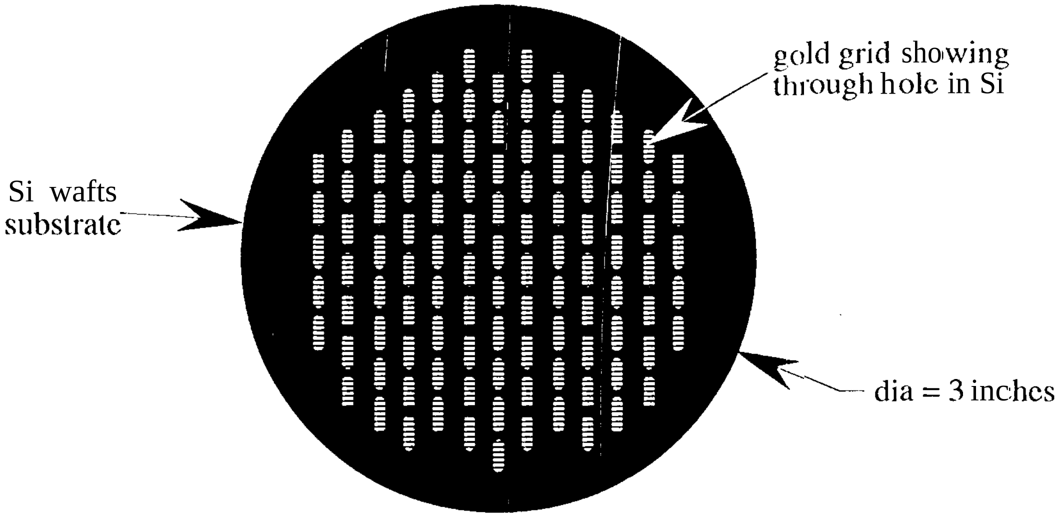

Figure 2. Schematic of grid assembly. Each hole is 1 mm wide by 4 mm long.

For proof-of-concept fabrication, a three inch (7.5 cm) diameter wafer of silicon is chosen for the substrate. Due to processing and mounting limitations, the gold grid on the substrate is limited 6 centimeters in diameter. The area with holes through the substrate is approximately 5.5 centimeters in diameter. Nominal size for each hole is 1 mm wide by 4 mm long with each end rounded as shown in Fig. 2. The grid pitch is 34 µm with each slat being 17 µm wide. A series of stiffeners with a pitch of 500 µm run perpendicular to the grids slats.

For characterization purposes, the holes must be placed such that a portion of each gold slat across the whole Si wafer is visible through the holes. This means that the boles must be staggered so that no grid slot is blocked by the solid parts of the wafer the full distance across the wafer.

For maximum mechanical strength and stability, the holes are separated by a distance of 3 millimeters and each line of holes is staggered by **50%**. This separation results in 3 directions of direct, continuous support offered by the silicon remaining between the holes as shown in Fig. 3.

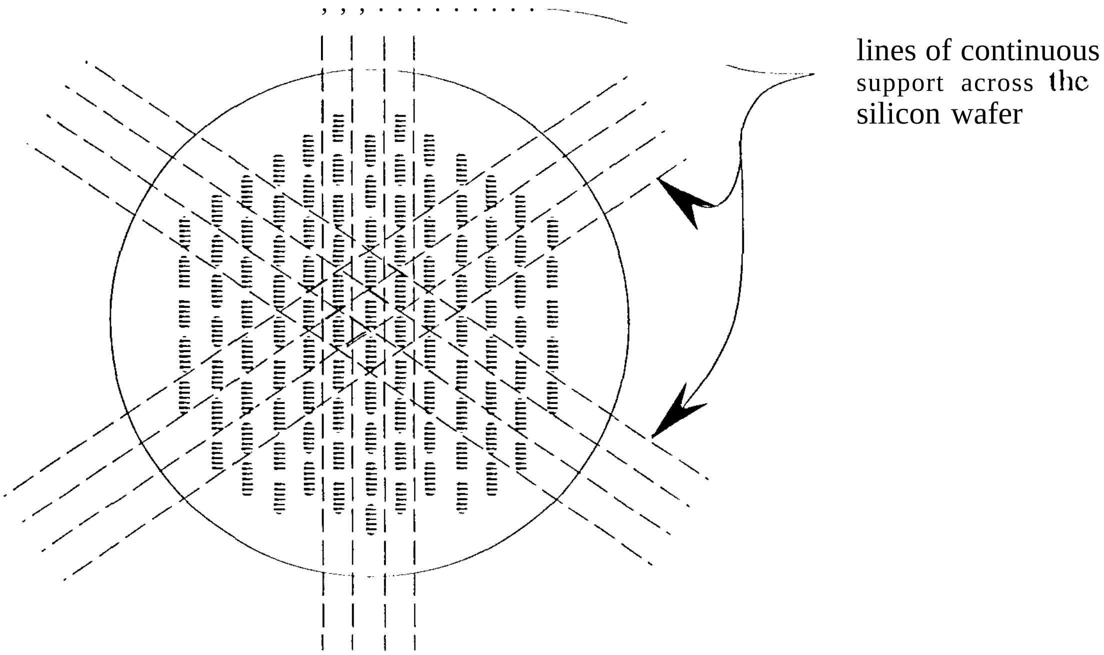

Figure 3. Schematic of silicon wafer with etched holes in it. The three sets of lines denote direct lines or beams of silicon.

4. FABRICATION

4.0 Fabrication summary

The grids are fabricated by depositing an electroplating strike on to a silicon wafer. A patterned layer of photoresist is put down on the strike and gold is then electroplated in 'to this photoresist mold. A dry film resist is deposited and holes are created in it through to the backside of the wafer. A xenon difluoride, XeF_2, gas phase etchant is then used to etch through the wafer to the gold grid on the front, The advantage of using the gas phase etchant being that there are no liquid/gas interfaces and the selectivity of the XeF_2 for silicon is very, very high. Then the first layer of the photoresist and the strike are removed and the wafer is mounted into an Invar ring.

4.1 Wafer preparation

Three inch silicon wafers are coated with an evaporated 50 Å Cr layer followed by a 200 to 300 A layer of gold which is used as a seed layer for electroplating. These wafers are then soaked for 5 minutes in AZ400K developer (from Hoechst) at room temperature followed by a water rinse. The wafers are blow-dried with nitrogen and further dried on a hotplate at 100 °C for at least 5 minutes. HMDS is then applied using a 20 second soak and' is then spin dried at 2500" rpm for 60 seconds.

4.2 Resist deposition, patterning, and development

The positive photoresist AZP4620 from Hoechst is spun on in a single, 25 µm thick layer at 400 rpm for 40 seconds followed by a 1 second, 1000” rpm spin to reduce edge bead effects. The wafer is then proximity-baked for 1 minute at a distance of 3 millimeters from a 110 °C surface. The wafer is then place on the 110 °C surface for 4 minutes. The resist is patterned using broad band (unfiltered) UV light from a mercury source for 1.9 minutes at 10 mW/cm^2 on a Karl Suss MJB3 contact aligner. The filter is removed because it has been found that exposure times are extremely long when the longer UV wavelengths are removed. The edge bead in the resist is exposed as well using a dark circle to shield the central portion of the wafer. The sample is developed approximately 5 minutes in 4:1 diluted AZ400K developer. The wafer is rinsed in DI water and dried with nitrogen,

4.3 Electroplating

An oxygen plasma cleaning is performed on the resist side of the wafer. This step is required to clean the surface of the gold seed layer. Without this step, the electroplating process is not reliable anti large variations in plating rate occur over the wafer. in extreme cases, no plating occurs at all. initial efforts in electroplating gold into the resist were made using a potassium gold cyanide. bath. This basis bath was not easily compatible with the AZP4620 resist and delamination of the resist from the substrate was only eliminated by doing an initial plating of copper. Subsequently an acidic gold electrolyte was found and the electroplating of gold is performed using a Technics 25E sodium gold sulfite bath with a pH of approximately 3.8 and a temperature of approximately 51.6 °C. The current density is 0.003 A/cm^2 (3 A/ft^3). The photoresist is left in place.

4.4 Si etching

Etching of silicon can be performed by using sublimed gas from XeF_2. The XeF_2 gas etches the silicon with reaction products that are all gaseous and can be carried away by a vacuum pump[3,4]. The etch is isotropic and very selective with respect to most other materials, including SiC, Si_3N_4, SiO_2, and photo resists as well as most metals and polymers. Photoresist masks were used for this work due to the ease of their application but non-polymeric materials are preferred for masking since the silicon etch rate is reduced with photoresist[5].

A negative dry film resist (Hercules MP215 1.5) is rolled onto the back side of the silicon wafer. The mask consists of a pattern printed on an overhead transparency using a 600 dots per inch laser printer since the resolution and accuracy of the pattern was not important for the holes through the silicon. The resist was exposed for 5 minutes under a flood UV lamp. This lamp is not optimized for UV photoresist exposure, The resist is then baked for 2 minutes at 90 °C. Developing is performed using a standard developer not designed for thick dry film resist. Develop time was 250 seconds with constant agitation. The sample is then immediately rinsed in water for 2 minutes with light agitation. The sample is baked again for 4 minutes at 60 °C to ensure adhesion. Areas of silicon, such as the wafer edges and sections of the front of the wafer that were not covered by the gold grid and thick resist, were coated with photoresist to prevent etching.

The silicon is etched within a glass bell jar approximately 1 liter in volume as shown in Fig. 4. The silicon wafer is placed back-side-up and the chamber pumped down to approximately 50 mTorr and purged with nitrogen 3 times to remove moisture. The valve to the chamber containing the XeF_2 crystals is opened and closed and the etching chamber is again purged. This process is then repeated.

Two types of etching are performed during this etch process – continuous etching and pulsed etching. The continuous etching consists of pumping the chamber down to 25 mTorr and then opening the valve to the XeF_2 chamber a small amount. The etching chamber vacuum pumping is adjusted such that the pressure remains a continuous 2000 mTorr while etching is desired. Pulsed etching consists of pumping down the etch chamber to 25 mTorr, closing tile pumping valve, opening the valve to the XeF_2 chamber, int reducing the XeF_2 gas until a pressure of 1800 mTorr is reached, closing the XeF_2 chamber valve, and then repeating the process. The etching time is determined by the time from the opening of valve to the XeF_2 chamber to the pumping, back down to 25 mTorr.

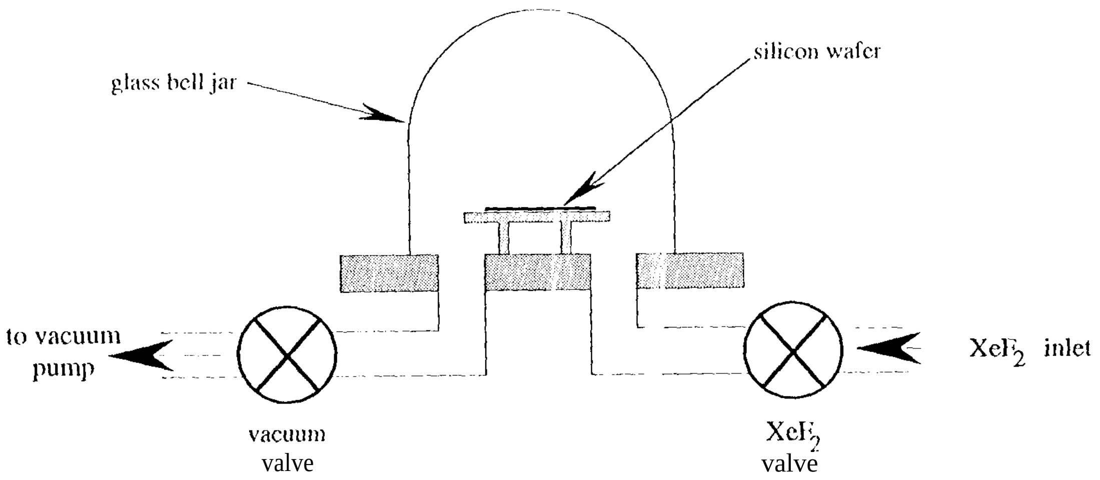

Figure 4. Schematic of XeF_2 etching chamber.

Both types of etching were used during the etching of the approximately 4 square centimeters of exposed silicon on the two samples presented here. On the first sample, there was 250 minutes of continuous etch time and 132 minutes of pulse etch time over 178 **cycles.** On the second sample, there was 270 minutes of continuous etch time and 95 minutes of pulse etch time over 115 cycles. Both samples were successfully etched through but the etch process configuration was slightly different between the two. There was a considerable loading effect that occurred over the exposed silicon surface of the wafer. The areas near the edges of the wafer etched faster than the center. The outer perimeter of the etching area was covered with a 1 centimeter wide ring of acetate after that outer 1 centimeter etched through to the grid. This slowed the etch process at the outer portions. A second ring was added when the next 1 centimeter of perimeter etched through. When the remaining central area etched through, the masking rings were removed and final etching was performed to etch back the edges of the holes so that they matched the mask holes.

4.5 Cleaning and mounting of the sample

The resist used to define the grid and the dry film resist used to mask the silicon for the XeF_2 etch are removed in a piranha bath ($5{:}1\ H_2SO_4{:}H_2O_2$). A very small amount of etching of the thin Cr/Au electroplating strike occurs during the process but a Cr etchant ($3{:}1\ HCL{:}H_2O_2$), which also very slowly etches gold, is used to remove thoroughly the strike from between the gold grid slats in the areas where the silicon is etched through.

The wafer is mounted in an Invar ring to reduce thermal expansion problems. The wafer is glued to the Invar ring using a clear fingernail polish. This polish provides good adhesion but is extremely easy to remove in the case that the wafer must be transferred to a different holder.

5. RESULTS AND CONCLUSIONS

The finished grids are shown in Fig. 5. The gold grid pattern remains intact and the holes through the silicon meet the requirements for transmissive area, particularly since the holes are overetched. The unetched silicon forms a strong support structure for the gold grid while the surrounding unetched silicon ring provides a good mounting interface.

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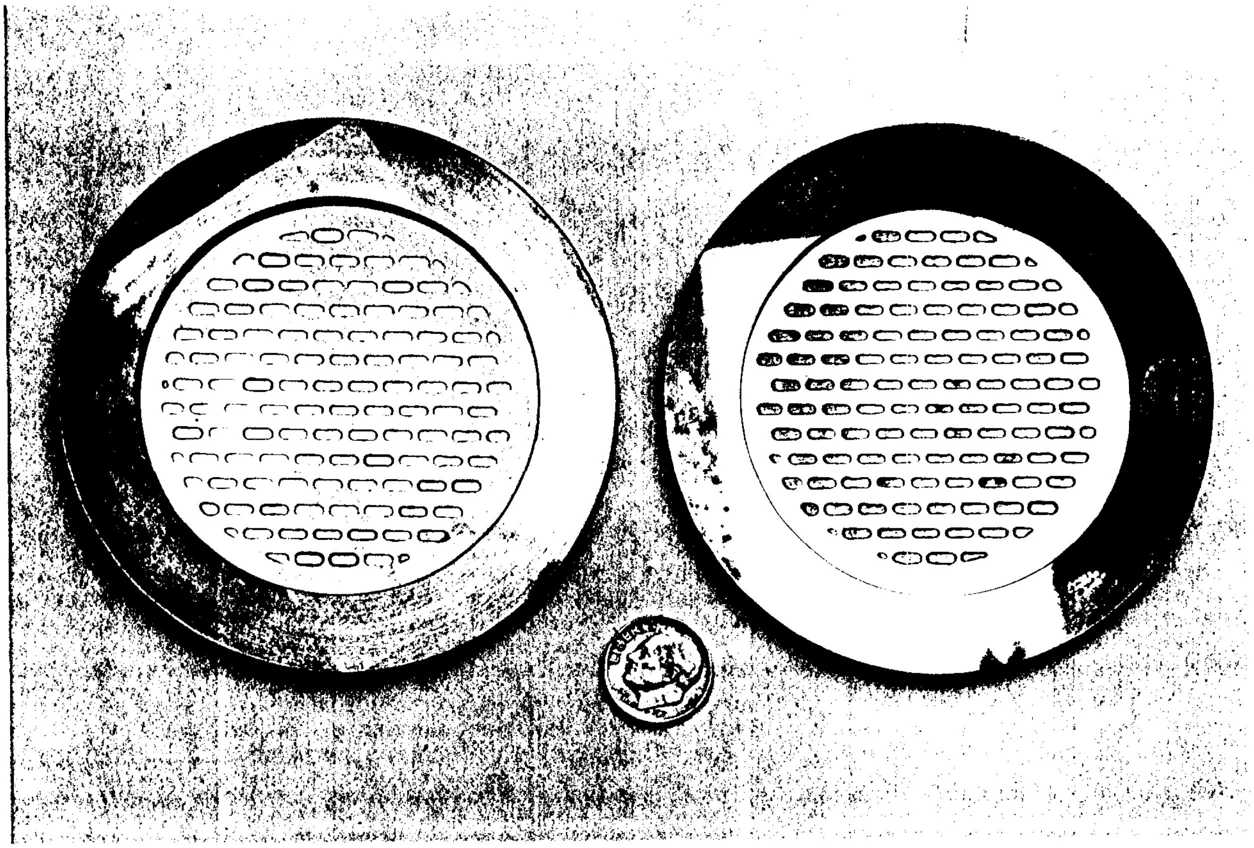

Figure 5. Photograph of gold grids from back side of the wafer. The diameter of the silicon visible through the Invar ring is 65 mm.

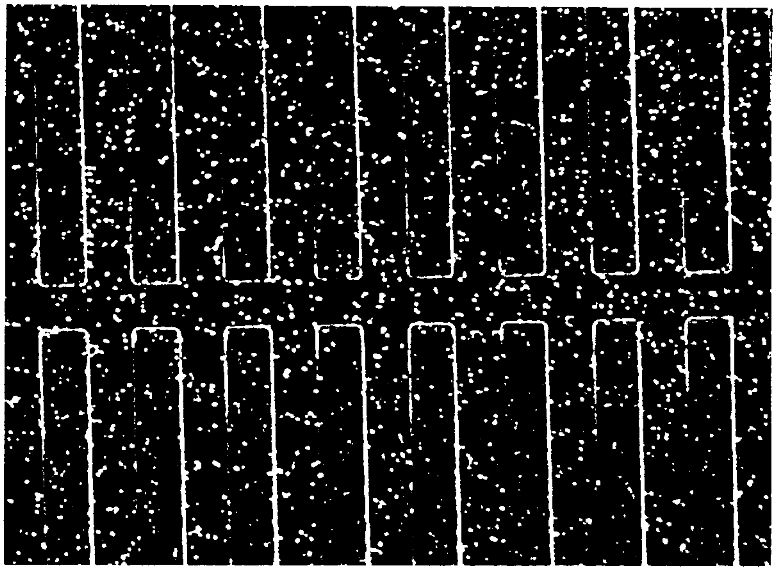

Figure 6. Photographic dark field image close up of grids from back side of wafer. The white specks are residue on the surface of the electroplating strike before removal. The dark horizontal bar is a gold stiffener connecting the dark vertical gold slats. Each bar is 17 μm wide.

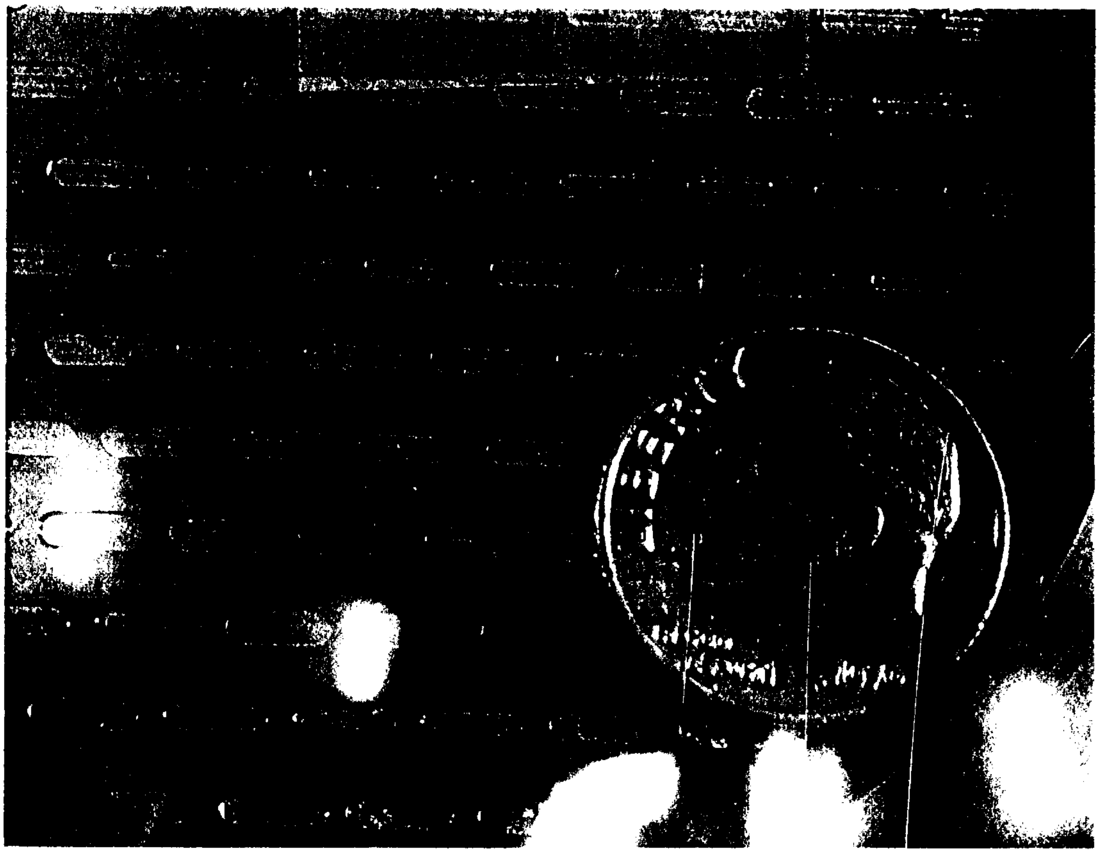

Figure 7. Photograph of gold grids from back side of the wafer (magnification = 3X). The grid slats run vertically in this view and the stiffeners run horizontally and parallel to the holes.

The electroplating strike is quite robust before removal and can withstand repeated rinsing in liquid and a moderate flow of nitrogen directed at it from an air gun. A photograph of the strike before removal is shown in Fig. 6. After strike removal, the slots between the gold slats are free of material and the strike appears to have been completely removed from between the gold grid slats. The gold grid adheres quite well to the silicon substrate. This is a concern because in an earlier test sample the grid partly delaminated from the silicon wafer, perhaps due to over-etching and undercutting during the removal of the electroplating: strike from between the grid slats. However, the gold grid is quite robust and during the partial delamination the grid maintained not only its integrity but also its registration.

The holes through the silicon wafer are all larger than the nominal 1 by 4 mm, as can be seen in Figs. 7 and 8. This was due to the difficulty in getting an even etch rate over the whole exposed area. Some areas etched faster than others and these areas had significant undercutting as the sidewalls show in Fig. 9. 'There was also some etching of small areas that had been coated with thin layers of resist for simple protection. This may have been due to flaws in the coating or there may have been some small amount of etching of the mist.

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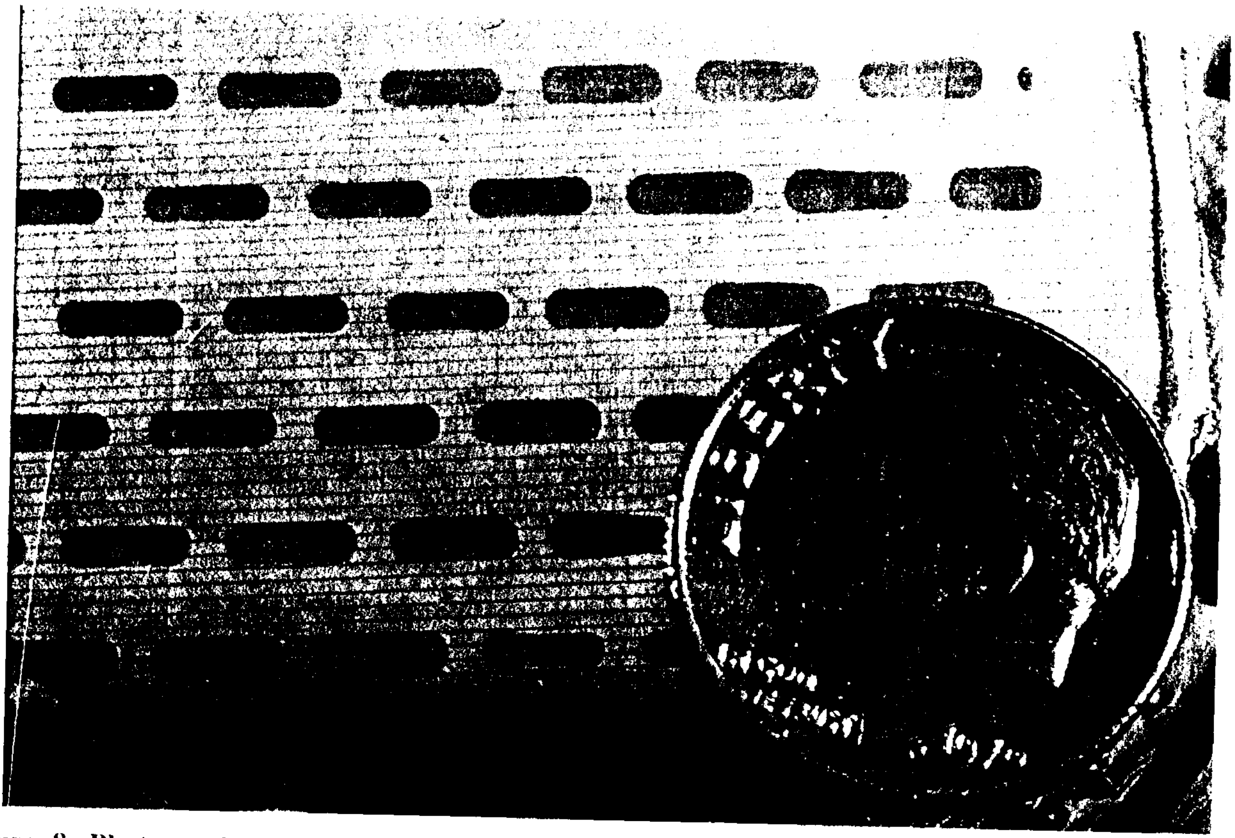

Figure 8. Photograph of gold grids from front side of the wafer - the side with the gold grids (magnification = 3X). The grid slats run vertically in this view and the stiffeners run horizontally and parallel to the holes.

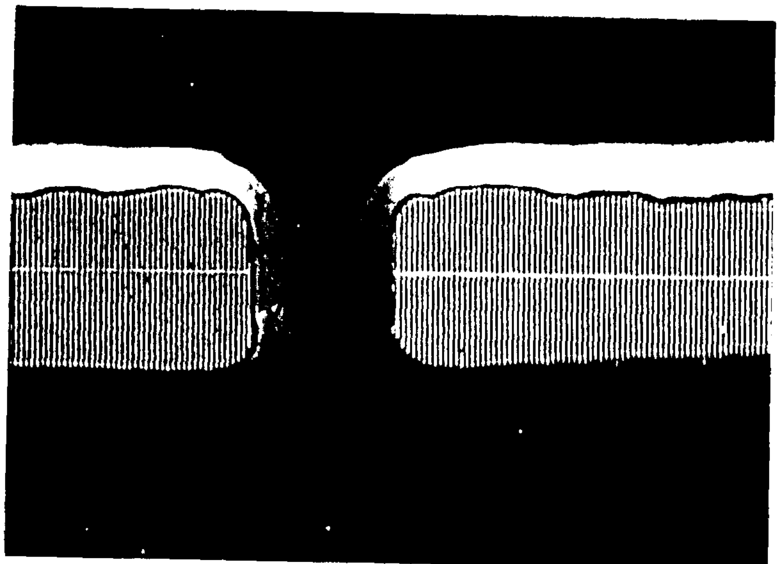

Figure 9. Photograph of gold grids from back side of wafer (magnification = 20X).

We have demonstrated a process by which thick gold patterns with high horizontal Resolution can be fabricated on a silicon substrate with subsequent removal of' sections of the silicon substrate to allow backside access to, and possible passage through, the gold patterns on the front side. This has potential applications not just for high energy photon optics but also for IR, visible light, and UV optics as well.

The grids have been characterized using a visible light calibration system to verify the required registration of the grids and the grids meet the registration specifications to the limit of the characterizing system. The gold grids are nominally 25 μm thick and are within 1 0% of that value over the area of the grid. These grids have been shown to be usable for the collimation purpose for which they were designed and are. capable of being easily tested by laser techniques while in place on a flight instrument.

6. ACKNOWLEDGMENTS

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