PPM-91-612

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78

UNISYS

Interoffice Memorandum

To
W. Beyah
Department
Code 300.1
From
K. Sahu KS
Department
7809
Subject
Radiation Report on ISTP
Non-Common Buy Part No. SMJ320C30GBM28

PPM-91-612
Date
October 11, 1991
Location
Lanham
Telephone
731-8954
Location
Lanham
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A radiation evaluation was performed on SMJ320C30GBM28 to determine the total dose tolerance of these parts. A brief summary of the test results is provided below. For detailed information, refer to Tables I through V and Figure 1.

The total dose testing was performed using a cobalt-60 gamma ray source. During the radiation testing, eight parts were irradiated under bias (see Figure 1 for bias configuration), and two parts were used as control samples. The total dose radiation steps were 2.5, 5, and 7.5 krads. After 7.5 krads, parts were annealed at 25°C for 68 hours. Irradiation was continued to 10 krads, followed by cumulative annealing steps of 24, 48, 72 and 168 hours at 25°C, and an additional annealing step of 48 hours at 100°C. The dose rate was between 125 to 170 rads/hour, depending on the total dose level (see Table II for radiation schedule). After each radiation exposure and annealing treatment, parts were electrically tested according to the test conditions and the specification limits listed in Table III.

All eight parts passed all functional and ICC tests up to 2.5 krads. After 5 krads, SN 53 failed three functional tests and five parts marginally exceeded the maximum specification limit of 1350mA for ICCD, the dynamic ICC, with maximum readings of 1400mA. After 7.5 krads, all parts failed functional tests and exceeded the specification limit for ICCD. After 68 hours of annealing, two parts (SNs 55 and 59) recovered to pass all tests and SN 52 recovered to pass ICCD.

On continued exposure to 10 krads (cumulative), all parts failed three functional tests (Nos. 3, 4 and 5). In addition, two parts (SNs 52 and 59) exceeded the maximum specification limit of 1350mA for ICCS, the static ICC, and one part (SN 59) failed functional test #2. However, no ICCS failures were observed after 24 hours of annealing, and fewer functional failures were

observed after cumulative annealing treatments of 48 and 72 hours. Also, SN 55 fully recovered to pass all tests. After 168 hours of annealing, two more parts (SNs 57 and 59) recovered to pass all tests and SNs 53 and 58 recovered to pass ICCD. After 48 hours of high temperature annealing (100°C), three more parts recovered to pass all functional tests and no ICCD failures were observed. Strangely, SN 57 failed three functional tests (Nos. 2, 4 and 5).

Table IV provides a summary of functional test results after each radiation/annealing step. Table V provides the mean and standard deviation values from the static and dynamic ICC measurements made after each radiation and annealing step. Appendix A is provided for detailed information on the functional testing of the parts.

Any further details about this evaluation can be obtained upon request. If you have any questions, please call me at 301-731-8954.

TABLE I. Part Information

Generic Part Number:	SMJ320C30GBM28
ISTP Non-Common Buy Part Number:	SMJ320C30GBM28
ISTP Non-Common Buy Control Number:	2149
Charge Number:	C14288
Manufacturer:	Texas Instruments
Quantity Procured:	16
Lot Date Code:	9025
Quantity Tested:	10
Serial Numbers of Radiation Samples:	52, 53, 54, 55 56, 57, 58, 59
Serial Numbers of Control Samples:	50, 51
Part Function:	32-bit Digital Signal Processor
Part Technology:	CMOS
Package Style:	180-pin grid array
Test Engineer:	J. Lander

TABLE II. Radiation Schedule

EVENTS	DATE
1) Initial Electrical Measurements	09/03/91
2) 2.5 krads irradiation @ 140 rads/hr	09/03/91
Post 2.5 krads Electrical Measurements	09/04/91
3) 5 krads irradiation @ 170 rads/hr	09/04/91
Post 5 krads Electrical Measurements	09/05/91
4) 7.5 krads irradiation @ 125 rads/hr	09/05/91
Post 7.5 krads Electrical Measurements	09/06/91
5) 68 hrs annealing at 25°C	09/06/91
Post 68 hr Electrical Measurements	09/09/91
6) 10 krads irradiation @ 150 rads/hr	09/09/91
Post 10 krads Electrical Measurements	09/10/91
7) 24 hrs annealing at 25°C	09/10/91
Post 24 hr Electrical Measurements	09/11/91
8) 48 hrs annealing at 25°C	09/10/91
Post 48 hr Electrical Measurements	09/12/91
9) 72 hrs annealing at 25°C	09/10/91
Post 72 hr Electrical Measurements	09/13/91
10) 168 hrs annealing at 25°C	09/10/91
Post 168 hr Electrical Measurements	09/17/91
11) 48 hrs annealing at 100°C	09/17/91
Post 48 hr Electrical Measurements	09/19/91

Notes:

- All parts were radiated under bias at the cobalt-60 gamma ray facility at GSFC.
- All electrical measurements were performed off-site at 25°C.
- Annealing performed at 25°C under bias.

Table III. Electrical Characteristics of SMJ320C30GBM28

(1) Functional #1 : Tests for the ability to Reset the DUT.
(2) Functional #2 : Tests for the ability to Receive and store Commands and DMA.
(3) Functional #3 : Tests Floating point Multiplier, registers, Internal RAM and Microinstructions.
(4) Functional #4 : Tests Digital Speech Processing Capabilities.
(5) Functional #5 : Tests Digital Waveform Processing Capabilities.
(6) ICCSB is the Stand-By current for the entire Evaluation module + DUT.
(7) ICCD is the Dynamic current at Maximum speed for the entire Evaluation module + DUT.
(8) Quiescient Current for the Evaluation module without the DUT measured 750mA.

These parts were tested using a 386 based PC, with an emulator board provided by Texas Instruments. Five different programs were used to test separate features of the CPU. All of these programs were used to test the functionality of the parts at maximum speed (30MHz) and for the ICC Dynamical test.

TABLE IV: Summary of Functional Test Results after Total Dose Exposures and Annealing for SMJ320C30GBM28

Functional Test	Initials	Total Dose Exposure (krads)			Anneal @ 25°C	TDE (krads)
		2.5	5	7.5	68 hrs	10
1	Pass	Pass	Pass	Pass	Pass	Pass
2	Pass	Pass	Pass	7P/1F	Pass	7P/1F
3	Pass	Pass	7P/1F	1P/7F	5P/3F	Fail
4	Pass	Pass	7P/1F	Fail	3P/5F	Fail
5	Pass	Pass	7P/1F	Fail	3P/5F	Fail

Functional Test	Annealing @ 25°C				Annealing @ 100°C
	24 hrs	48 hrs	72 hrs	168 hrs	48 hrs
1	Pass	Pass	Pass	Pass	Pass
2	7P/1F	Pass	6P/2F	Pass	6P/2F
3	2P/6F	2P/6F	3P/5F	5P/3F	7P/1F
4	1P/7F	1P/7F	1P/7F	3P/5F	5P/3F
5	1P/7F	2P/6F	3P/5F	4P/4F	5P/3F

TABLE V: Summary of Electrical Measurements after Total Dose Exposures and Annealing for SMJ320C30GBM28 1/

Parameters		Spec. Limits min	Spec. Limits max	Initials mean	Initials sd	Total Dose Exposure (krads) 2.5 mean	2.5 sd	5 mean	5 sd	7.5 mean	7.5 sd	Anneal @ 25°C 68 hrs mean	68 hrs sd	TDE (krads) 10 mean	10 sd
ICCS	mA	-	1350	900	0	934	17	1106	39	1259	35	1063	35	1297	64
ICCD	mA	-	1350	1119	43	1163	22	1344	39	1366	349	1309	47	1519	61

Parameters		Spec. Limits min	Spec. Limits max	Annealing @ 25°C 24 hrs mean	24 hrs sd	48 hrs mean	48 hrs sd	72 hrs mean	72 hrs sd	168 hrs mean	168 hrs sd	Annealing @ 100°C 48 hrs mean	48 hrs sd
ICCS	mA	-	1350	1197	59	1156	53	1138	48	1081	43	900	0
ICCD	mA	-	1350	1444	53	1419	54	1388	65	1325	50	1144	30

Note:

1/ The mean and standard deviation values were calculated over the eight parts irradiated in this testing. The control samples remained constant throughout the testing and are not included in this table.

Figure 1. Radiation Bias Circuit for SMJ320C30GBM28

PIN	NAME	FUNCTION	PIN DESCRIPTION	RADIATION BIAS
F14	EMU(0)	IN	*RESERVED*	TO 20KOHM TO VCC
E15	EMU(1)	IN	*RESERVED*	TO 20KOHM TO VCC
F13	EMU(2)	IN	*RESERVED*	TO 20KOHM TO VCC
E14	EMU3	OUT	*RESERVED*	TIE TO VCC/2
F12	EMU4	IN	*RESERVED*	TO 20KOHM TO VCC
C1	EMU(5)	*N/C*	*RESERVED*	*N/C*
M0	EMU(6)	*N/C*	*RESERVED*	*N/C*
J3	RSV(0)	IN	*RESERVED*	TO 20KOHM TO VCC
J4	RSV(1)	IN	*RESERVED*	TO 20KOHM TO VCC
K1	RSV(2)	IN	*RESERVED*	TO 20KOHM TO VCC
K2	RSV(3)	IN	*RESERVED*	TO 20KOHM TO VCC
L1	RSV(4)	IN	*RESERVED*	TO 20KOHM TO VCC
K3	RSV(5)	IN	*RESERVED*	TO 20KOHM TO VCC
L2	RSV(6)	IN	*RESERVED*	TO 20KOHM TO VCC
K4	RSV(7)	IN	*RESERVED*	TO 20KOHM TO VCC
M1	RSV(8)	IN	*RESERVED*	TO 20KOHM TO VCC
L3	RSV(9)	IN	*RESERVED*	TO 20KOHM TO VCC
M2	RSV(10)	IN	*RESERVED*	TO 20KOHM TO VCC

Figure 1. (continued)

(24 PINS)

PIN	NAME	FUNCTION	PIN DESCRIPTION	RADIATION BIAS
F15	A0	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
G12	A1	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
G13	A2	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
G14	A3	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
G15	A4	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
H15	A5	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
H14	A6	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
J15	A7	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
J14	A8	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
J13	A9	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
K15	A10	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
J12	A11	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
K14	A12	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
L15	A13	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
K13	A14	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
L14	A15	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
M15	A16	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
K12	A17	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
L13	A18	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
M14	A19	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
N15	A20	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
M13	A21	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
L12	A22	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2
N14	A23	OUT, HI-Z	PRI. BUS ADDRESS	TIE TO VCC/2

(13 PINS)

PIN	NAME	FUNCTION	PIN DESCRIPTION	RADIATION BIAS
A13	XA0	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
A14	XA1	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
D11	XA2	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
C12	XA3	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
B13	XA4	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
A15	XA5	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
B15	XA6	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
C14	XA7	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
E12	XA8	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
D13	XA9	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
C15	XA10	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
D14	XA11	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2
E13	XA12	OUT, HI-Z	SEC. BUS ADDRESS	TIE TO VCC/2

Figure 1. (continued)

(32 PINS)

PIN	NAME	FUNCTION	PIN DESCRIPTION	RADIATION BIAS
C4	D0	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
D5	D1	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A2	D2	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A3	D3	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
B4	D4	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
C5	D5	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
D6	D6	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A4	D7	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
B5	D8	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
C6	D9	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A5	D10	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
B6	D11	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
D7	D12	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A6	D13	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
C7	D14	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
B7	D15	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A7	D16	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A8	D17	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
B8	D18	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A9	D19	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
B9	D20	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
C9	D21	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A10	D22	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
D9	D23	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
B10	D24	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A11	D25	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
C10	D26	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
B11	D27	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
A12	D28	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
D10	D29	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
C11	D30	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2
B12	D31	I/O, HI-Z	PRIM. BUS DATA	TIE TO VCC/2

Figure 1. (continued)

(32 PINS)

PIN	NAME	FUNCTION	PIN DESCRIPTION	RADIATION BIAS
Q4	XD0	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
P5	XD1	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
N6	XD2	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q5	XD3	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
P6	XD4	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
M7	XD5	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q6	XD6	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
N7	XD7	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
P7	XD8	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q7	XD9	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
P8	XD10	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q8	XD11	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q9	XD12	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
P9	XD13	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
N9	XD14	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q10	XD15	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
M9	XD16	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
P10	XD17	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q11	XD18	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
N10	XD19	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
P11	XD20	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q12	XD21	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
M10	XD22	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
N11	XD23	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
P12	XD24	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q13	XD25	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q14	XD26	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
M11	XD27	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
N12	XD28	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
P13	XD29	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
Q15	XD30	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2
P15	XD31	I/O, HI-Z	SECOND. BUS DATA	TIE TO VCC/2

Figure 1. (continued)

(9 PINS)

PIN	NAME	FUNCTION	PIN DESCRIPTION	RADIATION BIAS
G4	R/W_	OUT, HI-Z	PRI. BUS RD WR	TIE TO VCC/2
F2	STRB_	OUT, HI-Z	PRI. BUS STROBE	TIE TO VCC/2
E1	RDY_	IN	PRI. BUS READY	TIE TO VCC
F3	HOLD_	IN	PRI. BUS HOLD	TIE TO VCC
E2	HOLDA_	OUT	PRI. BUS HOLDACK	TIE TO VCC/2
D1	XR/W_	OUT, HI-Z	SEC. BUS RD WR	TIE TO VCC/2
E3	MSTRB_	OUT	SEC. BUS MEM STROBE	TIE TO VCC/2
F4	IOSTRB_	OUT	SEC. BUS I/O STROBE	TIE TO VCC/2
D2	XRDY_	IN	SEC. BUS READY	TIE TO VCC

(9 PINS)

PIN	NAME	FUNCTION	PIN DESCRIPTION	RADIATION BIAS
F1	RESET_	IN	RESET PIN	TIE TO VCC
H2	INT0_	IN	EXTERNAL INT 0	TIE TO GND
H1	INT1_	IN	EXTERNAL INT 1	TIE TO VCC
J1	INT2_	IN	EXTERNAL INT 2	TIE TO GND
J2	INT3_	IN	EXTERNAL INT 3	TIE TO VCC
G1	IACK_	OUT	INTERRUPT ACKNOW.	TIE TO VCC/2
D15	MC/MP_	IN	MICROCOMP/MICROPROC	TIE TO GND
G2	XF0	I/O, HI-Z	EXTERNAL FLAG 0	TIE TO VCC/2
G3	XF1	I/O, HI-Z	EXTERNAL FLAG 1	TIE TO VCC/2

(14 PINS)

PIN	NAME	FUNCTION	PIN DESCRIPTION	RADIATION BIAS
M5	CLKX0	I/O	SERIAL PORT 0 XCLK	TIE TO VCC/2
Q3	DX0	OUT, HI-Z	PORT 0 DATA XMIT	TIE TO VCC/2
Q2	FSX0	I/O	FRAME SYNC FOR XMIT	TIE TO VCC/2
N4	CLKR0	I/O	PORT 0 SERIAL RECV	TIE TO VCC/2
Q1	DR0	IN	DATA RECEIVE PORT 0	TIE TO VCC
P3	FSR0	IN	FRAME SYNC FOR RECV	TIE TO VCC
N2	CLKX1	I/O	SERIAL PORT 1 XCLK	TIE TO VCC/2
P2	DX1	OUT, HI-Z	PORT 1 DATA XMIT	TIE TO VCC/2
P1	FSX1	I/O	FRAME SYNC FOR XMIT	TIE TO VCC/2
L4	CLKR1	I/O	PORT 1 SERIAL RECV	TIE TO VCC/2
N1	DR1	IN	DATA RECEIVE PORT 1	TIE TO GND
M3	FSR1	IN	FRAME SYNC FOR RECV	TIE TO VCC
P4	TCLK0	I/O	TIMER CLOCK 0	TIE TO VCC/2
N3	TCLK1	I/O	TIMER CLOCK 1	TIE TO VCC/2

Figure 1. (continued)

(50 PINS)

PIN	NAME	FUNCTION	PIN DESCRIPTION	RADIATION BIAS
E5	LOCATOR	*N/C*	ORIENTATION PIN	*N/C*
H4	VDD(0)	VCC	POWER HARDWIRED	TIE TO VCC
D8	VDD(1)	VCC	POWER HARDWIRED	TIE TO VCC
M8	VDD(2)	VCC	POWER HARDWIRED	TIE TO VCC
H12	VDD(3)	VCC	POWER HARDWIRED	TIE TO VCC
L8	IODVDD(0)	VCC	POWER HARDWIRED	TIE TO VCC
M12	IODVDD(1)	VCC	POWER HARDWIRED	TIE TO VCC
D12	ADVDD(0)	VCC	POWER HARDWIRED	TIE TO VCC
H11	ADVDD(1)	VCC	POWER HARDWIRED	TIE TO VCC
M4	PDVDD	VCC	POWER HARDWIRED	TIE TO VCC
D4	DDVDD(0)	VCC	POWER HARDWIRED	TIE TO VCC
E8	DDVDD(1)	VCC	POWER HARDWIRED	TIE TO VCC
H5	MDVDD	VCC	POWER HARDWIRED	TIE TO VCC
C8	VSS(0)	GND	GROUND HARDWIRED	TIE TO GND
H5	VSS(1)	GND	GROUND HARDWIRED	TIE TO GND
H13	VSS(2)	GND	GROUND HARDWIRED	TIE TO GND
N8	VSS(3)	GND	GROUND HARDWIRED	TIE TO GND
C5	DVSS(0)	GND	GROUND HARDWIRED	TIE TO GND
C13	DVSS(1)	GND	GROUND HARDWIRED	TIE TO GND
N5	DVSS(2)	GND	GROUND HARDWIRED	TIE TO GND
N13	DVSS(3)	GND	GROUND HARDWIRED	TIE TO GND
B2	CVSS(0)	GND	GROUND HARDWIRED	TIE TO GND
P14	CVSS(1)	GND	GROUND HARDWIRED	TIE TO GND
B14	IVSS	GND	GROUND HARDWIRED	TIE TO GND
D5	VBBP	*N/C*	VBB PUMP OSC. OUT	*N/C*
E4	VSUBS	GND	SUBSTRATE PIN	TIE TO GND
C2	X1	OUT	OUT OSC CRYSTAL	TIE TO VCC/2
B1	X2/CLKIN	IN	IN FROM CRYSTAL	TIE TO VCC
B5	H1	OUT	EXTERNAL H1 CLOCK	TIE TO VCC/2
A1	H3	OUT	EXTERNAL H3 CLOCKL	TIE TO VCC/2

RADIATION BIAS CIRCUIT CONDITIONS

1) TIE TO VCC/2 MEANS OUTPUT IS TIED TO VCC/2 THROUGH A RESISTOR.

2) ALL INPUT & OUTPUT RESISTOR VALUES -> 2.4K OHMS +/- 10% , 1/4 WATT
EXCEPT FOR EMU(0,1,2), EMU4 & RSV(0..12) WHERE THE RESISTOR VALUES
ARE -> 20K OHMS +/- 10% , 1/4 WATT

3) VCC = 5V +/- 0.25V , GND = 0.0V , VCC/2 = 2.5V +/- 0.25V

Appendix A

```
/*****************************************************************/
/*  EVM_reset()                                                  */
/*                                                               */
/*  Reset the TMS320C30 EVM and intialize the TBC for default operation.*/
/*                                                               */
/*  Operations:    Reset the EVM                                 */
/*         Intialize the TBC                                     */
/*         Toggle the TMS320C30 reset pin                        */
/*         Check to see if the EVM is reset                      */
/*         Poll the EVM for reset/intialization complete         */
/*****************************************************************/

int     EVM_reset()
  {
        int  i;

        outport(ctladdr+SC_C30EVM_RESET,0);

        outport(ctladdr+SC_REG_CNTL2,SC_CTL2_MODE0 | SC_CTL2_MODE1);

        outport(ctladdr+SC_REG_CNTL4,SC_DEFAULT_CABLE_DELAY |
                    SC_CTL4_DSOURCE_TDI0 |
                    SC_CTL4_TDI_FALL_EDGE |
                    SC_CTL4_EVENT_FALL_EDGE);

        outport(ctladdr+SC_REG_CNTL3,SC_CTL3_CLKOUT_OFF |
                    SC_CTL3_ECD |
                    SC_CTL3_FORMAT_MPSD);

        outport(ctladdr+SC_REG_CNTL5,SC_CTL5_EVT3_OUTPUT |  SC_CTL5_SET_EVT3);
        outport(ctladdr+SC_REG_CNTL5,SC_CTL5_EVT3_OUTPUT & ~SC_CTL5_SET_EVT3);

        outport(ctladdr+SC_REG_CNTL1, 5);
        if(inport(ctladdr+SC_REG_CNTL1) != 5)
        return(-1);
        else
        outport(ctladdr+SC_REG_CNTL1,0);

        /*************************************************************/
        /* The following code fixes an intialization timing bug.     */
        /* Wait until C30 indicates that reset intialization is complete.*/
        /*************************************************************/
        if(EVM_status(MREAD_ACK))   return(0);
        else return(-1);
```

FUNCTIONAL TEST #1

```
*************************************************************************
*                                                                       *
*      FUNCTIONAL TEST # 2 ----->   EVMTEST COMMAND                     *
*                                                                       *
*      Intializes the TMS320C30 EVM                                     *
*      then the following operations are tested :                       *
*                                                                       *
*      Operations:  Disable/clear interrupts                            *
*                   Set the data page and stack pointers                *
*                   Enable the cache                                    *
*                   Intialize the memory ports                          *
*                   Intialize the AIC                                   *
*                   Enable INT0 and GIE to handle command interrupts    *
*                   Wait in IDLE loop for interrupts                    *
*                   Set up timer 0 to supply AIC master clock           *
*                   Reset the AIC                                       *
*                   Intial the serial ports                             *
*                   Take AIC out of reset                               *
*                   Intialize the AIC                                   *
*                   Enable receive interrupts                           *
*                                                                       *
*************************************************************************
```

FUNC #2 (cont..)

E\ SET COMMAND ALSO USES THE FOLLOWING ROUTINES TO TEST THE TMS320C30 :

```
**************************************************************
*  dmaread                                                   *
*                                                            *
*  DMA setup routine to read data C30 memory and write to host *
*  communications register.  The transfers are interrupt driven *
*  from host reads.                                          *
*                                                            *
*  As the communications register is only 16 bits wide the   *
*  upper half of the data bus is garbage. The host must do   *
*  one dummy read on the front end to fill the buffer.       *
**************************************************************
*  dmawrite                                                  *
*                                                            *
*  DMA setup routine to read data from the communications reg. *
*  and write to C30 memory.  The transfers are interrupt driven *
*  from host writes.                                         *
*                                                            *
*  As the communications register is only 16 bits wide the   *
*  upper half of the data bus is garbage.                    *
*                                                            *
**************************************************************
*  -md_write()                                               *
*                                                            *
*    .ansfer command parameters from the comm. port to command *
*  structure.                                                *
**************************************************************
*  hwrite16                                                  *
*                                                            *
*  Read data from communications register and store in C30 mem. *
*  Data is stored as 16 bit value with 16 msb's set to zero. *
**************************************************************
*  hread()                                                   *
*                                                            *
*  Read data from c30 memory and write to communications reg. *
*                                                            *
**************************************************************
*  hwrite32                                                  *
*                                                            *
*  Read data from communications register and store in C30 mem. *
*  Data is read from host as two 16 bit values and added to  *
*  form a 32 bit value.                                      *
**************************************************************
*  hread32                                                   *
*                                                            *
*  Read data from C30 memory and store to communications reg. *
*  Data is read from c30 memory as 32 bit and adjusted to write *
*  16 bit values as required.                                *
*  **********************************************************
*    .adone                                                  *
*                                                            *
*  Turn off DMA on completion.                               *
**************************************************************
```

```
*-------------------------------------------------------------------*
*
*         UNISYS DEFENSE DIVISION
*         TMS320C30 COMMAND TEST PROGRAM -->  FUNCTIONAL TEST #3
*         DEVELOPED BY   : JUAN R. LANDER
*         LAST REVISION : 07-25-91
*
*-------------------------------------------------------------------*

*         PROCESSOR INITIALIZATION FOR THE TMS320C30.

*         RESET AND INTERRUPT VECTOR SPECIFICATION. THIS ARRANGMENT
*         ASSUMES THAT DURING THE LINKING, THE FOLLOWING TEXT SEGMENT
*         WILL BE PLACED TO START AT MEMORY LOCATION 0.

          THE FOLLOWING ARE USED TO VERIFY THE OPERATION OF
          THE TMS320C30 :

*         INITIALIZATION SEQUENCE SUBROUTINE

*         INTERNAL DATA MEMORY TESTING

*         STORE AND RECALL CONTENTS OF ALL REGISTERS

*         INTEGER DIVISION OF R0/R1 INTO R0 (RESULT)

*         FIND THE RECIPROCAL OF A FLOATING POINT NUMBER v

*         FIND THE SQUARE-ROOT OF A FLOATING POINT NUMBER v
```

LPC_READ

Functional Test #4

TMS320C30 Evaluation Module System Demonstration
2400 BPS Full-Duplex Linear Predictive Coder

This demonstration consists of the following files.

```
    LPC_READ      :THIS FILE
    C30       ASM :ASSEMEBLY LANGUAGE COMPILER OUTPUT FOR C30.C
    LPC_C30A  ASM :ASSEMBLY CODED LPC ROUTINES
    LPC_C30C  ASM :ASSEMBLY LANGUAGE COMPILER OUTPUT FOR LPC_C30C.C
    VECS      ASM :RESET AND INTERRUPT VECTORS
--> LPC       BAT :BATCH FILE TO RUN DEMO  <--
    C30       C   :'C30 GENERIC EVM PROGRAMS
    LPC_C30C  C   :'C30 LPC C-CODED PROGRAMS
    LPC_PC    C   :HOST LPC PROGRAM
    PC        C   :HOST GENERIC EVM PROGRAMS
    LPC       CMD :'C30 LPC LINK COMMAND FILE
    LPC_PC    EXE :HOST LPC PROGRAM
    C30_1     H   :'C30 GENERIC EVM HEADER FILE 1: MACROS, STRUCTURES, PROTOTYPES
    C30_2     H   :'C30 GENERIC EVM HEADER FILE 2: GLOBAL VARIABLES
    LPC_C30   H   :'C30 LPC HEADER FILE: MACROS, STRUCTURES, PROTOTYPES, GLOBALS
    LPC_CMD   H   :'C30 & HOST SHARED COMMAND HEADER FILE
    LPC_PC    H   :HOST LPC PROGRAM HEADER FILE
    PC_1      H   :HOST GENERIC EVM HEADER FILE 1: MACROS, STRUCTURES, PROTOTYPES
    PC_2      H   :HOST LPC PROGRAM HEADER FILE 2: GLOBAL VARIABLES
    C30       OBJ :'C30 GENERIC EVM SOFTWARE OBJECT FILE
    LPC_C30A  OBJ :'C30 LPC ASSEMBLY CODE PROGRAMS OBJECT FILE
    LPC_C30C  OBJ :'C30 LPC C          CODE PROGRAMS OBJECT FILE
    LPC_PC    OBJ :HOST LPC PROGRAM OBJECT FILE
    PC        OBJ :HOST GENERIC EVM SOFTWARE OBJECT FILE
    VECS      OBJ :'C30 GENERIC EVM RESET/INTERRUPT VECTOR OBJECT FILE
    LPC       OUT :'C30 EXECUTABLE LPC PROGRAM
```

BEFORE RUNNING LPC.BAT

Before running the demonstration please run the OSC.BAT program. This program will present the user with an oscilloscope display of the input data. For linear predictive coding to work the input to the AIC must be as close to full-scale as possible without clipping. Using OSC.BAT the user should set the application on his input wave for (through some user provided device such as a amplifier or tape deck) to create an input that ALMOST spans the entire +/- 8192 range.

RUNNING LPC.BAT

TMS320C30 Evaluation Module

Application Demonstration

LPC-10 2400 Bit-per-second Speech Coder

F1 Record
F2 Play
F3 Silence - Turn off Gain on Output
F4 Hear - Restore Output Gain
F5 Raise Pitch
F6 Lower Pitch
F7 Natural Pitch (Cancel F5,F6,F8)
F8 Whisper - Remove Voicing
F9 Stop (Playback or Record)
END Quit

The user screen is shown above. Unless a command is requested the program normally takes the analog input applies the LPC-10 coder and then decodes and resynthesizes the output. The following commands are available. NOTE THAT IF A COMMAND IS ENTERRED DURING PLAYBACK OR RECORD, A FRAME OF DATA WILL BE LOST.

F1 - RECORD: The coded data will be recorded onto disk. The user will be prompted for a valid filename. Once recording begins, it will continue until the user hits F9 - STOP or until the disk storage buffer is full. The host program makes room for 10000 frames of data or 3 minutes 20 seconds. NOTE any voice commands (F6, F8, F9) will be ignored and only the true speech data will be recorded. Similarly, if SILENCE is selected (F3) the input speech and not dead silence will be recorded.

F2 - PLAYBACK: Will playback a previously recorded file. Prompts the user the user for a valid filename. Once playback begins it will continue until the user hits F9 - STOP. Until then it will continue playing the recorded data in a loop. Again the maximum file size stores 3 minutes 20 seconds of coded speech.

- SILENCE: Removes gain from output so that the EVM's Analog Interface circuit generates only zeroes for output.

F4 - HEAR: Restores output gain so that output can be heard.

F5 - RAISE PITCH: Increases pitch of voiced sounds to make the voice sound higher than normal.

F6 - LOWER PITCH: Increases pitch of voiced sounds to make the voice sound lower than normal.

F7 - TRACK: Use true voicing of pitch (i.e. cancel F5, F6, F7).

F8 - WHISPER: Removes all voicing to make speech sound like a whisper.

F9 - STOP: Stop a playback or record command.

END - QUIT: Terminate PC program. 'C30 software will continue running in previous state.

TMS320C30 Compilation Notes

This software was compiled with the TMS320C30 Version 4.00 Optimizing ANSI C Compiler with the following statement:

```
CL30 -mmn -om2 -g -s c30
CL30 -mmn -om2 -g -s lpc_c30c
```

Note that the stack size in the RTS.LIB (run-time support library has been decreased to 0x40 (64) words so that all data and stack can fit in on-chip memory. The assembly portions of the file were assembled as follows:

```
ASM30 lpc_c30a
ASM30 vecs
```

The resulting object files were then linked with the output file as follows:

```
LNK30 lpc.cmd
```

generates the output file LPC.OUT for the EVM.

OSC_READ

Functional Test #5

TMS320C30 Evaluation Module System Demonstration
AIC Data Acquisition Demonstration Oscilloscope Program

This demonstration consists of the following files.

```
    OSC_READ      :THIS FILE
    C30       ASM :ASSEMBLY LANGUAGE COMPILER OUTPUT FOR C30.C
    OSC_C30   ASM :ASSEMBLY LANGUAGE COMPILER OUTPUT FOR OSC_C30.C
    VECS      ASM :RESET AND INTERRUPT VECTORS
--> OSC       BAT :BATCH FILE TO RUN DEMO  <--
    C30       C   :'C30 GENERIC EVM PROGRAMS
    OSC_C30C  C   :'C30 OSCILLOSCOPE C-CODED PROGRAMS
    OSC_PC    C   :HOST OSC PROGRAM
    PC        C   :HOST GENERIC EVM PROGRAMS
    OSC       CMD :'C30 OSCILLOSCOPE LINK COMMAND FILE
    OSC_PC    EXE :HOST OSCILLOSCOPE PROGRAM
    C30_1     H   :'C30 GENERIC EVM HEADER FILE 1: MACROS, STRUCTURES, PROTOTYPES
    C30_2     H   :'C30 GENERIC EVM HEADER FILE 2: GLOBAL VARIABLES
    OSC_C30   H   :'C30 OSC. HEADER FILE: MACROS, STRUCTURES, PROTOTYPES, GLOBALS
    OSC_CMD   H   :'C30 & HOST SHARED COMMAND HEADER FILE
    OSC_PC    H   :HOST OSCILLOSCOPE PROGRAM HEADER FILE
    PC_1      H   :HOST GENERIC EVM HEADER FILE 1: MACROS, STRUCTURES, PROTOTYPES
    PC_2      H   :HOST OSCILLOSCOPE PROGRAM HEADER FILE 2: GLOBAL VARIABLES
    C30       OBJ :'C30 GENERIC EVM SOFTWARE OBJECT FILE
    OSC_C30   OBJ :'C30 OSC C          CODE PROGRAMS OBJECT FILE
    OSC_PC    OBJ :HOST OSC PROGRAM OBJECT FILE
    PC        OBJ :HOST GENERIC EVM SOFTWARE OBJECT FILE
    VECS      OBJ :'C30 GENERIC EVM RESET/INTERRUPT VECTOR OBJECT FILE
    OSC       OUT :'C30 EXECUTABLE OSC PROGRAM
    VECS      OBJ :'C30 GENERIC EVM RESET/INTERRUPT VECTOR OBJECT FILE
```

BEFORE RUNNING OSC.BAT

Note that this program requires an EGA display adapter an monitor capable of displaying 640 x 350 resolution.
Before running the demonstration please run the OSC.BAT program. This program This program will present the user with an oscilloscope display of the input data. Using OSC.BAT the user can test various parameter of the AIC and see how they affect the signal. The user can also tune the amplification of the user-provided circuit the drives the AIC so that the output reaches as close to full-scale as possible without clipping. That is the input should nearly span the entire display when showing the entire +/- 8192 range.

RUNNING OSC.BAT

TMS320C30 Evaluation Module

Upon starting OSC.BAT the user will be presented with a menu. Unless a command is requested, the program simply requests data from the EVM and displays in an oscilloscope window. NOTE THAT IF A COMMAND IS ENTERRED DURING PLAYBACK OR RECORD, A FRAME OF DATA WILL BE LOST.

F2,F3,F4 INCRMENT/DECREMENT A/B: These functions alter the AIC sampling and filter frequency paramenters. The parameters are clipped to a minimum of 1 and a maximum of 31 and 63 (for A and B respectively.) Also, once the sampling rate excedes the maximum TLC32044 AIC specification of 19.2 kHz, no changes causing the sampling rate to further increase will be allowed.

F7 Natural Pitch (Cancel F5,F6,F8)

F5 - HIGHPASS: Toggles ON/OFF status of input highpass filter. This filter is useful for removing any DC offset or power-supply noise.

END Quit

F6 - GAIN: Toggles expected full-scale input to aic. For example, if this was set to +/- 1.5 volts, a 1.5 volt input would generate a digitized sample of magnitude 8191. This threshold can be set to 1.5, 3, or 6 volts.

resynthesizes the output. The following commands are available. NOTE THAT

F7 - SINX / X CORRECTION FILTER: This filter corrects for the roll off of the AIC's output lowpass anti-aliasing filter. This command toggles the fitlers on/off status.

F1 - RECORD: The coded data will be recorded onto disk. The user will be
F8 - RECORD: The data will be recorded onto disk. The user will be prompted for a valid filename. Once recording begins, it will continue until the user hits F9 - STOP or until the disk storage buffer is full. The host program makes room for 24 K samples of data. This is three seconds of speech sampled at 8 kHz. data will be recorded. Similarly, if SILENCE is selected (F3)

F9 - PLAYBACK: Will playback a previously recorded file. Prompts the user the user for a valid filename. Once playback begins it will continue until the user hits F9 - STOP. Until then it will continue playing the recorded data in a loop. Again the maximum file size stores 24 K samples.
continue playing the recorded data in a loop. Again the maximum

F10 - STOP: Stop a playback or record command.

HOME - TOGGLE MAGNIFICATION: Toggles magnification of screen view.
circuit generates only zeroes for output.

END - QUIT: Terminate PC program. 'C30 software will continue running in previous state.

TMS320C30 Compilation Notes

F6 - LOWER PITCH: Increases pitch of voiced sounds to make the voice sound
This software was compiled with the TMS320C30 Version 4.00 Optimizing ANSI
C Compiler with the following statements:
F7 - TRACK: Use true voicing of pitch (i.e. cancel F5, F6, F7).

```
CL30 -mmn -om2 -g -s c30
CL30 -mmn -om2 -g -s osc_c30
```

Note that the stack size in the RTS.LIB (run-time support library has been
decreased to 0x40 (64) words so that all data and stack can fit in on-chip
memory. The assembly portions of the file were assembled as follows:
previous state.

```
ASM30 vecs
```

The resulting object files were then linked file as follows:

```
LNK30 osc.cmd
```

This software was compiled with the TMS320C30 Version 4.00 Optimizing ANSI
This generates the output file OSC.OUT for the EVM.

```
CL30 -mmn -om2 -g -s c30
CL30 -mmn -om2 -g -s lpc_c30c
```

Note that the stack size in the RTS.LIB (run-time support library has been
decreased to 0x40 (64) words so that all data and stack can fit in on-chip
memory. The assembly portions of the file were assembled as follows:

```
ASM30 lpc_c30a
ASM30 vecs
```

The resulting object files were then linked with the output file as follows:

```
LNK30 lpc.cmd
```

This generates the output file LPC.OUT for the EVM.