Chapter 5

Silicon Vertex Detector (SVX II)

5.1 Introduction

In 1992, a silicon vertex detector (SVX) was added to CDF to detect secondary vertices from heavy flavor weak decays and has proved to be an excellent tool for b-tagging in top searches and for b-physics. To control radiation damage, the original SVX was replaced with the SVX$'$ detector of similar geometry but using AC-coupled silicon detectors and a radiation hard readout chip.

The planned increase in the number of p and $\overline{p}$ bunches in the accelerator for Run II, and the resulting shorter bunch spacing (132 ns or 396 ns) requires a replacement for the SVX$'$ detector. We call the Run II silicon vertex detector SVX II [1]. The overall specifications of the SVX II detector are as follows:

- SVX II will be longer to provide more complete geometric coverage of the luminous region and to provide track information to $|\eta| < 2$ as shown in Fig. 5.1.
- The detectors will be double-sided to provide r-z readout for improved pattern recognition and 3-D vertex reconstruction with an impact parameter resolution $\sigma_\phi < 30$ μm and $\sigma_z < 60$ μm for central high momentum tracks.
- The detector should be sufficiently radiation hard for operation after a delivered luminosity of up to 3 fb^{-1}. The expected radiation dose for the Layer 0 sensors is approximately 0.5 Mrad/fb^{-1}.
- A 42 cell analog pipeline will store the data during the formation of the Level 1 trigger for either 396 ns or 132 ns between bunch crossings.
- The pipeline will be buffered and dual-ported to support simultaneous digitization and readout of data while additional analog data is entering the pipeline ("SVX3" chip). This permits a high Level 1 trigger accept rate of order 50 kHz with minimal deadtime.
- Digitization and readout of the SVX II analog data for Level 2 processing will take approximately 6-7 μs following a Level 1 trigger. The high speed of the readout is required in order to use the SVX II data in a Level 2 vertex trigger processor. A new Silicon Vertex Tracker (SVT) will find tracks with large impact parameters to be used in the trigger.

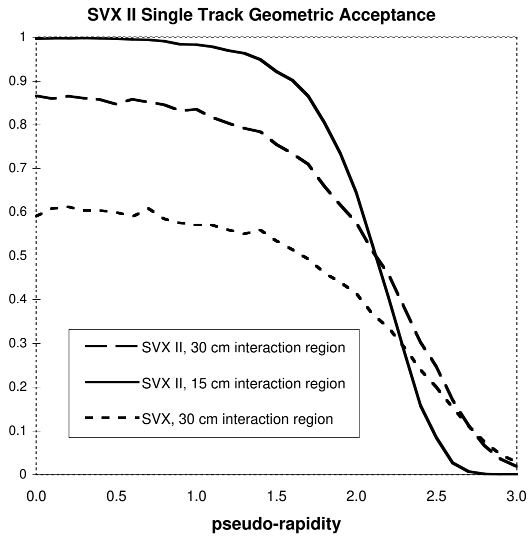

Figure 5.1: SVX II single track acceptance.

Table 5.1 compares SVX II design parameters with those of the current SVX$'$. The new detector will consist of three barrels, each 29 cm long. There are 12 wedges in ϕ, each with five layers of silicon. Of the five layers, three have 0°-90° stereo while two

Detector Parameter	SVX′	SVX II
Readout coordinates	r-ϕ	r-ϕ; r-z
Number of barrels	2	3
Number of layers per barrel	4	5
Number of wedges per barrel	12	12
Ladder length	25.5 cm	29.0 cm
Combined barrel length	51.0 cm	87.0 cm
Layer geometry	3° tilt	staggered radii
Radius innermost layer	3.0 cm	2.44 cm
Radius outermost layer	7.8 cm	10.6 cm
r-ϕ readout pitch	60;60;60;55 μm	60;62;60;60;65 μm
r-z readout pitch	absent	141;125.5;60;141;65 μm
Length of readout channel (r-ϕ)	25.5 cm	14.5 cm
r-ϕ readout chips per ladder	2;3;4;6	4;6;10;12;14
r-z readout chips per ladder	absent	4;6;10;8;14
r-ϕ readout channels	46,080	211,968
r-z readout channels	absent	193,536
Total number of channels	46,080	405,504
Total number of readout chips	360	3168
Total number of detectors	288	720
Total number of ladders	96	180

Table 5.1: Comparison of SVX′ and 5-layer SVX II.

have 1.2° small-angle stereo. This is designed to permit good resolution in locating the z-position of secondary vertices and to enhance the 3-D pattern recognition capability of the silicon tracker. For each barrel, the silicon ladders are mounted between two precision-machined beryllium bulkheads which also carry the water cooling channels for the readout electronics. Figure 5.2 shows a drawing of the SVX II bulkhead. The radial locations of the numbered labels shown in the figure are given in Table 5.2.

A sketch of the SVX II data acquisition system is shown in Fig. 5.3. The readout chips are mounted on an electrical hybrid on the surface of the silicon detectors. Including both sides of the detectors (r-ϕ and r-z or r-ϕ') there are 44 chips in a wedge with 12 wedges per barrel end and six barrel ends in total. Each readout chip set (SVX3) has 128 channels, each with a charge-sensitive amplifier, a 42-cell dual-ported pipeline with four additional cells for buffers, and an ADC. The chips from each wedge are read out over five high density interconnects (HDI), one per layer. The HDI's from each wedge are connected to a port card (PC) located around the periphery of the barrel ends. The PC decodes the control signals from the fiber interface board (FIB). Also at the PC, the analog data, already in digital form, are converted from electrical to optical signals by dense optical interface modules (DOIM's). Each DOIM drives a ribbon of optical fibers (eight data and one clock) at 53 MHz approximately 10 m to VME crates located on the sides of the CDF detector. This highly parallel readout permits the entire detector ($\approx$ 406,000 channels) to be read out in approximately 10 μs. The r-ϕ information is delivered to the SVT before the r-z/ϕ' information is read out.

Three VME crates on the west side of the CDF detector together house the FIB's and FIB fanout modules. Each PC is controlled by its respective FIB through a set of copper control lines with one FIB controlling 2 PC's. The FIB board generates control signals for the PC based on commands sent from the silicon readout controller (SRC) located in the CDF counting room. The command signals from the SRC are transmitted serially over a single high speed optical link (G-link) running at 1.5 GHz. They are processed at the FIB crate by a fanout module which distributes them to the FIB boards over the J3 backplane. In addition to its command function, each

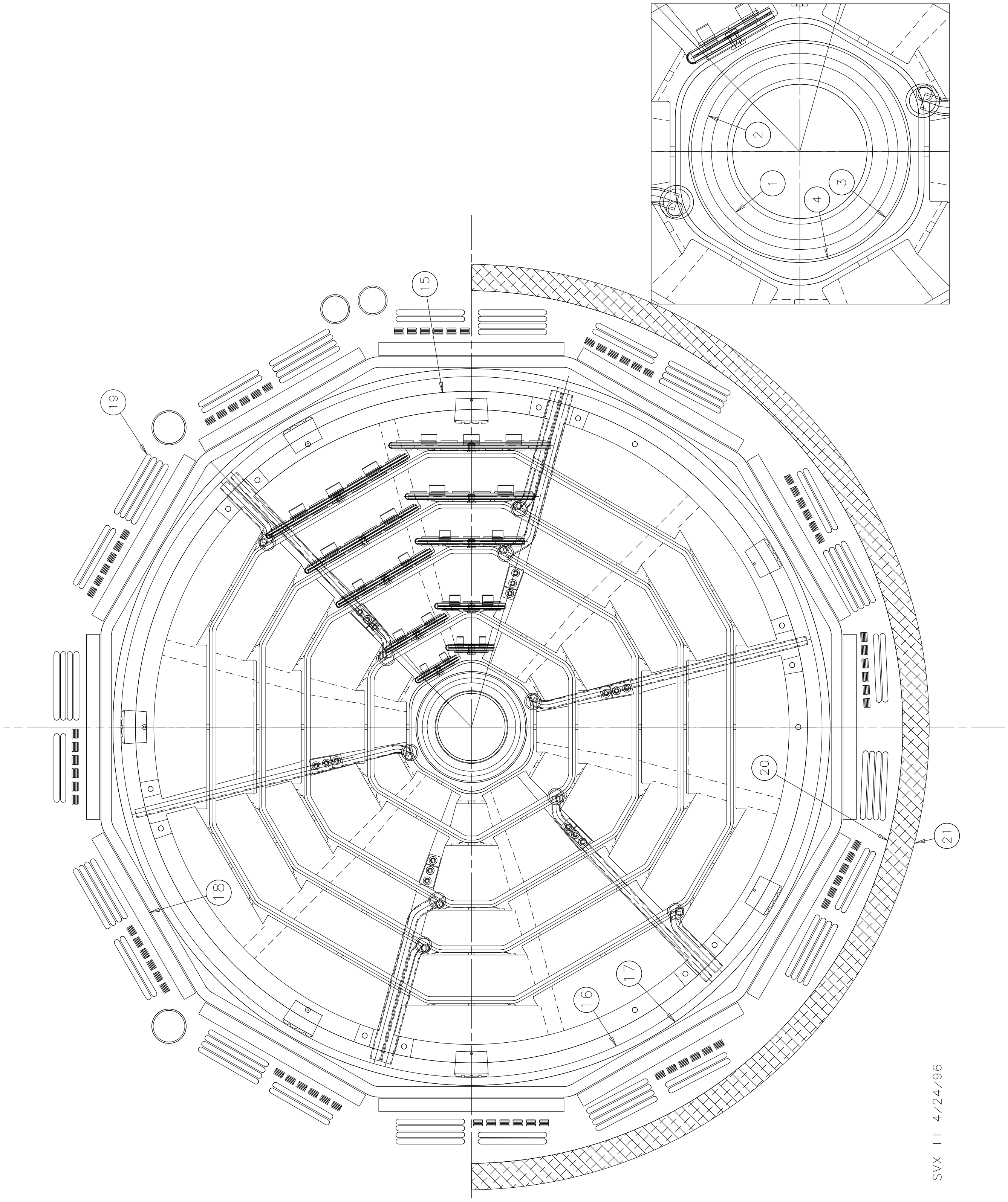

Figure 5.2: The SVX II bulkhead design

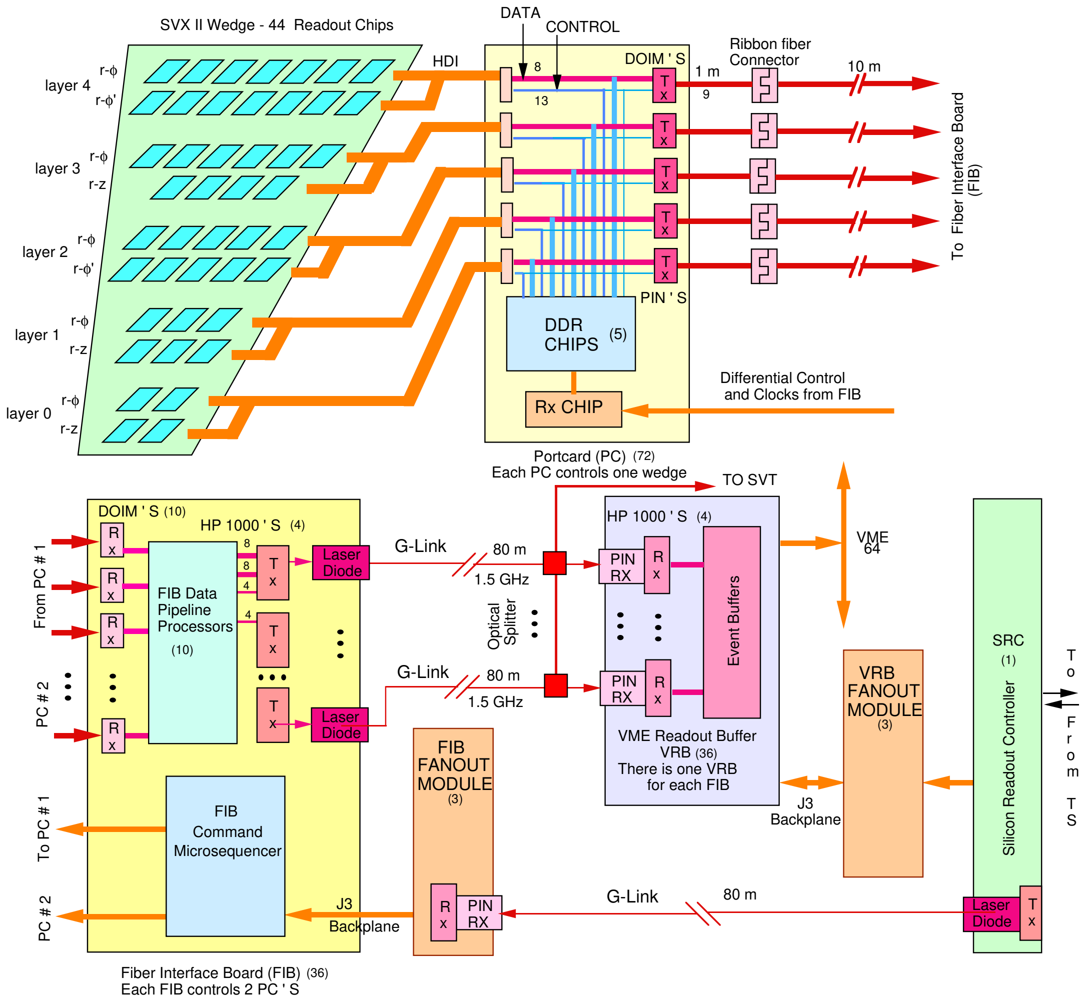

Figure 5.3: Schematic of the SVX II data acquisition system.

	Description	R (cm)
1	Beam pipe outer radius	1.6700
2	Beam pipe flange outer radius	1.8542
3	Inner screen inner radius	2.0500
4	Bulkhead inner radius	2.1000
5	Layer 0a *	2.5450
6	Layer 0b	2.9950
7	Layer 1a	4.1200
8	Layer 1b	4.5700
9	Layer 2a	6.5200
10	Layer 2b	7.0200
11	Layer 3a	8.2200
12	Layer 3b	8.7200
13	Layer 4a	10.0950
14	Layer 4b	10.6450
15	Bulkhead outer radius	12.9000
16	Outer screen inner radius	12.9000
17	Outer screen outer radius	13.2500
18	Port card inner radius	14.1000
19	Cables	16.1000
20	Half cylinder inner radius	16.3000
21	Half cylinder outer radius	17.3000

* All layer radii are relative to center of silicon.

Table 5.2: SVX II Bulkhead Information

FIB serializes the data from 10 DOIM's onto high-speed optical G-links. For each FIB the data from 90 low-speed fibers are sent by only four high-speed fibers. These high-speed optical fibers carry the data approximately 70 m to the counting room where the data are stored in event buffers located on the VME readout buffer cards (VRB's) where it waits for a Level 2 trigger decision and subsequent readout into Level 3.

In the counting room there are three VRB VME crates, one for each barrel of the detector, and each containing 12 VRB's. Each crate is controlled by the SRC through the VRB fanout board located in each crate. The SRC in turn communicates by a serial optical fiber with the CDF Trigger System Interface. Control of the VRB boards by the VRB fanout module is accomplished over the J3 backplane. A set of optical splitters located just in front of the VRB modules sends a completely parallel stream of data to the SVT trigger processor so that the silicon data can be used in the Level 2 trigger decision.

5.2 Silicon Crystals

The primary physics goals of the CDF vertex detector are to allow good secondary vertex reconstruction and pattern recognition. Monte Carlo studies showed that these require five layers of double-sided silicon microstrip sensors. Optimization of both vertex resolution and pattern recognition considerations lead to the first, second and fourth layers (Layers 0, 1 and 3) having a "90° stereo" design while the third and fifth layers (Layers 2 and 4) have a "small angle stereo" design. Technically, the "90° technology" is more difficult to design and construct than the small angle technology, so it will be described in greater detail. Some mechanical and electrical properties are given in Tables 5.3 and 5.4.

5.2.1 Silicon Detector Layout

Many characteristics are common to all the detectors regardless of layer or stereo angle. The HV biasing uses polysilicon resistors with 2.5 ± 0.5 Mohm resistance, and the readout is AC coupled. The detector bulk silicon thickness is 300 ± 15 μm for the double metal layers and 275 ± 15 μm for the small angle layers. The thickness variation within one detector is ± 5 μm. Bowing should be less than 100 μm in a detector. There should be fewer than 3% dead chan-

Property	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4
number of ϕ strips	256	384	640	768	896
number of Z strips	256	576	640	512	896
number of ϕ chips	2	3	5	6	7
number of Z chips	2	3	5	4	7
stereo angle	90^o	90^o	$+1.2^o$	90^o	-1.2^o
ϕ strip pitch (μm)	60	62	60	60	65
Z strip pitch (μm)	141	125.5	60	141	65
total width (mm)	17.140	25.594	40.300	47.860	60.170
total length (mm)	74.3	74.3	74.3	74.3	74.3
active width (mm)	15.300	23.746	38.340	46.020	58.175
active length (mm)	72.43	72.43	72.38	72.43	72.38
number of detectors	144	144	144	144	144

Table 5.3: Silicon detector mechanical dimensions

nels per side and 50% of the detectors should have fewer than 2% dead channels.

5.2.2 The 90° stereo sensors

The 90° stereo sensors have strips running lengthwise on the sensor's p-n junction side to measure the r-ϕ position of the particle, and strips running laterally on the ohmic contact side (n-side) to measure the r-z position. Both sets of strips are read out from the end of the sensors. For the r-z signals this requires an additional layer of strips running longitudinally and contacting the lateral r-z strips through a 5 μm insulating layer of SiO_2 by means of small "via's". This is referred to as a double metal layer technology.

Key parameters associated with the SVX II 90° stereo sensors have been chosen to minimize readout capacitance, in order to minimize the amplifier noise level and to maximize radiation hardness. The readout capacitance is larger for the 90°, ohmic-side strips than for the p-n junction side strips. This is caused by several factors. One factor is that, to maintain electrical isolation of the n-side readout strips under high radiation levels, extra p-implant strips are placed between the ohmic contact strips. This gives operational simplicity and radiation hardness [2]. A second factor increasing the ohmic side capacitance is the double metal layer readout. It introduces additional capacitance because the second metal (longitudinal) strips couple to the first metal (90°) strips through the insulation layer.

Several steps were taken to reduce the 90° capacitance. The coupling capacitance of the double layer readout was minimized by making the insulating silicon dioxide (SiO_2) between the two metal layers as thick as possible, while maintaining the via reliability. SiO_2 was chosen as the insulator because of fabrication reliability and good radiation resistance. A new idea for the isolation p-stop pattern was introduced, in which a combination of an individual p-stop and a common p-stop is used.

The critical item limiting the useful lifetime of the silicon sensors is the radiation hardness. For a peak luminosity of 10^{32} cm^{-2}s^{-1} the fluence received by Layer 0 is expected to be about 1.7 x 10^{13} particles/cm^2/year, i.e. about a half Mrad/year. This is the same order of magnitude radiation level as expected on the LHC silicon trackers, which are placed further from the beamline. This radiation causes the silicon bulk to change from n-type to p-type during the operation of Run II. This is referred to as "type inversion" [3]. Because of type inversion and accumulation of defects caused by radiation damage, the bias voltage needed for full depletion of the bulk can become as high as 150V. The rate at which type inversion occurs depends strongly on the operation temperature [4], being slower at lower temperatures. High bias voltages need to be avoided if possible because they cause micro-discharge noise [5], which takes place before a junction breakdown. The design of surface structures for the SVX II incorporated many ideas [6] from our research in order to suppress the micro-discharge.

The coupling capacitors which are integrated onto

Electric Properties of Detectors	
initial $I_{leakage}$ at V_{bias}=80 V, T=20 °C:	
(bulk, surface and edge contribution)	< 100 nA/cm^2
initial full depletion voltage (V_{full}):	45 V$<V_{full}<$70 V
junction breakdown with open readout electrodes:	> 200 V
The breakdown is defined as:	$I_{break} > 10 \times I_{leak}$ with $V_{bias} = 80$V
onset voltage of micro discharge:	*p*-side, *n*-side balanced bias ($\pm V_{bias}/2$), both-side readout electrodes grounded
p-side	> 150 V (total bias potential)
n-side	> 150 V (total bias potential)
$V_{Breakdown}$ of coupling capacitor:	
n and *p*-side:	> 100 V
Interstrip resistance (DC):	>2 Gohm
Poly-silicon resistor value:	
mean value:	2.5 ± 0.5 Mohm
variation within one detector:	< 0.5 Mohm
resistivity of implant-strip:	<100 kohm/cm
resistivity of all metal layers: *n* & *p*-sides	<30 ohm/cm
capacitance of coupling capacitor:	
n and *p*-side:	>10 pF/cm
total capacitance (full length, at bias voltage of 1.2 x V_{full}):	
p-side (Layers 0, 1 and 3):	<10 pF
n-side (Layer 0):	<13 pF
n-side (Layer 1):	<14 pF
n-side (Layer 3):	<15 pF
p-side and *n*-side (Layer 2 and 4):	<10 pF
Specifications for Radiation Damage Tests for Pilot Detectors	
Ten days after irradiation of 500 krad Gamma-ray:	
leakage current at 20 °C:	<3 μAmp/cm^2
bias resistor change:	<20%
p-strip, *n*-strip $R_{interstrip}$:	>1 Gohm
junction breakdown voltage:	>200 V
onset voltage of the micro discharge:	>150 V
total capacitance (full length, at bias voltage of 1.2 x V_{full})	
p-side (Layers 0 and 1):	<11 pF
n-side (Layer 0):	<14 pF
n-side (Layer 1):	<15 pF
n-side (Layer 3):	<16 pF
p-side and *n*-side (Layer 2 and 4):	<11 pF

Table 5.4: Electrical Properties of Detectors

the sensor are another critical technological issue. They must be free of "pin holes" which allow breakdown. A double layer structure consisting of SiO_2 and silicon nitride (Si_3N_4) is employed to improve the capacitor production yield. But careful design and processing is required to avoid problems of electrical charge-up between the SiO_2 and Si_3N_4 layers.

5.2.3 Small Angle Stereo Detectors

The Layer 2 and Layer 4 sensors utilize "small angle stereo" for the strip layout instead of the 90° layout. The design requirements for radiation resistance, capacitance, etc. are very similar to those of the 90° sensors, so that discussion will not be repeated here. One difference is the wafer construction, which will be discussed.

Recent technological developments in the silicon detector manufacturing industry have increased the size of available wafers from 4 inch to 6 inch. The design of the detectors for Layers 2 and 4 takes advantage of the availability of 6 inch wafers. Such large wafers can host both a Layer 2 and a Layer 4 detector reducing dramatically the mask fabrication and processing costs. The 6" wafers are a new technology, but they have been proven to work on large area detectors. However, because our 90° sensors require challenging technology such as the double metal processing, they have intrinsically some extra degree of difficulty. For this reason it seemed appropriate to choose the 6" technology only for the small angle stereo design, shown in Fig. 5.4, where we do not require the double metal processing. If production problems happen to arise, the use of the standard 4" wafer approach is still possible for Layer 2 without any design modifications, but some modifications might be required for Layer 4.

The technical specifications we have required for Layer 2 and 4 are very similar to those of the other layers, though here the radiation hardness demand is less stringent. For example, the Layer 2 detectors are expected to receive only about 1/7 of the Layer 0 expected dose. One big difference is the fact that the 6" wafers available for manufacturing at the moment have a relatively low resistivity of about 3 kΩ-cm. Consequently we decided to reduce the thickness of the detectors to about 275 μm in order to keep the depletion voltage below 80 V. There are a minimum of 13 masks needed for the double side process. We added 2 more to allow for 1) the option of Si_3N_4 deposition to enhance the breakdown voltage of the coupling oxide and 2) a n^+ well implant extending to the junction side scribe line to avoid large currents being injected into the active area from the edges of the detector.

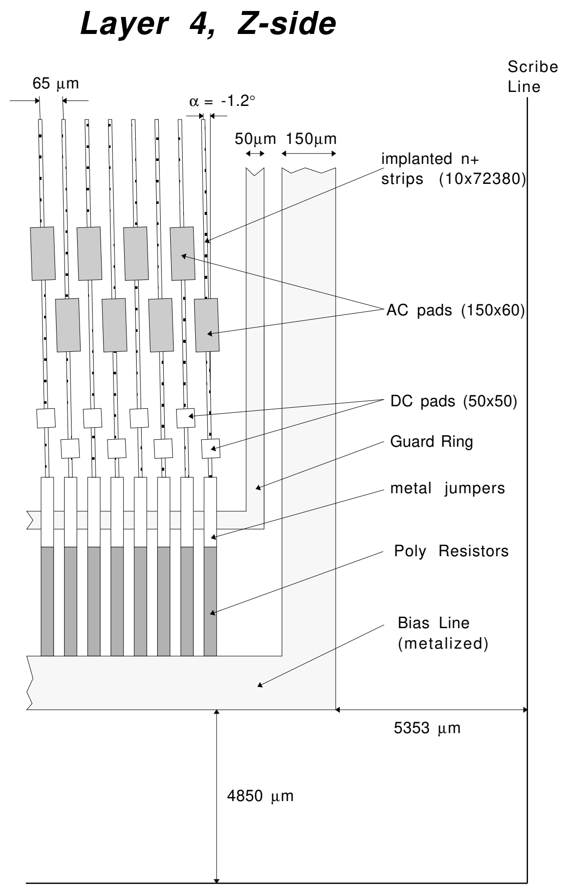

Figure 5.4: Silicon detector small angle stereo design.

5.2.4 Silicon Detector Tests

A substantial R&D program on silicon sensors has been carried out to achieve the full potential of the silicon tracker upgrade. This program has resulted in significant technical developments in the areas of capacitance and microdischarge minimization, geometrical layout optimization, large area detectors from 6 inch wafers, and determination of processing and operating conditions. The program has also investigated the sensors' signal-to-noise (S/N) ratio, efficiency, and position resolution before and after radiation damage similar to what is expected at Layer

0 during Run II. The program included full characterization of sensors utilizing many design options. These sensors were manufactured by three different vendors—Hamamatsu, SINTEF/SI and Micron Semiconductor. The characterization program involved the measurement of the electrical properties of the sensors on a probe station [7, 8, 9, 10, 11, 12], the study of the charge collection efficiency and determination of the optimal operating conditions with a pulsed laser system [13], and the operation of the detectors in conjunction with the SVXH [14] and SVX2 [15] chips in two beam tests [16, 17].

5.2.4.1 Capacitance Minimization

The detector capacitance plays a key role in determining the S/N ratio. The important components are the many parallel capacitances that load the amplifier front end, including C_{is}, the capacitance between implant strips, C_{back}, the backplane capacitance (between the implant strip and the opposite side of the detector), C_{ir}, the capacitance between the readout traces, and $C_{overlap}$, the capacitance between the second metal traces on the z-side and the AC-coupled first metal electrodes.

On the p-side (whose strips measure the r-ϕ coordinate), C_{is} and C_{back} have the largest effect. The capacitance with respect to the ground of the implant depends primarily on the ratio of the strip width to the pitch. To minimize this contribution to the total detector capacitance, the strip should be as narrow as possible.

The capacitance of the n-side strips (which measure the r-z coordinate) is the sum of C_{is}, C_{ir}, C_{back}, and $C_{overlap}$. We measured the n-side capacitance of prototype detectors [9, 11] and found agreement between the direct measurement of the capacitance with respect to ground and the sum of the various capacitive components. A fit of the measured total capacitance to a geometrical model [18] and a SPICE simulation [11] agree within 20%. For example, the measured n-side capacitance of the Layer 0 prototype detectors from Hamamatsu is 17 pF, in good agreement with two independent simulations which together predict a capacitance between 17 and 21 pF. The same two simulations applied to the Layer 0 production detectors predict an n-side capacitance for them between 10 and 12 pF.

By comparing detectors with different geometries, we have designed a readout scheme to minimize the n-side capacitance by

1. maximizing the thickness and minimizing the dielectric constant, ϵ_r, of the insulator between the metal layers,
2. limiting the multiplexing,
3. minimizing the width and length of the second metal strips and
4. avoiding ganging and intermediate strips.

A summary of the predicted capacitance for a full electrical unit consisting of two double metal production detectors wirebonded together is in Table 5.5.

Layer	p-side Husson	p-side Spice	n-side Husson	n-side Spice
0	15	17	20-24	21-25
1	15	16.5	22-26	22-26
2	19	19	24	26
3	15	17	24-28	24-29
4	19	19	26	27

Table 5.5: Predicted capacitance in pF

The RMS noise of the SVX2 chip versus input capacitance has been measured [19] for integration times of 107 ns and 371 ns and is shown in Fig. 5.5. Using a linear extrapolation between the measured data points an input capacitance of 25 pF predicts noise values of $\approx 2100\ e^-$ and $\approx 1100\ e^-$ for integration times of 107 ns and 371 ns, respectively.

5.2.4.2 Optimal Geometry and Processing

Studies of prototypes having a variety of geometrical options allowed us to investigate several issues, including the effect of intermediate strips on the p– and n-sides, the performance of double metal readout compared with readout by interconnects on glass or Kapton, and the optimal insulator to be used in the double metal structure and/or for passivation. One of the major results of these investigations was the elimination of the option for intermediate strips on the n-side. Laser studies [13] and results from our first KEK run [16] showed that double metal detectors with intermediate strips lose efficiency by more than 90% when the beam strikes directly on the intermediate strip.

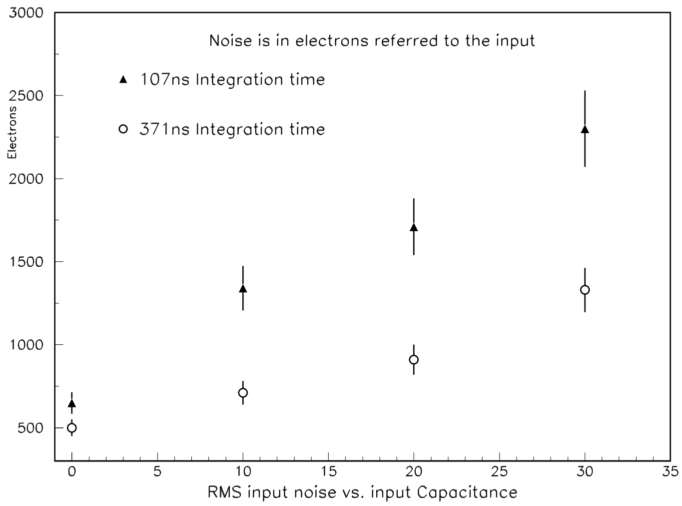

Figure 5.5: SVX2 measured noise as a function of input capacitance for integrations times of 107 ns (triangles) and 371 ns (circles).

5.2.5 Radiation Issues

The radiation levels experienced by silicon detectors have a multitude of effects. These have been investigated by irradiating detectors at TRIUMF and then checking them in the lab and in KEK test beams. Below we discuss the radiation levels we expect to encounter during Run II and the effects we have observed during our radiation tests.

5.2.5.1 Run II Expected Radiation Levels

The radiation levels in SVX II have been estimated for the Run II beam intensities and CDF geometry [20, 4]. The expected radiation dose is shown in Fig. 5.6 for SVX II Layers 0-4 as a function of time during Run II [4]. For the purpose of this study the CDF yearly integrated luminosity for Run II is assumed to be 1 fb^{-1} and 2 fb^{-1} for years 1 and 2, then 0 fb^{-1} for year 3, followed by 2 fb^{-1} and 3 fb^{-1} for years 4 and 5. We assume that SVX II Layer 0, and possibly Layer 1, will be replaced part way through Run II. This is shown happening during year 3 for SVX II Layer 0. The radiation dose is given as the equivalent fluence of 500 MeV protons [4]. This allows for a direct comparison with radiation damage results in the SVX II sensor prototypes at the TRIUMF radiation tests. As shown in the figure, the maximum fluence at TRIUMF ($\sim$ 0.9 Mrad) is comparable to the maximum fluence expected for SVX II sensors. Also shown in the figure is the approximate fluence when the silicon sensors will change from n-type bulk to p-type bulk, i.e., undergo type inversion. At inversion the n-p junction moves from the p-strip side of the sensor, which measures r-ϕ, to the n-strip side, which measures r-z.

5.2.5.2 Radiation effects

The expected radiation levels in SVX II require radiation hard electronics and sensors. The SVX3 chips will be fabricated using Honeywell's radiation hard CMOS processing. This is guaranteed radiation hard to 1.5 Mrad. A measurable but acceptable level of degradation is expected up to radiation levels of 5 Mrad [21]. Thus the SVX3 chip should perform satisfactorily at the expected radiation levels of 1-2 Mrad.

The effects of radiation on the SVX II sensors are more complex than on the SVX3 chip. The individual structures on the SVX II sensors, including bias resistors, n- and p-implants, p-block implants, metal readout strip geometry, AC coupling capacitors, etc., were chosen to be as radiation tolerant as possible [22, 23, 5]. The SVX II production sensors will have SiO_2 (ϵ_r = 3.8) as an insulator between the double metal layers because of its demonstrated hardness to high radiation. Extensive pre- and post-irradiation testing of SVX II sensor prototypes from Hamamatsu, Micron and SINTEF/SI are continuing. Initial results [7, 24, 8, 25, 10, 26] are all consistent with a stability at the 10% level of these structures against radiation except for the interstrip resistance, where a substantial decrease with radiation was found [8]. Nonetheless, the value of the interstrip resistance remains large enough, $> 100\text{M}\Omega$, that the sensor performance is not expected to be compromised.

Several other features of the silicon microstrip sensors show significant changes with radiation. These include the detector leakage current, the depletion voltage, and the interstrip capacitance. The changes in the leakage current and depletion voltage are a result of radiation damage in the bulk silicon and have been extensively studied [4]. Initial measurements of the radiation-induced bulk damage in the SVX II prototypes are in good agreement with expectations [25, 26]. The leakage current and depletion voltage changes affect the power dissipated in the detectors, which has implications for the SVX II cooling and power system designs. Furthermore, the increased leakage current decreases the S/N because of increased shot noise [27, 28].

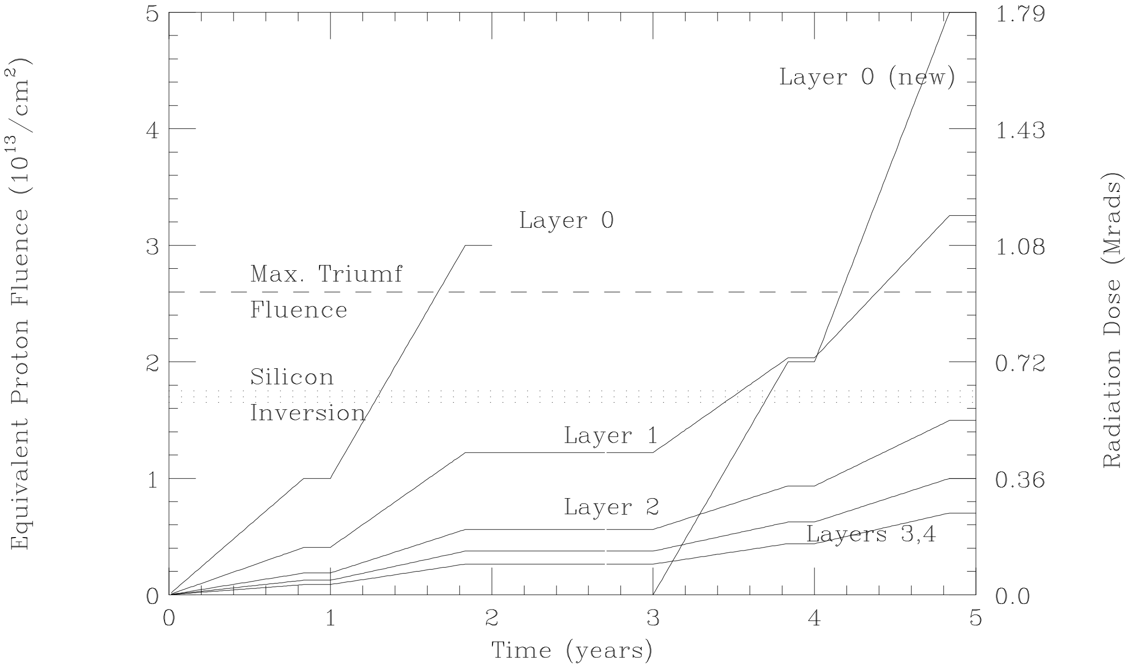

Figure 5.6: Estimated radiation levels for Layers 0-4 of SVX II in Tevatron Run II. The integrated luminosity is assumed to be 1 fb^{-1}, 2 fb^{-1}, 0 fb^{-1}, 2 fb^{-1}, 3 fb^{-1} for years 1, 2, 3, 4, and 5 respectively.

The change in the sensor interstrip capacitance is a result of surface damage caused by radiation at or near the silicon-SiO_2 interface. The observed trends at the sensor p-side are for the interstrip capacitance to increase by 20%-40% for the first few 100 Krads and then to become independent of radiation until type inversion occurs [29]. Following inversion the p-side interstrip capacitance becomes 1.4 to 2 times the unirradiated value [30]. Before inversion, the dependence on radiation of the interstrip capacitance of the sensor n-side with double metal readout should be much weaker than the p-side. Following inversion the n-side interstrip capacitance should decrease to a value less than that seen before irradiation [29].

Measurements of the interstrip and total input capacitance for unirradiated and irradiated SVX II prototype sensors are being made [11, 9]. The initial measurements are consistent with the above expectations [25, 26]. Because the sensor interstrip capacitance is a major component of the preamplifier input capacitance, increases in the sensor interstrip capacitance result in an increase in the noise [28].

Another issue is charge trapping due to radiation. Present evidence is that the radiation levels for Run II should not be enough to cause SVX II signal loss due to charge trapping [31].

5.2.5.3 KEK Test Beam Results

The principle difference between the two beam tests at KEK was the type of chip used to read out the sensors. In the first beam test the well-understood SVXH chip was used, while in the second test the prototype SVX2 chip was used [16, 17].

In the first KEK beam test, five (SINTEF/SI and Hamamatsu) double metal detectors were tested. The position resolution of these detectors as a function of angle is shown in Fig. 5.7. At normal incidence the strip pitch/$\sqrt{12}$ accounts for the resolution. For particles with oblique incident angles the resolution varies between 12 and 25 μm.

The S/N of irradiated and unirradiated SVX II prototype sensors was measured in the two beam tests at KEK. The unirradiated detectors have n-side S/N ratios of 17, 21 and 16, while detectors irradiated with between 0.25 and 1.0 MR have S/N ratios of 13 and 14. In the second KEK beam test, S/N ratios were measured for seven double metal detectors

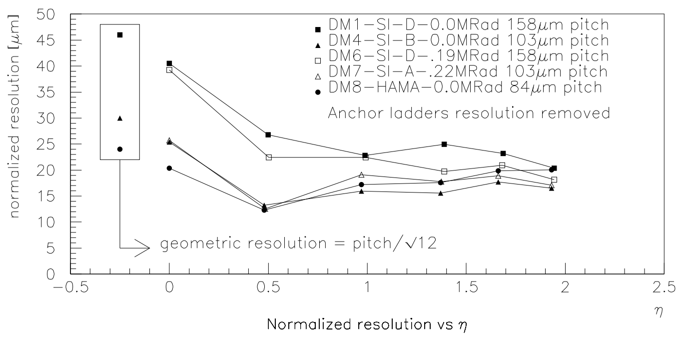

Figure 5.7: Silicon detector resolution versus particle angle of incidence.

supplied by SINTEF/SI, Hamamatsu, and Micron. Unirradiated detectors have ratios of 11, 14 and 10, while irradiated detectors, having doses between 0.1 and 0.7 MR, have ratios of 9, 10, 10 and 7.

The S/N measured during the second test beam is somewhat lower due to several effects. The dominant effect is from the increased noise of the SVX2 chip as operated for the KEK test, i.e. there was excess noise beyond what can be expected for optimized running conditions. Several $\approx$ 10% effects, including charge loss from the limited integration time window and the clustering algorithm, appear to account for the majority of the remaining difference. The gain of the SVX2 chip is a parameter in the calculation of the theoretical signal and noise, but it cancels in the calculation of the S/N ratio.

Prior to the beam test the leakage currents were measured in the sensors. The increases seen as a result of the radiation dosages were consistent with values found in the literature [27]. The noise as a function of average radiation dose is plotted for the p-side in Fig. 5.8 and for the n-side in Fig. 5.9. The p-side detectors had strips of two different lengths, 4.1 and 8.2 cm. The results for these are plotted separately. Whereas the n-side shows no evidence for an increase of noise with radiation dose, the p-side shows an increase. The n-side results are consistent with our expectation based on the first KEK test results, where the increase in noise could be accounted for by an increase in the shot noise. Since the SVX2 chip has an integration time an order of magnitude shorter than the SVXH chip, we expect almost no contribution to the noise due to shot noise. For the p-side, the solid lines in Fig. 5.8 indicate a range of expected noise as a function of dose. We have assumed the interstrip capacitance increases between 20% and 40%, representing the lower and upper lines. We have included the effect of the increased leakage current based on the radiation dose.

There are several potentially large uncertainties in these measurements. First, the temperature was not well controlled, an effect which could easily introduce a 10% variation in the noise. Second, the radiation dose used is an average value, whereas the dose profile is known from foil measurements to be non-uniform. Nonetheless, the observed increase in the noise on the p-side is consistent with our expectations.

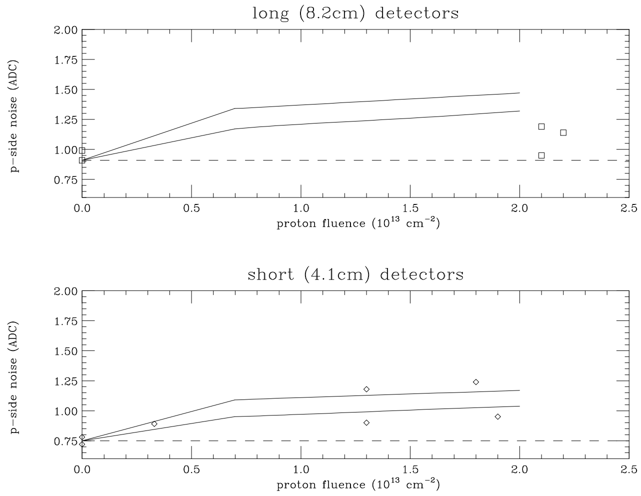

Figure 5.8: p-side noise versus average radiation dose for the 5 long and 7 short detectors. The solid lines in the figures indicate a range of expected noise as a function of dose. The dotted line indicates the average unirradiated noise value. None of the detectors were believed to have been inverted at the time of the measurements.

The signal, aside from clustering effects, is not expected to degrade with radiation dose. The data are consistent with this expectation. The S/N prior to irradiation was measured on average to be 10 on the p-side and 11.5 on the n-side. However, there was considerable variation in the p-side signal, so efforts are continuing to understand the p-side S/N.

5.2.5.4 Layer 0 and Layer 1 Replacement

It is anticipated that Layer 0 and possibly Layer 1 will need to be replaced after a delivered integrated luminosity of 2 or 3 fb^{-1}. This replacement could be silicon or a more radiation-hard device. Detectors based on chemical-vapor-deposition (CVD) diamond

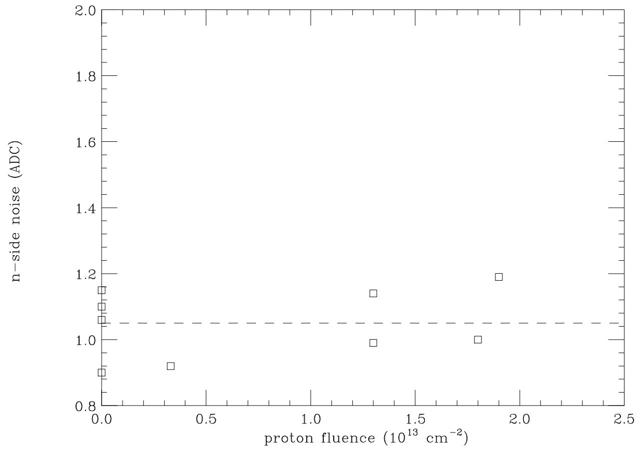

Figure 5.9: n-side noise versus radiation dose. The dotted line indicates the average unirradiated noise value. The irradiated n-side results are all of the short variety. None of the detectors were believed to have been inverted at the time of the measurements.

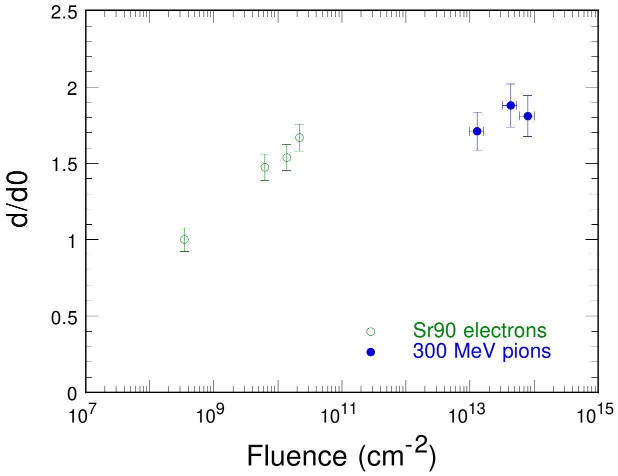

Figure 5.10: Charge collection in CVD diamond as a function of exposure to ^{90}Sr electrons and 300 MeV/c π^- relative to that of an unirradiated detector.

film rather than silicon offer a potential solution to this problem.

CVD diamond has numerous properties which make it attractive as a detection medium: it is highly electrically resistive, has high material strength, high thermal conductivity, low thermal expansion, and low density. The high electron and hole mobilities result in a very fast signal, on the order of 2 ns. Its stiff crystal lattice and low neutron transmutation cross section lead to extremely good radiation tolerance. Figure 5.10 shows, as an example, the relative signal size as a function of exposure to 300 MeV pions. No loss of signal appears after 10^{14} π^-/cm^2.

The main challenge in making CVD diamond-based detectors lies in the fact that electrons and holes travel only a certain distance in the crystal before being stopped by traps or lattice imperfections. This "collection distance" limits the size of the induced signal to a fraction of the deposited charge, which is 3600 e$^-$ per 100 μm thickness. The expected signal size is thus the ratio of the collection distance to 100 μm times 3600 e$^-$.

Collaboration with industry led to great improvements to CVD diamond quality, resulting in a CVD diamond calorimeter in 1993 [32]. Attention then turned to tracking detectors, and early in 1995 microstrip detectors made from CVD diamond wafers with collection distances in the range of 70-90 μm resulted on the pulse height and position resolution distributions shown in Fig. 5.11.

The goal in the near term is to obtain a 2 cm $\times$ 4 cm sample of the best possible quality, and test a microstrip detector made from it it in beam tests which commence late this fall. Construction of smaller prototypes with CDF SVX II electronics will begin in the mean time to gain experience.

5.2.5.5 Future Detector Testing at Fermilab

During the upcoming fixed target running period the SVX II detector groups will use the Fermilab Booster AP4 line for irradiating prototype detectors and the CDF test beam in Meson for detector studies. The Booster area has been used previously on at least a couple of occasions for irradiating single detector elements. The Booster cycles 8 GeV/c protons. One can achieve detector fluences well in excess of a Mrad in the course of a week by extracting a few percent of the normal 84 bunches. Most of the Booster protons are, of course, eventually delivered to fixed target areas.

The Meson Test line has historically been the site where CDF has conducted test beam studies during fixed target operations. The SVX II upgrade group intends to take full advantage of this facility, which is scheduled to commence operations starting in the fall of this year. A rotatable and translatable detector box is being prepared along with a set of "anchor plane" boxes, which will be fixed along the beamline. The primary focus of the silicon tests will be to study the detector ladders' response to negative pion beams (ranging from 100 to 200 GeV/c) as a function

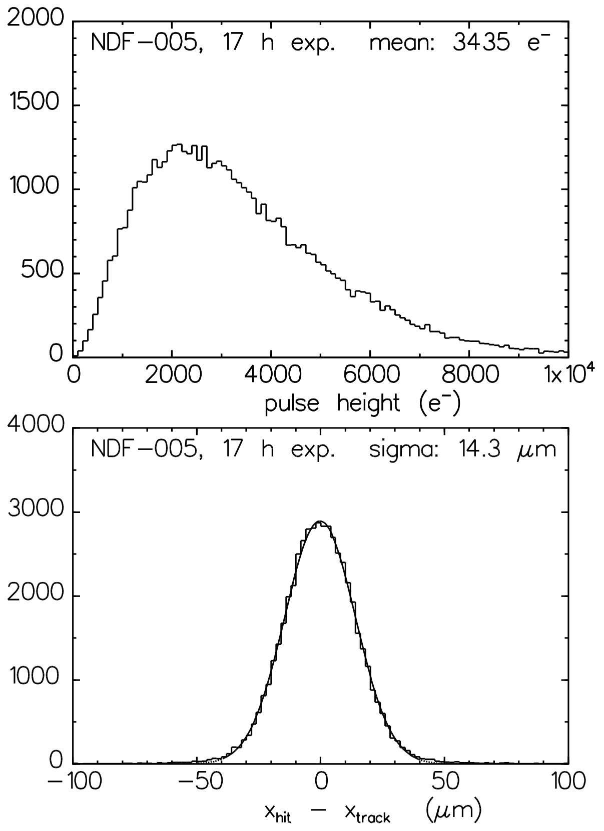

Figure 5.11: Pulse height in central three strips (above) and position resolution (below) for 50-micron-pitch CVD diamond microstrip detector.

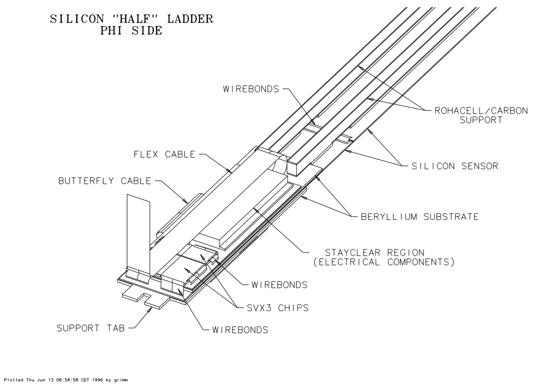

Figure 5.12: Perspective view of the ϕ-side of a Layer 0 ladder.

of the incident angle. The S/N, position resolution, cluster size, etc. will be of particular interest. The test beam activities will serve as an invaluable focus for the various sub-groups of the SVX II project, and results from test beam running will help refine detector design and construction techniques. It is also important to irradiate and beam test pilot versions of each detector type so that any future signal-to-noise degradation, due to long-term radiation damage, can at least be anticipated if not avoided.

5.3 Mechanical Design

5.3.1 Ladder Design

Shown in Figs. 5.12 and 5.13 are perspective views of a Layer 0 ladder. A notch on the ladder end is used during ladder construction and will precisely locate ladders relative to the support structure. The ϕ-side of the detector, i.e. the side with implant strips parallel to the beam line, is on the top of the ladder with the ϕ-side SVX3 chips directly opposite the cooling channel. This is the side shown in Fig. 5.12. The z-side SVX3 chips are on the underside of the ladder located inboard of the cooling channel. This this is the side shown in Fig. 5.13.

The SVX3 chips are mounted on hybrid integrated circuits. Two hybrid technologies are currently under consideration; copper on kapton thin film and BeO thick film (see Section 5.3.2). By the end of 1996 we expect to choose one of these two technologies. The hybrids are mounted directly on the surface of the

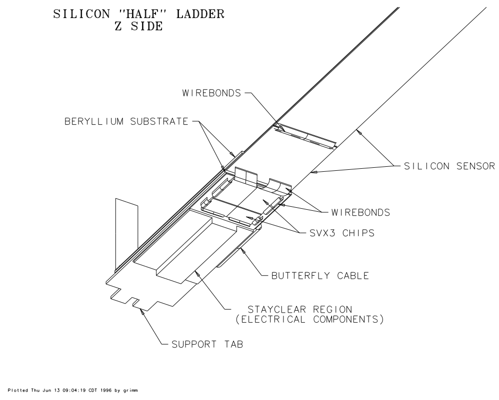

Figure 5.13: Perspective view of the z-side of a Layer 0 ladder.

silicon. The spacial requirements of the hybrid for passive components dictates the length of the hybrid, hence the location of the wirebonding pads on the z-side of the detector.

The thin film hybrids are mounted on beryllium substrates, chosen due to the structural integrity of beryllium, its thermal conductivity, and its favorable radiation length. The thickness of the substrate is chosen in order to adequately cool the z-side SVX3 chips. Cooling will be discussed in the next section.

The BeO hybrid can be designed in such a way that it requires less space for passive component placement than the thin film copper/kapton hybrid. For this reason, two rows of wirebond pads have been placed on the z-side of all detectors in order that the choice of technology may be delayed beyond the mask design of the silicon detectors.

The ladders will be constructed in halves, of length two crystals each. Once the ϕ-side hybrid is adhered to the surface, the second detector will be located precisely relative to the first and the two detectors will be wirebonded. After passing inspection the support rail will be adhered to the surface to make a single structure which can be flipped and the z-side completed.

The support rail itself is constructed of a mix of foam, epoxy, and fiber not unlike those used for SVX and SVX$'$. Fiber is adhered to Rohacell foam by applying an epoxy mix on the foam surface, and curing in a compression mold. The expansion coefficient of pure carbon fiber (as used in SVX and SVX$'$) is lower than that of silicon ($\approx$ 0 ppm/°C for carbon fiber vs. 2.6 ppm/°C for that of silicon) and could present structural bowing problems when the ladder is cooled to operating temperature. For this reason the rails will be constructed of a mix of carbon and boron fiber, which combined have an expansion coefficient equal to that of silicon [33]. The ladders will be joined in halves, once completed and tested, using an overlap joint in the ladder middle.

5.3.2 SVX II Readout Hybrid

The SVX II readout hybrid processes the detector signals into a format suitable for the port card. The hybrids are being developed in two technologies: (1) the high density flex circuit technology, and (2) the thick film (beryllia) technology. One of these will be chosen for the final detector depending upon the behavior of the prototypes. Associated with the readout hybrid is a cable that connects the power/signal functions from the hybrid to the port card. Hybrid prototypes which accommodate the SVX2 readout chip have already been fabricated using both technologies. The hybrids to read the SVX3 chip set have been designed and are being ordered. Their delivery time coincides with availability of the SVX3 chip.

5.3.2.1 Structure of the Flex Technology Hybrid and Cable

The hybrid and cable have both been fabricated using the multilayer flex technology. The hybrid has four layers of 10 μm Cu metal interconnect separated by three layers of 50 μm thick polyimide dielectric. This is covered with a top and bottom 'coverlay' dielectric. The coverlay provides 100% coverage of the ground planes on the back side of the hybrid. On the top side it has windows for the surface mounting of passive components and the wire bonding to SVX3 dies. The top layer metal includes Ni/Au layers to facilitate the surface mount soldering of passive components and the wire bonding to the readout dies. The signal line path and pitch are 100 μm and 200 μm, respectively. The layer to layer interconnect is provided by 150 μm diameter vias with 380 μm diameter connect pads. The minimum via pitch is 480 μm which gives a pad-pad gap of 100 μm. This is consistent with the signal line gap. The total thickness of the 4 layer hybrid is nominally $4*10+3*50+2*25 = 240$ μm, while the cable is nominally $2*10+1*50+2*25 = 120$ μm thick.

The hybrid and cable are designed to be separate parts which are surface soldered together during the assembly process. Identical arrays of via pads on both the cables and hybrids provide for interconnecting the cable and the hybrid. The SVX3 hybrid design, with differential paired readout signals, has 48 to 53 separate interconnections between the hybrid and the cable. The cable has fanout regions to the test connector field on one end and the hybrid/cable term field on the other end. The present cable design is $\approx$ 8000 μm wide between the fanouts.

The connection between the ϕ and z-side hybrids is a 'wrap' design. The ϕ and z-side hybrids are interconnected along their edges by a short 'wrap' cable, with the power cable connected to the end of the ϕ-side hybrid.

5.3.2.2 Beryllia Hybrid

Beryllia hybrid prototypes for the SVX2b chip and for the SVX3 chip set are being manufactured by two different vendors. They are constructed of thick film artwork printed on 95% beryllium oxide ceramic. This is a technology widely used for commercial chip-on-board assemblies. Both manufacturers use low temperature firing (800 °C) after the printing of each layer, but one vendor uses tape dielectric while the other vendor prints the dielectric as well as the metal layers. The minimum features on the artwork in both cases are 100 μm traces on 200 μm pitch, with 250 μm square vias for one vendor and 100 μm round via's for the other. These feature sizes are standard for these companies. Both hybrids consist of 6 interconnected gold ink layers, separated by dielectric, on top of the ceramic substrate. This is a standard ink for applications that require wire bonding. Additionally, there are palladium-gold ink pads on the top layer to permit soldering of surface mount components. Both vendors have manufactured parts with a larger number of layers. The total thickness of the printed material is less than 250 μm for the SVX2 hybrid. It will be 50% larger for the SVX3 prototypes, but can be special-ordered to be about 250 μm for production quantities.

Both hybrids are Layer 0 prototypes, which is to say that they contain 2 side-by-side chips. The width is determined by the ladder width, while the length is determined by the layout and component requirements. The length is 3.1 cm in the SVX2b case and 3.3 cm for SVX3. The SVX2 hybrid was not designed to minimize length, while the SVX3 was. Both hybrids have 2 rows of solder pads with 750 μm pitch on the end opposite the chips. This permits the soldering of a flexible circuit cable to connect the hybrid to the port card. Soldering of these test cables was found to be simple and reliable. Only one generic prototype SVX2 hybrid design was manufactured, with no special provision for interconnecting the ϕ and z-side hybrids on the ladder.

The SVX3 design is also a single layout, rather than separate ϕ and z- side designs. It includes a bonding pad field on one side to allow for the same hybrid to be used on the ϕ and z-sides of a ladder. The $\phi - z$ interconnection is accomplished via a custom thin film jumper which is glued to the side of the ladder. This jumper has not yet been prototyped, but a technology choice and prospective vendor have both been identified.

5.3.2.3 Test Results on Hybrids

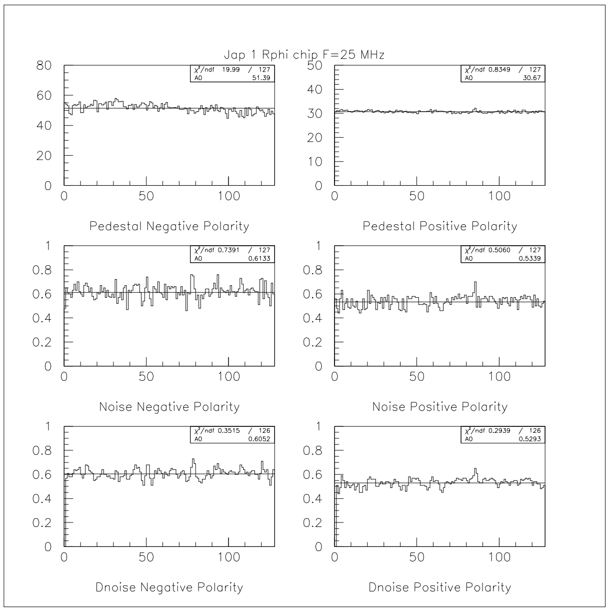

Figure 5.14: Hybrid Test Results: Pedestal and Noise Measurements.

Prototype hybrids equipped with SVX2 chips were tested using a prototype DAQ test stand. Noise, differential noise and chip gain were monitored for positive and negative input pulses. All of the measurements shown here were made with the SVX II DAQ system working at half speed (25 MHz). Future tests are planned at full speed (53 MHz). The test results show almost identical performance of both circuits.

ADC counts	J1	J2	US1	BeO
Ped. $r-\phi$	30.67	28.70	25.59	28.55
Ped. $r-z$	28.94	28.21	26.95	26.39
Noise $r-\phi$	0.53	0.57	0.58	0.53
Noise $r-z$	0.54	0.53	0.54	0.62
Dnoise $r-\phi$	0.53	0.56	0.59	0.48
Dnoise $r-z$	0.53	0.52	0.54	0.57

Table 5.6: Pedestal, Noise and Dnoise average values over 128 channels with chips configured in Positive Polarity

ADC counts	J1	J2	US1	BeO
Ped. $r-\phi$	51.39	55.10	50.40	56.02
Ped. $r-z$	54.20	57.97	53.97	57.18
Noise $r-\phi$	0.61	0.59	0.58	0.62
Noise $r-z$	0.58	0.59	0.59	0.63
Dnoise $r-\phi$	0.61	0.59	0.59	0.60
Dnoise $r-z$	0.58	0.59	0.57	0.62

Table 5.7: Pedestal, Noise and Dnoise average values over 128 channels with chips configured in Negative Polarity

	J1	J2	US1	BeO
Gain $(r-\phi)$ + *Pol.*	4.49	4.57	4.54	4.48
Gain $(r-\phi)$ - *Pol.*	4.81	4.38	4.34	4.72
Gain $(r-z)$ + *Pol.*	4.67	4.51	4.41	4.70
Gain $(r-z)$ - *Pol.*	4.61	4.58	4.47	4.57

Table 5.8: Hybrid gain measurements in ADC per fC for positive and negative polarity

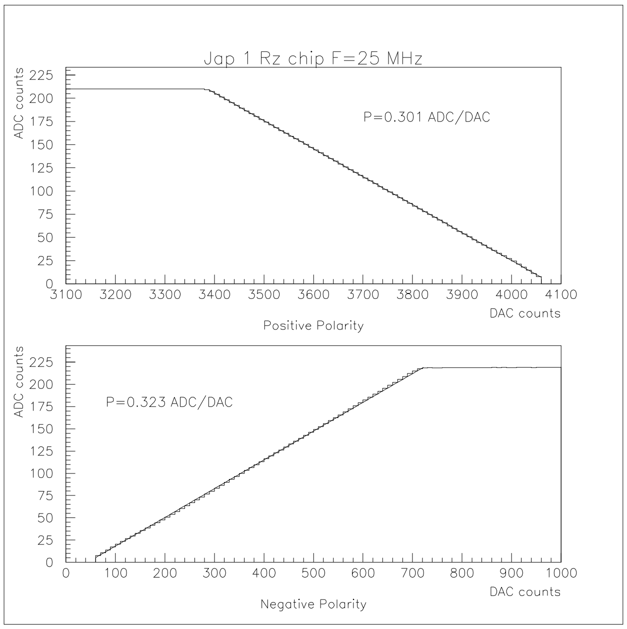

Figure 5.15: Hybrid Test Results: Linearity and Gain Check.

The tests were done on four different hybrids: 3 flexible hybrids and 1 BeO. One of the flexible hybrids was made in the USA ("US1") and the other 2 were made in Japan ("J1" and "J2"). The noise, differential noise and the pedestal have been measured channel by channel. The gain for positive and negative polarity has been calculated for every chip on each test hybrid.

The noise for a given channel was defined as the RMS of the digital output for that channel. Because of the potential susceptibility of the system to external noise we also defined the "differential noise" for a given channel as $1/\sqrt{2}$ of the RMS of the difference between the output for that channel and the output of a neighboring channel. Typical results for the first chip of the J1 hybrid are shown in Fig. 5.14. Results for all of the hybrids are summarized in Table 5.6 and 5.7.

The internal calibration capacitor, which is implemented on the chip itself, is used to measure the gain. It is connected at the input of every single channel. A specific voltage is injected into this capacitance and the output is read out for those channels that have been pulsed. Figure 5.15 plots the channels' output after pedestal subtraction versus the input DAC counts (proportional to the injected calibration voltage). It shows that the output of the chip is linear with respect to the injected charge. The gain for individual channels has been measured and shows a variation of less than 2% within a chip. The results of the gain measurements for the 4 hybrids are summarized in Table 5.8.

5.3.3 Ladder Cabling

There are severe mechanical and electrical constraints for cables from the portcard to the ladder. The cables must have a negligible profile, both for assembly and for achieving a minimal barrel spacing. The cables must exit through the bulkhead, which constrains the width of the Layer 0 cable to less than 5 mm. The cables must make several very tight bends (radius $\sim$ 1.5 mm). Electrically, the principal issues are EMI and pulse shapes for the high speed clock and data lines. In addition, the cables carry a substantial amount of power. The total length for the longest (Layer 0) cable is about 25 cm.

The chosen technology is a conventional copper-kapton laminate flex cable. We have made a design of a prototype SVX3 cable, as shown in Fig. 5.16. This cable is made of two conducting layers of 0.5 oz copper (18 μm thick) and a 3 mil kapton dielectric layer. The signal traces are 100 μm on a 200 μm pitch. The power lines are made 700 μm wide to limit the IR drop to less than 100 mV. The width for this design is 8 mm, which is too wide for Layer 0. Our preferred solution to this Layer 0 problem is to split the cable into separate digital and analog cables. To limit the cable profile, the connector on the ladder will be a permanent (probably solder) connection; connections to the portcard will use a disconnectable technology.

The electrical issues related to cross talk, pulse shape, reflections, etc. were studied with prototypes and in simulation [34]. The cross talk was measured to be small for microstrips (signal lines over ground plane), and should be even smaller for broad-side coupled lines. Reflections were studied both in simulation and through prototype measurements. Acceptable digital pulse shapes were obtained. The remaining concerns were cross talk between neighboring cables and EMI picked up through detectors by the analog front end. For the SVXH3 chip we measured a 10 percent increase in noise from a nearby 53 MHz asynchronous clock driven differentially across two neighboring microstrip traces. While we expect the EMI from differentially driven, broad-side coupled lines to be reduced, this will be remeasured with SVX3 prototype cables.

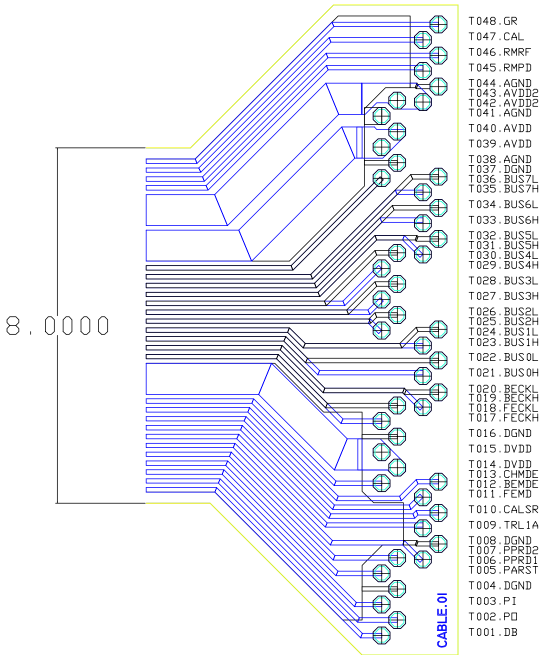

Figure 5.16: Prototype portcard-hybrid SVX3 flex cable. Total width of the cable is 8 mm. There are separate analog and digital ground planes. The data lines are broad-side coupled pairs of 100 μm (4 mil) traces on 200 μm pitch.

5.3.4 Bulkhead

The ladders are positioned between two intricately machined bulkheads. These bulkheads support the ladders at each end and serve as a heat sink for the electrical components mounted on the ends of the ladders. They establish the precision of the barrel assembly and, therefore, must be machined to very close tolerances. Beryllium is used because of its long radiation length and high stiffness. The bulkheads have integrated cooling channels through which the coolant is circulated at approximately -5 °C.

5.3.4.1 Baseline Bulkhead Design

The bulkhead geometry consists of 5 layers. Each layer is a 12 sided ring with flat faces corresponding to the 12 wedges of the detector. The layers are connected by 6 radial spokes that extend from the inner most layer to an outer ring. Ladders are mounted on flat surfaces of each layer, called ledges. Ledges of adjacent wedges are at different radii determined by balancing the requirements for detector overlap and clearance for ladder installation. Ladders are positioned by pins which are installed through notches in each end of the ladder and matching notches in the bulkheads.

Cooling channels are machined directly into the bulkhead. Each layer has an independent cooling channel. The cooling channels are formed by gluing L-shaped covers to each layer of the bulkhead to form a 1 mm $\times$ 8 mm rectangular channel. The design provides close proximity of the ladder mounting surface to the cooling fluid. The fluid is distributed to each layer by aluminum tubes which run radially to each layer and are positioned in line with the bulkhead spokes so not to interfere with ladder installation.

In order to allow possible replacement of the inner two layers, the bulkhead assembly will be constructed of two parts, with the inner two layers separate from the outer three layers. This feature will allow for removal and replacement of the inner two layers of detectors part way through collider Run II without requiring complete disassembly of the entire barrel. The inner sections will be attached to the outer section with pins and splice plates that lie along the radial spokes.

During ladder installation into the barrel the bulkheads will be supported in a rotating fixture similar to that used for construction of SVX and SVX$'$. After ladder assembly is complete an outer screen will be slid over the barrel and attached to the outer ring of each bulkhead at 6 locations. Mounting blocks of the kinematic support system that will position the barrel in the spaceframe will also attach to the outer ring. The screen and support mounting blocks will be machined beryllium blocks that are glued with epoxy to the bulkhead outer ring.

5.3.4.2 Bulkhead Prototype Tests

One beryllium prototype bulkhead and two aluminum prototype bulkheads have been constructed for an earlier four layer design. Except for the fifth layer these prototypes are very similar to the baseline design. A number of tests have been conducted using these prototypes.

- The beryllium bulkhead was inspected on a coordinate measurement machine to compare the actual dimensions to the drawing specifications.

- A test was conducted on a prototype of the pin joint to be used to connect the inner bulkhead section to the outer section. The joint was reassembled several times and provided repeatable location of two parts within 3 μm.

- One aluminum prototype was used to measure pressure drops in the cooling channels. It was determined that the pressure drop will be acceptable for the flow rate required for a ΔT of 1.5°C of the cooling fluid from inlet to outlet. The measurements were made for pure water and for a 30% ethylene glycol/water mixture.

- Two candidate epoxies have been selected for gluing the covers to the cooling channels. Tests are under way to study the effects on the epoxies from long term exposure to the cooling fluids. Cyclic heating/cooling tests are also under way on cooling channel prototypes and the prototype beryllium bulkhead.

5.3.5 Spaceframe Specifications

The alignment of the SVX II barrels with respect to the beam axis is critical for the proper operation of the SVT. Studies indicate that the axis of the barrels must be aligned to within a slope of ± 100 μrad relative to the beam axis, corresponding to a placement of ± 25 μm from end-to-end along a barrel. To achieve such tight tolerances, the barrels will be mounted into a rigid spaceframe using high precision coordinate measurement machines to monitor and adjust the barrel position. The frame will then maintain the precise barrel alignment after the assembly is removed from the measurement platform.

The full mounting requirements for the barrels are:

1. slope within ± 100 μrad of nominal,
2. transverse position within ± 250 μm, and
3. longitudinal position within ± 1 mm.

These values include internal mis-alignments. The spaceframe and mounting specifications then follow.

1. The deflections under full load must be stable and repeatable to ± 10 μm before, during and after installation into the ISL.
2. The transverse barrel translation error must be less than ± 250 μm.

3. The longitudinal barrel translation error must be less than ± 1 mm.

4. The thermal stability must be better than ± 10 μm over a 25° C range.

5. The spaceframe should be of minimum mass.

6. The thermal resistance should be equal to 0.5 cm of foam, equivalent.

7. The torsional deflection due to variations in the strain from the cable, cooling pipe and other asymmetric loads should be less than 10 μm at the mounting points of the detector.

Because it is likely that the overall deflection of the spaceframe will be much larger than 10 μm, the frame will probably be pre-loaded during barrel installation. The barrel mounts will be adjustable at the level of 10 μm. Consequently, there must be accessibility to these adjustment points as well as to the cables and cooling pipes.

5.3.5.1 Baseline Mechanical Design of the Spaceframe

The main structural element of the spaceframe is a 1.4 m long, carbon fiber composite cylinder that contains the barrels. This geometry provides exceptional stiffness with a minimum of material. The cylinder consists of two, 300 μm thick carbon fiber skins separated by a 1 cm thick layer of polymethacrylimide foam. Each carbon fiber skin is made of three layers of epoxy-empregnated carbon fibers, with the fibers in each oriented for maximum strength. The tube is kinematically supported at the ends by the ISL (see Section 6.2.6). Carbon-fiber rings at the ends of the cylinder and other strategically located positions will prevent deformation of the cylindrical cross section under load.

Initially, the spaceframe is constructed as two, independent half-cylinders. The barrels and associated cables and cooling tubes will be mounted into the lower half-cylinder. This open geometry allows full access to the interior of the cylinder for the purpose of surveying and adjusting barrel positions. Once barrels are installed, the top half-cylinder will be bonded to the lower half-cylinder. In order to preserve the precise alignment of the barrels, this procedure may introduce no significant internal stresses. Experience with similar problems in constructing the SVX and SVX′ detectors suggests that this issue is easily solved using common construction techniques.

The barrels are kinematically mounted inside the spaceframe. Mounting blocks connected directly to the beryllium bulkheads transfer the barrel loads to a corresponding set of blocks located on the interior surface of the spaceframe. Carbon fiber ribs inside the spaceframe at these locations distribute this load over the surface of the frame. The initial positions of the blocks on the spaceframe will be set by fixturing to a precision better than 50 μm. The final position will be adjustable over a range of ± 0.5 mm.

The radius of the outermost layer of the bulkhead is expected to decrease by about 20 μm as the bulkhead cools from room temperature to its operating temperature. A judicious choice for the configuration of the mounting blocks can significantly reduce the effect of this contraction on the barrel alignment, and obviate the need to compensate the barrel alignment for thermal contraction of the bulkhead.

5.3.5.2 Barrel and Spaceframe Installation

Barrel installation will occur on a precision coordinate measurement machine. Fiducial markers on each barrel will allow the position of the internal barrel axis to be measured without direct reference to the silicon strips. Similar markers on the frame will characterize the position of the spaceframe. Once the barrels are mounted, the barrel references will be transferred to these frame markers so that the barrels can be aligned with external detectors.

The assembly of the barrels into the spaceframe takes several steps. Each barrel will be placed into the pre-loaded half-cylinder in an order dictated by the cable and cooling pipe layouts, etc., and then coarsely adjusted to some nominal position. After all of the barrels are installed, the cables and cooling pipes will be arranged into their final configurations. With the full load to the spaceframe now fixed, the final adjustment of the barrel positions proceeds. Once the final checks of the alignment are completed, the top half-cylinder is bonded to the lower half, and the end rings installed and glued in place.

After the cylinder is closed, the assembly will be mounted to a transfer fixture that will guide the frame through the ISL. The beam pipe is then threaded through the SVX II and attached to the spaceframe and transfer fixture. Once the detector is installed inside the ISL, the pipe will be rigidly attached to the ISL support cylinder at several places. By carefully over-constraining the pipe, we can greatly reduce the amplitude of oscillations at the middle of the pipe induced by jarring the pipe near its ends. The pipe mounts on the SVX II spaceframe will then serve only as deflection limiters.

5.3.5.3 Alignment with the Beam Axis

After the installation into the CDF central detector is complete, the position of SVX II will be adjusted by moving the combined SVX/ISL assembly. The initial position of the detectors will be determined and adjusted by referencing the fiducial markers on the ISL and SVX II with markers on the quadrupoles in B0. This alignment should place the detector within 1-2 mm of the correct position. Final adjustment of the detector's position is performed using CDF $p\bar{p}$ data to determine the position of the $p\bar{p}$ beams relative to the SVX II detector and then by moving the detector. It is possible that steering of the Tevatron beams can provide this final alignment instead of moving the SVX II. In either case, $p\bar{p}$ beam steering will certainly be used to maintain the position and alignment of the beams between and during stores so that adjustments in the SVX II detector's position should be needed only rarely. Beam steering is discussed in more detail in Sec. 5.9.2.

5.3.6 Cooling and Gas Systems

5.3.6.1 Ladder Cooling

Thin film copper on kapton hybrids mounted to a beryllium substrate are currently considered the baseline design, so the focus of the cooling analysis has been on this technology. A full thermal analysis of the CDF SVX II detector, assuming copper on kapton hybrids mounted on beryllium substrates, can be found in references [35, 36].

Two guidelines have been imposed which drive the design of the ladder from a cooling perspective:

- The silicon should be under 10 °C for nominal operating conditions.
- Thermal runaway does not occur in the innermost layer at the maximum expected chip power dissipation for 2 fb^{-1} of integrated luminosity.

A two dimensional finite difference cooling model has been constructed of a ladder. A one mm wide slice ladder is modeled with all proper scaling to represent the total 3 barrel, 5 layer detector. Nominal operating conditions are determined by the expected chip power dissipation under normal conditions; 300 mW per SVX3 front and back end chip pair. The maximum permissible chip power dissipation is 500 mW per SVX3 chip pair.

The ladder modeling has been broken up into two separate models in order to simplify the solution. First, the conduction region of the ladder is that region from the ladder end at the cooling channel, inboard to the end of the beryllium substrates. The silicon temperature profile is dictated in this region by SVX3 power dissipation, the coolant temperature, and the hybrid substrate thermal resistance (which is inversely proportional to the substrate thermal conductivity and the thickness).

The region inboard of the substrates to the ladder center is composed (in the thermal model) of only silicon, with a gap at the quarter points where there are only wirebonds. The temperature profile of the silicon in this region is dominated by convection. Conduction is inhibited in this region due to the low conduction area of the wirebonds at the ladder quarter points, and the thin silicon detector (300 μm) along the ladder length. It is this region which is heavily affected by external heat loads (such as high power dissipation in the signal cables or poor insulation between the detector region and the surrounding environment), high SVX3 chip temperatures, and internal power dissipation in the silicon due to high radiation damage.

Radiation damage in silicon detectors will result not only in a higher required bias voltage, but also a higher leakage current [4, 20]. The leakage current is temperature dependent, so potentially leads to the condition of thermal runaway in the ladders. Thermal runaway occurs when the internal (temperature dependent) heat generation within the silicon exceeds the heat removal rate by conduction and convection. The effect increases with radiation dose. Hence L0 is the most susceptible to thermal runaway. This effect has been observed experimentally [37] and the measurements have been successfully simulated in a test stand [37, 38]. Analytical approximations to thermal runaway have been provided in [39], some of which have been simulated using the finite difference technique [38].

The baseline temperature profile of the ladders, at the start of the run, is shown in Fig. 5.17. The tem-

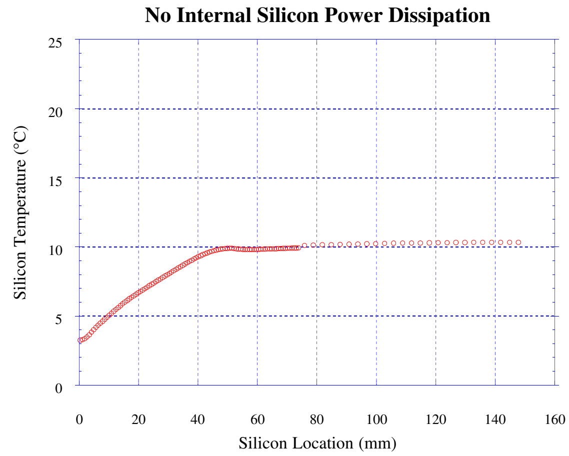

Figure 5.17: Baseline silicon temperature profile at the start of Run II.

perature increases along the conduction region from 3 °C near the cooling channel to 10 °C at the end of the conduction region. The temperature beyond the conduction region remains at 10 °C, due to the assumed insulation between the surrounding environment and the silicon region. These temperatures in the ladder are obtained by providing coolant to the bulkhead sufficient to keep the support ledge on which the ladders rest at 0 °C.

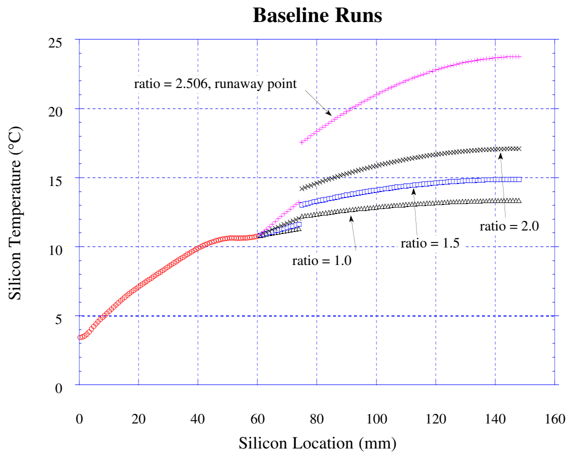

Figure 5.18: Silicon temperature profile after varying degrees of radiation damage assuming 300 mW SVX3 chip power dissipation.

When considering radiation damage, the temperature profile in the conduction region is determined to be essentially constant for variations in the power dissipation within the silicon. The convection region temperature profile varies widely as a function of the assumed level of radiation damage. Applying an upper limit for the bias voltage of 150 V at the end of the run with approximately 1 Mrad radiation damage [4], the leakage current at 0 °C is calculated using the method described in reference [20]. The temperature dependence of the leakage current is calculated on a per-node basis in the finite difference code. The expected temperature profile is shown in Fig. 5.18 at the value of "ratio" equal to 1.0. The power dissipated within the silicon is directly proportional to the integrated luminosity, the damage coefficient, and the applied bias voltage. For this reason other solutions of the temperature profile are determined by applying a multiplication factor to the leakage current at 0 °C, represented in Fig. 5.18 by other curves with differing values of ratio, which allows simple extrapolation to other conditions.

The temperature profile shown for ratio equal to 1.0 is the expected temperature profile at the end of Run II. Thermal runway occurs above the value of 2.506, which in some ways represents a safety factor against thermal runaway in the inner ladders of the SVX II.

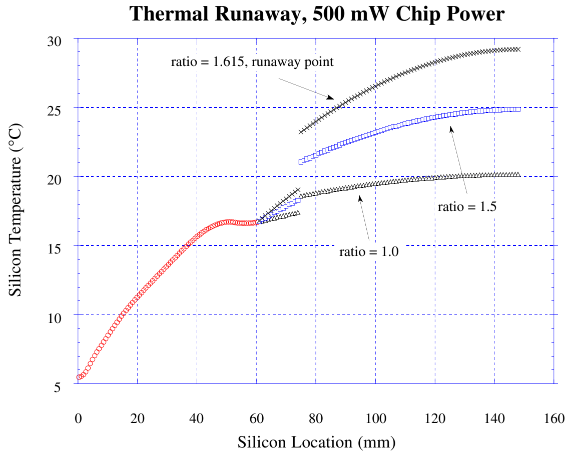

Figure 5.19: Silicon temperature profile with varying degrees of radiation damage assuming 500 mW SVX3 chip power dissipation.

In order to satisfy all design requirements, the temperature profile under higher SVX3 chip power is considered. Applying the same principles as for Fig. 5.18 above, the SVX3 chip power was increased to 500 mW (300 mW was used for Fig. 5.18). Figure 5.19

Ladders	Heat load/ ladder (W)	Ladders / barrel	Heat load/ barrel (W)
Layer 0	2.4	12	28.8
Layer 1	3.6	12	43.2
Layer 2	6.0	12	72.0
Layer 3	6.0	12	72.0
Layer 4	8.4	12	100.8
Total			316.8
Portcards	Heat load/ portcard (W)	Portcards/ barrel	Heat load/ barrel (W)
	12	24	288
Detector Total (W)			1814.4

Table 5.9: SVX II Detector Heat Load

shows the expected silicon temperature profile using the 0 °C support channel assumption as for Fig. 5.18. Although thermal runaway does not occur for the nominal operating conditions after 1 Mrad radiation damage (corresponds to ratio equal to 1.0), the level of safety against thermal runaway is somewhat diminished from the factor of 2.506 as stated above to 1.615 as shown in Fig. 5.19.

The heat load from the detector electronics is summarized in Table 5.9. The majority of the heat will be removed by a water mixture cooling system. A very small amount of heat will be removed by a nitrogen flow through the detector.

A flow rate of 287 g/s will be required to limit the rise in coolant temperature to 1.5 °C for the bulkhead cooling channels and 2.0 °C for the portcard cooling loops with a 30% ethylene glycol/water mixture. To prevent coolant from leaking into the detector, if a leak does occur, the system will be operated under a partial vacuum so that the system pressure in the cooling lines throughout the detector is less than 1 atmosphere.

The system will consists of a recirculating chiller, reservoir, deionizer, flow control and vacuum pump. The general design and operation of the system will be similar to the system for SVX and SVX′. Most components will be scaled in size or capacity for the higher cooling and flow requirements.

The present design provides for separate manifolds to distribute coolant for bulkhead and portcard cooling. Separate manifolds will allow the more critical flow to the bulkheads to be balanced more accurately. The insulated supply and return lines will pass through the 3 degree cone of the modified end plug. The supply and return lines will feed from one end of the spaceframe to simplify spaceframe installation into the ISL. The manifolds that distribute the coolant to the bulkheads and portcard loops will be located along the top half of the space frame to allow access to make connections during barrel installation into the spaceframe. Connections between the manifold and bulkheads will be made with flexible tubing to eliminate the possibility of transmitting loads that may affect barrel alignment.

The gas system for the detector will provide a constant gas flow of nitrogen at 20 SCFH to the barrels. The gas will be introduced to the detector at a temperature 10 °C cooler than the average gas temperature in the detector. The design of the gas cooling system has not begun but a similar system was designed for SVX and SVX′. The system will probably employ a small heat exchanger between the inlet gas and the outlet coolant lines of the portcard cooling. The gas supply will be monitored to prevent impurities from entering the system.

5.4 SVX II Frontend Electronics

The SVX II frontend electronics consists of a pair of radiation hardened CMOS custom integrated circuits which are mounted on the ladder hybrids. These chips are controlled over a high density copper cable through so-called “Port Cards”. The hybrids have been discussed in Sec. 5.3.2, the readout chips and the Port Card are described below. The rest of the data acquisition electronics is discussed in Sec. 5.5.

5.4.1 The SVX3 Readout Chips

The silicon signals are readout by onboard, radiation hardened CMOS integrated circuits called SVX3FE and SVX3BE. Each chip set has 128 parallel input channels. The SVX3FE chip contains the input amplifier and integrator, the variable length pipeline and the logic necessary to handle pipeline and buffer control functions. Any four cells of the pipeline can be set to hold data awaiting readout. The SVX3BE chip contains a Wilkinson ADC, a readout FIFO, and differential output current drivers [15, 5]. The chips are mounted in tandem on the hybrids.

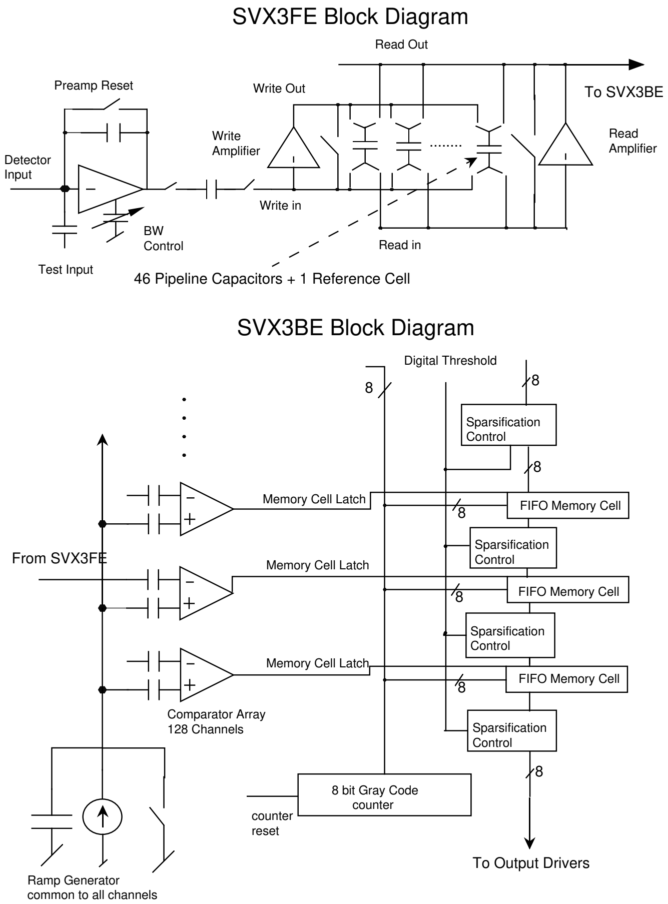

Figure 5.20: A block diagram of the SVX3 chip set.

Figure 5.20 is a block diagram showing the functionality of the SVX3 chip set. The analog SVX3FE chip contains the integrator and dual-ported pipeline while the digital SVX3BE chip houses the ADC (comparator, ramp, and counter), the sparsification logic, data FIFO, and the output drivers (not shown). This block diagram shows only one channel of the chip.

The SVX3FE has two gain stages. The first stage is a charge-to-voltage amplifier with a large dynamic range. The switch across the feedback capacitor resets the front end integrator. This is only done during abort gaps. Approximately 1.6 μs is required for both reset and settling time of this amplifier. The preamplifier gain is specified to be 5.0 mV/fC. The rise time is bandwidth dependent and adjustable (see below), but a 10-90% rise time of 60 ns with an input capacitance of 30 pF is achievable. The integrator's dynamic range is 450fC for unipolar operation.

During SVX3FE initialization, one has the option of switching extra capacitors into the node associated with the dominant pole of the amplifier. This provides control of the integrator's bandwidth and is used to optimize the chip set for the different input capacitances expected on the r-ϕ and r-z sides of the SVX II detector for a range of integration times down to 100 ns.

The second analog stage is another integrating amplifier with a 46 cell pipeline of capacitors in its feedback loop. This amplifier writes the data to the appropriate cell by selecting one and only one of the capacitors as a feedback element. Only the difference in integrated charge from before and after a beam crossing is placed in the pipeline. This allows the second analog stage to have a smaller dynamic range. The gain for the second stage is 3.0 V/V for a total gain of 15 mV/fC or approximately 60 mV/MIP.

The pipeline cell is reset just prior to a beam crossing. A reset time of 25 ns is required. The pipeline must hold the data long enough for a Level 1 trigger to arrive in order that the analog data can be flagged for eventual digitization and readout. The pipeline depth can be set to a maximum of 42 cells. At 132 ns between beam crossings this corresponds to a maximum delay of 5.5 μs. If a Level 1 trigger does not arrive in this time, the cell is overwritten.

If a Level 1 trigger does arrive, a pointer at the correct pipeline depth is set and that cell is bypassed by subsequent pipeline write operations until the analog information contained in the cell is digitized and read out. These bypassed cells are digitized and read out in the order in which Level 1 triggers are received by a unity gain read amplifier which feeds a comparator on the SVX3BE chip. By having four extra cells to hold data for later processing, and by being able to continue to write analog data into pipeline cells while bypassed cells are being digitized and readout, the SVX3 chip set is capable of operating with very little deadtime for Level 1 trigger rates up to 50 kHz.

Figure 5.21 shows a simplified block diagram of the SVX3FE pipeline controller. There are a total of 46 capacitors available in the pipeline for each of the 128 inputs. Up to 4 groups of cells can be queued for digitization and readout at one time.

A central element in the controller is the write pointer shift register. It consists of a ring of flip-flops which pass a token in response to a beam cross-

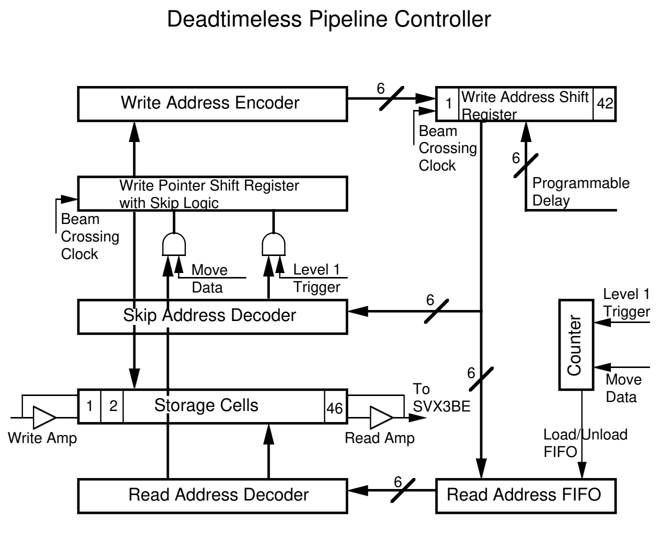

Figure 5.21: Simplified block diagram of the SVX3FE pipeline controller showing the buffering and skip logic architecture required for deadtimeless readout.

ing clock which is synchronized to the collider. Each flip-flop points to a set of 128 capacitor storage cells corresponding to the 128 independent input channels. The flip-flop which has the token causes the 128 pipeline write amplifiers to store the difference in integrated charge before and after the beam crossing in one particular set of the 46 groups of storage cells.

The 6-bit address of the set of cells corresponding to the token's position is passed by the write address encoder to a 6-bit 42 cell shift register and is shifted along from cell to cell once each beam crossing. At the time the chip is initialized a fixed delay from 1 to 42 beam crossings is set into its logic. This establish the Level 1 trigger latency. After the programmed number of crossings has occurred, the write address is shifted back out of the write address shift register and is passed to both the read address FIFO and the skip address decoder. If this occurs in coincidence with the arrival of a Level 1 trigger, then the write address is saved by the read address FIFO and is immediately acted on by the skip address decoder; otherwise, it is ignored. If it is ignored, then those pipeline storage cells referenced by the write address are available to be cleared and overwritten by analog data from subsequent beam crossings.

If a Level 1 trigger did occur, the skip address decoder immediately sets a bypass condition on the appropriate flip-flop in the write pointer shift register. This means that the token will be passed over this flip-flop and the corresponding pipeline storage cells cannot be overwritten by the write amplifiers. Hence, this analog data is saved for later transfer to the SVX3BE chip for digitization and readout.

The Level 1 trigger increments a counter which in turn causes the next available cell in the four cell read address FIFO to be loaded. The oldest address in the read address FIFO, if any, is always available to the read address decoder. When instructed by commands coming from the SVX3BE chip, the read address decoder causes the read amplifiers to pass the analog data from the appropriate group of capacitor storage cells to the comparators on the SVX3BE chip for digitization and readout.

Once the data has been digitized, the 128 pipeline cells associated with this event can be returned to the pipeline for further use. This is accomplished by a signal called "move data" coming from the SVX3BE chip. The signal is used in coincidence with the decoded address from the read address decoder to remove the bypass condition on the appropriate flip-flop in the write pointer shift register. Move data is also use to decrement the counter which effectively removes the oldest address in the read address FIFO.

The block diagram for the SVX3BE chip shown in Fig. 5.20 starts with the array of 128 comparators which are part of a Wilkinson ADC. This ADC simultaneously digitizes the analog voltages presented by the read amplifiers on the SVX3FE chip.

When digitization begins, the proper cell in the pipeline is compared to a voltage ramp generated by a capacitor connected to a current source. The size of the current is fixed by the value of a resistor external to the chip. The ramp voltage rises linearly as a Gray code counter counts cycles on both the rising and falling edges of a 53 MHz clock. The ramp voltage exceeds the read amplifier output voltage at some point and the comparator turns on, latching the counter's current value into the sparsification FIFO. This digital number is proportional to the charge collected for that event. The maximum count is 255, but CDF intends to use only 7 bits which requires 1.2 μs for the complete digitization cycle.

The SVX3BE chip can be configured to read out either all channels, only channels above a user defined threshold, or channels above threshold and their nearest neighbors. In normal operation the digital

SVX3BE chip sparsifies the data, keeping the data only from channels which are above a preset threshold and their nearest neighbors. After digitization at least 500ns is required for sparsification before readout can begin. During readout the data is presented on an 8-bit differential I/O bus. The data are read out on both the high and low levels of a 50% duty cycle 26.5 MHz clock.

Before the readout starts, the I/O bus is acting as an input to the chips and the chips are tri-stated. During readout, a “priority-in” (PI) pad on the first chip of a bus is set high, and it begins to download its data. When that chip finishes, it sends a “priority-out” (PO) pin high which is connected to the PI of the next chip. The last chip on a bus can be set to always readout channel 127. This provides a marker indicating the end of the readout of that bus. Because of sparsification, the actual readout time is highly dependent on the occupancy of the detector. Current estimates based on Monte Carlo studies indicate that the complete readout of a bus will take approximately 10 μs. The first 5-6 μs if for digitization and readout of the r-ϕ side of the detector, and the remaining time is for readout of the r-z side.

5.4.2 SVX 3 Port Card

The Port Card (PC) interfaces with the Fiber Interface Board (FIB) and with the hybrid containing several (4–14) SVX3 chip sets. Most of the communication of the PC is with the SVX3BE chip, while the SVX3FE connects directly to the silicon strip detectors. A schematic diagram of the PC is shown in Fig. 5.22. The basic features of the PC are as follows:

- Connects to five layers of SVX3 chips by means of the high density interconnects (HDI’s).

- Initializes, controls and reads out the SVX3 chips through the HDI’s.

- Provides regulated power supplies for the analog section of the SVX3 chips through the HDI’s.

- Implements two digital-to-analog converters (DAC’s) to generate the calibration voltages for the ϕ and z-sides of the silicon detector.

- Implements the PC Decoder, which interfaces with the FIB and decodes commands to the SVX3 chips.

- Forwards the Level 1 Accept (L1A) control signal to the SVX3 chips.

- Selects the appropriate HDI to download the initialization bit stream during SVX3 chip initialization.

- Transmits SVX3 event data (BUS[0:7]) with associated Odd Byte Data Valid strobe (OBDV) to the FIB.

- Buffers the front end clock (FECLK) and back end clock (BECLK) to the SVX3 chips.

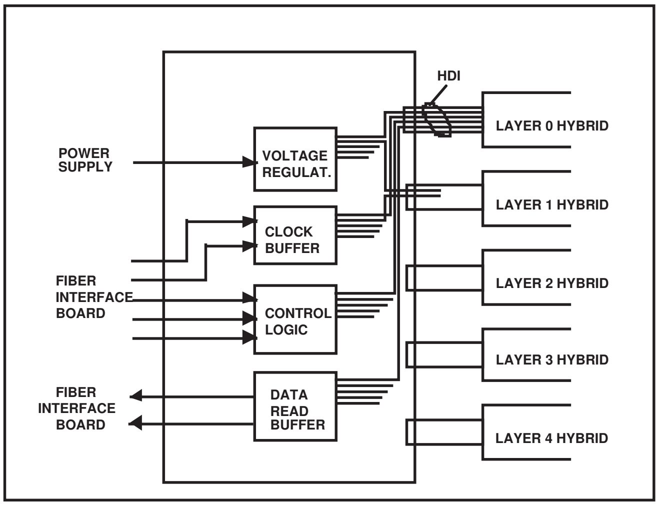

Figure 5.22: Schematic of SVX II Portcard.

5.4.2.1 Cabling

Data from the detector will travel over optical fibers while control signals, power and bias (high) voltage will travel over conventional copper lines. There are 11 differential control signals per PC, one of which is a 53 MHz clock while the other is a beam crossing clock. Each ladder will have an independent bias voltage and three power voltages. In addition, the PC requires 4 separate voltages. The complete cable scheme is not yet designed, but will tend to follow the SVX scheme whereby inside the detector conventional cables will connect at some point to a lower mass, copper-kapton flex cable.

We have estimated the amount of space required to cable SVX II. The low voltages will require 19 AWG 20 pairs per wedge, and the bias voltage will require 10 coax cables per wedge. These connections are in addition to 11 signal twisted pairs plus 5 optic fiber ribbons, possibly bundled within a single protective coating. We expect 45-50 slots of the 125 available slots on one side will be needed.

5.4.2.2 Power Supply Regulators

Analog voltages (2) for the operation of the SVX3 chip are brought in from the power supplies and separated and controlled for each layer by series voltage regulators. The digital supply voltage is controlled by the external power supply.

5.4.2.3 Digital Control

The control lines from the Fiber Interface Board (FIB) that determine the operating mode (initialization, digitization or readout) are set and reset by individual commands via 5 control lines (C0 – C4), a direction signal (DIR), and a strobe clock; the maximum rate for the strobe is 26 MHz. All control signals are transmitted from the FIB to the PC as differential signals. Fanout of the command lines to the hybrids are single ended (TTL) for some and differential (PECL) for others. Enable logic in the control logic block allows individual control for each layer, i.e. commands can be fanned out to any one layer or several layers simultaneously.

5.4.2.4 Clock Buffering

The two clocks necessary for the proper operation of the SVX3 chips are the front end clock (FECLK) and the back end clock (BECLK). These clock signals come from the FIB in differential format, are buffered on board and repeated to each hybrid in differential format. The maximum frequency for the BE clock is 53 MHz. Except during initialization, the FE clock is the beam crossing clock. The single ended (TTL) asynchronous Level 1 Accept signal (L1A) is also buffered on the port card.

5.4.2.5 Data Readback

Data is read back on 8 differential data lines and a data valid signal (OBDV) from each hybrid. The signals are buffered and transmitted over a 9 bit wide fiber optic link (DOIM) to the FIB at a maximum rate of 53 Mbytes/s. During idle times this driver is disabled.

5.4.2.6 Calibration Voltage

A D/A converter in the control logic provides a calibration voltage in 2 ranges (0–0.5 V and 4.5–5.0 V) at a 5 bit resolution. Setting of this D/A is through the digital control by the FIB.

5.4.2.7 Port Card Construction

The PC circuitry will be packaged on a multilayer thick film board on beryllia substrate. Because even at the outer radius of the SVX II a fluence of nearly 300 kRad is anticipated during the lifetime of the detector, the PC components must be radiation hard. All logic functions will be performed in 5 identical multi-function ASIC's (one per layer). Additionally the receiver necessary to buffer the control signals reaching the PC must also be radiation hard ASIC's. Ten voltage regulators per PC will be implemented using control circuitry inside the the multi-function ASIC's together with Darlington pairs of commercial power transistors. These transistors have been shown to withstand the expected radiation dose.

5.5 SVX Data Acquisition

5.5.1 Dense Optical Interface Module

The dense optical interface module (DOIM) is the data link between PC and the FIB. It is a fiber optic transmission/receiver system that incorporates electrical and optical components integrated into densely packaged modules. The transmitter and receiver modules are connected with ribbon fiber that carry 8 data bits and a clock in parallel to the FIB. Below we will discuss the system requirements, characteristics and functioning of the DOIM.

5.5.1.1 System Requirements

Five DOIM transmitters are mounted on each PC. The total number of DOIM's for the 3 barrels is 360. The same number of receivers are located on the FIB's. Some of the system requirements are as follows:

1. Provide the path for 8 data bits and a clock.
2. The physical size should be as small as possible to fit into a very densely packed PC.
3. The power consumption should be small to reduce the burden on the cooling system.

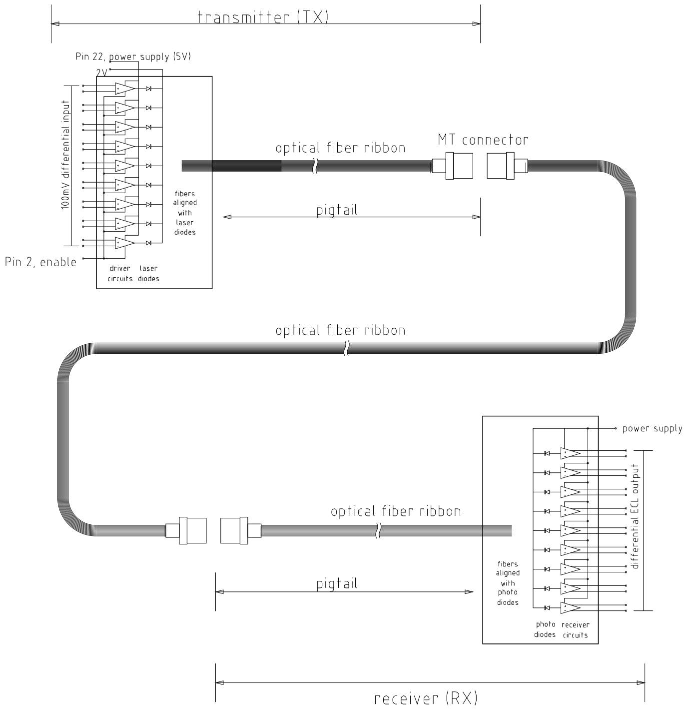

Figure 5.23: Block diagram of DOIM

4. Introduce as little material as possible to reduce the total radiation length.

5. Be radiation hard enough to run continuously and reliably.

5.5.1.2 Function and Operation

The DOIM provides a virtual circuit between the PC and the FIB. It accepts electric signals from the PC and delivers electric signals to the FIB. The electro-optical and opto-electric conversion are hidden from both the PC and the FIB. A block diagram is shown in Fig. 5.23 which demonstrates it's function and operation. The transmitter is a 9 channel laser array driven by a custom designed driver circuit. The driver accepts low current differential signals from the SVX3BE chip and provides the current necessary to turn on and off the laser according to the pattern of the data. The data in optical format is coupled to a ribbon fiber and transmitted to the FIB. On the receiver end, the optical signals are converted back to electric signals by a photodiode and an amplifier array which bring the signals to ECL levels.

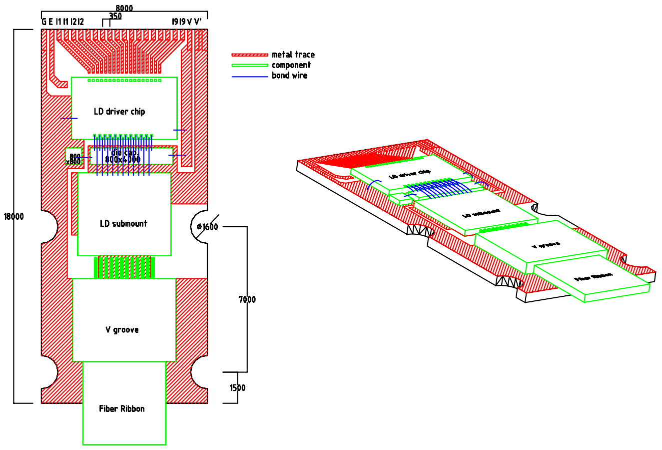

Figure 5.24: Layout of transmitter DOIM

5.5.1.3 Integration and Package

Figure 5.24 shows the layout of the transmitter module. The receiver module is the same in concept and very similar in design. The laser diode array is attached to its own individual submount. This submount, along with other components and the driver chip, are mounted on an aluminum nitride substrate. This material was chosen because of its good thermal conductivity. The components on the substrate are wire-bonded to provide the electric connections. The coupling of the optical fiber to the laser diode array is done with a silicon V-groove block. The V-grooves on the block guide the individual fibers in the ribbon so that they are face-to-face with one of the laser diodes of the array. The other end of the ribbon is terminated with a MT connector. The receiver chip is very similar except that the array of laser diodes is replaced with an array of PIN diodes and the driver chip becomes a set of amplifiers.

5.5.1.4 Characteristics

Both the laser and PIN diode arrays are being developed by the Telecommunication Laboratory in Taiwan. The transmitters are 1550 nm InGaAsP/InP edge emitting laser diodes. The receivers are InGaAs/InP planar PIN's. Their characteristics are listed in Tables 5.10 and 5.11.

Both the driver and receiver chips are also being developed in Taiwan. The input of the driver chip is a low current differential signal defined by a SVX3BE chip. The driver will deliver approximately 20 mA to

Laser Diode	
1550nm InGaAsP/InP edge emitting laser diode	
Wavelength	1550 nm nominal
Bias Current	20 mA
Threshold Current	10 mA
Optical Power	$\geq$ 200 mW coupled to fiber
Forward Voltage	1 V
Operating Temperature	0–40 (°C)

Table 5.10: Characteristics of laser diode

Photo Diode	
Description: InGaAs/InP planar PIN	
Sensitive Wavelength	1000–1605 nm
Responsivity (A/W)	0.9 @1550 nm
Dark Current (nA)	$\leq$ 1.5 @-5V 25°C
Capacitance (pf)	≤ 4
Breakdown Voltage	15 V
Bandwidth (GHz)	1.9 @3dB
Operating Temperature	0–40 °C

Table 5.11: Characteristics of photodiode

Driver Chip	
Input	Differential with common mode voltage $2.5 \pm 0.5\ V$ and differential swing greater than 100 mV
Data rate	53 MHz
Switching time	$t_r, t_f \leq 1.5$ ns
Channel skew	$< 1ns$
Supply Voltage	5 V
Control input	TTL signal to disable driver
Power dissipation	$<$ 2.3 mW

Table 5.12: Characteristics of driver circuit

Receiver Chip	
Output	ECL
Data rate (MHz)	53
Switching time (ns)	$t_r, t_f \leq 2.0$
Channel skew (ns)	< 1
Supply Voltage (V)	5
Power dissipation (mW)	< 2.0

Table 5.13: Characteristics of receiver circuit

the laser diode for a data high bit. The receiver has a transimpedance input stage followed by 2 or 3 amplification stages. The output is an ECL level. Some of the characteristics of driver and receiver are listed in Tables 5.12 and 5.13, respectively. Prototypes of both the driver and receiver chips are being implemented in CMOS, bipolar and GaAs technologies. The CMOS and bipolar versions have been submitted through Eurochip. The GaAs versions will be submitted to a local foundry in Taiwan.

5.5.2 Fiber Interface Board (FIB)

5.5.2.1 Functionality of the FIB

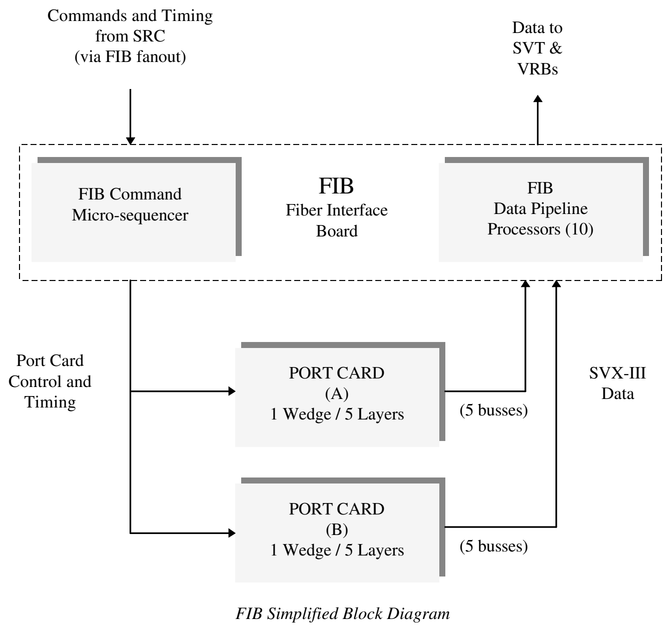

Figure 5.25: Schematic diagram of the FIB.

The FIB will be used to both control the SVX3 chips through the PC and to transfer collision event data from the SVX3 chips to the VRB's and to the SVT system [41]. A schematic diagram of the FIB is shown in Fig. 5.25. During operation, the FIB receives commands and timing from the SRC via the FIB Fanout. The FIB interprets these in-coming commands and delivers encoded control and timing information to the two target PC's. The control information is decoded on the PC's which then generate the logic levels to control the SVX3 chips. Following a request for data (readout command from SRC), the PC's also transfer the SVX3 data back to the FIB where header information is added, gray-code conversion, pedestal subtraction, and gain corrections are completed, and end of record information is added. As the data stream is being processed it is also being transferred to the SVT and VRB's via fiber optic cable at a peak rate of 1.06 Gigabits per second.

The following is a list of the FIB requirements:

- 9U x 400 mm single width VME board.
- VME slave interface for status and control.
- Four G-Link transmitter daughter card interfaces for sending SVX3 data to the VRB's and SVT system.
- Interface to custom J3 backplane for receiving control and timing information from the SRC via the FIB Fanout.
- Interface to control two PC's.
- Ten data ports to receive data from two PC's at a data rate of 53 MBytes/sec in each.
- Append Bunch Crossing and HDI identification header frames to the data from the PC's.
- Gray Code convert all incoming data from the SVX3 chips.
- Perform pedestal subtraction and gain corrections on a channel by channel basis for all incoming SVX3 data.
- Append EOR frames at the end of the data from the SVX3 chips. Either End of Record Normal or End of Record Truncate (2x) followed by End of Record Fill (2x).
- Synchronize and shape the clocks for the SVX3 chips.
- Allow diagnostic testing of the SVX3 chips and PC.

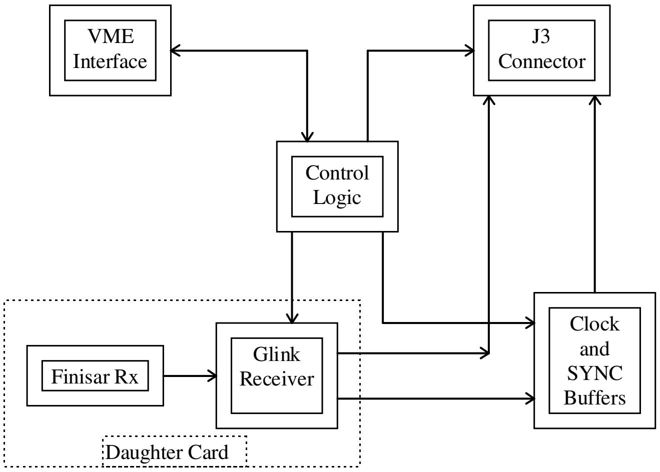

Figure 5.26: Schematic diagram of the FIB Fanout.

5.5.2.2 FIB Crate Fanout Board

The FIB Fanout is a 9Ux400 VME card which resides in a FIB crate. A schematic diagram of the FIB Fanout is shown in Fig. 5.26. The FIB Fanout provides the interface between the SRC module and the multiple FIB boards within the FIB VME crate. There is a single FIB Fanout board in slot 15 of each FIB crate. The FIB Fanout board receives commands and timing signals from the SRC module on a fiber optic G-Link and places them on the J3 backplane for use by the FIB's. The FIB Fanout is configured by the VME master in the FIB crate.

The following is a list of the FIB Fanout requirements:

- 9U x 400mm single width VME board.
- VME slave interface for status and control.
- G-Link receiver daughter card interface for receiving SRC control and timing. Interface to custom J3 backplane for sending control and timing information to FIB's.
- Generate a VME crate reset on command from the SRC.
- Provide MCLK and SYNC buffers for each FIB slot.

5.5.3 High Speed Fiber Link

The high speed Gigahertz fiber transmitter or G-Link TX is a daughter card that mounts on the FIB. Up

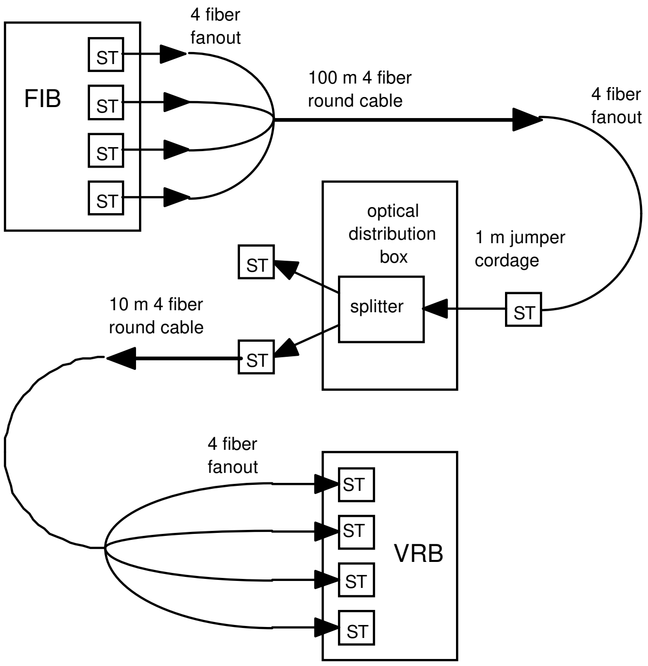

Figure 5.27: Schematic diagram of the G-link data path.

Device	Supply Voltage	Supply Current	Power
G-Link TX	+5.0 V	120 mA	0.63 W
	-5.2 V	400 mA	2.00 W
G-Link RX	+5.0 V	90 mA	0.48 W
	-5.2 V	520 mA	2.60 W

Table 5.14: Power requirements for G-link cards

to 20 bits of parallel data is serialized and transmitted over fiber at data rate speeds up to 1.25 Ghz. There will be four G-Link TX cards on a FIB. The Finisar optical devices on the G-Link card use a ST fiber connector and 50/125 μm or 62.5/125 μm multimode fiber. The four G-Link card fibers will have ST connectors on the front panel of the FIB. The data is transmitted over 4 individual fibers within a cable to an optical splitter. The data leaves the optical splitter on two fibers. One fiber goes to the G-Link receivers mounted on the VRB while the other fiber goes to the G-Link receivers at the SVT. A block diagram of the hardware that makes up the data path is shown in Fig. 5.27.

The G-Link TX is a 2 inch by 3.75 inch card containing a 60 pin AMP 104068-6 connector, a HP HDMP-1012 transmitter, a Finisar FTM-8510 transmitter, and a few discrete surface mount components. The G-Link cards are general purpose serial optical link cards that can be operated in several configurations. Control signals are available at the AMP connector to allow the motherboards to select the mode of operation. Table 5.14 provides an estimate on the power requirements for the G-Link TX and G-Link RX.

5.5.4 VRB and VRB Fanout Modules

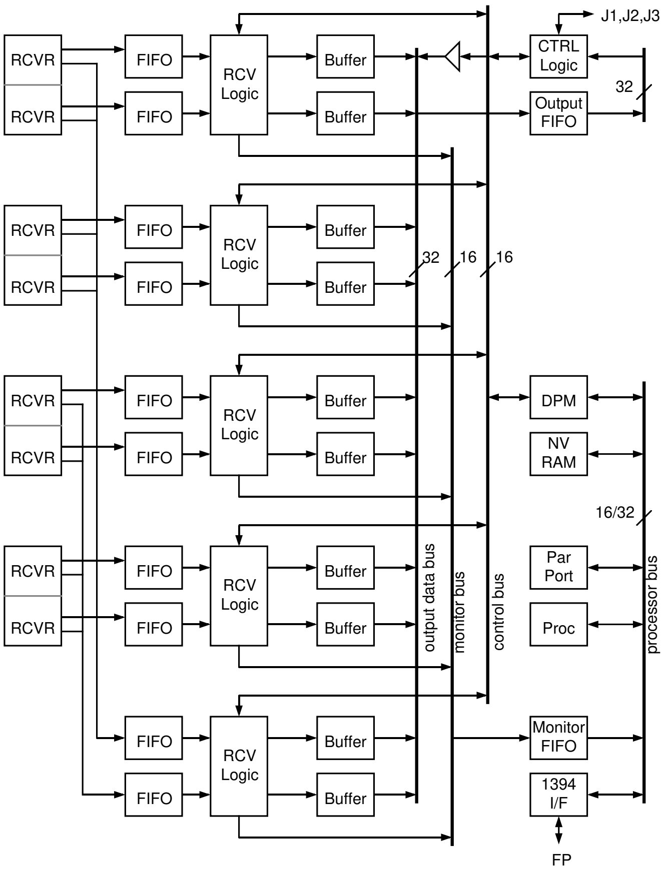

Figure 5.28: Schematic diagram of the VRB module.

The VRB (VME Readout Buffer) serves as an input buffer for the Level 3 trigger processors. It receives data from the FIB's following a Level 1 trigger accept and holds that data while the Level 2 trigger decision is made. To support very fast data readout, the VRB can accept input data at up to 60 Mbytes/s on each of ten channels. The output rate, following a Level 2 accept, is limited by VME bandwidth to approximately 50 Mbytes/s for each group of VRB modules. A schematic diagram of the VRB module is shown in Fig. 5.28.

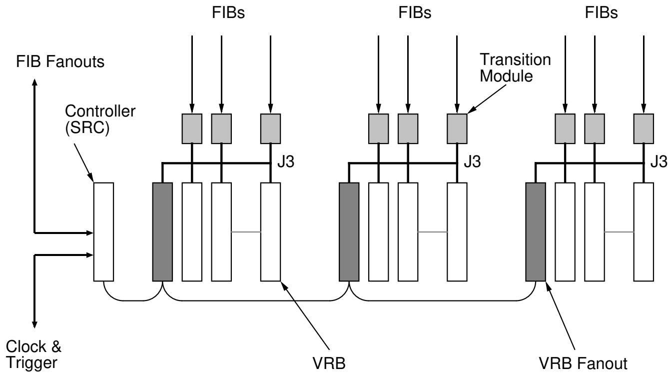

Figure 5.29: Schematic showing the use of the VRB Fanout module in a multicrate system.

The VRB supports a programmable number of internal dual-port buffers which are randomly accessible for simultaneous input and output. In the SVX application, the selection of input and output buffer number for each event is determined by the SRC module, which transmits this information to the VRB's through the VRB Fanout module and a special backplane in each VRB crate. Four buffers in the VRB are assigned to the corresponding four CDF trigger system buffers and the remainder are used to hold events awaiting transmission to the Level 3 system. The mapping of CDF trigger buffers to VRB internal buffers is also handled by the SRC. The VRB Fanout module serves as a repeater for SRC control messages. This allows use of a single SRC module which may be placed in or near one of the VRB crates. Figure 5.29 shows how the fanout module is used in a multicrate system.

When the VRB receives a write buffer message, it is accompanied by global SVX pipeline capacitor and bunch crossing numbers. This information is used by the VRB to check the integrity and synchronization of arriving data. On output, the read buffer message is accompanied by a Level 2 event number which is appended to the event for tracking by the Level 3 processors.

The VRB is a 9U X 400 mm, VME64 compatible module. The VME interface is designed to be very simple, with a 16 bit register providing the total byte count for all active channels and a single FIFO register for accessing the data in either 32 or 64 bit block transfer mode. The data is read out by a standard VME Processor module and transmitted to the Event Builder.

Functionality of the VRB is highly programmable, so that it can accommodate almost any input and output data format, with error checking and optional inline data processing. The buffer logic is implemented on mezzanine cards to allow upgrades in buffer size or processing features. The receivers for the high speed serial links are on a transition module which is common to that used in the SVT system. This transition module accepts data from ten logical channels multiplexed onto four physical data links. Each channel corresponds directly to one layer of an SVX wedge. The backplane which supplies SRC control messages and return status is identical to the FIB crate backplane.

A small on-board processor is used to initialize the programmable logic and to control an independent fast serial interface. The serial interface allows statistical sampling of the event stream without interrupting normal data flow. A non-volatile memory holds the processor code, programmable logic configuration data and the current module initialization information (active channels, number of buffers, buffer sizes, error detection features, etc). The VRB normally requires no external initialization at startup.

5.5.5 The SRC

The Silicon Readout Controller (SRC) operates as the interface of the SVX II DAQ subsystem with the Trigger Supervisor and the CDF Master Clock as well as the upper level controller over the state of the readout electronics. It therefore controls the mediation, interpretation, generation, execution and timing of all the commands that initiate, realize and complete the readout of the silicon detectors with the SVX3 chip set. The SRC is a D16 9U VME slave module, with most of the logic implemented via Xilinx FPGA's. Figure 5.30 shows the relation of the SRC to the rest of the DAQ system. The links of the SRC to the various components of the system are described below.

1. The unidirectional Master Clock link is implemented with 4 copper lines carrying the 53.104 MHz CDF Master Clock (synchronized to the Tevatron) , the SYNC signal which is 1/7 of the Master Clock rate and marks the time of possible proton-antiproton interaction, the Beam Crossing signal which tags the RF buckets with beam particles and the Bunch Zero signal that marks a

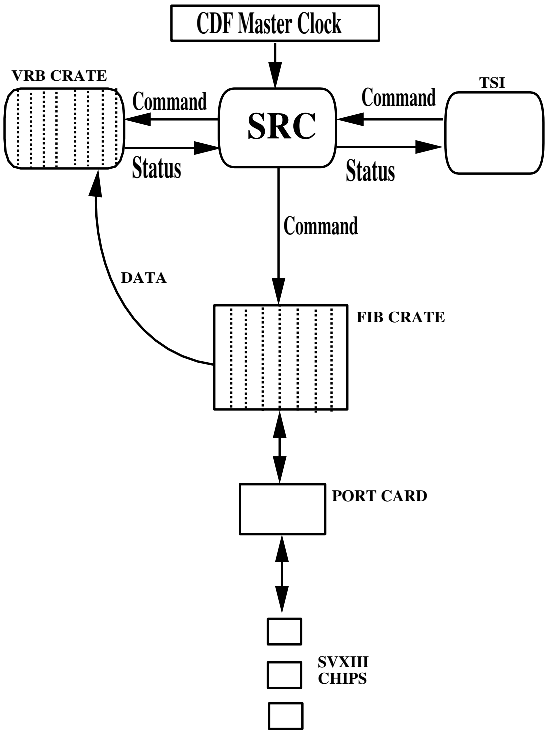

Figure 5.30: Schematic diagram of the SRC function.

reference bucket used for counting.The SRC provides a Phase-locked Loop to ensure the timing stability required by the G-Links used throughout the DAQ system.

2. The bidirectional Trigger Supervisor (TS) link is implemented with 9 lines of optical fiber carrying commands from the TS and 4 lines of copper returning status signals to the TS. The TS can broadcast up to 2 words every 132 ns: a Level 1 Accept (L1A) word and a Level 2 word (either L2-Accept (L2A) or L2-Reject (L2R)). The L1A word consists of the L1A code and a buffer number (0-3) in which to store the event while waiting for the L2 decision. It is the responsibility of the TS to ensure that the buffer allocated is free for use. The L2 word consists of the accept/reject code and the buffer number of the corresponding L1A.

   There are four signals returned from the SRC to the TSI, namely: L1_DONE, DONE, WAIT, ERROR. They serve as follows:

   The L1_DONE signal marks the return of a L1-Accepted cell to the chip pipeline. Upon receipt of a L1 Accept from the TS, the SRC sets the L1A line on the SVX3 chip high via the Fiber Interface Board (FIB), thus tagging a chip pipeline cell as the L1-Accepted cell and removing it from the pipeline. At a later time when the SRC is free, it initiates the digitization and readout cycle for the tagged event. Information about the event is sent to the VME Readout Board (VRB) as detailed in the following section. Once the digitization of the data has been completed and the beam structure allows it, the SRC issues a command to the SVX3 chip to untag the cell element and send it back to the pipeline. At this time L1_DONE is returned to the TS.

   Upon receipt of a L2A the SRC deasserts the DONE line to the TS. When the transfer of the data for the L2-Accepted buffer has been successfully completed to a VRB buffer location this buffer will then be marked as a Scan Buffer indicating that readout into L3 can take place. The SRC then reasserts DONE.

   If the VRB has no buffer location available to store another L2-Accepted event the SRC asserts WAIT. This results in the TS inhibiting further L2A's. When a buffer in the VRB is freed WAIT is deasserted.

   The ERROR signal is asserted only in the case of catastrophic error such as mismatch between the event being read by different wedges or loss of synchronization between the chips. This will cause the TS to initiate the HALT-RESET-RUN sequence. The errors which are considered catastrophic by the SRC are programmable at run time. A time history and statistics on each error type is stored for readout via VME.

3. The bidirectional VRB link is implemented via 23 copper lines of which 10 are status/error lines and 13 are command. The status/error lines from all the VRB's are OR'ed together.

   Upon receipt of a L1A the SRC sends to the VRB the buffer number in which the data is to be stored, the pipeline cell number and the bunch crossing number. The VRB indicates that it will be busy reading data from the chip by asserting the READOUT_BUSY line to the SRC. Once the transfer of the data from the chip to this VRB location has been completed the VRB deasserts the READOUT_BUSY line. Upon receipt of L2A the SRC sends to the VRB the buffer number from which the data will be read into L3 as well as the event id, at which time the VRB asserts the SCAN_BUSY line to the SRC. When the data have been readout into L3, the VRB deasserts the SCAN_BUSY line.

It is the responsibility of the SRC to monitor and manage the data buffers in the VRB.

4. The unidirectional FIB link is implemented by means of 4 optical G-Links (one to each crate of FIB's). Twenty bits of information are transferred every 132 ns over each serial line implemented using the G-Links (each of which carries the same information to the 4 FIB crates). However, the signals on each can be delayed separately, allowing the synchronization of the system without having to match cable lengths. In addition to the command word, the SRC provides the Master Clock to the FIB (and hence to the SVX3 chips). Two of the 20 bits transmitted mark the status of the SVX3BE chip for any given L1A, marking whether it was quiescent, digitizing or reading out.

To aid in system integration tests, the SRC has the ability to emulate the CDF Master Clock and commands from the TS as well as to send arbitrary command sequences to the FIB.

5.5.6 Readout into Level 3

The output port of the VRB module is a VME connection supporting 64 bit block transfers. A commercial VME64 processor module (scan processor) in the VRB crate is used to access data from each VRB sequentially. The VRB contains an internal DMA controller which concatenates buffers to allow a single block transfer read of all data. The VRB output port is pipelined to permit VME transfers at up to 80 Mbytes/s with a high speed readout processor. The speed of available VME processors and output data links, plus normal VME overheads, will limit this rate to 30–40 Mbytes/s initially. A schematic diagram of the transfer of the data to Level 3 is shown in Fig. 5.31.

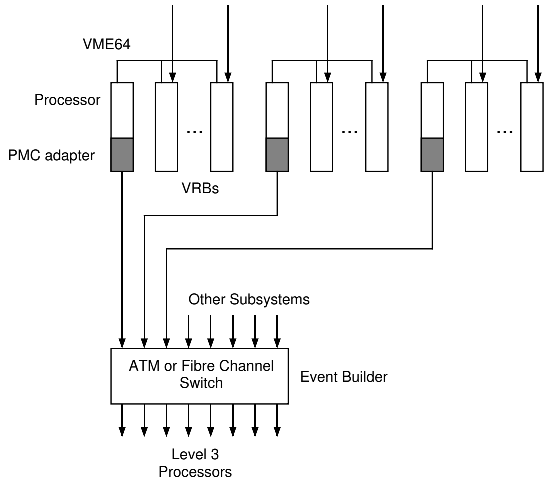

Figure 5.31: Schematic diagram of the transfer of SVX II data to Level 3.

Depending on the VME transfer rate achieved, the VRB modules will be partitioned into three or six readout crates. Each crate drives a single data link to the Event Builder and Level 3 trigger system. The VRB crates are scanned in parallel, so doubling the number of VRB crates will, in principle, reduce the readout time to Level 3 by 50%. At an occupancy of 3 kbytes/event per VRB (data from ten layers), the scan time would be approximately 1 ms for a three VRB crate system, resulting in an average Level 2 accept rate of 1 kHz.

The readout processor in the VRB crate will likely include a PMC (PCI Mezzanine Card) port. This port is used for direct connection to the Event Builder through either a Fibre Channel or ATM adapter. Testing of a 500 Mbyte/s ATM switch for Event Builder applications is currently in progress, using the CDF Data Acquisition software. This switch supports input at rates of 15 Mbytes/s/port (up to 32 ports) or 60 Mbytes/s/port (up to 8 ports). The SVX II system would use three of the high speed ports or twelve of the low speed ports on this switch.

Readout of VRB data by the processors and transmission of this data to the Event Builder is an asynchronous process. The VRB's will signal the SRC when all data for an event has been copied to the scan processor so that the SRC can reuse the VRB scan buffer. If all VRB scan buffers are filled, the SRC will return a WAIT signal to the trigger system.

5.6 SVX II Power Supplies

The three basic requirements for the SVX II Power Supply system are: (1) to provide all the power for the silicon ladders, the SVX3 chip set, and the PC's, (2) to control and monitor all the relevant output voltages and currents, and (3) to provide failure mode protection for safe power supply and system operation.

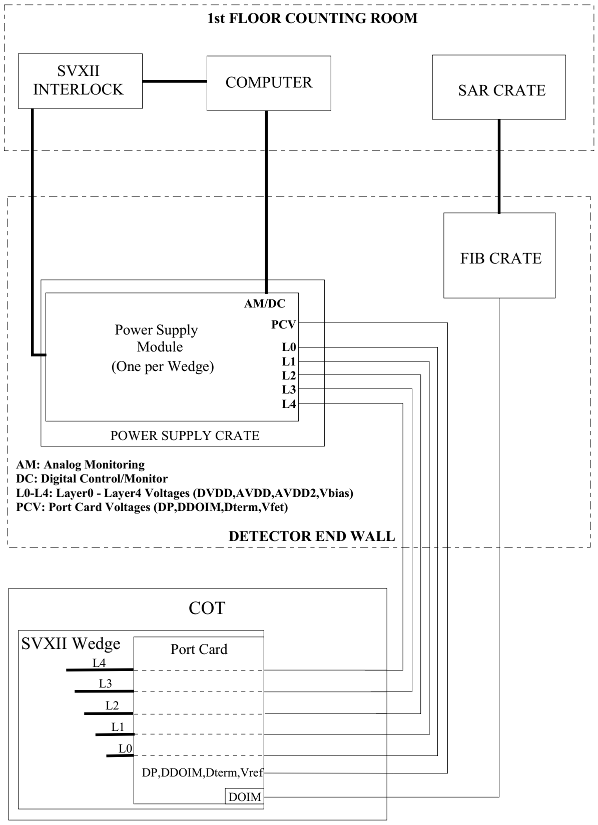

Figure 5.32: Silicon detector general power distribution layout.

The basic building block of the SVX II silicon vertex detector is the silicon ladder. The ladder consists of double-sided AC coupled silicon microstrip detectors, the analog and digital frontend electronics (SVX3 chip set), and a hybrid device with I/O drivers and receivers. DC high voltage (less than 200 V) power is needed to bias the silicon detectors, and DC low voltage (5 V) is needed to power the analog, digital, and I/O electronics. Thus, a Power Supply Module must deliver a number of voltages with different current, stability, and monitoring requirements. To compensate for radiation induced bulk damage to the silicon detectors, the cabling, power supply, monitoring and control systems allow for the setting of different detector bias voltages in different regions of the detector. Also required is a fail-safe system for monitoring and controlling all the output voltages and currents. Finally, the Power Supply System is integrated into the overall monitor, control, and interlock system for the CDF experiment.

While the preceding general requirements are based on the SVX′ Power Supply System, there are some major changes to the SVX′ system that directly impact specific requirements for the SVX II Power Supply System. The major changes include: 1) greater than a factor of 3 increase in components, caused by increasing the number of wedges from 24 to 72 and the number of layers from 4 to 5, 2) a significant increase in detector bias voltage (from 80 V to 200 V) and of power supplied to each wedge (from 6.5 W to 50 W), and 3) independent low voltage outputs to each of 5 layers on a wedge. Table (5.15) provides the specific power requirements for one SVX II wedge. Several comments apply to these specifications:

1. The DVDD outputs are not post-regulated on the PC. Thus, local current sensing at the Power Supply Module is used to compensate for the cable drop.

2. The AVDD and AVDD2 outputs are post-regulated on the PC.

3. All output voltages and currents are monitored to track the operating characteristics of the detector, electronics, and power supply.

4. All low voltage outputs have over-voltage and under-voltage trips, the V_{bias} outputs have over-voltage trips, and all output currents have over-current trips.

5. We will implement a split-bias voltage scheme to symmetrically bias the detectors.

6. The question of linear vs switching supplies to supply all outputs is being studied.

Figure (5.32) shows the general power distribution layout. Remote control of a Power Supply Crate is achieved through a computer located on the first floor counting room. A Power Supply Crate contains the

Layer 0 through Layer 4								
Output	V_o	V_{select}	Sense	I_o(L0)	I_o(L1)	I_o(L2)	I_o(L3)	I_o(L4)
DVDD	+5.0 V	Fixed	Current	0.20 A	0.30 A	0.45 A	0.45 A	0.60 A
AVDD	+6.0 V	Fixed	None	0.14 A	0.20 A	0.34 A	0.34 A	0.48 A
AVDD2	+4.5 V	Fixed	None	0.10 A	0.15 A	0.30 A	0.30 A	0.40 A
V_{bias}	0-200 V	Program	None	0.01 A	0.01 A	0.01 A	0.01 A	0.01 A
		Port Card						
DP	+5.0 V	Fixed	Voltage	2.0 A				
DDOIM	+2.0 V	Fixed	Voltage	-1.5 A				
Dterm	+2.5 V	Fixed	None	0.1 A				
V_{FET}	+8.0 V	Fixed	None	0.1 A				

Table 5.15: SVX II Power Supply Requirements for One Wedge

Power Supply Modules and is located at the Detector End Wall. Each Power Supply Module supplies one wedge of the SVX II detector where one wedge includes 5 silicon ladder ends (Layer 0 through Layer 4) and a PC. Also, power to each of the 5 detector layers supplied by a single Power Supply Module is independent of the power supplied to any of the other layers. This is an important safety feature so that failures in one wedge do not affect the operation of any other wedge, and failures in a particular layer do not affect the other layers of the wedge. Each Power Supply Module contains on-board circuitry to implement the digital control and analog monitoring of the output voltages and currents. Power supply fault trip monitoring is designed into the Power Supply Module in terms of monitor and trip detection circuits that shut down power to a particular layer in the event that voltages or currents exceed predefined trip points. The second level is an interlock signal that turns off the Power Supply Modules in emergencies not related to the Power Supply System (eg. fire alarm, loss of cooling). This effectively integrates the Power Supply System monitoring and control into the overall monitor and control system for the SVX II detector.

5.7 SVX II Alarms and Limits System

The electrical power and cooling systems of the SVX II detector require monitoring in order to detect possible problems. This monitoring is implemented at two levels. At the first level, certain critical system parameters, such as the detector temperature and various low voltage levels, may reach values that require immediate intervention in order to prevent damage to the detector. These parameters will be continuously monitored by the controlling hardware, and these devices will intervene as necessary to maintain safe operating conditions. At the second level, parameters will be monitored by a passive "alarms and limits" system in order to observe the operating state of the system, track system performance, understand the cause of any protective actions taken by the first level and notify operators whenever anomalous conditions exist.

The alarms and limits system for SVX II will be modelled after that used by SVX and SVX′. As for the previous silicon detectors, the system will be based upon the accelerator control system, ACNET. The ACNET system provides a CAMAC-based front end and data acquisition system for measured parameters, a transparent communications protocol between the data acquisition hardware and workstations running ACNET software, a high-level software interface that allows access to each monitored channel and a graphical user interface. ACNET allows each monitored channel to have an upper and lower limit defined. Excursions of a parameter beyond either limit will set an alarm condition. Automatic data-logging systems are also available in ACNET and may be used to log information for later analysis.

The power supplies for SVX II will probably be controlled and monitored directly by a PC. In this configuration, the ACNET system will query the PC for power supply information, as was done for many

CDF sub-systems in Run I. This information will be integrated into the CDF detector-wide alarms and limits system. Temperatures and other cooling system parameters will be measured by CAMAC modules directly under control of the ACNET system.

5.8 SVX II Performance Issues

5.8.1 Hit Occupancies in the SVX II

Because both the tracking reconstruction resolution and the Level 2 trigger (through the SVT) depend critically on the SVX II, considerable effort has gone into understanding the expected hit occupancies in the SVX II detector [42]. Since much of the occupancy is the result of minimum bias interactions which accompany the triggered event, a careful effort was made to tune the Pythia event generator to the observed occupancy seen in the SVX′ detector during Run Ib [43]. Pythia was then used to generate minium bias events at the level of 2.7 interactions/crossing, the expected number at the beginning of Run II. In Table 5.16 we show the average and maximum occupancies for the various parts of the detector. The numbers are in percent and correspond to the case of 2.7 minimum bias events per crossing. Modules 0 and 5 are the outer most half ladders, 1 and 4 are the inner half ladders of the end barrels, and 2 and 3 are the two halves of the central barrel. We assumed nearest neighbor readout, a Gaussian shaped luminous regions with $\sigma_z = 24$ cm, signal/noise of 16, and a readout threshold of $3 \times \sigma_{noise}$. The columns labelled "most" mean that this is an average of the occupancy for this wedge when it had the highest occupancy of any wedge being readout. This is important in determing the time to read out the data because the wedge with the largest occupancy will always determine the readout time.

To estimate the readout time we assumed that a triggered event had an occupancy which was twice the maximal min bias occupancy. We added the average occupancy associated with 2.7 additional interactions. Finally we added an additional 2% occupancy for noise. In Table 5.17 is shown the actual number of hits for the various layers for the r-ϕ and r-z sides under these assumptions. The time to read out the data is also shown in Table 5.17.

5.9 Operating the SVX II

There are several challenges involved in successfully operating a system as complex as SVX II for an extended period of time. The biggest challenges are primarily calibrating the detector and monitoring it for problems. Fortunately, CDF has operated two silicon vertex detectors over the last four years, and that experience is a useful guide in planning for the operation of SVX II.

5.9.1 Calibration

CDF's previous silicon detectors were calibrated daily during quiet time by measuring the pedestal, noise, gain, and optimal threshold for each channel. As expected, these measurements exhibited no problematic short term variations, and all long term variations were common to all channels in a specific electrical segment (chip or ladder). The SVX II will have a larger channel count, but this should not be a problem since the segmentation of the readout is similar. Thus, we expect that the calibration approach for SVX II can be very similar to that for SVX and SVX′.

The primary operational challenges faced by the previous detectors were problems in the readout chain. The key to dealing with these problems was early detection through real time monitoring. This was accomplished with online monitoring programs which measured the occupancy of each chip and checked for readout problems. This approach identified most problems within minutes. Offline monitoring measured the occupancy of each channel and the tracking efficiency for each chip. It also provided redundancy for the online checks. A similar monitoring approach will be used for SVX II.

5.9.2 Beam Steering and Feedback Control

A program has begun to implement a beam steering and feedback control system to stabilize the position and angle of the beam with respect to the SVX II detector. Because the proposed SVT trigger hardware does not reconstruct a primary vertex, stability of the beam position is necessary for successful triggering. In addition, with SVT tracks only in the r-ϕ plane, it is essential that the detector axis and the beam axis be very close to parallel.

PYTHIA generator with pile up 2.7 events/crossing					
		Min bias occupancy		Min bias occupancy	
MODULE	LAYER	AVG R_ϕ	AVG Z	MOST R_ϕ	MOST Z
0 & 5	0	2.343	4.258	5.634	13.697
	1	1.362	1.661	3.306	5.359
	2	0.750	0.764	1.969	2.030
	3	0.605	0.885	1.607	2.779
	4	0.466	0.469	1.180	1.191
1 & 4	0	3.257	4.729	7.071	13.134
	1	1.836	1.889	4.202	5.457
	2	0.941	0.955	2.225	2.252
	3	0.743	1.001	1.830	2.787
	4	0.554	0.557	1.331	1.340
2 & 3	0	4.311	5.285	8.401	12.693
	1	2.278	2.070	4.726	5.276
	2	1.139	1.150	2.560	2.577
	3	0.887	1.147	2.052	2.904
	4	0.661	0.660	1.507	1.503

Table 5.16: Occupancies in % for average and maximal minimum bias events assuming 2.7 events/crossing and a luminous region with $\sigma_z = 24$ cm.

Expected hits in each layer and required time to readout the data					
		Hits in each layer		Time (μs) to readout data	
MODULE	LAYER	HITS R_ϕ	HITS Z	TIME R_ϕ	TIME Z
0 & 5	0	42	88	1.6	3.3
	1	41	58	1.6	2.2
	2	48	49	1.8	1.8
	3	51	47	1.9	1.8
	4	50	50	1.9	1.9
1 & 4	0	52	86	2.0	3.3
	1	50	60	1.9	2.3
	2	52	53	2.0	2.0
	3	55	48	2.1	1.8
	4	54	54	2.0	2.0
2 & 3	0	61	86	2.3	3.2
	1	56	59	2.1	2.2
	2	58	58	2.2	2.2
	3	60	50	2.3	1.9
	4	58	58	2.2	2.2

Table 5.17: Estimated hits by layer and side for triggered events. Also shown is the readout time for these events.

During Run Ia and Ib, changes in the beam position and beam angle were observed from store to store. The beam position even changed within the time period of a store, with time scales ranging from 10 minutes to hours. By using local bumps at the correction dipoles in the A4 and B1 sectors of the Tevatron, it is possible to correct for these changes in the beam position and angle at the B0 interaction region. However, a precise measurement of both the angle and position (in the horizontal and vertical planes) is required.

CDF will be able to make these measurements by using the information from the SVX II detector. During Run Ib, CDF used the information from the SVX′ detector to measure these 4 quantities and communicated them through the Accelerator Controls Network. The Accelerator Division Controls group implemented a program to use this information, along with desired positions and angles, to adjust the correction elements. Studies done during the Tevatron operation in January and February 1996 showed that the system works in principle. The AD/Controls group is creating a software based feedback algorithm for this interaction region beam steering.

Though we have demonstrated that the system will work in principle, there are additional questions that need to be answered before it works in practice. The most significant is possible limits in the range of motion. The correction dipoles used for the local bumps are also used in the establishment of a smooth closed orbit in the Tevatron, so it is possible that making local changes could disrupt the total Tevatron orbit. Consequently, we are continuing to work with the AD/Controls and AD/Main Accelerator groups on the design and implementation of a reliable and appropriate beam steering system.

Bibliography

[1] SVX II Upgrade Proposal and Simulation Study, CDF/DOC/SEC_VTX/CDFR/1922. Proposal submitted to the Fermilab Directorate on January 13, 1993 and approved in May, 1993.

[2] N. Tamura et al., NIM A342 (1994) 131.

[3] H. Ziock et al., NIM A342 (1994) 96.

[4] John A. J. Matthews, *et. al.,* Bulk Radiation Damage in Silicon Detectors and Implications for SVX II, November 1, 1995, CDF Note 3408.

[5] T. Ohsugi *et al.,* A Study of the Microdischarge Phenomenon at the Strip Edge of the Microstrip Sensors, I.E.E.E. Nucl. Sci. Sym., Norfolk, Virginia, November 1994, NIM A342 (1994) 22.

[6] T. Ohsugi et al., HUPD 9507, HUPD 9508, to be published in the proceedings of the 2nd International Symposium on Development and Application of Semiconductor Tracking Detectors at Hiroshima, Oct. 10 -13, 1995.

[7] D. Bortoletto, *et al.,* Evaluation of single metal SVX II prototypes manufactured by Micron Semiconductor, CDF/DOC/SEC_VTX/CDFR/3259.

[8] D. Bortoletto, *et al.,* Irradiated SVX II prototype probing results, CDF/DOC/SEC_VTX-/CDFR/3295.
A. Brandl, et al., Measurement of Proton-Induced Radiation Damage Effects in Double Sided Silicon Microstrip Detectors, CDF/DOC/SEC_VTX/PUBLIC/3512 (1996).

[9] D. Bortoletto, *et al.,* Capacitance measurement of double metal double sided silicon microstrip detector, Proc. Second International Symposium on Development and Application of Semiconductor Tracking Detectors, Hiroshima, 1995, to be published in Nucl. Inst. and Meth.

[10] A. Patton, *et al.,* Electrical Characterization of SINTEF/SI Prototype Double-sided Silicon Microstrip Detectors, CDF/DOC/SEC_VTX-/CDFR/2835.

[11] M. A. Frautschi, *et al.,* Capacitance Measurements of Double-sided Silicon Microstrip Detectors, FERMILAB-PUB-96/008-E, submitted to Nucl. Instr. and Meth.

[12] S. C. Seidel, *et al.,* Studies of Double-sided Silicon Microstrip Detectors, Proc. Second International Symposium on the Development and Application of Semiconductor Tracking Detectors, Hiroshima, 1995, FERMILAB-CONF-96/049-E, to be published in Nucl. Instr. and Meth.

[13] K. Hoffman, *et al.*, Laser Studies of Charge Collection Efficiency in SVX II Prototype Sensors, CDF/DOC/SEC_VTX/PUBLIC/3438.

[14] S. Kleinfelder,*et al.*, A flexible 128 channel silicon microstrip detector integrated circuit with sparse data readout, IEEE Trans. Nucl. Sci., Vol. 35, No.1, 171 (1988).

[15] R. Yarema, *et al.*, A Beginner's Guide to the SVX2, FERMILAB-TM-1892.

[16] N. Bacchetta, *et al.*, Resolution of Double-Sided Silicon Microstrip Sensors, CDF/DOC-/TRACKING/PUBLIC/3277.

[17] N. Bacchetta, *et al.*, Results of the KEK Beam Test of SVX II Prototype Detectors, CDF/DOC/TRACKING/PUBLIC/3547.

[18] D. Husson, IEEE Trans. Nucl. Sci. NS-36 (1994) 811.

[19] T. Huffman, private communication.

[20] M. A. Frautschi, Radiation Damage Issues for the SVX II Detector, January 27, 1994, CDF Note 2368.

[21] Alex Grillo, UCSC, private communication

[22] H-J. Ziock *et al.,* Tests of the Radiation Hardness of VLSI Integrated Circuits and Silicon Strip Detectors for the SSC Under n, p, and γ Irradiations, LANL Report LA-UR-90-4184 (1990).

[23] A.J. Weinstein, *et al.,* Silicon Tracking Conceptual Design Report, SCIPP 92/04 and SDC-91-133, March 1992.

[24] G. Bolla *et al.,* Double Metal SVX II Prototype Probing Results, CDF Note 3288 (1995).

[25] D. Bortoletto, private communication.

[26] S. Worm, private communication.

[27] P. Azzi *et al.,* Noise and Radiation Effects on SVX$'$ and other Silicon Sensors, CDF Note 3278 (1995).

[28] J. Matthews and T. Thomas, SVX II Signal to Noise Ratio, CDF Note 2397 (1994).

[29] E. Barberis *et al.,* Capacitance in Silicon Microstrip Detectors, Proceedings of the International Symposium on Development and Application of Semiconductor Tracking Detectors, May 22-24, 1993, Hiroshima, Japan, SCIPP 93/16 (1993); K. Yamamoto *et al.,* Interstrip Capacitance of the Double Sided Silicon Strip Detector, Proceedings of the SDC Collaboration Meeting at KEK, May 1991, SDC-91-33 (1991); R. Sonnenblick *et al.,* NIM **A310**, 189 (1991).

[30] RD20 Collaboration, A. Holmes-Siedle *et al.,* Radiation Tolerance of Single Sided Silicon Microstrips, CERN-PPE/93-137 (1993).

[31] Y. Unno *et al.,* Characterization of an Irradiated Double-sided Silicon Strip Detector with Fast Binary Readout Electronics in a Pion Beam, IEEE 1995 Nuclear Science Symposium, San Francisco, CA Oct 25, 1995, KEK Preprint 95-172 (1995).

[32] Nucl. Instrum. Meth. A349 (1994) 96-105.

[33] P. M. Ratzmann, Analysis of Ladder Support Fiber Options, December 2, 1993, CDF Note 2393.

[34] M. Albanese, M. Gold, M. R. Hoeferkamp, T. L. Thomas, S. Wells, Studies of a High Density Interconnect Cable for SVX II, CDF note 2785.

[35] P. M. Ratzmann, Ladder Thermal Analysis for CDF with SVX III Chips, June 5, 1995, CDF Note 3507.

[36] P. M. Ratzmann, SVX II Ladder Thermal Analysis, January 5, 1996, CDF Note 3508.

[37] Kohriki, *et. al.,* First Observation of Thermal Runaway in the Radiation Damaged Silicon Detector, submitted to the IEEE Trans. on Nucl. Sci., IEEE Nuclear Symposium, San Francisco, October, 1995 and KEK Preprint 95-157, November, 1995.

[38] P. M. Ratzmann, Thermal Analysis of the CDF SVX II Silicon Vertex Detector, FERMILAB-Pub-96/031-E, submitted for publication to Nuclear Instruments and Methods March, 1996.

[39] J. A. Hanlon, and H. J. Ziock, Design Equations for Silicon Detector Ladders with Heat Generated by Damage Induced Leakage Current LA-UR-95-893.

[40] The current SVX3 specifications are contained in "Device Specifications for the SVX3 Chip Set", Raimund Strohmer and Walter Knopf, http://www-ese.fnal.gov/eseproj/svx/svx3/svx3spec.htm.

[41] Hypertext references on the FIB and FIB Fanout can be found at: http://www-ese.fnal.gov/eseproj/svx/default.htm

[42] Hsaio Ying Chao and Jaroslav Antos, Occupancy Study for the SVX II, CDF note 2386, Nove. 21, 1994.

[43] R. Culbertson and G. Punzi, Occupancy in SVX II, December 14, 1995.