Design of an IEEE-1588 Interface for Sub-nanosecond Performance

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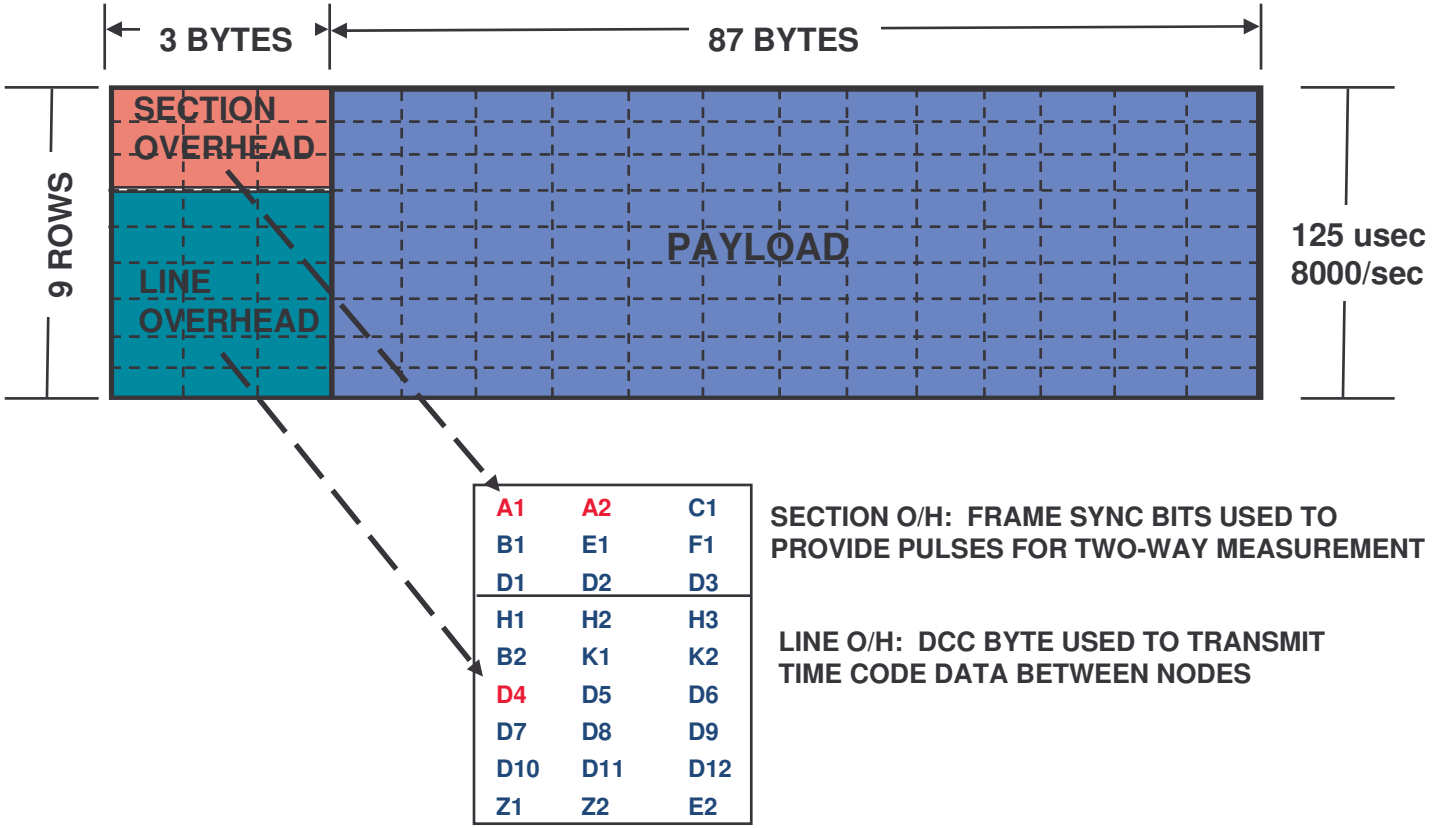
Background

- TSC has specialized in 2-way timing at high levels of precision
  - SONET OC-3 in 1998
    - » 20 ps stability
  - 155.52 MHz bi-phase on an optical carrier
    - » 0.5 ps stability
  - Via satellite for ground-to-ground and ground-to-air applications
    - » 500 ps stability
- Last year we decided to explore the possibility of achieving sub-nanosecond performance using IEEE-1588
  - Work funded by the US Air Force SBIR
    - » Reduce the weight of timing cables on collection aircraft
- TSC is experienced in precision timing but inexperienced with Ethernet

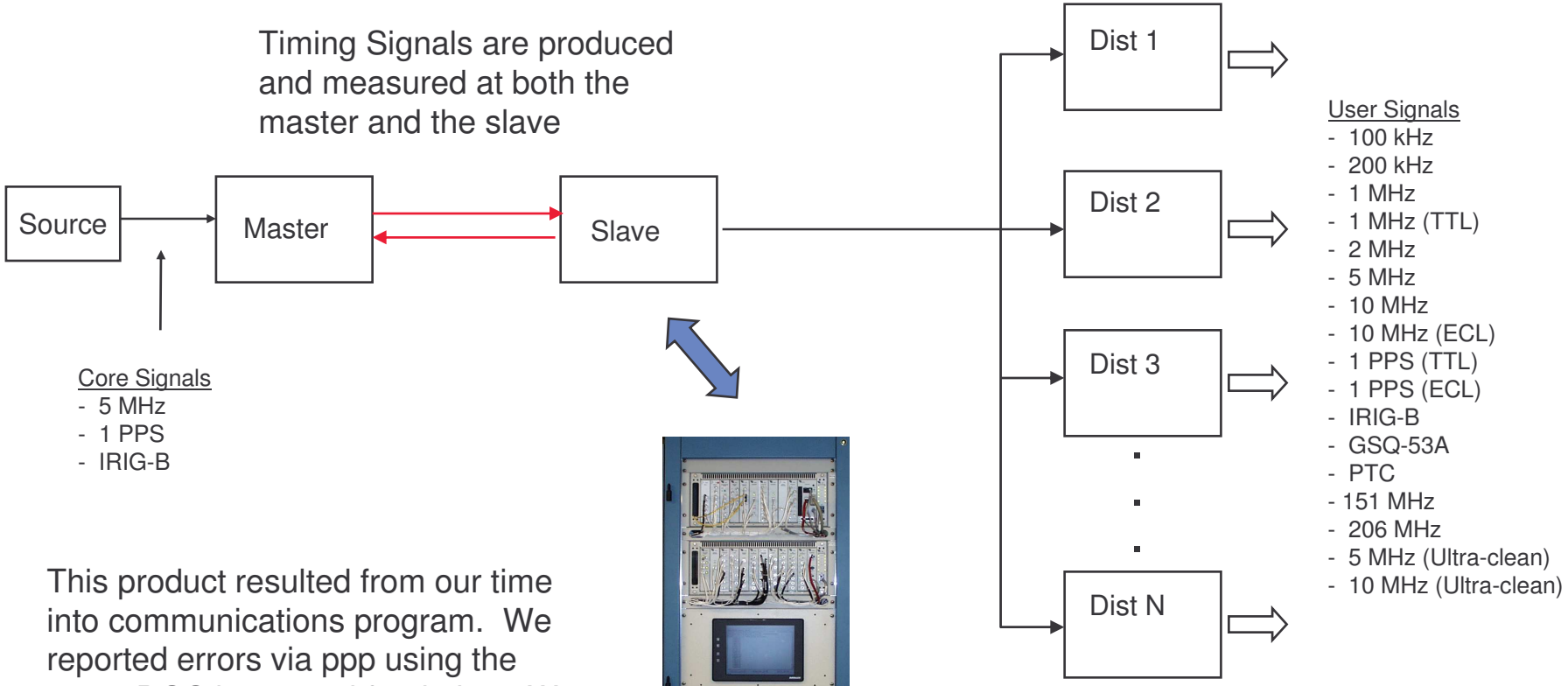
Sonet Time Transfer
STS-1 Frame Structure

- (U) SONET TRANSPORT OVERHEAD CONSISTS OF LINE AND SECTION OVERHEAD WHICH CAN BE EXPLOITED FOR TWO-WAY CALCULATION



2-Way Timing over SONET (1996)

Timing Signals are produced and measured at both the master and the slave

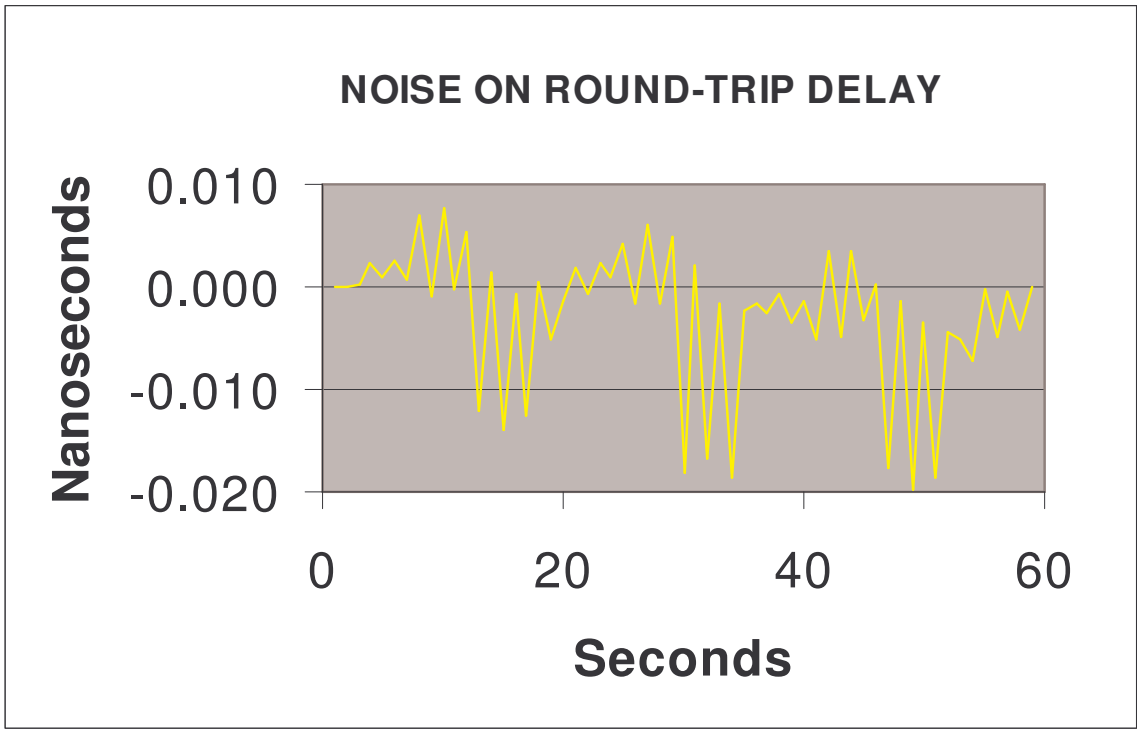


This product resulted from our time into communications program. We reported errors via ppp using the same DCC byte used for timing. We provided a full ATM interface. We built a transparent ATM clock. We weren't smart enough to think about using Ethernet.

Stability of 2nd Generation SONET Timing Sysem

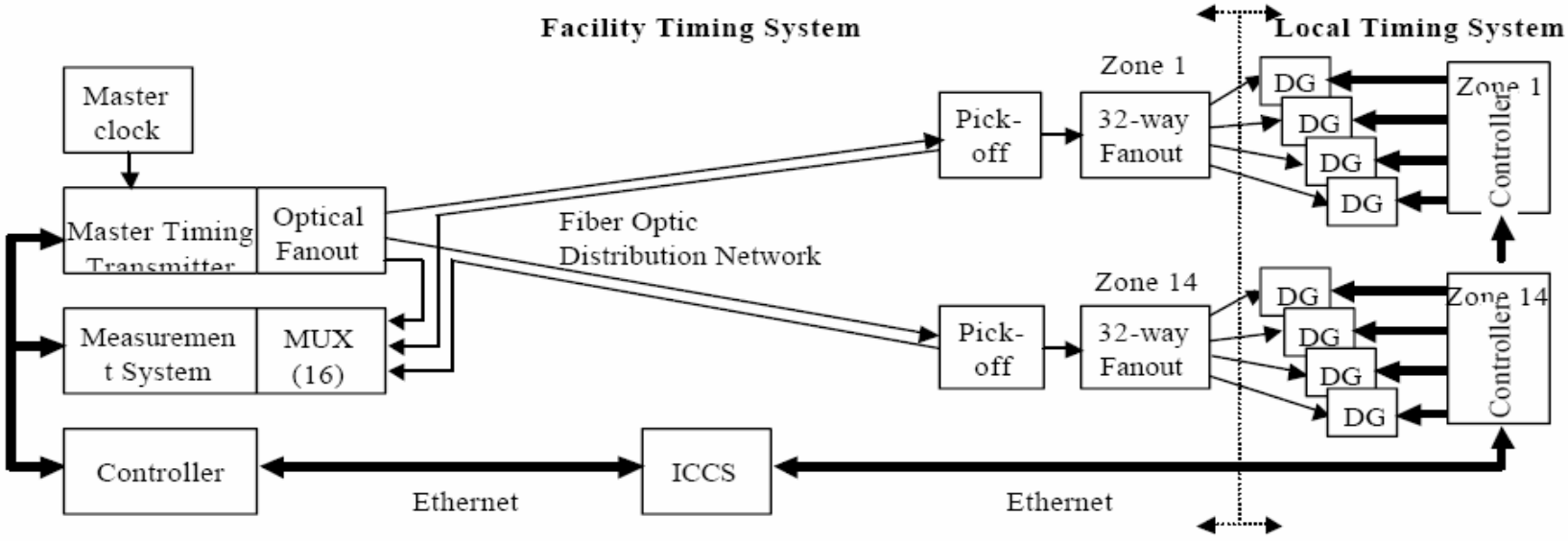
SONET Performance Limitation

Measurements made in loop-back mode indicate that the performance limitation in the SONET 2-Way time distribution is pattern noise from the SONET framing structure

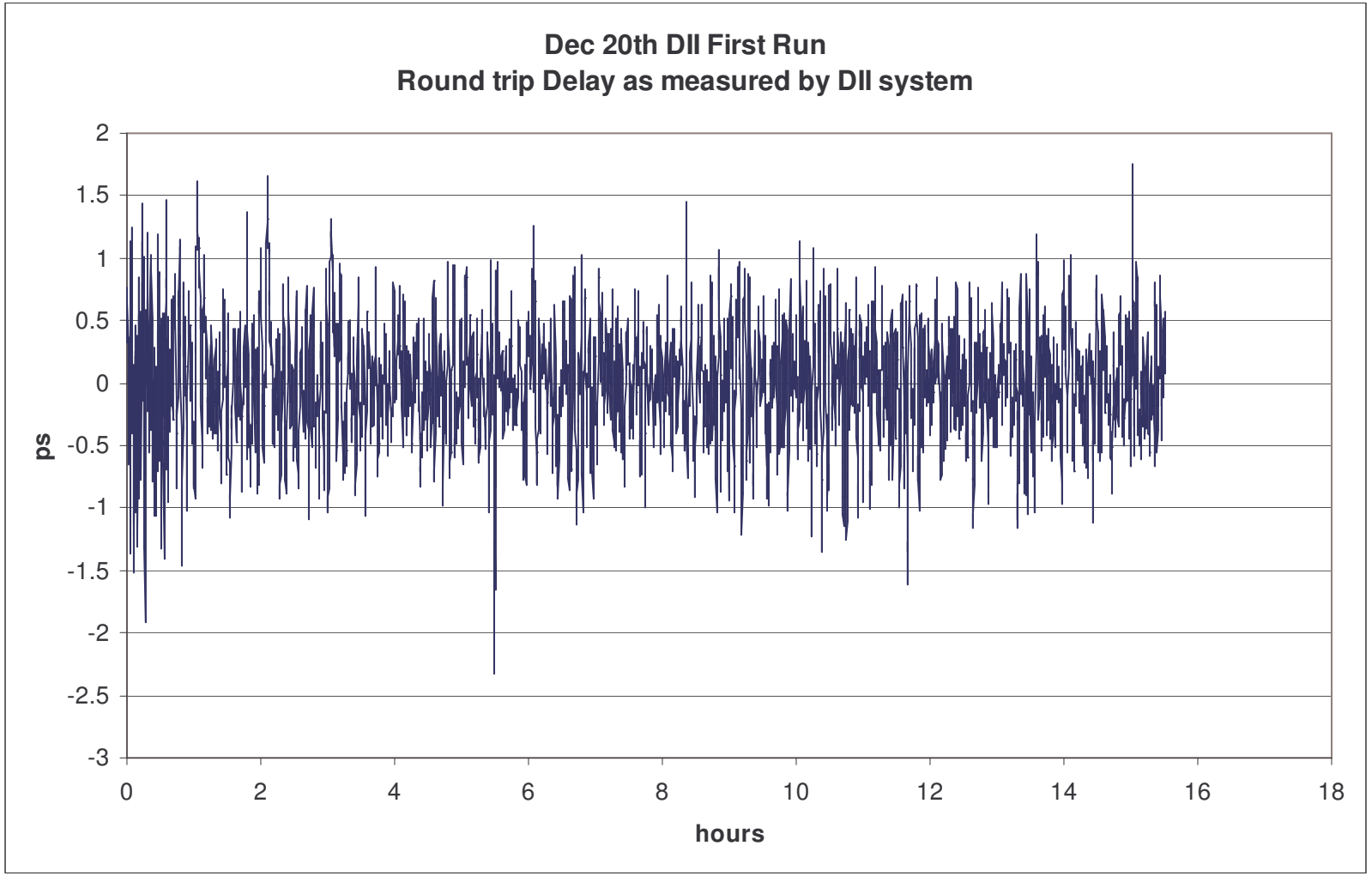


0.5 ps Timing System for the National Ignition Facility

- Timing signals are produced and measured only at the master resulting common mode rejection of many noise sources
- SFD occurs after a long series of constant bits (biphase)

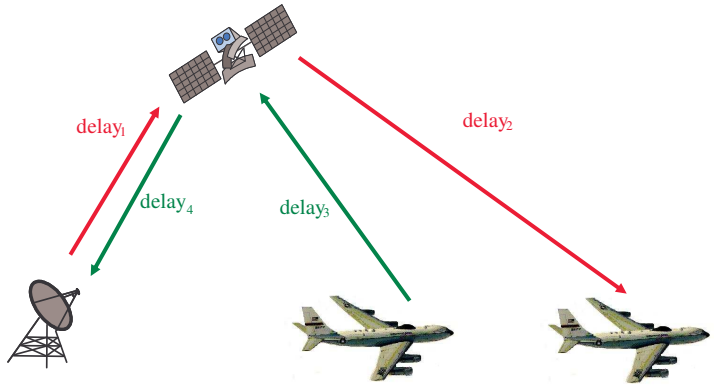


NIF Performance
50 X Better than SONET

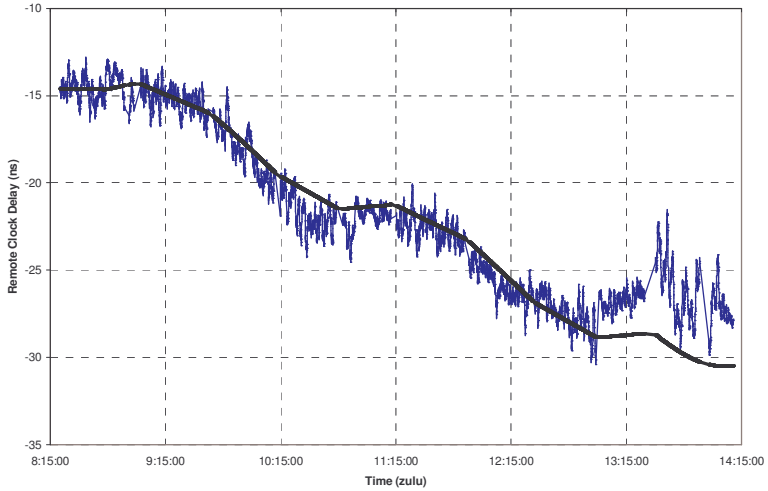


Satellite 2-Way Time Transfer

- Designed, developed, and demonstrated a 2-way modem with emphasis placed on timing performance. Airborne application requires accounting for
  - — Different send / receive path delays due to aircraft motion
  - — Relativistic effects
  - — Sagnac effect
- Performed ground and flight test demonstrations with new hardware operating in real-time



DTWTT Data

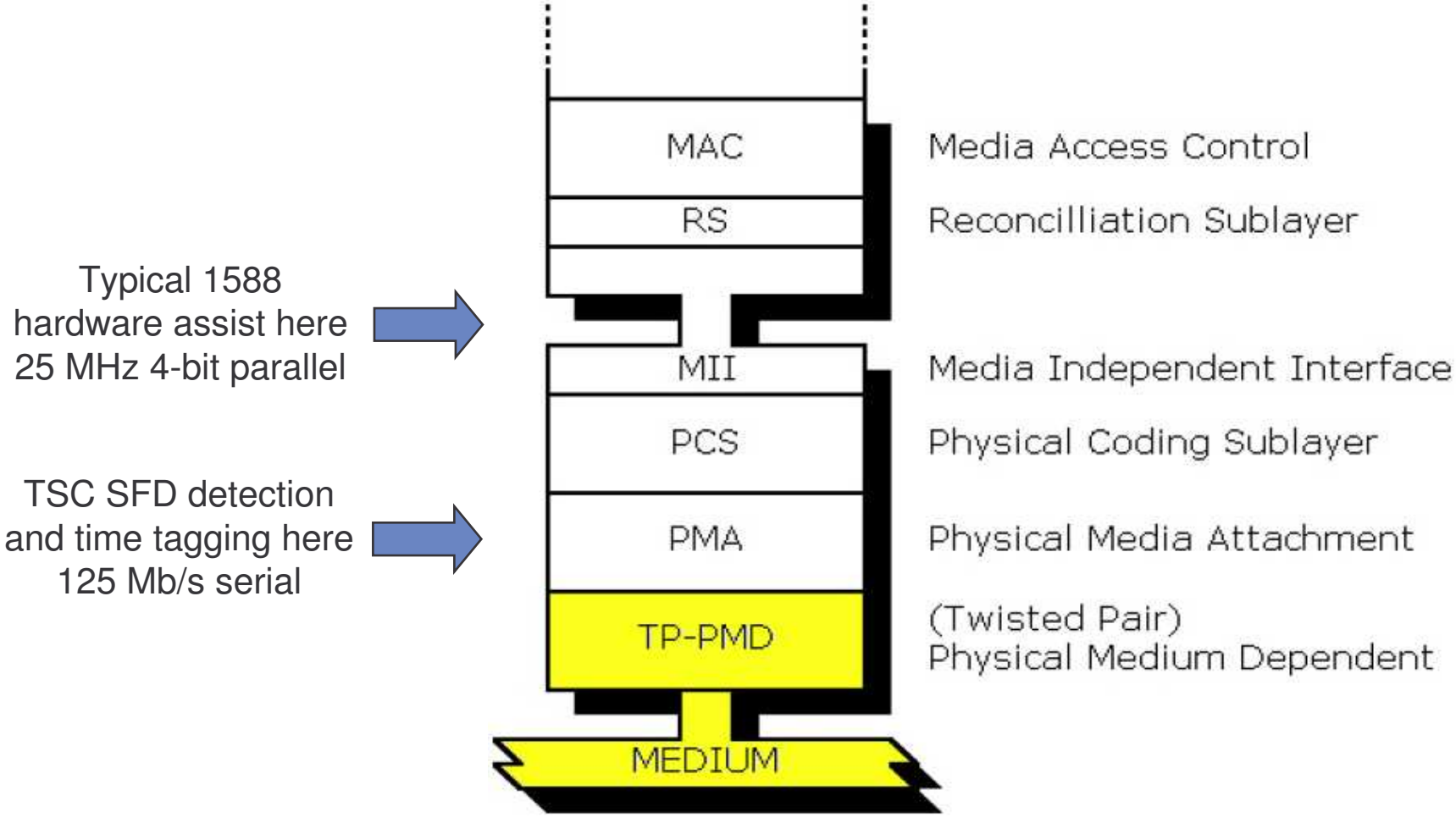


Desirable Properties *vs.* Ethernet Properties

Best 2-way timing Lessons Learned	100BASE-Tx Capabilities
• Zero or fixed FIFO delay	• 5 bits at 125 Mb/s = 40 ns inaccuracy
• Symmetric comms medium	• 10% cable asymmetry
• Identical Tx & Rx hardware	• Different Tx and Rx hardware
• All time processing at master	• Time processing at master and slave
• Continuous signal	• Signal gaps between idle and packet
• Clock embedded in signal	• Suppressed carrier
• Minimal patterns	• Framing and idle patterns
• Timing user has control	• IT admin and vendors have control

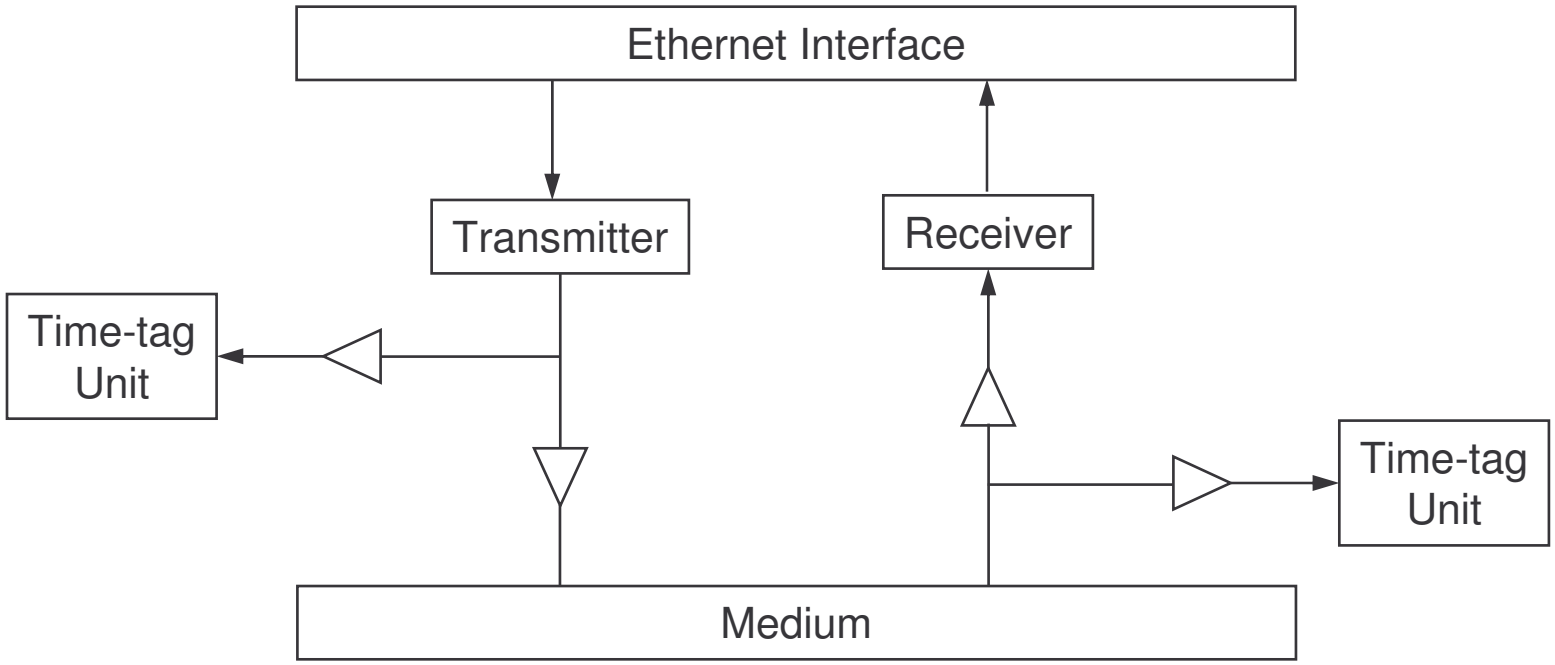
Our objective is to improve the two items in green.
The cable asymmetry can be removed using GiGE

Time Tag before the FIFO Used to Convert Serial Data to Parallel

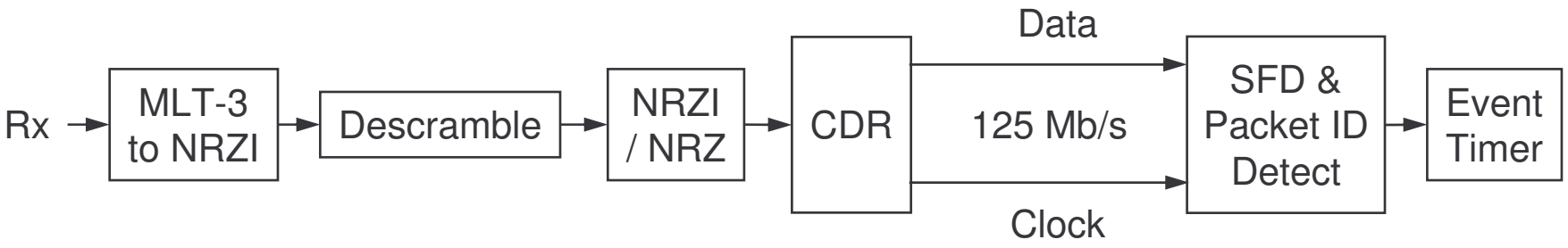


Symmetrical Tx / Rx Architecture

Our time-tag module uses independent clock and data recovery to support the SFD event timing



PMA Time-Tag Unit Design

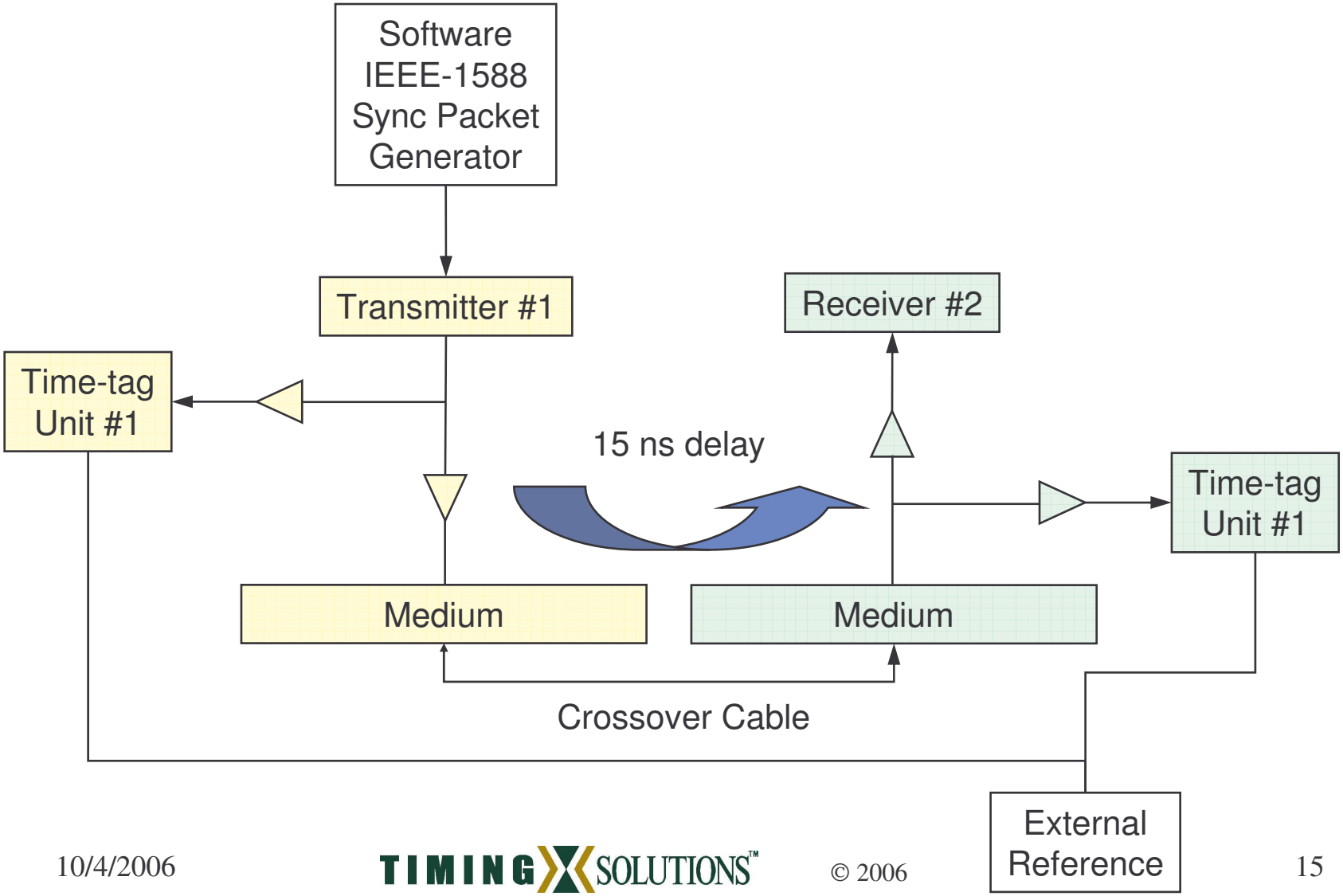


Execution Problems

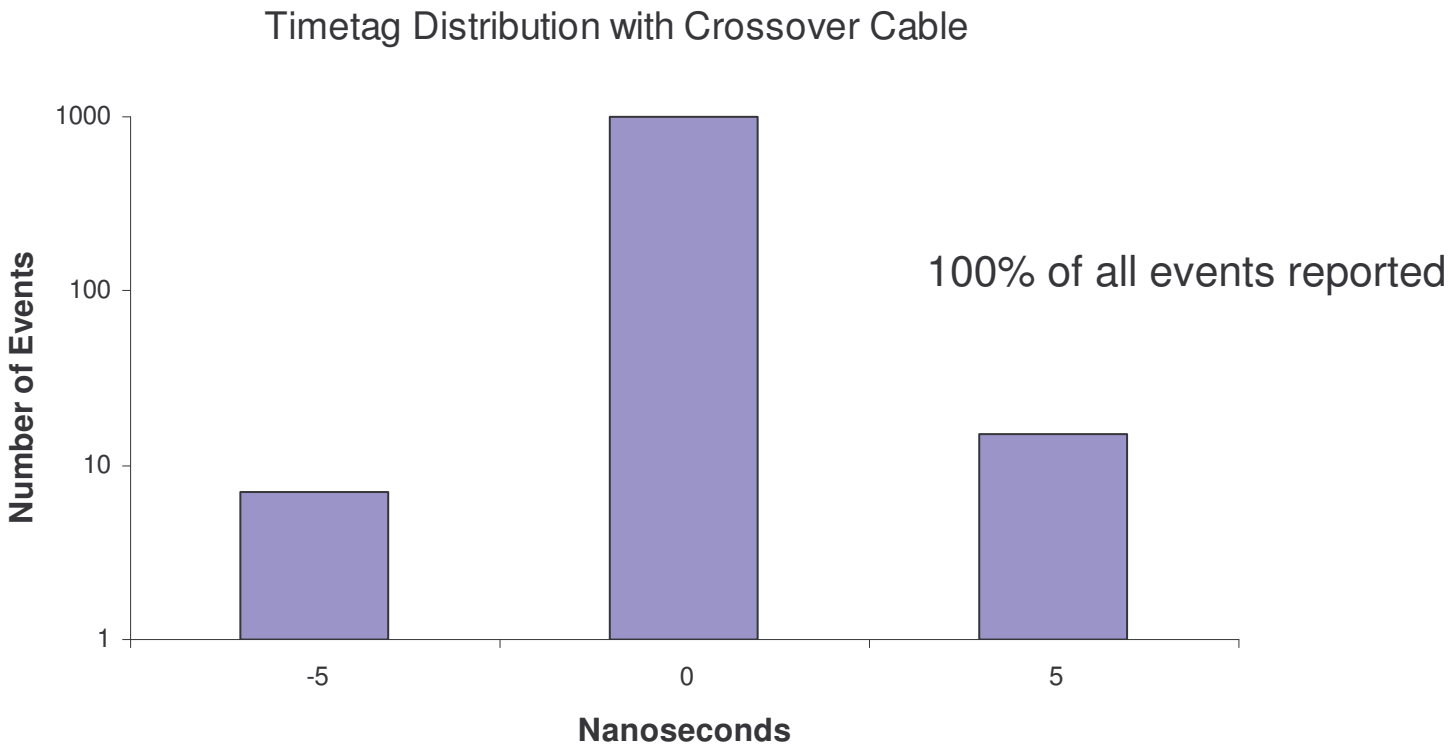
- Chips from 2 vendors did not successfully perform clock recovery on the 100BASE-Tx serial data stream
  - Vitesse
  - Micrel
- There are no longer any independent MLT-3 decoders in distribution
- We know timing but we started out without detailed knowledge of Ethernet
- Results have come slower than planned

That which doesn't kill you, makes you stronger

Experimental Set-up with Crossover Cable

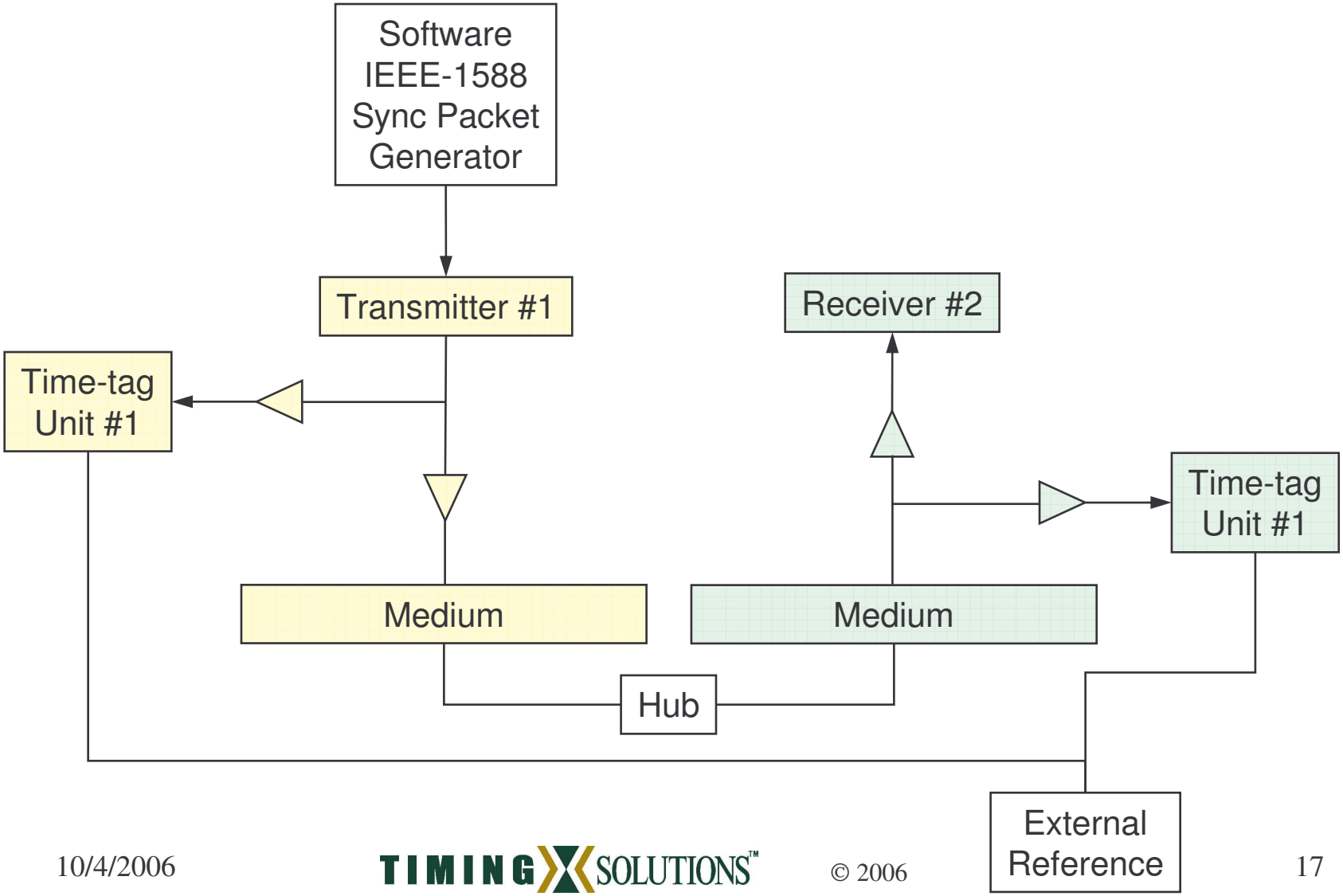


Point-to-Point Crossover Connection

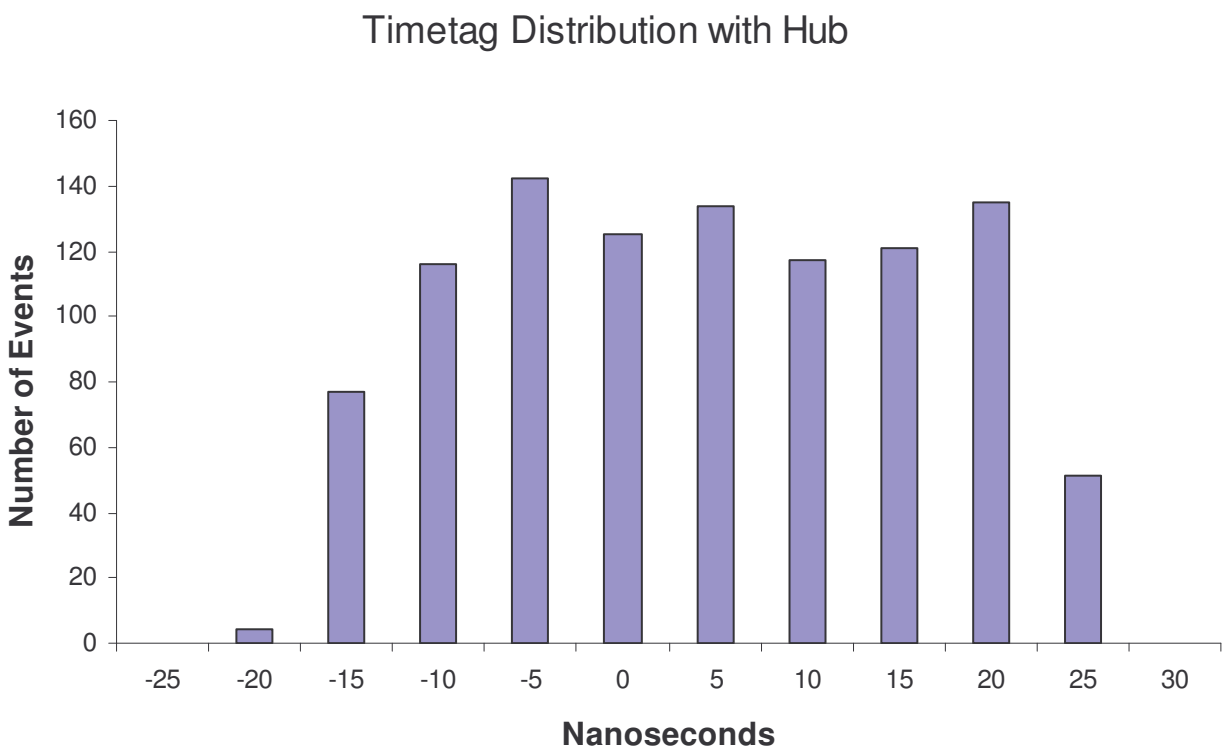


The number of events outside the ±2.5 ns central bin is consistent with σ = .9 ns

Experimental Set-up with Hub



Connection through Hub



Elimination of the 40 ns FIFO Origin Inaccuracy

- Crossover cable disconnected to allow CDR to dephase from the transmitted clock
- Crossover cable re-connected
  - 10 out of 10 recoveries resulted in 15 ns offset
  - 1 power-on reset resulted in the same 15 ns offset
  - Consistent with the design of the components selected for this demonstration

Concluding Remarks

- We plan to enable the on-board interpolators to improve the event timing accuracy to 100 ps
- We have ported ptpd to BSD Unix and will use it to implement an IEEE-1588 plug-in for our TFLEX mainframe
  - Master clock with GPS reference
  - Slave clock with TCXO or OCXO time base

Backup Slides

100BASE-Tx Idle Pattern