Facilities and Equipment

i. LBNL MicroSystems Laboratory

The majority of the CCD fabrication is carried out in the LBNL Microsystems Laboratory. This facility, which has been on-line since 1991, is operated by the LBNL Physics Division. The need for a silicon R&D fabrication facility in the U.S. high-energy physics community was due to the major role played by silicon radiation detectors in present day high-energy physics experiments. In conjunction with advanced integrated-circuit readout, silicon strip detectors are important parts of nearly all present and future planned high-energy physics detectors.

The high spatial resolution of segmented strip detectors, typically arranged in a barrel configuration with multiple layers, allows for accurate reconstruction of high energy physics events in collider machines. The ability to detect secondary vertices from B meson decay played a significant role in the discovery of the top quark at the Fermilab Tevatron, and the silicon vertex detector for the upcoming B-factory at the Stanford Linear Accelerator is absolutely essential to the goals of that experiment. In addition, silicon detectors will play a critical role at the future Large Hadron Collider, where both vertex detection and particle tracking will be performed by silicon detectors. LBNL has a major role in the silicon detector development effort at all the above mentioned experiments, and hence the decision was made in 1986 to pursue the development of a silicon detector fabrication facility.

Since the signal produced by high energy particles in silicon is small (80 electron/hole pairs per micron for minimum ionizing particles), a relatively large active thickness is necessary for silicon radiation detectors. In general the active thickess should be depleted of mobile carriers so that an electric field is produced in the entire bulk of the silicon. Significant field free regions should be avoided since thermal diffusion of the generated electron-hole pairs will result in degraded spatial resolution, making particle tracking more difficult. The electric field in a thickness X_d of silicon depleted of mobile carriers is equal to q N_d X_d/e_{si} where q is the electronic charge, N_d is the concentration of dopants (assumed n type) per cm^3, and e_{si} is the permittivity of silicon. In order to have an electric field throughout the entire thickness of silicon (typically 300 μm) one requires that N_d be very small in order that the electric field produced be less than the field at which the silicon breaks down. A low value of N_d requires that the silicon be of high purity, much higher than what is typically used in the integrated circuits industry.

Standard Czochralski-grown silicon as used in the IC industry is limited to a resistivity of about 50 Ω-cm. Resistivities of $\sim$10 kΩ-cm are required for radiation detectors, and this silicon is produced by float-zone refining. In that method a portion of the silicon is melted locally by rf heaters placed around the ingot, and preferential segregation of impurities into the liquid phase along with repeated passing of the ingot through the heating zone results in highly purified silicon. High resistivity silicon of the quality needed for radiation detectors is produced by only a few vendors worldwide. Wacker Chemitronic in Germany, Topsil in Denmark, and Komatsu in Japan are the major suppliers.

The LBNL Microsystems Laboratory was designed with the requirements of processing high resistivity silicon in mind. One of the major concerns with the processing of such high resistivity material is maintaining the purity of the silicon during processing. A resistivity of 10,000 Ω-cm corresponds to a purity level of about 1 part in 10^{11}, and this purity level must be maintained during the high temperature processing steps typically used in silicon device manufacturing (900-1000°C).

In addition, dark current is another major concern. Thermal generation of electron-hole pairs via energy levels near the middle of the silicon bandgap is the major source of dark current in silicon depletion regions. Since the entire volume of a silicon radiation detector is depleted, dark current minimization is a key issue. Metal contaminants such as gold give rise to mid-gap energy levels in silicon, and concentrations corresponding to a small fraction of a monolayer will lead to unacceptably high dark currents.

Given this background, care was taken in the design of the LBNL Microsystems Laboratory to ensure that high quality radiation detectors with low dark current could be reliably fabricated. For all critical items, state of the art techniques as used in the IC industry were employed to realize a high quality fabrication facility.

For example, the high purity water system design was overseen by the head of Balaz's Laboratory, which is a leader in the monitoring and troubleshooting of high purity water systems in the Silicon Valley. They are also at the forefront of the development and use of advanced analytical techniques used for the determination of contaminant levels in both high purity water and process chemicals used in the IC industry.

The high purity water system of the LBNL Microsystems Laboratory reliably produces water with 18 MΩ-cm resistivity, about the theoretical resistivity for pure water at room temperature. The water quality is also periodically monitored by Balaz's Laboratories.

The water distribution system is also designed with high purity in mind. The piping is realized with PVDF plastic, which is commonly used in state of the art IC facilities due to its low leachability and smooth inner surfaces which minimize the formation of stagnant layers that can lead to bacteria growth. In addition, the wet process stations used for chemical cleaning, etching, and water rinsing of wafers have built in timers that periodically cycle the water handling components, so as not to allow bacteria growth in stagnant lines.

High purity gases are used extensively in the Microsystems Laboratory. Gas purity is maintained at a high level by the manufacturer, and gases are distributed via high quality, chemically polished stainless steel gas lines as used in the IC industry. Particle filters are also used, and are typically located at the process tool requiring the high purity gas. On-site liquid sources are used for nitrogen and oxygen production.

ii. Clean Room

The clean room itself features 88% hepa filter ceiling coverage, resulting in a nominal Class 10 rating (less than 10 particles larger than 0.3 μm per cubic foot of air). A total of 700 ft^2 of clean room space is available, layed out in 4 clean rooms separated by bays where the bulk of equipment maintenance is performed. The majority of process equipment in the Microsystems Laboratory is designed for this kind of layout. Temperature is controlled to typically ± 1 °F, and humidity is controlled to $\pm 2\%$.

iii. Lithography

As far as process technology is concerned, the fabrication equipment was chosen to allow for the development of processes as complicated as a full CMOS process. Since most other IC technologies are subsets of the CMOS process, it was felt that CMOS capability would be a useful goal. The equipment can be divided into the following areas: thermal processing, wet chemical cleaning and etching, photolithography, thin film deposition, dry etching, and characterization.

In terms of thermal processing, we purchased a custom furnace system from SVG/Thermco, the largest U.S. supplier of furnaces for the IC industry. Capabilities include dry oxidation, steam oxidation using hydrogen and oxygen, n-type doping using $POCl_3$, and low and high temperature annealing in both nitrogen and 4% H_2 in N_2 ambients. Most doping steps are done via ion implantation, and this is accomplished at a commercial ion implant vendor located in Santa Clara, CA.

All the previously mentioned furnace tubes operate at atmospheric pressure. In addition we have low pressure chemical vapor deposition (LPCVD) capabilities. The LPCVD films that can be deposited in the Microsystems Laboratory are silicon nitride, undoped and phosphorus in-situ doped polycrystalline silicon, and undoped, phosphorus doped and boron/phosphorus doped silicon dioxide. As well as these standard CMOS thin films we have N_2O capability. That allows for deposition of oxygen doped polycrystalline silicon, which is a semi-insulating film used for power device passivation, and for the deposition of so-called high temperature silicon dioxide, which is deposited in the silicon nitride furnace. The thickness uniformities typically achieved across a 50 wafer load range from 1-2% for thermally grown oxides and deposited nitrides to 5-10% for deposited silicon dioxide and polycrystalline silicon.

The photolithography capability includes two lithography tools. Our original tool is a GCA step and repeat system utilizing the Hg g-line for exposure (436 nm). This tool features 1um linewidth capability and can be upgraded to Hg i-line (365 nm) if finer resolution is required in the future. Extremely accurate stage placement for the step and repeat function is provided by a laser interferometrically controlled fine positioning stage. Placement accuracy is rated at ± 0.1 μm. A 5X reduction lens is used, and the maximum exposure area at the wafer level is a circle of 2 cm diameter. Layer to layer registration is specified at ± 0.35 μm.

The main limitation of the GCA tool for our purposes is the small exposure area, which limits the size of the CCD we can fabricate. Although we have developed a "stitching" technique for the realization of large area strip detectors, we have augmented our lithography capabilities with a SVG/Perkin Elmer 641 projection aligner. This instrument uses 1X reflective optics, which allows for exposure areas of up to a full 6" diameter wafer. At present the machine is configured for the 4" diameter wafers presently used in the Microsystems Laboratory. The resolution that can be achieved is slightly less than the GCA (1.5 μm as opposed to 1 μm), but with the use of the automatic fine alignment system the registration is comparable or better than the GCA. This machine was recently donated by Intel, and has been installed and is operating to original equipment manufacturer specifications. It should be noted that there is a trend in the commercial CCD industry to use stitching technques to develop large area CCDs with wafer steppers, (e.g., Phillips and EEV), but given the complexity of mask design and image reversal processing we have opted to develop our large area CCDs on a projection aligner. The ability to put several different CCD designs on the same wafer is very useful in terms of development, and the projection aligner is more flexible in that regard.

The Microsystems Laboratory contains 5 wet process stations. Two of the stations are dedicated to cleaning wafers before thermal processing in the SVG/Thermco furnaces. An industry standard clean is performed, and includes so-called megasonic cleans in which the wafers are placed in either a HCl or NH_4OH mixture with hydrogen peroxide and high purity water. A transducer located at the bottom of the containment vessel generates 1 MHz waves, which reduce the thickness of the stagnant layer of fluid which is recirculating past the wafer surfaces. This technique enhances particle removal and is industry standard. The remaining 3 wet process stations are used for wet chemical etching of various thin films, and for photoresist development. The majority of chemical process baths recirculate the process fluid through particle filters, and are temperature controlled.

Deposition of metals and other thin films is done by sputtering in the MRC 603 system. This machine has the capability of depositing both conducting and insulating thin films, and can add process gases such as nitrogen and oxygen for reactive sputtering. Three cathode targets are included, including an RF target for the sputtering of insulators. At present the targets include a standard Al-Si alloy for metallization, a Ti-W alloy for refractive metal applications, silicon dioxide and indium tin oxide which are used as the back side contact and anti-reflection coating in our CCD process. The MRC 603 also has sputter etch capability.

Characterization equipment includes film thickness measurement via spectrophotometry, ellipsometry, and movable stylus contact for non transparent films. Sheet resistance is monitored with a 4-point probe. A high quality microscope with up to 2000X magnification capability is used for detailed wafer inspection. This system also includes a CCD camera with associated computer hardware for documentation purposes.

iv. UC-Berkeley facilities

A limitation to wet chemical etching is the relatively poor linewidth control due to the isotropic nature of the process. Several etch steps in the CCD process require tight linewidth control, and as a result these etch steps are performed at the UC-Berkeley Microfabrication Laboratory. Lam Research Corporation plasma etchers available at UCB are used for etching nitride and polycrystalline silicon.

The UC-Berkeley Microfabrication Laboratory consists of approximately 10,000 square feet, of which half is maintained under Class-100 clean room conditions. The VLSI area, which includes the Lam Research plasma etchers, contains full 4 inch diameter CMOS processing capability. The laboratory is used primarily by UCB faculty and graduate students in electrical engineering, with other users from materials science, physics, mechanical and chemical engineering, UCB/LBNL and others. The laboratory receives support from NSF, SEMATECH, SRC, DARPA and other funding agencies. The Berkeley Sensor and Actuator Center (BSAC), an NSF/industry/university cooperative research center, is the single largest group utilizing the Microfabrication Laboratory. An associated machine shop derives much of its work from the Microfabrication Laboratory. More information is avaiable at http://argon.eecs.berkeley.edu:8080/.

In addition, the UCB Physics department maintains a high quality machine shop that includes computer controlled lathes, milling machines, and a 3.5 axis CNC machining center for precision machining. It is anticipated that tooling for CCD packaging will be developed at the UCB Physics Department machine shop.

v. Safety

In addition to the process equipment mentioned above, numerous personnel safety systems are in use. These include continuous monitoring for both hydrogen and toxic gases used in the furnace systems. The safety systems are linked to the LBNL Fire Department, and the facility is compliant with the Uniform Fire Code Article 80. The facility also operates under an air quality permit issued by the Bay Area Air Quality Management District, and all acid waste generated by the Laboratory is processed by an State of California permitted acid treatment system located at LBNL.