Lecroy 2367 ULM Features if Configured for AGS CNI Polarimeter

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1 Files

The design is located: `rikpc14.rhic.bnl.gov//c:/projects/time3267/`. The files are:

- `time3276.opj, time3276.dsn` – OrCad project
- `xproj/time3276.xpj` – Xilinx Aliance project
- `Time3276.bit` – resulting file for Xilnx programming

To program Lc2367, ftp `time3276.bit` to `cnipol.ags.bnl.gov:/home/igor/ags2003/lrs2367/`, cd to this directory, then issue command:
`./prog2367 N Time3276.bit X`

2 Suggested Timing

The timing diagram is shown in fig. 1. The sequence can be described as follows:

External T0 coming from AGS starts the whole sequence. At this event the millisecond counter starts, and NotReady flipflop is set. Next T0 will only be accepted if the software resets the NotReady ff (F16A15) before that.

Ramp Begin event happens when the millisecond counter reaches the value, preprogrammed with F16A2, and is not supposed to happen before the AGS RF and BunchZero signal become stable and the RF frequency exceeds 4 MHz. On this event the clock (RF) output is switched from internal 4 MHz to external AGS RF, BZ starts going through and the GCC prescaler starts counting according to the value preprogrammed with F16A1. Also the values of Spill+ and Spill− signals is latched at this moment.

Inhibit Remove event occurs when either the *ms* counter or the number of prescaled GCC equals the value F16A3, dependent on CSR0 setting (0/1). On this event WFD start taking data.

LAM1–LAM4 events are intended to cause some additional reprogramming of the WFD during the ramp or on the flattop, for example when the phase transition in AGS happens. The corresponding LAM trigger is set and CAMAC LAM line is activated when the *ms* counter reaches the value F16A8–A11. After serving the interrupt, the software must remove the corresponding LAM source through F16A14 (RS-LAM). Also the inhibit is set for the whole period of the interrupt serving.

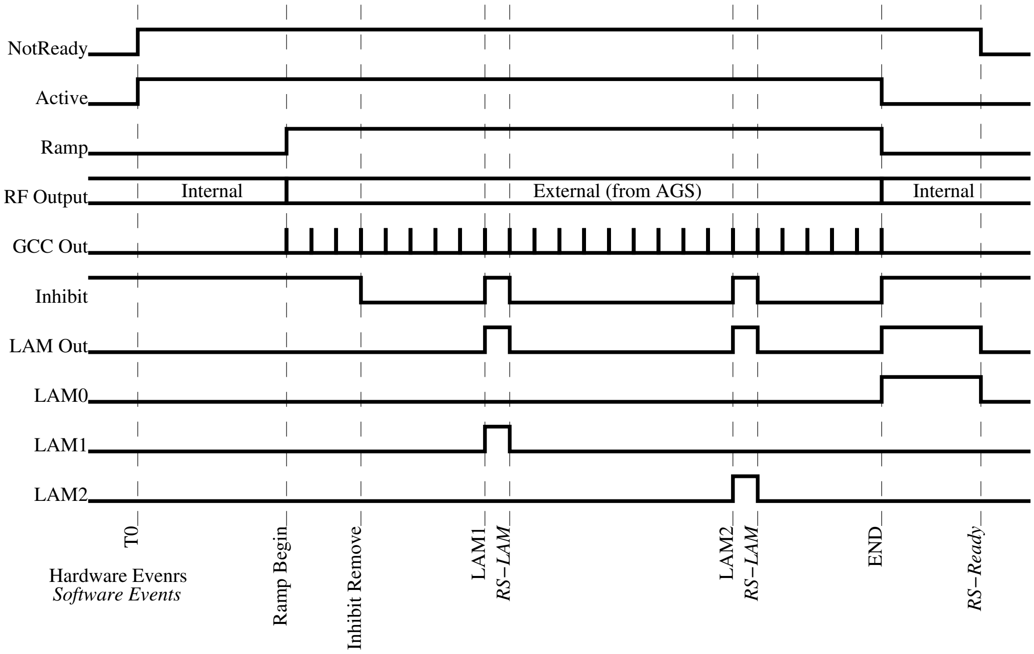

Figure 1: Suggested timing.

End event can also be programmed in terms of *ms* or prescaled GCC (F16A4), dependent on CSR1 bit. On this event the clock output is switched to the internal, BZ and GCC stop going out, inhibit is set designating the end of data taking, LAM0 is set to notify the software of the end of the cycle to start data readout.

RS-Ready When the software finishes reading data and the system is ready to accept new data, RS-Ready (F16A15) must be issued to make the module accept next T0 signal.

3 Additional features

- BunchZero can be delayed in terms of RF periods by setting F16A5 (0–15).
- The module detects the presence of the RF frequency between Ramp Begin and End events. Frequency Lost condition occures in case of RF absence, causing switching to internal clocks and ignoring subsequent T0s. This condition must be rest by the software through F16A13.
- Setting CSR4 bit will ignore NotReady and Frequency Lost condition and make the system cycle without the interference of the software.

4 Camac Functions and Registers.

Note: All time values are relative to T0. All numeric values (events, GCC prescaler, BZ delay) are actually '+1', which means writing 0 effectively means the value 1.

<table>
<tr>
<td>F0A0/F16A0</td>
<td>R/W Command and Status Register CSR[23:0].
Note: All other registers are 16 bit.
<table>
<tr><td>CSR0</td><td>R/W</td><td>Inhibit Remove Event unit: 0 – ms, 1 – prescaled GCC</td></tr>
<tr><td>CSR1</td><td>R/W</td><td>End Event unit: 0 – ms, 1 – prescaled GCC</td></tr>
<tr><td>CSR2</td><td>R/W</td><td>Enable final inhibit on the output</td></tr>
<tr><td>CSR3</td><td>R/W</td><td>Enable final LAM on the output</td></tr>
<tr><td>CSR4</td><td>R/W</td><td>Cycle Whatever, ignore software Ready and Frequency Lost conditions</td></tr>
<tr><td>CSR[7:5]</td><td>R/W</td><td>Reserved</td></tr>
<tr><td>CSR8</td><td>R</td><td>Cycle Active, reads 1 from T0 till the End Event</td></tr>
<tr><td>CSR9</td><td>R</td><td>NotReady, set at T0, must be reset by the software (F16A15) to indicate Ready for the next T0; if not, T0 is ignored and nothing is done</td></tr>
<tr><td>CSR10</td><td>R</td><td>Data Taking, reads 1 from Inhibit Remove Event till End Event</td></tr>
<tr><td>CSR11</td><td>R</td><td>LAM0 Active, if CSR3=1 LAM is present on the CAMAC bus. Gets set always on the End Event, must be reset by the software with RS-LAM (F16A14), also is reset together with Ready (F16A15)</td></tr>
<tr><td>CSR12</td><td>R</td><td>Frequency Lost, reads 1 if lost of external frequency was detected during the period when it must go to the output (from Ramp Begin till End). If set, blocks the T0 recognition. Must be reset by the software (F16A13)</td></tr>
<tr><td>CSR13</td><td>R</td><td>Reserved, always reds 0</td></tr>
<tr><td>CSR14</td><td>R</td><td>Spill− value, latched on Ramp Begin Event</td></tr>
<tr><td>CSR15</td><td>R</td><td>Same for Spill+</td></tr>
<tr><td>CSR[19:16]</td><td>R/W</td><td>If set to 1, enables corresponding LAM[4:1] Event. LAMx is ORed with LAM0 to form the final LAM output, which can be disabled with CSR3=0. While any of LAMx is set, final inhibit will also be present if not disabled with CSR2=0. Needs RS-LAM (F16A14) to be reset</td></tr>
<tr><td>CSR[23:20]</td><td>R</td><td>Current status for LAM[4:1]</td></tr>
</table>
</td>
</tr>
</table>

F0A1/F16A1	R/W GCC prescaler value.
F0A2/F16A2	R/W Ramp Begin Event, always in *ms*. On this event: • the RF frequency output is switched to the AGS clocks; • gcc prescaler starts counting; • the values of the Spill+ and Spill- signals are latched. **Note:** Make this event later than End Event in order to stay at crystal 4 MHz clocks and to avoid GCC output.
F0A3/F16A3	R/W Inhibit Remove Event. The value is either in *ms* (if CSR0=0) or in prescaled GCC counts (CSR0=1). On this event the inhibit is removed so that WFD start taking data.
F0A4/F16A4	R/W End Event. The value is either in *ms* (if CSR1=0) or in prescaled GCC counts (CSR1=1). On this event: • the RF frequency output is switched to the internal crystal oscillator 4 MHz clocks; • gcc prescaler stops counting; • inhibit is set, data taking stops; • LAM0 flipflop is set;
F0A5/F16A5	R/W Bunch Zero Delay ('coarse') in terms of current RF frequency periods. Only 4 bits are used in BZD[3:0], others always read 0.
F0A6	R General Purpose Input register, reads the state of ECL lines [16:9] on front panel connector B. Only 9th ECL line is connected to the input of 726 Level Translator (input 9), corresponding to bit 0 of this register.
F16A6	W General Purpose Output register, write to bits [3:0] will set ECL lines [8:5] on front panel connector A. ECL lines [7:5] are connected to the output of 726 Level Translator (outputs [16:14]), corresponding to the bits [2:0] of this register
F16A8	R/W LAM1 Event value, *ms*
F16A9	R/W LAM2 Event value, *ms*
F16A10	R/W LAM3 Event value, *ms*
F16A11	R/W LAM4 Event value, *ms*
F16A12	W Global Reset of all module registers to their initial state, which is in most cases 0.
F16A13	W Reset the Frequency Lost condition.
F16A14	W Reset LAM[4:0] according to the mask written in bits [4:0]. In case there is more than one LAM pending, this function will retrigger the state of CAMAC LAM line.
F16A15	W Reset NotReady condition. Also reset all LAMs.