Chapter 3

Pad Chambers

3.1 Chevron Pad Cathode

The primary functions of the pad chambers (PC) are to perform measurements of non-projective three dimensional spatial points to be used for both momentum determination and pattern recognition, and to provide information for the trigger. There are three pad chambers (PC1, PC2 and PC3) in each arm of the PHENIX detector system (Fig. ??). PC1 is placed immediately behind the DC and in front of the RICH. Both PC2 and PC3 are behind the RICH, on either side of the TEC tracking detector. The high resolution p_T measurements provided by the DC enable the PC to give good measurements of p_z/p_T. The three dimensional spatial points measured by the PC will allow track elements determined by the DC and TEC to be linked and projected back to the interaction vertex. Charged particle tracks pointing at RICH and EMCal will help to distinguish electrons from other particles. In addition, the PC are expected to provide track information at the second level trigger to match the electron signals of RICH or EMCal.

Several pad cathode schemes for charge interpolation are in use [1]. The PC for PHENIX have been designed using the pad cathode with a chevron geometry for charge interpolation. The advantages of such a design are good spatial resolution, large pad size to reduce channel counts, low mass and proven reliability [2, 3]. The chevron-geometry PC offer good position resolution capability and relatively large readout node separation to reduce cost. However, the feasibility of a pixel pad cathode option using much finer pixel pads with low cost readout electronics is being investigated as an alternative PC design for PHENIX. First the chevron geometry pads, and then the pixel pad cathode option are discussed below.

During the past few months, considerable attention was devoted to the question of chevron-pad versus pixel-pad cathode readout scheme for the pad chambers. After careful deliberation, the chevron interpolating-pad scheme was adopted. Although the pixel-pad scheme offers potential advantages in both occupancy and double-track resolution, further R&D work is required. The University of Lund group is encouraged to continue to develop the pixel-pad system as a possible future upgrade to the pad chambers. There are a number of significant new developments in the conceptual design of all the pad chambers (PC1, PC2, and PC3), both in mechanical structure and electronic readout scheme.

3.1.1 Mechanical Design

The physical layout of the pad chambers in one arm of the PHENIX detector system is shown in Fig. ??. The PC1 detector, which occupies a radial position of 245–250 cm from the beam axis, has eight planar sectors joined in a uni-structure without physical boundary between sectors. Both PC2 and PC3 are made in two planar sectors, each with a thickness of 6 cm. The inner walls of PC2 and PC3 have inscribed radii of 405 cm and 480 cm, respectively. The design of these chambers are driven by the following considerations:

- Good spatial resolution for momentum measurements and pattern recognition;
- Adequate two track separation for track reconstruction and cross section measurements;
- Low mass to minimize the secondary particle production and multiple scattering;
- Optimum hit occupancy versus channel count.

The multiwire gas chamber with interpolating pad cathode, or simply pad chamber, offers an effective scheme to achieve these objectives. The basic structure of a pad chamber consists of a wire plane with anode and field wires interspersed as illustrated in Fig. 3.1. Beneath the wire plane is a cathode plane divided into pad strips and ground strips lying underneath the anode wires and field wires, respectively. A second cathode plane is located at an equal distance above the wire plane. Charged particles traversing the detector produce ionization in the chamber gas. Electrons are accelerated toward the nearest anode wire and eventually produce an avalanche in its vicinity which images a charge on the cathode pads close to the avalanche.

Figure 3.1 shows the wire-cathode geometry for a chevron pad PC1. The wires run parallel to the z axis. The anode wire spacing is 4 mm, which fixes the resolution in r-ϕ direction to that value. The resolution in the z direction is about 1–2% of the chevron spacing (apex-to-apex) [1]. The chevron pad geometry is normally defined as follows: if the apex-apex spacing between two adjacent chevrons is L, the distance between the apex of a chevron to the tip of the wing of the preceding chevron is usually denoted by $f{\cdot}L$, where f is called the form factor and assumed to be 1. The tracking system will have good momentum measurement capability, if the resolution in z is 2 mm rms. This implies a chevron pad spacing of 22.1 cm for PC1. Because the width of the chamber along the z direction is 177.1 cm, this gives eight pads per cathode strip. Based on previous experience [2, 3], the desired resolution in z is achievable with a pad width of 3.05 mm and a ground strip width of 0.95 mm. This gives 972 anode wires and 973 field wires in PC1. The anode wires are 20-μm diameter gold plated tungsten and the field wires are 125 μm stainless steel.

As illustrated in Fig. 3.10, PC1 consists of eight planar sectors with each sector having a width of 43.4 cm and inclined at an angle 10° in ϕ relative to the adjacent sector. The pad cathode plane and the wire plane are always arranged so that a ground strip lies along the seam between two sectors with a field wire lying 4 mm above it. The shallowness of the angle of inclination between sectors minimizes the distortion in the electric field lines; thus

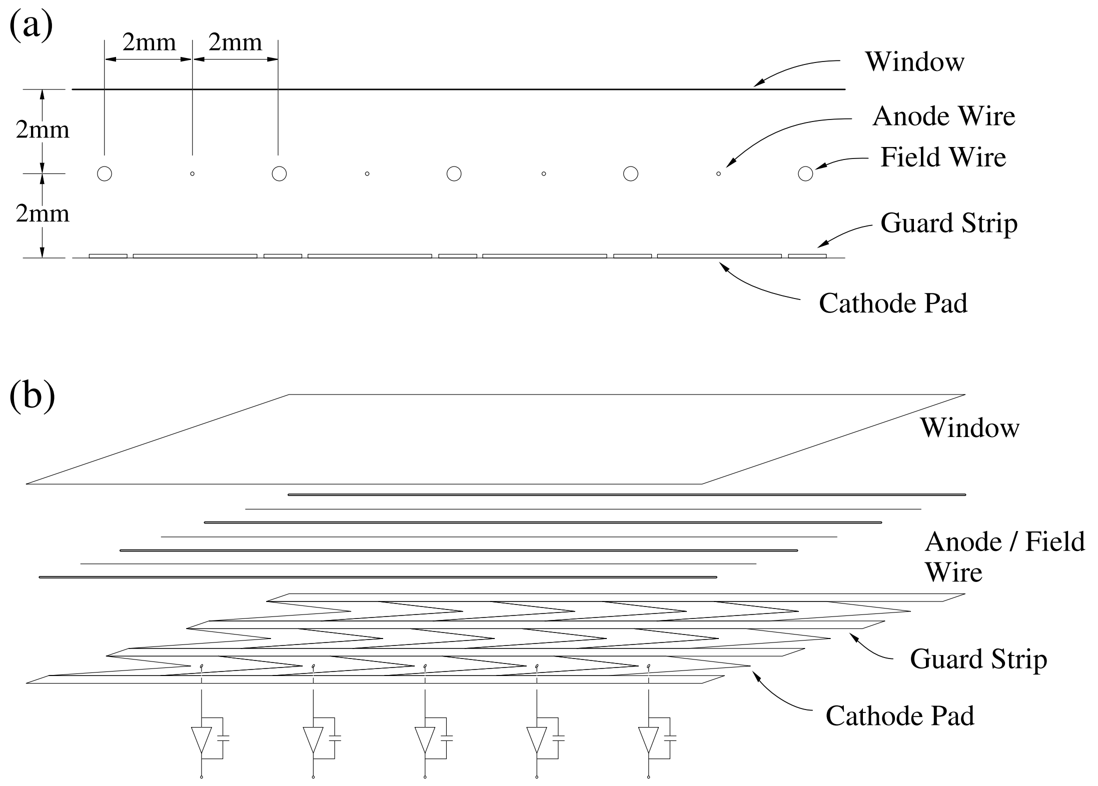


Figure 3.1: Wire-cathode geometry: a) sectional view along z direction showing wire cell structure, b) oblique top view show cathode-wire-pad planes. Dimensions are given for PC1.

a dead space is avoided. Figure 3.2 shows the sectional side view of PC1 in the rϕ plane. Figure 3.3 displays a view of PC1 in the z-plane.

The pad cathode plane is 0.5 mm fiberglass with chevron pads etched on one side and readout printed circuit on the other. The two sides are connected by plated through holes. The cathode board is backed by a honeycomb (approximately 4-mm thick) and a thin (about 250 μm) fiberglass skin. The aluminized mylar cathode above the wire plane is 25-μm thick supported by 2–3 mm honeycomb and a mylar skin (probably 150 μm fiberglass). The wire planes are mounted on a G-10 frame. The dimensions of these frames will be determined upon the completion of the structural analysis and modeling. The holes on the sidewall of the chamber frame are electrical feed through connectors and gas manifold. The gas is 50–50 argon-ethane mixture at atmospheric pressure, and its containment is provided by a 25 μm mylar jacket (not shown).

Four planar sectors, each covering 22.5° in ϕ, comprise PC2 and PC3. There detailed design can be seen in figures **??**, **??**, **??**, **??**.

For PC2 the dimensions of each sector are 162.7 cm in the ϕ direction and 295.0 cm in the z direction, and for PC3 198.3 cm and 348.0 cm, respectively. The design of these chambers is similar to that of PC1; each sector of PC2 and PC3 is scaled up accordingly from

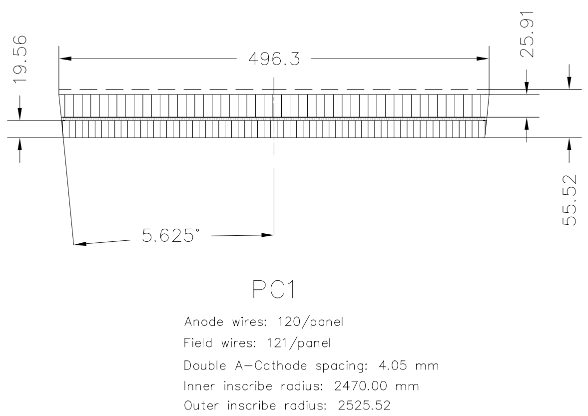


Figure 3.2: Pad chamber 1 cross section in rϕ plane

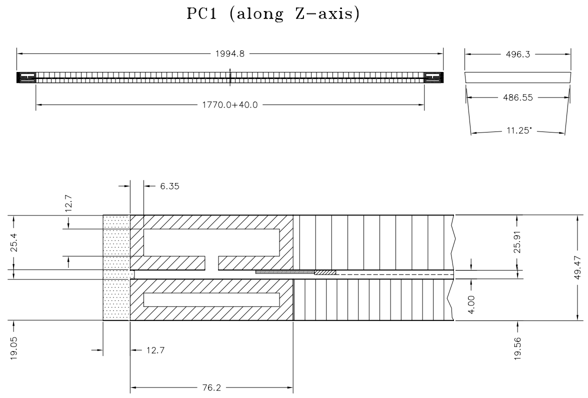


Figure 3.3: PC1 cross section along z plane

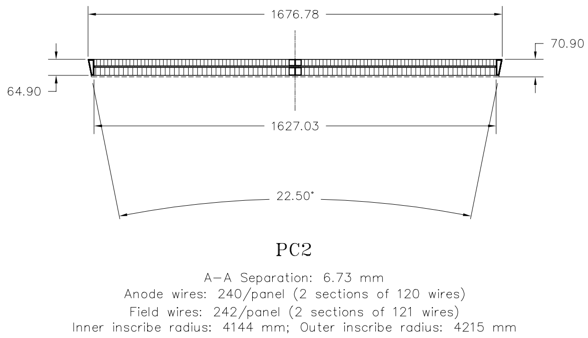


Figure 3.4: Pad chamber 2 cross section in rϕ plane

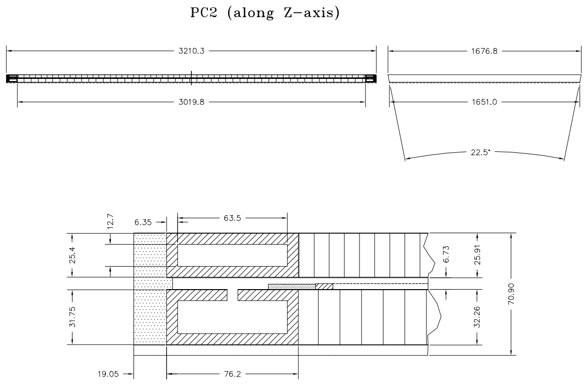


Figure 3.5: PC2 cross section along z plane

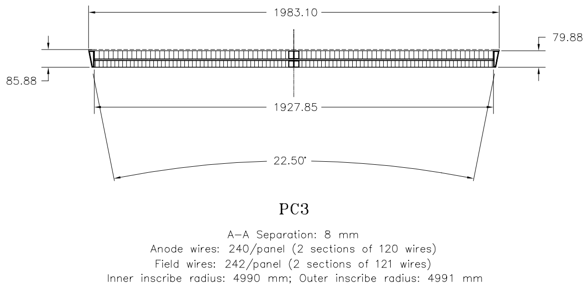


Figure 3.6: Pad chamber 3 cross section in rϕ plane

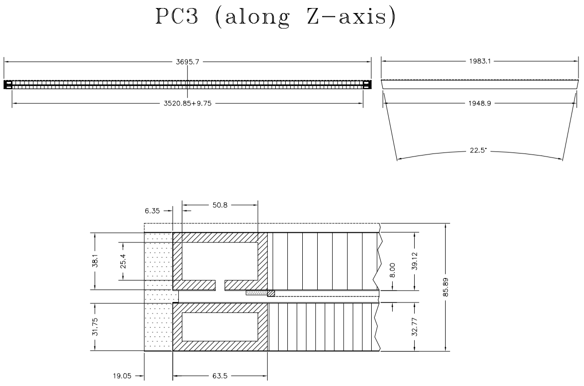


Figure 3.7: PC3 cross section along z plane

PC2 (details)

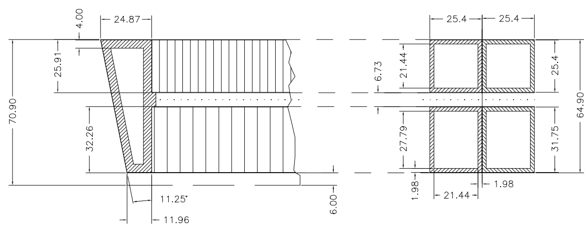


Figure 3.8: Pad chamber 2 detailed cross section showing end frame and central strut

a single sector of PC1. To avoid the increase of channel count, the number of pads per wire is kept at eight, which implies a pad length (apex-to-apex) of 36.8 cm and 43.5 cm for PC2 and PC3, respectively. Maintaining the ground strips at 1 mm wide, the pad strip widths would be 5.66 mm and 6.85 mm, and anode to cathode separation 6.7 mm and 7.8 mm for PC2 and PC3, respectively. Because the wires in these chambers have lengths of about 3 m and 3.5 m, respectively, along the z direction, they need two equal spacing supports between their ends in order to attain the very stringent requirement of maintaining the anode-cathode separation at a constant value to within 2%, which corresponds to a gas gain variation of less than 10%. The sheer size of these chambers demands that their frames require cross strut support in both the r-ϕ direction as well as the z direction. The dimensions of the whole frame including the cross struts will be fixed are shown in figures **??**,**??**. The design is based on a detailed engineering structural analysis.

The PC1, which occupies the radial space between inscribed radii 247.50 and 252.50 cm, was changed from a eight-sector to an eight-sector per detector arm design, as illustrated in Fig. 3.10. The eight sectors are completely modularized and attached to each other by detachable mechanical locks. Adjacent sectors are separated by a 25-μm aluminized mylar gas seal on each side, and along the seam between two wire planes there is a one-millimeter dead space. The cathode panels, which have areal dimensions 490.00×1887.02 mm^2, are to be fabricated with HEXCELL sandwiched between 250-μm FR4 skins. The chevron cathode panel has 25.40 mm of HEXCELL, and the panel heads are made of FR4 rectangular pipes of 6-mm wall thickness and outer dimensions of $25.40 \times 35.00 \times 490.00$ mm^2. The chevron pattern is etched on the FR4 skin facing the wire plane. For the plain cathode, the FR4 skin is metalized and the HEXCELL is 19.05-mm thick, and the panel heads are FR4 with

PC3 (details)

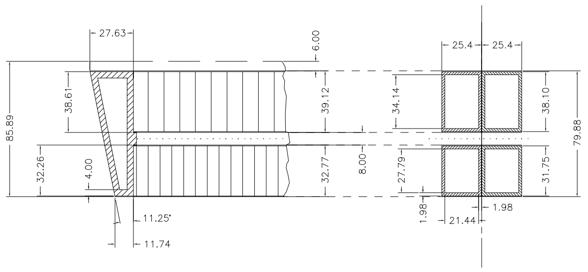


Figure 3.9: Pad chamber 3 detailed cross section showing end frame and central strut

dimensions 19.05 × 35.00 × 490.00 mm^2. The hollow panel heads of the chevron cathode also serve as gas inlet and outlet manifolds such that gas flows only through the region between the cathodes. The FR4 spacers between the cathodes define the separation between the wire plane and the cathodes. The sector detectors, which are mechanically locked to each other, are supported by an external frame consisting two parallel 90° sectorial arches interconnected at the ends. The arches are made up of rectangular carbon fiber pipes. Table 3.1 lists the revised characteristics of PC1.

The design of PC2 and PC3 is four sectors per detector arm, similar to the TEC geometry. The PC2 occupies the radial space defined between inscribed radii 415.00 and 421.00 cm, and PC3 sits between 491.00 and 498.00 cm. The mechanical structure of PC2 and PC3 are the same, except that the dimensions are different. Figures. 3.11 and 3.12 show isometric and sectional views of PC2 and PC3. The basic design concept of each sector detector is similar to that used in PC1. except that these detectors are much larger in area and each sector detector requires a carbon fiber frame around its boundary for support. The panel dimensions are 1659.40 × 3069.80 mm^2 for PC2 and 1960.70 × 3610.85 mm^2 for PC3. The larger panel area requires more material for strength. For PC2, the HEXCELL thickness for the chevron cathode is 31.75 mm, and for the plain cathode it is 25.40 mm. For PC3, the HEXCELL is 38.10 mm thick for the chevron cathode and 25.40 mm for the plain cathode. However, the FR4 skin for the cathode panels remains 250 μm thick for PC2, but must be increased to 500 μm for PC3. The rectangular hollow pipe FR4 panel head for the chevron cathode has a wall thickness of 6.00 mm and cross-sectional dimensions of 31.75 × 50.00 mm^2 for PC2 and 38.10 × 50.00 mm^2 for PC3. For the plain cathode, the panel heads have cross-sectional dimensions 25.40 × 50.00 mm^2 for both PC2 and PC3. The carbon fiber plates

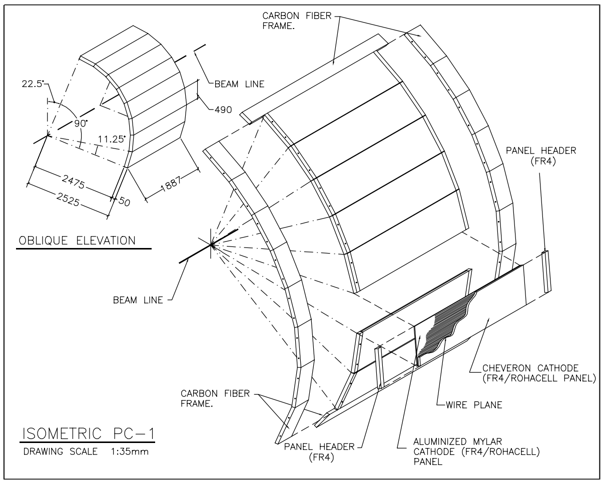


Figure 3.10: Isometric and sectional views of PC1. All measurements are in millimeters.

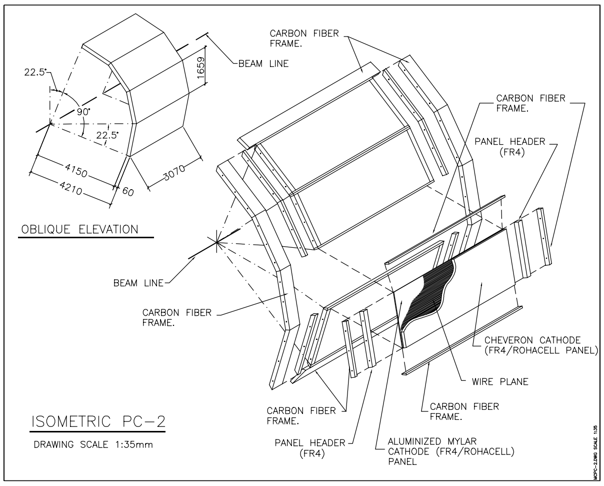


Figure 3.11: Isometric and sectional views of PC2. All measurements are in millimeters.

Table 3.1: Pad Chamber Characteristics

Item	PC1	PC2	PC3
No. of sectors/arm	8	4	4
No. of anode (A) wires	122	238	243
A-wire diameter	20 μm	20 μm	20 μm
A-wire tension	30 g	30 g	30 g
A-A separation (2·A-Cathode spacing)	4.0 mm	6.8 mm	7.9 mm
No. of field (F) wires	123	239	244
F-wire diameter	100 μm	100 μm	100 μm
F-wire tension	100 g	100 g	100 g
Chevron width	3.0 mm	5.2 mm	6.3 mm
Ground strip width	0.8 mm	1.4 mm	1.4 mm
Space line width	0.2 mm	0.2 mm	0.2 mm
Active wire length	1777.02 mm	2979.80 mm	3520.85 mm
Panel width	490.0 mm	1619.40 mm	1920.70 mm
Chevron pad length (apex-apex)	246.47 mm	417.92 mm	495.20 mm
F value	1.20	1.12	1.10
No. of readout nodes/wire	8	8	8
Readout nodes/panel	976	1904	1944
Readout nodes/arm	7808	7616	7776
Total readout nodes	15,616	15,232	15,552

surrounding each sector detector are 20.00-mm thick with a cross-sectional dimension the same as the sector detectors. The sectors, which are mechanically locked to each other, form a 90° four-sector arc, and are supported externally by a pair of parallel sectorial arches (similar to PC1) via adjustable screw bolts. The arch frame is made of rectangular carbon fiber pipes. Table 3.1 also lists the revised specifications for PC2 and PC3.

The present amount of material located in the active region of PHENIX due to the pad detectors is shown in the table below.

NOTES

1. The fiberglass is Scotchply of density 1.9 g/cm*3 and radiation length Xo=17.1 cm, used as facing material for the chevron cathode boards
2. The tape-graphite sheets are used as facing material for the ground cathode, and it has a density = 1.7 g/cm*3 and Xo=19.4 cm
3. The hexcell is the core material for both the chevron and ground cathode panels, and its density=0.024 g/cm*3 and an average Xo=81.7 m, which is deduced from the data used by GEM with the assumption that the radiation is emitted from

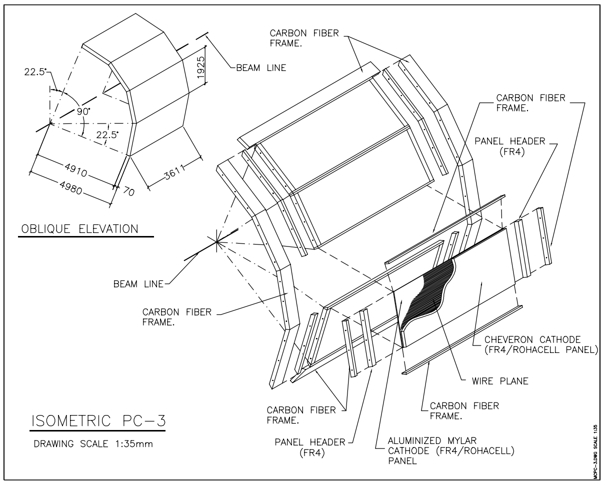


Figure 3.12: Isometric and sectional views of PC3. All measurements are in millimeters.

Table 3.2: Pad Chamber Material

	PC1		PC2		PC3	
COMPONENT	Thickness	%Xo	Thickness	%Xo	Thickness	%Xo
Fiberglass	0.51 mm	0.26	0.51 mm	0.26	1.02 mm	0.53
Tape-Graphite	0.51 mm	0.24	0.51 mm	0.24	1.02 mm	0.48
Hexcell	44.45 mm	0.05	57.15 mm	0.07	69.85 mm	0.08
Copper	18.82 um	0.13	18.82 um	0.13	18.82 um	0.13
Gas Gap	4.00 mm		6.80 mm		7.90 mm	
Electronics	6.00 mm		6.00 mm		6.00 mm	
Total	55.47 mm	0.68	70.97 mm	0.70	85.79 mm	1.22

a point source into a cone of 6 degrees with respect to its central axis, incident upon the hexcell (facing the holes) of infinite extent. N.B. Each panel of PC1 subtends 11.25 degrees in phi at the collision center.

4. The copper has density=8.96 g/cm*3 and Xo=1.43 cm, and is used on the plain ground cathode, chevron cathode, ground plane on mother board and signal traces on mother board. The average copper thickness in these four areas are respectively, 1/8 oz/ft*2 (4.18 um), 1/4 oz/ft*2 (8.36 um), 1/8 oz/ft*2 (4.18 um), and 1/16 oz/ft*2 (2.09 um).

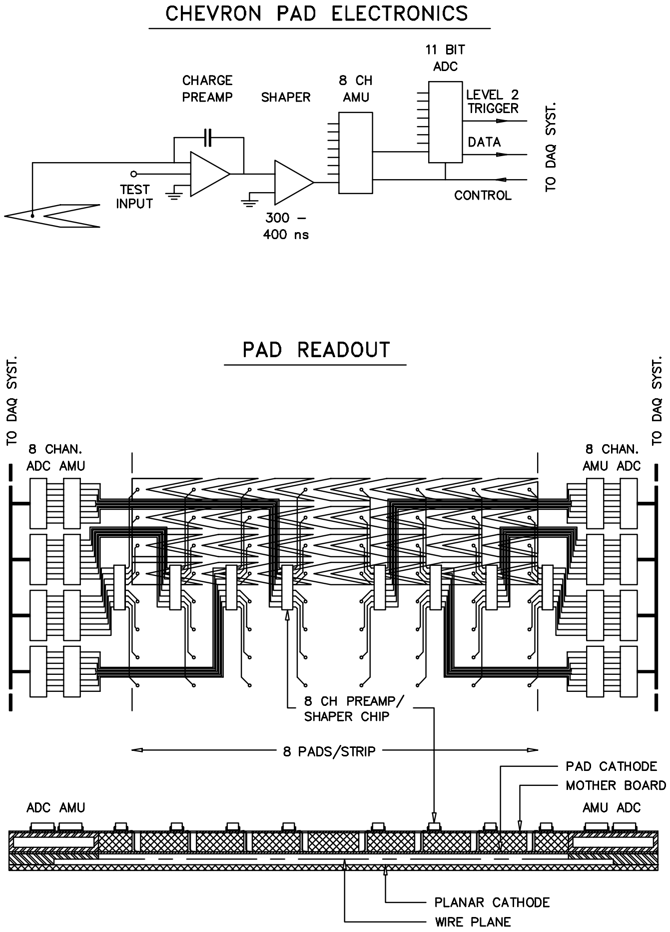


Figure 3.13: Electronic readout scheme: (top) FEE for one channel and (bottom) top view of back plane of chevron cathode board.

5. The final gas gap might vary by a fraction of a mm, depending on the final radial position of the PC's.
6. The electronics thickness is mostly due to the daughter boards which house the AMU/ADC/Buffer/Interface/Heap-Manager/Driver/connectors. These boards are located on the edge of the detectors just outside the fiducial volume. The Preamp/Shaper/Calibration chips are distributed on the back of the cathode panels covering about 1/and 0.1/

3.1.2 Electronics

There are 15,552 pads in PC1, 15,232 in PC2 and 15,552 in PC3. This makes a total of 46,336 pads in the whole PHENIX detector system. The charges induced in these cathode

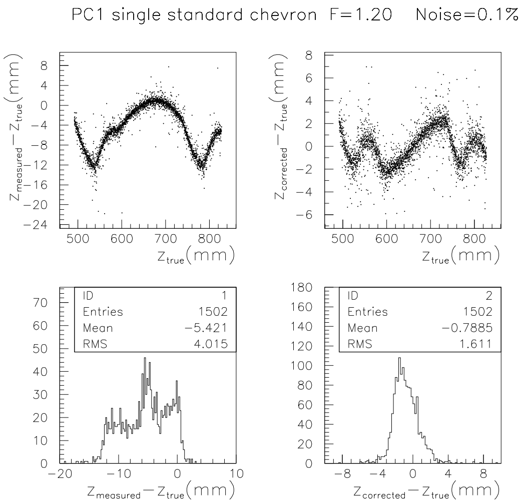


Figure 3.14: Simulations of spatial resolution of PC1, using space linewidth 250 μ. Calculation parameters were taken from Table 6.2.

pads must first be processed by the front end electronics and then passed on to the data processing and trigger systems in the form of analog or digital information. The usual front end electronics consists of a charge sensitive preamplifier followed by a shaper as shown in Fig. **??**a. The preamplifier must have low noise (less than a few tenths of a fC) and be capable of handling large detector capacitance (20–60 pF). Based on the chamber geometry used in this conceptual design, the optimum signal to noise ratio would be obtained with a shaping time in the range of 200–400 ns. At present no preamp-shaper system has been adopted for this detector.

It is possible that the hybrid preamp (BNL-IO-454-4) and shaper which have been used so successfully at BNL for smaller pad chambers could be miniaturized in CMOS technology and adapted to the present chambers. Because of the large number of channels involved, it is necessary to condense them into multichannel, say 16-channel, chips. Because of the length of time (many beam crossings) to process a pad chamber signal, an analog memory unit (AMU) must be provided to store the signals until a first level trigger decision is reached. This AMU is being developed at the Oak Ridge National Laboratories. Each output of the AMU is digitized by an 11-bit ADC before sending to the external processing systems. The 11-bit conversion is needed to preserve the 1% spatial resolution expected of the detectors. To minimize the noise problem due to long signal leads, the present plan is to mount the 16-channel preamp-shaper CMOS chips directly on the opposite side of the cathode board as illustrated in Fig. **??**b. The CMOS chips can be made with an area less than 1 cm^2 and a

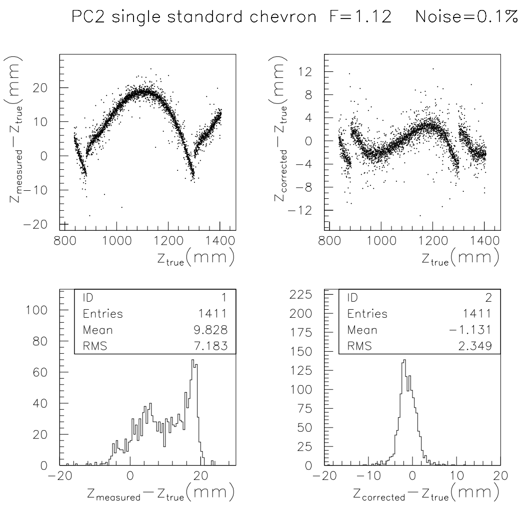


Figure 3.15: Simulations of spatial resolution of PC2, using space linewidth 250 μm. Calculation parameters were taken from Table 6.2.

thickness of about 300–400 μm. The chips will occupy less than 0.7% and 0.2% of the active detector area of PC1 and PC3, respectively. This is tolerable. However, the AMU and the ADC can be mounted on the edge of the board outside the active fiducial volume.

All electrical connections to the wires, cathodes and electronics will be arranged in such a way so as to minimize the chance of loosing a significant part of the detector. The calibration of the PC will involve separate pulsing of the anode wires and the input to the preamplifiers similar to the system used in experiment E814 at the BNL/AGS [2].

The front-end electronics readout system for the pad chamber comprises a preamplifier, shaper, AMU, and ADC. The detailed designs of these units are being specified. Figure 3.13 illustrates the readout chain for each channel. The preamplifier and the shaper is housed in one eight-channel chip. This preamplifier/shaper chip is a modified version of the unit designed at BNL for GEM to handle the large detector capacitance (80–200 pF) with an optimum shaping time of 400 ns. The shaper, which is equipped with pole-zero cancellation, returns the signal to within 0.1% of the baseline in four times the peaking time. The output stage drives a 2-m long low impedance line.

The original plan was to create a readout "mother board" on the back plane of the chevron cathode to house the preamplifier/shaper chip; however, there is a relatively large coupling between the shaper output lines and the chevrons on the opposite side. Therefore, it was necessary to isolate the shaper output from the chevron board in order to minimize these feedback effects. Figure 3.13 illustrates this scheme. Because a multilayer board isolating the

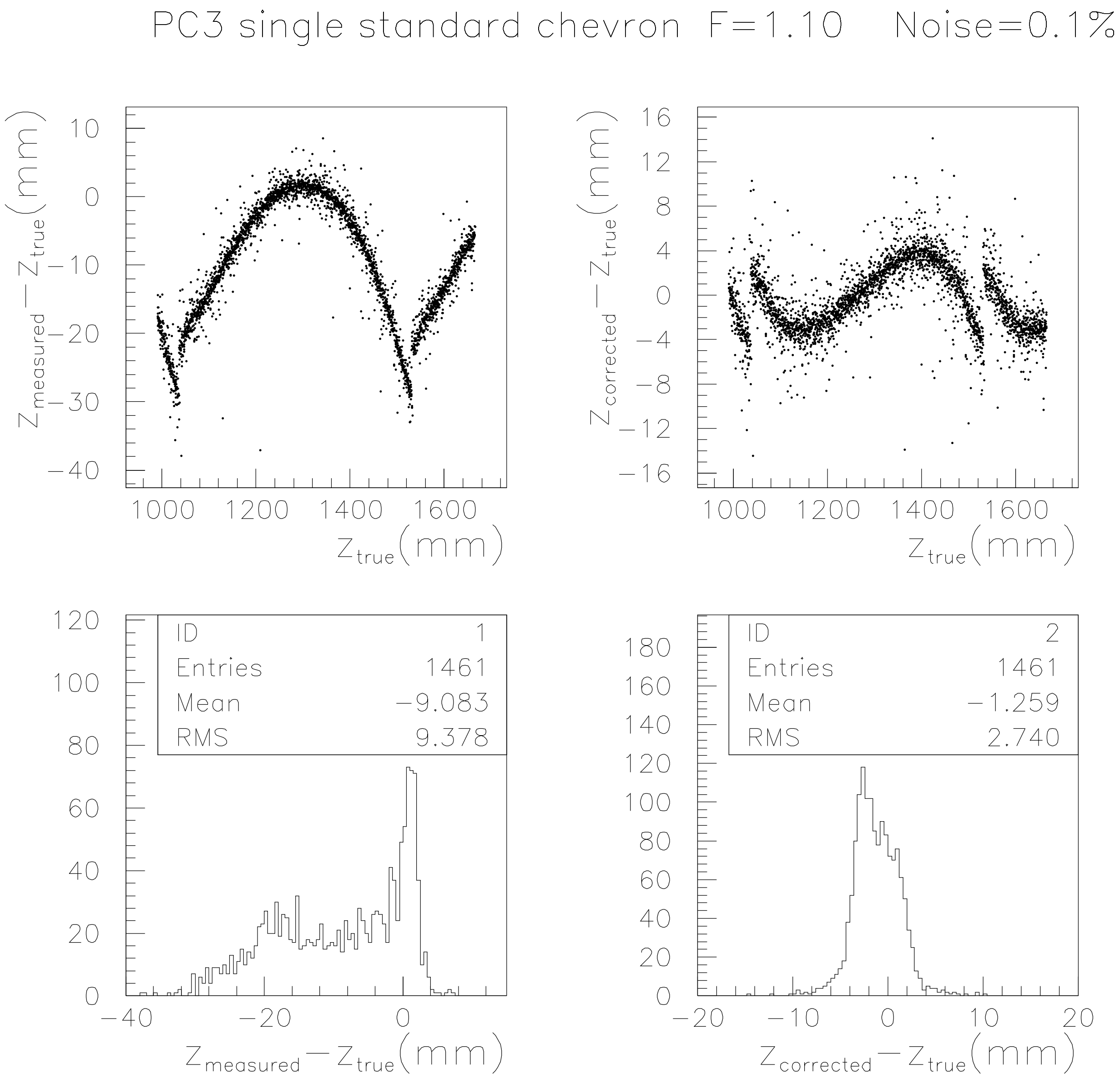


Figure 3.16: Simulations of spatial resolution of PC3, with space linewidths of 250 μm. Calculation parameters were taken from Table 6.2.

Table 3.3: Some Specifications of Pad Chambers

	PC1	PC2	PC3
Spatial resolution in z and r-ϕ (about 1% of pad length)	± 2 mm	± 3 mm	± 4 mm
Two track separation (about 40% of pad length)	$\sim$8 cm	$\sim$12 cm	$\sim$16 cm
Thickness	0.68% $X_\circ$	0.7% $X_\circ$	1.22% $X_\circ$

chevrons with a ground plane from the signal lines would introduce too much capacitance to the chevrons, their charge signals are brought together in groups of eight on the back of the chevron-cathode plane. These grouped signals are then routed through the HEXCELL using flexible printed circuit strips (kapton cables) to the outer side of the outer FR4 skin of the cathode panel. An electronic mother board for these signals is then created. The inner surface of the mother board will be metalized to form a ground plane shielding the chevrons from external interferences.

The illustration at the bottom of Fig. 3.13 shows that the AMU, ADC, serial-interface, and heap-manager chips are all located on a daughter board that attaches to the of the mother board, outside of the active volume of the detector. These chips are being developed at ORNL. The AMU is an eight-channel chip with 64 cells per channel. AMU input signals are to be sampled at three points at a rate of 10 MHz. Each output of the AMU is digitized by an 11-bit ADC. The choice of 11-bits accommodates the full charge range and preserves the 1% spatial resolution of the chamber.

3.1.3 Operation and Performance

Specifications of PC performance parameters are shown in Table 3.3. In addition, they also have:

- differential nonlinearity of less than 10%;
- low channel count achieved by using large pads.

Combining the PC performance with that of the DC yields measurements on $\Delta p/p < 1\%$.

Measurements

The performance specifications of the pad chambers have not been verified experimentally, although bench tests and test beam studies will be performed with prototype chambers this year. However, these specifications were based on experience derived from constructing and operating many smaller chambers [1], particularly those used in the E814 experiment at the BNL/AGS [2, 3]. The spatial resolution in r-ϕ is fixed by the chamber wire spacing and the 1% resolution in z has been obtained consistently. The 10% non-linearity requirement is a direct reflection of the gas gain and demands a maintenance of the anode-cathode spacing at a constant distance to within ±2%. This presents a great challenge in the construction of the chambers because of their large size. The ±2 mm resolution along z for PC1 when combined with the excellent p_T measurement capability of the DC will fulfill the momentum resolution requirement. The hit occupancy and the two track separation will be analyzed further in the next subsection. The use of honeycomb and thin fiberglass and mylar allows the chambers to be made thin and strong to satisfy the low mass requirement.

Calculations

The spatial resolution of the pad detectors is determined by many factors. Because the absolute resolution required from the present detector is greater than or equal to 1 mm, contributions from the spatial spread of the primary ionization or the physical spread of the avalanche is negligible. The main contributions to the resolution come from the signal-to-noise ratio of the readout electronics and the nonlinearity of the pad system. A program has been written to study these two effects. The results for the PC1 and PC3 detectors are shown in Figs. **??** and **??**, respectively. The chevron-to-chevron distance and pad width is as given in Table **??**. In each detector the chevron pattern is assumed to have a form factor $f = 1.05$ and $f = 1.025$, for PC1 and PC3 respectively. The form factor f represents the amount of overlap between chevrons. The values adopted for f were optimized for best performance. An etched away insulated line having a width of 60 μm between pads is assumed. The width of the charge distribution induced on the pad is taken to be a gaussian with a width determined by the distance between the anode and the pad plane (σ =1.5 mm for PC1 and σ =3.2 mm for PC3). The measured position is determined by a weighted average of the position of the pads, where the weights are taken to be the signal measured on the two pads collecting the largest charge. The top part of the figures shows the difference between the exact position and the deduced position using this simple interpolation, neglecting the effect of noise. This is a representation of the position resolution due to the nonlinearity of the detectors. For both detectors the maximum deviation, which happens when the particle is close to the apex of one pad, is 4 mm. However, it is possible to partly correct for some of this non-linearity off-line. Furthermore, this non-linearity can probably be improved by changing slightly the shape of the pads.

The effect of the noise was studied by Monte Carlo. It was assumed that each pad has a noise equivalent to 0.1% of the mean of the total charge induced on the anode wire. For an anode signal charge of 0.2 pC, a typical value, this corresponds to an input noise for each preamplifier of 1200 equivalent noise charge (ENC). The charge distribution on the anode is a Landau distribution, in agreement with previous measurements [1]. In calculating the charge induced on the pad, the partial shielding due to the field wires was taken into account. Roughly 50% of the charge at the anode is induced on the pad plane. The center part of the figure shows the effect of noise on the position measurement as a function of the position of the particle. The bottom spectra show the distribution of difference between the measured and exact position assuming that the detector is uniformly irradiated. The variance of the distribution is calculated to be 1.1 mm and 1.5 mm for PC1 and PC3, respectively, which is inside the desired resolution. Of these numbers, the electronic noise contributes roughly 0.5 mm and 0.8 mm, respectively.

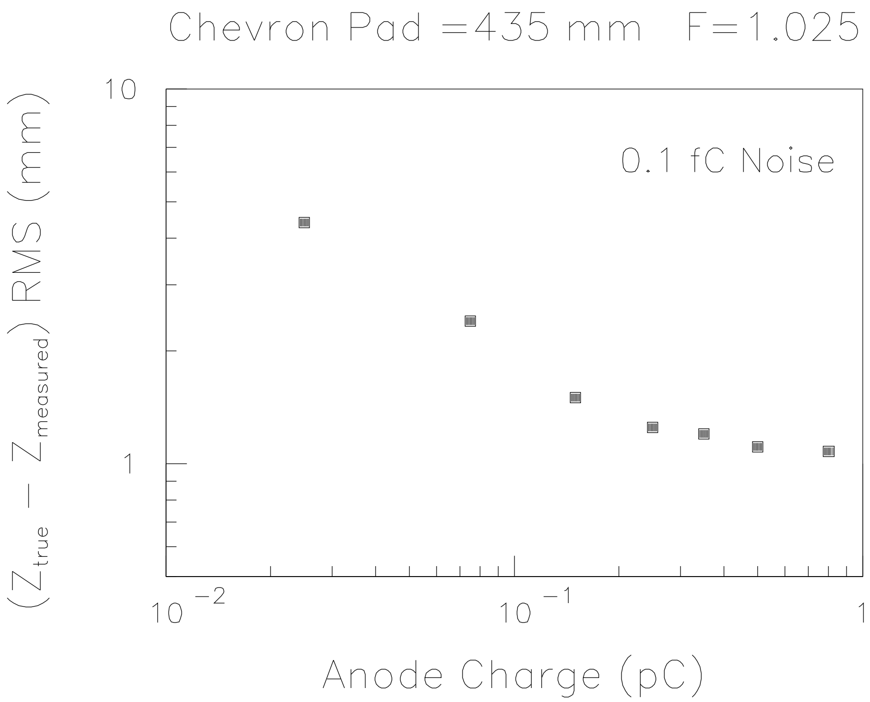


Figure 3.17: Position resolution as a function of anode wire charge.

Assuming the charge at the anode has a Landau distribution [1] and folding in an equivalent noise of 0.2 fC, the position resolution computed is plotted as a function of anode charge as shown in Fig. 3.17. The optimum position resolution is consistent with the values deduced and confirms the design specifications on the position resolution.

All PC1, PC2, and PC3 have more or less the same average hit occupancy because their pad sizes are simply scaled from each other. Assuming a double HIJET distribution in a Au + Au central collision, the probability for different number of hits per pad is given in Table **??** .

Even though the double hit probability is small, some of them can be resolved. If the double hits within a pad are separated by a distance greater than a certain value, they can be recognized from the total amount of charge on the pads and the sharing of this charge amongst them. Because the energy deposited has a Landau distribution, the charge induced on the pads also has a Landau distribution. Using the charge distribution data given in [1] and the noise given above, it has been estimated that the two track separation in the present pad chambers is about 40% of the pad length. This rather poor resolution is an inherent weakness of the interpolating pad cathode design. Fortunately, the double occupancy is rather small (see Table **??**) and should not degrade the chamber performance.

The spatial resolutions of the pad chambers were simulated in the CDR. In those calculations, it was assumed that the space lines separating the chevrons from each other and from the ground strips in the chevron cathode were uniformly 60-μm wide. However, due to technical reasons, this relatively narrow linewidth can not be preserved in the fabrication of large cathode boards. Industrial assurance can only be obtained for a linewidth of 250 μm. With this information, we recalculated the achievable spatial resolution of all three chambers by optimizing the chevron form factor (F) value and using a new linearization technique. Figures 3.14–3.16 display the results. The resultant resolutions are still within the design specifications in the z coordinate of $\sigma_z = 2$, 3, and 4 mm, respectively. IHEP (Beijing) has facilities to fabricate large cathode boards with an assured uniform-space linewidth of 200 μm, which would provide further improvement of chamber performance.

3.2 Pixel Pad Cathode Option

As noted above the chevron geometry pads offer good spatial resolution, large pad size to reduce channel counts, low mass and proven reliability [2, 3]. However, the construction of such chambers for detection over a large area is fairly demanding. The anode-cathode geometry and the pad geometry have tight tolerances. Because of the requirement of relatively high precision analog readout electronics, the cost per channel is comparatively high. Furthermore, the large pad size makes them less than ideal for two track resolution. These shortcomings could be remedied by the use of a fine pixel pad design for the cathode with a digital yes or no readout system. The good spatial resolution feature of the interpolating pads can be retained if the pixel pad size is chosen to coincide with the required spatial resolution. Unfortunately, this dramatically increases the total channel count to about three million (one million for each of the PC1, PC2 and PC3). This need not be exorbitant if a clever scheme could be found to reduce the channel count by a factor of three to about one million, and adopt a low cost electronic readout system (less than $1 per channel). Chambers using the pixel pad design would also markedly improve the double hit resolution, by reducing the average occupancy rate per pad to less than 1% of that for the chevron pad design. This scheme will be pursued further with the investigative work being undertaken at the University of Lund (Sweden).

The update of the pixel pad solution concentrates on the studies and modifications done after the completion of the CDR. These include:

1. Test measurements on a small chamber.

2. Simulations based on the test results.

3. Modified mechanical construction based on the mechanical engineering performed for the chevron pads.

4. Cost estimates for IC development, fabrication and chip-on-board assembly.

The pixel-pad solution has many advantages compared to the chevron solution. In particular the fine granularity ensures reliable pattern recognition at extreme multiplicities. The major uncertainty with the pixel system is that it makes use of the chip-on-board (COB) construction technique, which is not yet used in HEP experiments. Therefore, an evaluation of a full scale system is needed to determine whether this new technique is reliable enough to be used in an essential detector system.

As a consequence, the pixel pad solution is not currently a part of the baseline detector, instead it is considered to be an upgrade with the special status that it could potentially have lower cost than the baseline version once additional resources are considered. The goal is to complete a full scale prototype (one sector of PC1) on a time scale that would allow the upgrade option to be implemented in the baseline detector. The development of the pixel readout electronics will be performed by the Lund University group.

Some important recent improvements in the design are:

1. A scheme now exists for feeding the signals through the HEXCELL backplane.

2. The FEE electronics (preamp/shaper/Discr/DMU) is now (dis)mountable on the pad chamber backplane even if the access is only from the side. This would allow for repair of the pixel FEE in the same time frame as for other FEE systems with only side mounted electronics.

3. The local FPGA controllers readout FI/FOs and cable drivers are on the motherboards on the side of the chambers.

4. The dicriminator function is moved from the amplifier CHIP to the DMU CHIP.

Item 1 and 2 offer very large advantages, because the design/fabrication of electronics is decoupled from that of the chambers. The servicability of the electronics reduces the demands on extreme reliability to the same level as for other systems. This makes the work on a small size prototype (1600 channels) more worthwhile and it may in fact be possible to make a final positive decision on pixels based on the small prototype. As a consequence we will put extra emphasis on the small prototype before starting on a large size prototype electronics since this step to large chip quantities is expensive.

3.2.1 Mechanical Design

The scheme employed to reduce the number of independent pads is illustrated in Fig. 3.18. Rectangular pads span three wires in one direction. The width of the pad along the wire is chosen to be the desired position resolution in the z direction and the wire spacing fixes the r-ϕ resolution. Assuming that the signal from a hit is always sensed on three pads, the staggered pad positions across the wires make it possible to determine which wire was hit. The desired position resolution is kept, but the number of pads is reduced by a factor of three. The expense is an increase in pad occupancy to the level of 1%, which is acceptable. A drawback of this geometrical shape is that, in order to detect the signal on three pads, the chamber must be made thicker. This occurs because the signal width as seen on the pad plane is determined by the wire-pad distance. On the other hand, because most tracks are not perpendicular to the chamber, a thin chamber is desired.

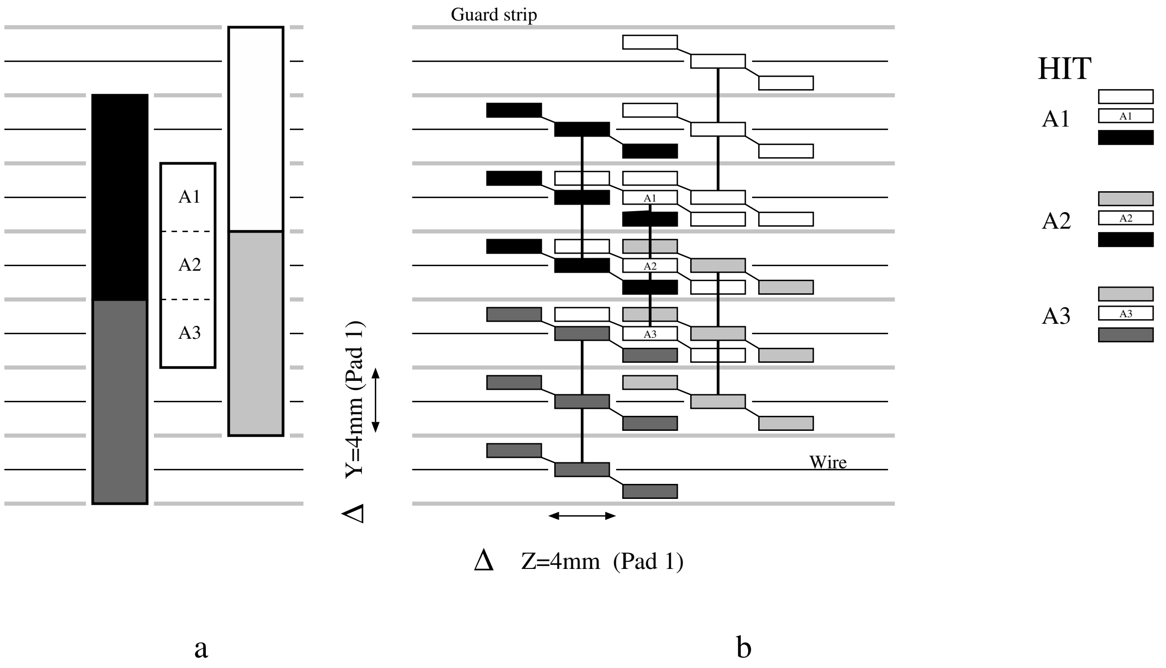


Figure 3.18: Pixel pad logic layout: a) rectangular pads over 3 anode wires, b) each pad split into 3 adjacent pads.

The shape of the pad is modified according to Fig. 3.18b. Logically, this solution is the same as for the rectangular pads in so far as to determine which wire is being hit from the staggering pads. The only difference is the geometrical shape of the pads which is now split into the neighboring pads. For symmetry reasons the signals on both sidestrips must be identical. Thereby the requirement "at least three pads fired" is always fulfilled. Because the guard strips prevent crosstalk between wires, there will not be more than three pads fired due to the pulse spread across the wires. If a signal is observed on four adjacent pads, then the hit was in the middle of these four pads. Thus, in principle the position resolution along the wire is better than the pad size.

A major concern is the thickness of the cathode plane which must not exceed 0.5% of a radiation length. The copper pads could be etched on one side of a thin fiberglass and a printed circuit on the opposite side with plated through holes. The board could be as thin as 200 μm. This is true because crosstalk due to coupling between pads and electronic leads is not as important as in the case of the chevron pads. However, it is possible to make a three-layer 300-μm thick board with a ground plane in between if crosstalk is proven to be serious. In this case, the pad capacitance would increase significantly. The mounting and support structure of the board is similar to that of the chevron pad cathode described previously. Because of the large number of pads, signals must be processed on board with the chip-on-board (COB) technique. In the COB technique, the naked chips are glued onto a PC-board and the electrical connections are made with micron thick wires by ultrasonic bonding. A chip is typically only about 300-μm thick and 10 mm^2 in area, and on PC1, one chip serves 7.7 cm^2 of the cathode plane area, which is only 1.3% of the detector surface covered by silicon. Averaged over the detector area this is negligible.

As described in Section 3.1.2, the back plane will be fabricated from HEXCELL backed on both sides by 250 μm PC-board material. One of these FR4 plates will be the cathode board. The signals are brought through the HEXCELL to the top PC board where the preamp/shaper chips are located. This board also has the printed leads bringing the signals to the sides of the detector.

For the pixel readout we anticipate a similar solution; however, the integrated circuits and the leads to the sides are to be on a separate 120-μm thin PC-board fabricated with the COB technique. This board should connect directly to the signal feedthru through the HEXCELL. The upper skin would then be without a printed pattern.

This solution allows the mechanical design of the pad chambers to be fixed, but keeps open the possibility of subsequently adopting the pixel-pad solution. The method used to bring the signals through the sandwich structure, which is of common interest to both readout solutions, needs to be developed for large scale solutions.

With mounted IC and gloptop the additional readout PC-boards will add about 0.08% of a radiation length to the material in PC1, and a factor four less in PC3 due to the larger area served by each IC. This would add less than 0.01%, if the signal feedthru is made of a 5-mm wide 120-μm PC-board material. We estimate the additional material from the pixel readout electronics to be 0.1% of a radiation length.

3.2.2 Electronics

In the chevron pad design, the front-end electronic chips are housed inside the gas volume of the chamber. This solution can also be adopted to the pixel pad design. The low power consumption (10 mW per chip) keeps the heating effect at a tolerable level. Furthermore, the pad/chip connections can always be arranged in such a way that the three pads defining a hit are connected to three different chips so that losing one channel would not hinder the reconstruction of a hit. This would greatly reduce the need for service. However, there is a certain desirability to mount the readout board outside the gas volume and sense the signals through a window. The advantage of this scheme is that the system can be made modular to allow modules to be replaced for repair without opening up the gas volume. A typical module could be 10 cm wide and have a length of one full wire. It is necessary to break the staggering of pads at the edge of each readout board. Effectively this increases the number of pads by 15% if the board width is 5 cm on PC1 and 10 cm on PC3. Figure 3.19 shows a layout and mounting of a readout module board.

The front-end readout electronics system for the pixel pads is relatively simple, and one channel of it is shown in Fig. 3.20. For each channel the front-end has a preamplifier and a shaper with a shaping time of the order of 100 ns, feeding a discriminator, from which a bit in a bit pattern is set. The bit pattern is clocked through a digital memory with the beam clock until the decision on readout has been made. It seems attractive to fit 16 channels on each chip. A fast signal from the chip indicating a hit can be delivered for the first level trigger.

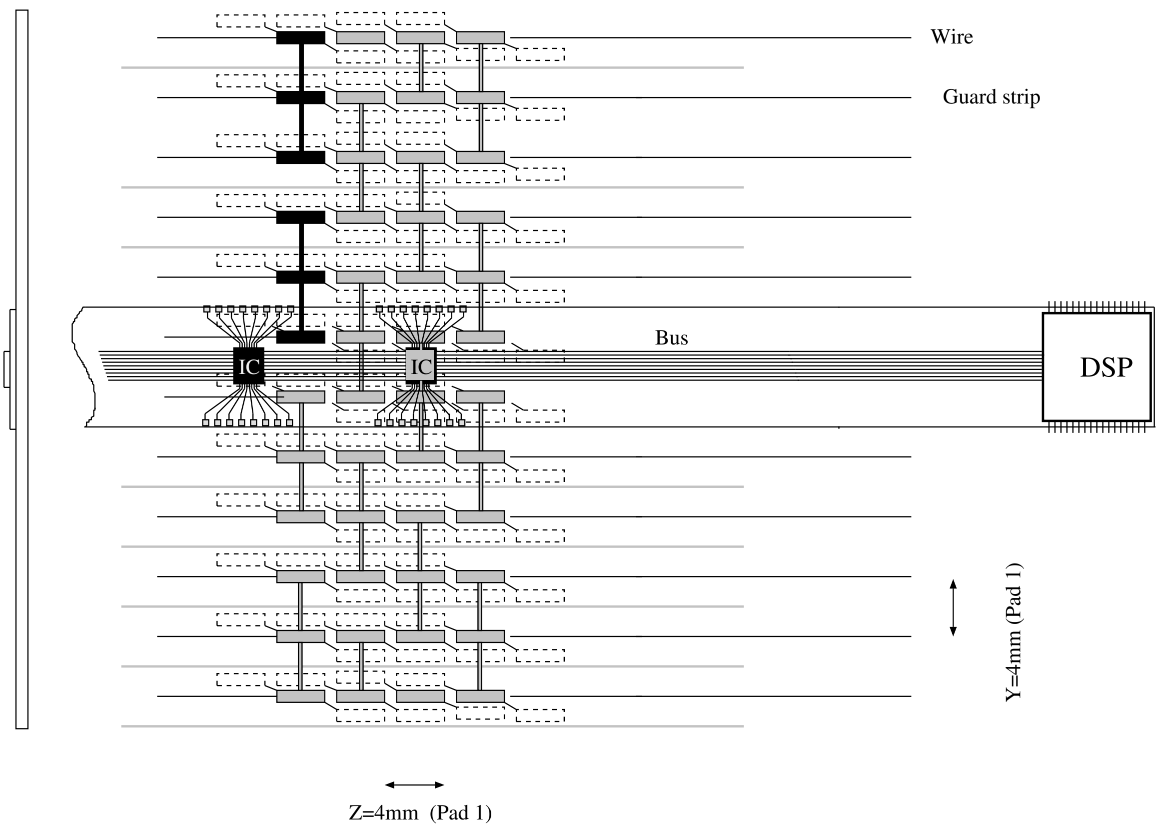


Figure 3.19: Modularized chip-on-board mounting structure for pixel pads.

The multiplicity of fired chips is proportional to the total multiplicity and complements the PHENIX multiplicity trigger.

All 150 chips on a module are read out into one microprocessor placed outside the chamber volume (e.g., a 40 MHz DSP, Analog Devices ADSP-2100). Choosing a bus speed of 15 MHz should enable readout of the module in 10 μs. The DSP would have sufficient time to perform operations to reduce the data to three bytes per hit: one byte for module number, one for chip number and one for the hit pixel. This amounts to 1.5 kByte per plane in a central Au + Au collision to be handled by the data acquisition system.

Because the occupancy is low (below 1%), very clean information is expected. There may not be any need for further off-line analysis. This renders it possible for on-line trigger, because the full position information does not have to wait for long digitizing times. In order to take Full advantage of this could be taken in the trigger, if the readout is done faster (a higher bus speed is likely achievable). For example, more parallel processors could be introduced at the module level such as two DSPs per module.

Although this is a new solution to the readout of PC, not much development is needed to determine the performance of such a system. Tests with this pad geometry need to be performed on a small test chamber. Important questions to be answered are: What is the

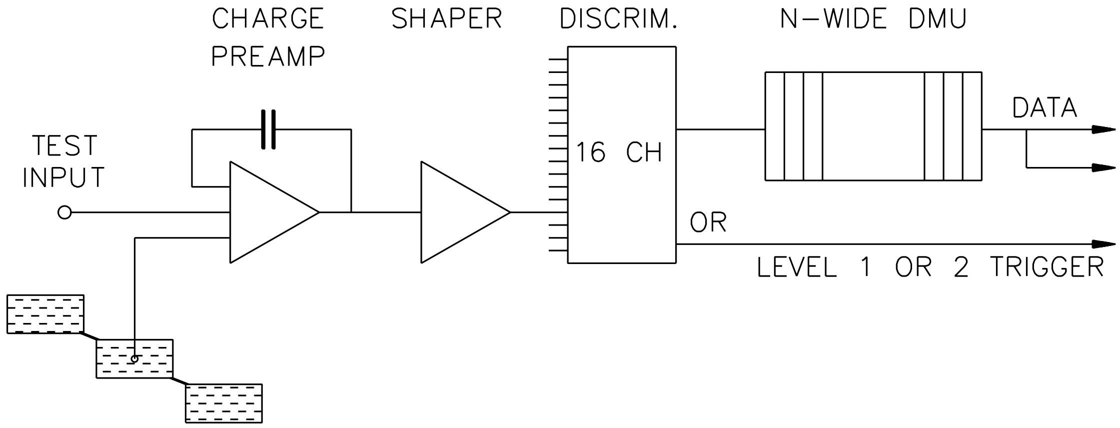


Figure 3.20: Front-end electronics for pixel pad readout.

efficiency to have three adjacent pads fired? What is the probability that noise produces three fired pads? Can a position resolution better than the pad width be achieved?

Most questions on backplane construction, such as COB mounting and chip design, will be answered during the winter of 1992–93, when the prototyping of a pad readout module for a multistep avalanche chamber will be made by the University of Lund group together with the chip design company (SiCon, Linköping, Sweden) and the COB company (XICON, Malmö, Sweden). An operating prototype is expected by May 1993.

For this type of readout solution with 900,000 channels it is essential that the cost per channel be kept low (less than one dollar per channel as shown in the WBS) and that the electronics can be mounted on the detector backplane. These goals can be achieved with a high degree of integration and the COB mounting technique.

Since signals are processed locally, little signal driving is required. Together with moderate demands on resolution this ensures low power consumption of the order of a few milliwatts per channel. We plan to develop new integrated circuits for the full readout chain and to place the analog/discriminator function and the digital pipeline in two separate integrated circuits in order to minimize the risk of crosstalk.

We plan to fabricate the IC analog in a 1.2-μm BiCMOS process. It will contain 16 channels of preamp/shaper plus discriminator. The shaping time will be about 100 ns. The output of the discriminator will cover two beam crossings in order to make sure that the time slice corresponding to the event will have the information. Therefore only one time slice needs to be transferred to the DSP. The IC area is estimated to be 3×3 mm^2.

The digital IC will include a 64-cell deep digital pipeline (DMU) timed with the beam clock. It will be followed by a five-events-deep derandomizer and bus output. The width of the DMU will probably be 48 or 64 channels. When transported on a 16-bit wide (10 MHz) data bus, 4096 channels can be read out within the limits set by the average LVL-1 trigger rate (30 μs). The chip area will be about 4×4 mm^2.

Both IC will be mounted as bare silicon wire bonded down to a 120-micron thick PC-board. After the wire bonding the IC and wire bonds are embedded in an epoxy gloptop. This gloptop can be covered by a conductive layer applied by screen printing. The digital and analog parts of the readout system will be shielded from each other by a ground plane.

Once assembled and tested the COB mounting should provide a very reliable and stable system. The difficulty is that the electronics must be tested thoroughly between the stages of bonding and sealing with the gloptop. These "burn-in" tests should be an integral part of the production line. The Lund group has a close collaboration with a COB company in Sweden, which would afford the possibility of performing such tests. The mounting technique is most suitable for electronics with moderate resolution, because lengthy tests of individual chips would not be required.

The cathode board

The procedures how to fabricate the large cathode boards are still not quite worked out. The difficulties are to a large extent the same as those of the Chevron Boards and we understand from Tommy that additional difficulties have come up.

In some aspects the pixels put less demands on the cathode board. By simulations we have found that the performance of the pixel system is very little affected by a displacement of the pads by a few hundred microns perpendicular to the wires in the plane of the board. We also find that variation of the anode cathode distance is not a crucial point from the readout point of view. Any problems here for the pixels should be due to the electrostatics of the chamber which was not included in the study.

The pixels require a very large number of plated through holes (3 vias per channel, one hole per 4x4mm square on PC1) from the cathode side to the top side of the board. This is a major cost issue. Although the number of holes is not dramatic for normal PC-board construction it may be a difficulty for the non standard procedures when fabricating very large boards.

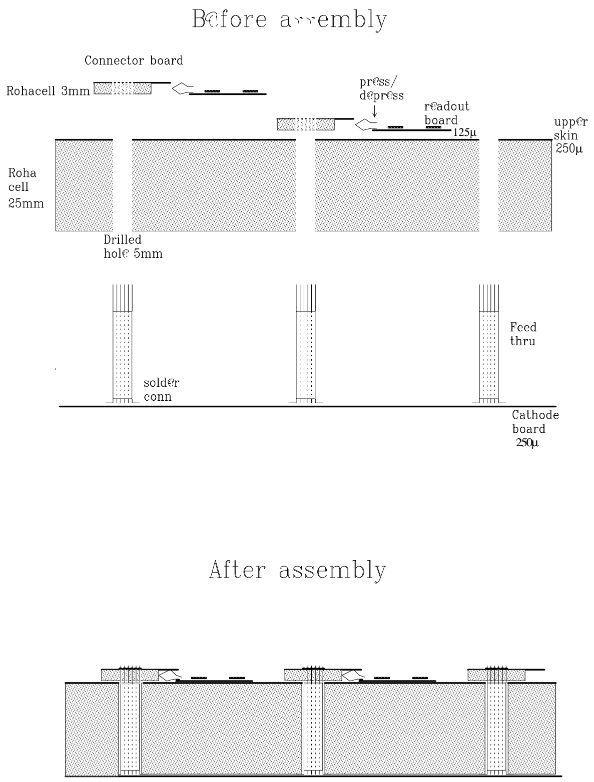
Although it is preferable to make the cathode board in one piece, we think it is worthwile to find out if one can make the cathode board for the pixels out of smaller pieces (as large as possible but still inside standard PC-board fabrication which probably means the size of a fastbus board) which are glued together on a HEXCELL sandwich backing.

The procedure may be be as follows:

Make the HEXCELL sandwich with upper skin of 10 mill fiberglass and the bottom skin as thin as possible, maybe 4 mill mylar. The top skin is covered with copper on one side in order to provide proper shielding between electronics and pads. Drill 5mm diameter holes through which the feedthroughs are brought, one hole per 48x16mm area. Solder the feedthru onto the cathode board. Glue the cathode boards on onto the mylar skin (see fig).

I think that the mechanical strength of this is not much less than that of a continuous bottom board. The additional radiation thickness from the mylar is not much. A stronger construction would be to use a full fiberglass skin and make the cathode pattern on Kapton or mylar instead.

Considering the slightly relaxed demands on the mechanical accuracy of the pixel cathode board we think it should be possible to find a solution along these ideas. Another advantage



with small cathode boards is that the assembly of the feedthrus on the standard size cathode boards can be done by automised SMD soldering methods. We want to use soldering here since gluing with conducting glue should be done only to gold plated contacts and we want to avoid goldplating of the large cathode boards.

The feedthru

Our partner, the XICON company in Malmo, suggested an elegant solution to the problem how to feed the large number of signals thru the HEXCELL structure. When making straws, one uses an extrusion technique. The crossection of a straw can have almost any shape. One can make the extrusion tool so that 16 thin wires can be embedded in the cylindrical straw wall.

The wires are cut a bit longer than the straw itself so that they can be bent at a right angle at one end for soldering to the PC-board. The soldering can probably be done in a semiautomatic way. This is done before the cathode board is glued on the HEXCELL. In order to help the feedthru to fit into the holes in the HEXCELL one uses a conical guiding tool which is temporarily fixed on the feedthru.

In the other end, the wires sticking out of the straw fit into the vias of a thin PC-board (we call it connector board). This board, which is glued onto the upper skin of the sandwich structure, is lifted a few mm above this fiberglass by a spacer made of HEXCELL. The purpose is to allow the flexible readout boards to be connected underneath the connector board. The traces of this board are goldplated in order make a reliable connection between the traces, which are on the bottom side of the connector-board and the springloaded, goldplated connectors on the readout board. The printed pattern on the connector-board brings the signals from the circular pattern of feedthru wires to a linear row of contact traces with 1mm pitch.

The cathode board+HEXCELL structure with the connector board mounted on is a separate unit which should be tested electrically during assembly. After testing we assume that the electrical connections don't break and if they do, it will be just single channels, a type of failure which we can live with.

There are alternative solutions to the extruded straw. One possibility is to make a homogeneous cylinder out of HEXCELL, punch out holes for the wires, feed the wires thru the holes, fix the wires in the holes by a glueblob and bend the wires at 90 degree in one end.

The readout board

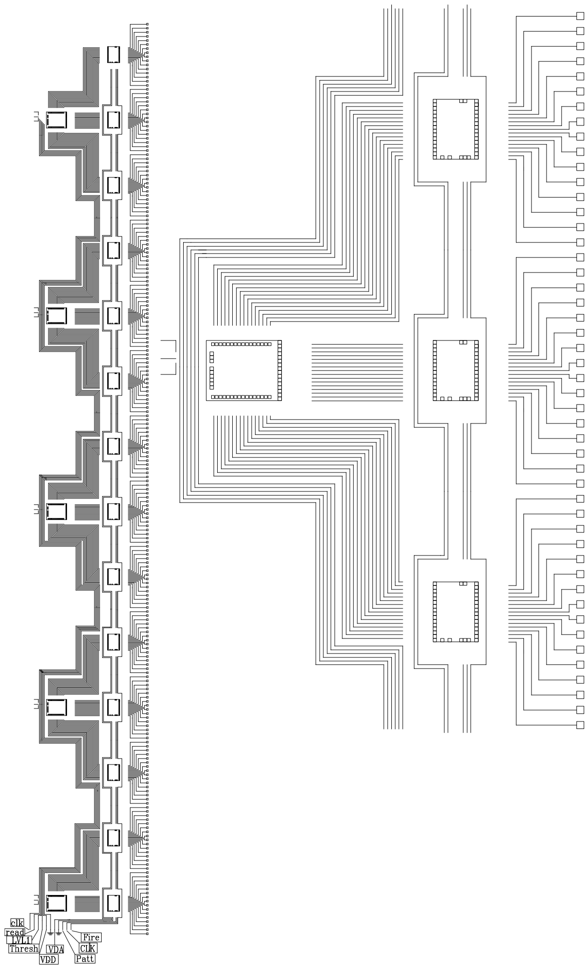
The readout boards will on one edge have thin goldplated metallic pieces which have been bent in such a way that they press with enough force against the traces on the bottom side of the connector board. During assembly, the readout board is carried in an assembly tool with which it is slid in position steered by steering pins on the connector board. The force of the springs must probably be taken up by the mounting tool by pressing the metallic pieces down during the mounting procedure.

The readout boards will be manufactured as single pieces of G10 of 224 mm length, each carrying amplifier and DMU CHIPs to handle 14x16 channels. All communication lines and DC supplies (about 30) which belong to one such readout board will be distributed separately in a 100micron kapton flat cable ending in a flexible connector which connects to the motherboard at the side of the chamber. The cable may be a commercial one or specially made if we want to reduce the line spacing.

The timing can be matched by external delays so that time critical signals can arrive to the CHIPs with a maximum time spread corresponding to 22cm trace length. Each DMU sends the result of 16 channels as 16 serial bits to a FI/FO placed on the motherboard. The driving ability of the DMU output must be enough for a 1.5m cable length (PC3).

We want to have the local controller, the FPGA on the side of the chamber. One FPGA will control as many readout boards as possible, at least half the length of a chamber (4 readout boards (56x16ch), call it a strip). The FI/FO's of 4 such strips (call it a readout chain) are all read into the same front end processor. The data stream to one processor is then. 16 ticks to bring the serial data to the FI/FOs which are 56x4=224 words deep which will be emptied well in time to match the average level 1 trigger rate (30-40 microsecs). One could even allow larger seriality in the transfer from DMUs to the FI/FOs. The advantage of this is a reduced number of lines on the detector backplane but this has to be valued against the increased damage caused by dead DMUs. For the time being we prefer to go as little serial as possible.

A cover of aluminized mylar over the analog CHIP and the connector board provides shielding between the analog and digital parts.

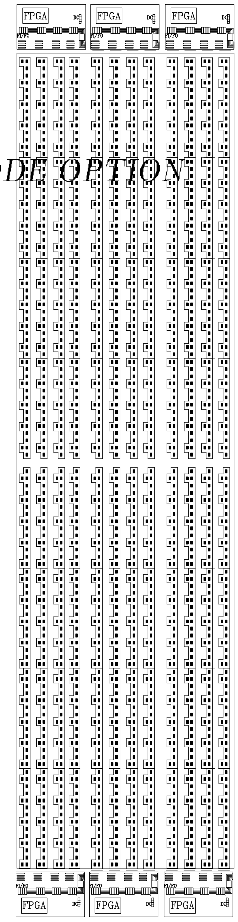


We think that this design has many advantages and we think it is very worthwhile to spend some development work on the mounting procedure to achieve all the benefits of dismountable electronics. We also strongly prefer to place all electronics except the amplifier and DMU with full access on the chamber sides.

The analog CHIP

We have decided to divide the FEE in two CHIPs one CHIP containing the preamp/shaper and the other containing the discriminator and DMU. This is a bit different from the ideas a couple of months ago which placed the discriminator in the analog CHIP. The reason for the old ideas was general considerations that it is better to drive logical signals than analog over some distance. However, this is not a major concern in the pixelcase where the distance between analog and digital CHIPs is only a couple of cm.

Instead, by placing the discriminator in the DMU CHIP we avoid the possible crosstalk between discriminator output and the sensitive preamp input. Imagine, the discriminator fires occasionally on noise which results in a full size signal on the discriminator output which



mother boards with FI/FOs, 20 bit bus, cable driver, FPGA and connectors to readout boards

talks across to the input producing a cluster of fired pads looking like a good hit. With the discriminator in the DMU we will only risc crosstalk from the shaper output to the preamp input for the largest signals (which sometimes are as high as a ttl pulse, but with longer risetime). Consequently, noise, making up fake hits by crosstalk will not happen.

One could also consider to have the discriminator controlled by the clocking if it is located in the DMU, which may result in better performance than having it running free.

There are some analog CHIPs which have been developed for readout of cathode pads on MWPCs. Two of them are developed for GEM, one at BNL and one at Oak Ridge and we strongly consider to use one of them in the prototype work. The closest contacts have been with Oak Ridge in this matter and the feasibility to do minor modifications due to our pixel wishes are under way.

When we go to production for a full system we will decide whether we should develop a new analog CHIP with fully optimized characteristics for the pixels or not .This may also be a cost issue since the prices quoted by the European Silicon foundry, AMS, seem at first glance to be substantially lower than those of ORBIT. Maybe one can translate the design to the AMS process??

The test pulsing is a little problematic for the pixels since the number of channels is so large that it is impossible to feed a separate pulser on/off signal to each channel which in principle is desired. Instead we want to pulse all channels by an on-CHIP pulser (or by pulsing the wires). Prior to that, a hit pattern has been distributed and stored in each CHIP via a slow serial communication which runs through a large number of CHIPs. According to this pattern, channels are shut off, in order to produce realistic pulser hits.

The Digital CHIP

We are eager to get started on the development of the discr/DMU CHIP. There is one MPW run which has to be submitted on february 13 which is too early to catch. We must aim at the next one, two months later which means that we need to get started in January with the design.

We have not made a final choice how many channels to handle in each DMU. 48 is a nice number since each DMU then controls a square surface (48x48mm on PC1). This is advantageous if this info is going into the lvl1 trigger. This is not requested at the moment and then it is better to choose 16 channels per DMU which reduces the dead area in case a DMU goes dead.

The DMU part of the digital CHIP should be very similar to the DMU required for the TEC and we think it will be possible to use most of the design done for the pixel DMU also for that.

3.2.3 Operation and Performance

The basic functional principles of the pixel-pad readout were studied in bench tests performed in Lund. A MWPC with the same 4-mm wire spacing as PC1 was equipped with a cathode plane (2-mm distance to wires) segmented in small rectangular pads as shown in Fig. 3.21. When operated with P10 gas, the chamber was thin enough to allow electrons from a Sr source to pass through the chamber as well as the cathode plane and the entrance/exit windows. The only electrons producing a trigger were the ones in the collimated (1 mm circular) beam from the source. These had high enough kinetic energy to produce a coincidence between a thin (0.1 mm) and a thick scintillator on the opposite side of the chamber. Thus, the electrons producing a readout trigger were simulating the dE/dx of a minimum-ionizing particle (mip).

Each pad was read out and software simulated the connection of pads to form the pad structure of the pixel-pad system (i.e., software added Cl + C + Cr in Fig. 3.21). Software was also used to apply a threshold, which simulated the discriminator level.

Figure 3.22 shows the pulse-height spectra of each individual pad when the source is positioned in the center of pad C. The requirement that three pads should always be fired is obviously well fulfilled, since the distributions are shifted away from zero for the three pads closest to the source. It is evident that it is possible to define a threshold which sets the three middle pads true and all others false. In this case the hit would be classified as being in the center of the pixel defined by the three fired pads. In the few cases when a neighbor

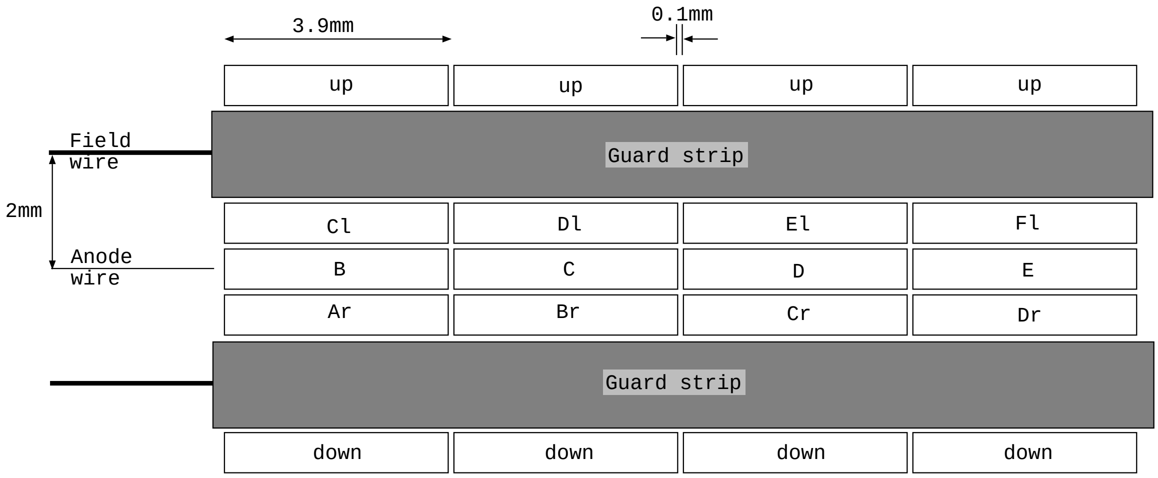


Figure 3.21: Schematic of the pad configuration in the Pixel test chamber.

pad along the wire becomes true, the maximal error would be made and the hit would be reconstructed with an offset of 2 mm. When there is crosstalk to pads under the neighboring anode wire, the hit would be treated as logically incorrect. In reality, such crosstalk events will be accepted as valid hits with a special flag indicating that this may be a hit right between two neighboring pixels (across the wires).

The least favorable case occurs when a hit is between two pads along the wire. When this happens, the charge is shared among a maximum number of pads producing the minimal pulse height, which determines the threshold setting.

Figure 3.23 summarizes the position reconstruction when the source has been moved in steps of 0.5 mm from the center of one pad to the center of the next pad. The figure shows the difference between the reconstructed position and the position of the collimated source. Evidently the hit is always reconstructed to better than ± 2 mm and the width of the distribution is about 1 mm. The position resolution is actually even better, because the collimator has an opening diameter of 1 mm.

The reconstruction efficiency was tested for different thresholds and found to be stable for variations of the threshold by at least a factor of three. The absolute efficiency is difficult to measure with a beta source, but the results indicate an efficiency close to 100%. This implies that the system should perform well with moderate demands on resolution in the electronics readout, and that a rather large variation in gas gain over the area of a chamber can be tolerated. The test results are very promising. The position resolution should be substantially better than ± 2 mm, which was the design criterion for PC1.

We plan to fabricate a full size prototype, one octant of PC1, to evaluate the performance and reliability of the system. Within a year we hope to construct a full-length readout chain equipped with prototype ICs. Construction of a full sector would require actual fabrication of integrated circuits and would need about another half year of work. The prototype studies can be made with the existing ICs. This would allow the prototyping to run considerably

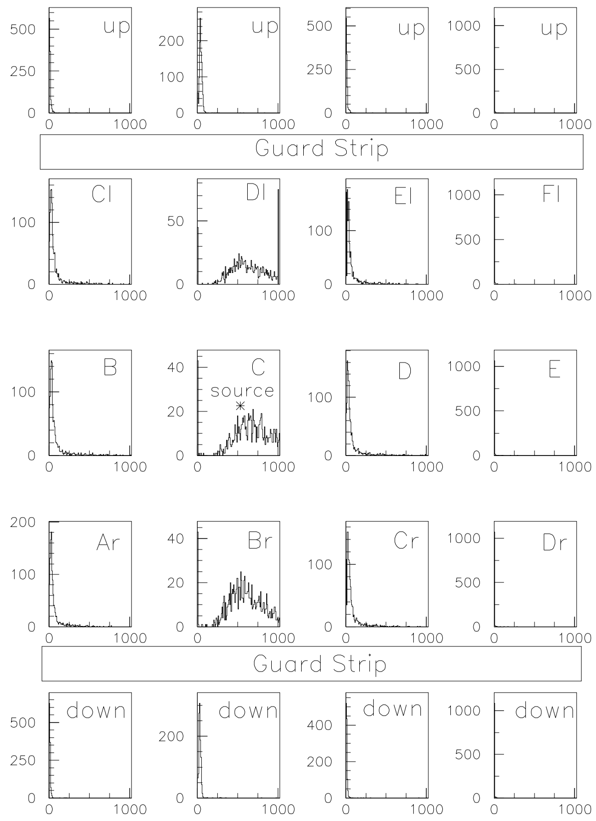


Figure 3.22: Pad pulse height spectra created with source placed at center of pad C.

faster, but the cost and technical feasibility of this option must be carefully evaluated.

A detailed Monte Carlo study was begun to develop the pixel-system software and to investigate the two-track separation. The pulse height and charge-distribution results were tuned to the test measurements. The first studies indicate that when the distance between the hits is 4 mm, a double-hit is identified in 50% of the cases. At 10 mm the two-track reconstruction is almost perfect, as long as all particles are minimum ionizing. A realistic dE/dx mixture from particles with different energies gives very little difference in the reconstructive efficiency and position resolution. There is only a small increase in the number of hits flagged as possible double hits.

For the LVL-2 trigger it should be possible to identify the specific pixel hit (4×4 mm^2 square in PC1) and to flag it as either definitely a single hit or possibly a double-hit. For the LVL-1 trigger it should be possible to provide coarse position information, which could be combined with the EMCal electron trigger and possibly with the RICH signal. For LVL-1 the position resolution achievable (several cm in PC3) is limited by the maximum possible number of detector leads.

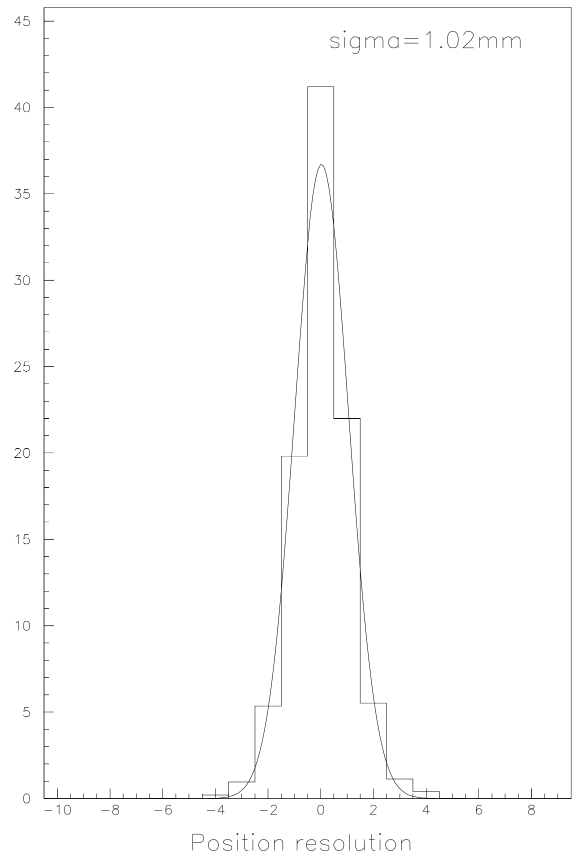


Figure 3.23: Pad position resolution. A collimated source has been moved in 0.5 mm steps between two pads. Reconstructed position minus source position has been plotted and a resolution of ∼1 mm *rms* has been obtained.

Prototype

Our strategy for the prototype work is the following. Up to the level of about 100 CHIPs (1600 channels) one can get the CHIPs without going to Silicon production. Going to production is a very expensive step, in particular since we have to do it on two CHIPs. We also think that at the time we have to go to fab for the full scale prototype (summer 94) may be too early to settle the final design since we are maybe a year ahead most other CHIP projects in PHENIX. A change at that stage means that we have to pay costs of transfer to production once again.

The reasons to build a full scale prototype were two: a;to verify the feasibility of the cathode board and the chamber performance, b; to get a large enough number of electronics channels in operation so we gain experience with the failure rate.

Aiming at a system that can be repaired during monthly shutdowns we think that we can relax a little on the latter point and that we can learn enough about reliability from a 1600 channels system. Tests of fabrication and operation of a large chamber are still desired but the readout can be done with the 1600 chips system by moving the readout boards around to different positions on the chamber.

So, we think that we will put the emphasis on the tests of the 100 CHIPs system so that the final decision about pixels can be based on that.

Bibliography

[1] B. Yu, Ph. D Thesis, University of Pittsburgh (1991); BNL Internal Report 47055 (1991).

[2] R. Debbe et al. IEEE Trans, in Nucl. Sci. **37**, 82 (1990).

[3] J. Fischer et al. IEEE Trans, in Nucl. Sci. **37**, 89 (1990).

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