Meeting Notes 3/13/01

Padova (Stefania, anyone else?) are tentatively scheduled to come to LBL on April 17 to begin layout of the back-end circuits.

We will have our first design review on April 26 and 27 at LBL. The goal will be to have our designs done at the schematic level, with simulation results available for all the major subcells. Maurice suggests any schedule changes be decided by the outcome of the design review. A list of items needed for the review will be provided by LBL.
Editorial comment: LBL should provide this list by the next meeting time (1-2wks), or at the next meeting (i.e. transparencies and hardcopies of schematics, plots of critical simulations with explanation, overview of cell function, design approach etc.), as well as a general format and schedule for the review.

Padova has a concern about the total propagation delay of 17ns for the worst-case readout scenario. Although there are 40 ns available (25 MHz read clock), the concern is that wiring loading delays will increase this value substantially. Padova felt they may need to change the design. Brad felt that the interconnects would not add significantly to the delay, and that they should be checked before starting on a different design. Henrik suggested calculating the capacitance of the metal interconnect, and modifying the delay value in the verilog model to reflect the sum of the interconnect load and the gate delay, as a method for checking. Padova will send verilog description of their circuit to LBL.

The cells for which each group are responsible were confirmed. LBL is doing the frontend, ADC, bidirectional pad drivers, and config register. FNAL is doing all the pipeline (control, analog pipeline, bias). Padova is doing the remaining I/O control (mode, readout, and neighbor logic, as well as the FIFO, counter and ADC latch).

FNAL would like to have power estimates for the standard cells from LBL if available. FNAL has "Pixel" library.

Ray Yarema reported that Tom Zimmerman had not yet started work on the pipeline because his previous commitment was running longer than expected. Ray said that as soon as he had all the required personnel working on this project he would be able to make a detailed schedule for the pipeline work. As a rough estimate he said that the complete pipeline layout may be done by the end of June, 2001.

Marc presented results of the frontend testing. Four chips were tested so far. Overall their performance is encouraging. The bias voltages of the chips agree with each other and the simulations to within a few per cent or better. Two chips show a problem with a CMOS receiver but are fine otherwise. The gain of the amplifier is less than expected by a factor of ~4 since the size of the feedback capacitor in the layout (and chip) was found to be ~800 fF instead of the 200 fF assumed in the simulation. The rise times are short as expected and the band width bits work properly (with exception of chip I). A possible leakage effect across the reset switch was observed for two chips but not for chip IV.