STABILITY, YIELD AND EFFICIENCY OF CdS/CdTe DEVICES

September 2001 - September 2004
Thin Film Partnership Program
Subcontract ADJ-1-30630-07
National Renewable Energy Laboratory

Final Report

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1. SUMMARY

Under this thin film partnership program (TFPP) project, significant scientific and technological advancements have been made for CdTe thin film photovoltaics (PV). Excellent progress has been made in demonstrating consistent device performance, particularly device stability. Major results have been shown in the areas of device characterization, experimental infrastructure improvements and processing larger area substrates.

1.1. Device Stability

We have made significant progress towards demonstrating consistent stability (resistance to degradation) for thin film CdTe photovoltaics. We have repeatedly shown that devices with good stability can be produced if processed at the right set of conditions. Small changes in processes can lead to significant differences in device stability. Among the processing steps for fabrication of CdTe devices, the $CdCl_2$ treatment and back contact processing have the most effect on performance. A quality control metric has been developed to predict the stability of devices utilizing simple photovoltage measurements at the time of device fabrication. Accelerated stress testing and the exposure of devices to outdoor conditions are ongoing. Extremely long duration stress testing (65°C, open circuit conditions for ~20,000 hours with 5 hours of illumination out of 8 hour cycle) has demonstrated that the rate of efficiency loss levels out with final efficiencies in the range of 8.5% ~ 9.5%.

1.2. Device Characterization

In an effort to improve the understanding of device performance, we have characterized our devices by a variety of analytical techniques in collaboration with many research groups. Among the methods used to study the electronic structure of our devices, the thermal admittance spectroscopy (TAS) and transient ion diffusion (TID) techniques have been the most fruitful. TAS studies have demonstrated that the devices with optimal $CdCl_2$ processing have lower measured defect concentrations. There is an initial correlation between lower measured defects and better stability. Capacitance studies and SIMS analysis have demonstrated that there is doping at the back of CdTe due to the copper based back contact processing and that there is little change in this copper distribution with stress (65°C, open circuit conditions for ~3,000 hours with 5 hours of illumination out of 8 hour cycle)

1.3. Improvements and Advancements in Experimental Infrastructure

Significant improvements have been made to our laboratory's research capabilities. The pilot system for CdS/CdTe PV fabrication has been upgraded. New hardware designs suitable for conditions seen in industrial production (long duration continuous operation of 16+ hours) have been implemented. We have identified an optimum baseline process condition for the fabrication of CdTe PV using the new hardware. The baseline absorber/$CdCl_2$ process has run for over 9 hours of operation with the same source charge. During these runs, the Voc and Jsc of devices with no intentional copper (fabricated up to but not including the back contact processing) have remained consistent. Current efforts are underway to advance the back contact processing to this level of consistency for long duration processing. Device testing facilities have been improved with: (1) more accurate, faster current-voltage (J-V) measurement systems; (2) the addition of capacitance measuring

and cryostat hardware; and (3) the construction of fixtures for exposing devices to indoor accelerated stress and outdoor conditions.

1.4. Large Area Processing and Joint Venture Development

The pilot system with the improved hardware will allow the processing conditions and device results to be directly applied to processing systems for large area substrates. Design and construction activity for a prototype manufacturing system with a nominal capacity of 2 MW/year is currently underway, supported through DOE-EERE. The deposition of device quality CdTe films on 16x16 inch substrates has been demonstrated. Significant progress towards developing a joint venture has been made with National Starch and Chemical (NSC), the US subsidiary of the ICI Group (an international chemical and technology company with approximately $10B annual turnover). The joint venture would manufacture and bring CdTe PV to market utilizing our technology. NSC is contributing significant cost share to the DOE-EERE project to complete the 2 MW prototype manufacturing system.

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2. INTRODUCTION

The goal of this research was to develop a detailed understanding of process/device stability, efficiency and yield. This understanding has led to the demonstration of consistent performance when devices are exposed to accelerated stress and outdoor conditions (stability). Devices are processed with a unique, continuous, in-line pilot system. The pilot system enables unique processing steps and conditions not available with batch processing and allows the fabrication of a large number of devices. Results from the pilot scale system are applicable to systems processing larger areas.

2.1. Pilot System

The pilot scale system is a continuous, all in-line system where all device fabrication steps are performed in one vacuum boundary. These processing steps include glass heating, CdS and CdTe deposition, $CdCl_2$ heat treatment, back contact formation and back contact heat-treatment. The system operates at 40m Torr N_2. The required base pressure for the system is only 10^{-4} Torr, allowing the use of low cost hardware. A residual gas analyzer (RGA) is used to monitor chamber gas composition. Process stations are nearly identical in design and construction. A schematic of the pilot scale is shown in Figure 1.

An automated conveyor belt extends from air, through all the processing stations in vacuum and then back to air. The cycle time of each process station is 2 minutes, thus one substrate emerges from the system every 2 minutes. Currently the substrate size is 3.6 x 3.1 inches. The pilot system has been used to process over 4000 films and devices.

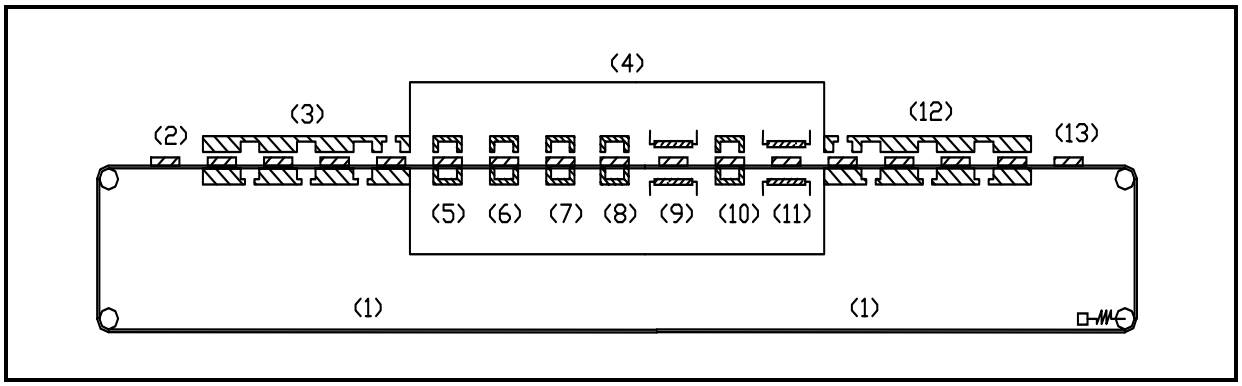


Figure 1: Schematic of the pilot system for CdTe PV fabrication, (1) belt conveyor, (2) glass substrate, (3) Air to vacuum to air (AVA) seal, (4) vacuum chamber, (5) heating module, (6) CdS deposition, (7) CdTe deposition, (8) $CdCl_2$ deposition and heat treatment, (9) $CdCl_2$ annealing and stripping, (10) back contact formation, (11) contact annealing, (12) AVA seal, (13) completed cell

2.2. Initial Device Performance

Devices have consistently been fabricated with 10.5 to 12.5% conversion efficiency with an NREL verified 12.44% with 71% fill factor. The highest efficiency measured on the devices produced with the pilot system is 13.0%. The device structure is glass/SnO_x:F/ CdS/CdTe/carbon/nickel. The substrates are soda lime glass with the tin oxide coating from Pilkington (TEC 15); the tin oxide is unmodified. These devices had no anti-reflection coating. The back contact is formed in vacuum through the vapor deposition of a copper compound followed by annealing [Barth 2002]. Metallization (carbon and nickel) is performed by low cost spray processing outside of vacuum.

3. UNDERSTANDING DEVICE STABILITY

3.1. Results of Ongoing Stability Testing

The ability of devices to withstand exposure to accelerated stress or outdoor conditions is "device stability". The stability of approximately 500 devices, processed at different conditions, has been studied. The stability of devices processed at optimal conditions is very promising. The stress conditions typically consist of 1 sun illumination, 65º C, open circuit conditions (OC) with 5 hours of illumination out of an 8 hour cycle. Devices are also subjected to 77º C, 100º C and outdoor conditions. Many tests are continuing.

3.1.1. Device Stability for Indoor Accelerated Stress Testing

The stability performance of devices fabricated at the optimum process conditions (to date) and subjected to indoor accelerated stress is shown in Figure 2. These two groups of devices were fabricated in two different process runs (runs 65 and 66). The fabrication process parameters including source temperatures, substrate temperatures, and lot numbers of source material were kept identical for both runs. Each group is from the same substrate. Both groups have lost approximately 10% of their initial efficiency after approximately 7500 hours of stress. This demonstrates that stability can be reproduced if process conditions are optimized and maintained. A plot of dV/dJ vs. the inverse current density in light (not shown) has no curvature indicating no evidence of the formation of a blocking contact during stress.

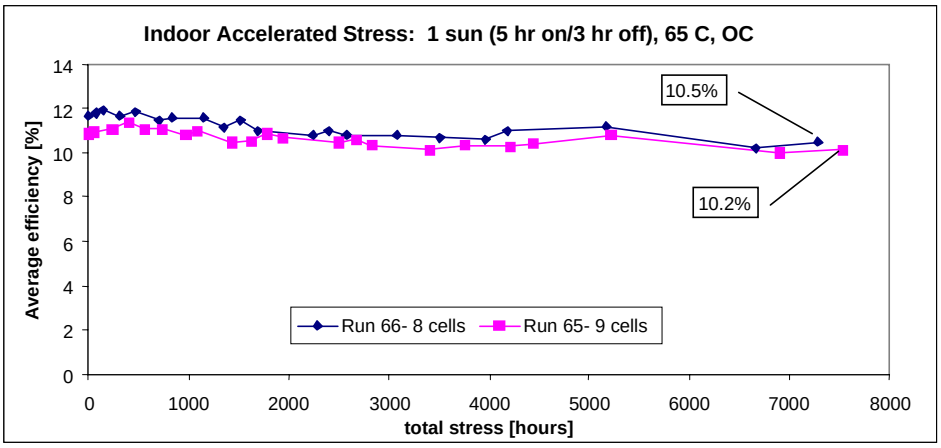


Figure 2: Stability of two groups of devices stressed indoors

3.1.2. Performance of Devices Subjected to Outdoor Conditions

Fixtures which allow devices to be exposed to the thermal conditions of encapsulated modules are utilized to study the performance of devices in outdoor conditions [Sampath 2002]. Figure 3 shows the device stability results for devices exposed to outdoor conditions using these fixtures

Devices produced at optimal conditions have been exposed to outdoor conditions at open circuit conditions for over **900 days with no significant change in efficiency**. This is referred to as "Type I behavior" [Barth 2002] and is shown by the 9 devices in Figure 3. There is a seasonal variation in efficiency with peaks occurring in the warmer summer months. Two of these peaks can be observed in Figure 3 at about 320 and 710 days

respectively. Certain devices processed at non-optimal conditions have demonstrated a current loss mechanism of degradation, referred to as "Type II behavior" (See Barth 2002 for more information). The 10 devices in the bottom 3 curves in Figure 3 demonstrate this behavior. One of the devices with a significant Type II behavior had much higher quantum efficiency (QE) at 800nm (≈ 30%) and a much lower QE at 600nm (≈ 7%). The loss of current and the differences in QE could be due to deep junction formation. The reason a device shows Type I or Type II behavior is due primarily to differences in the $CdCl_2$ treatment.

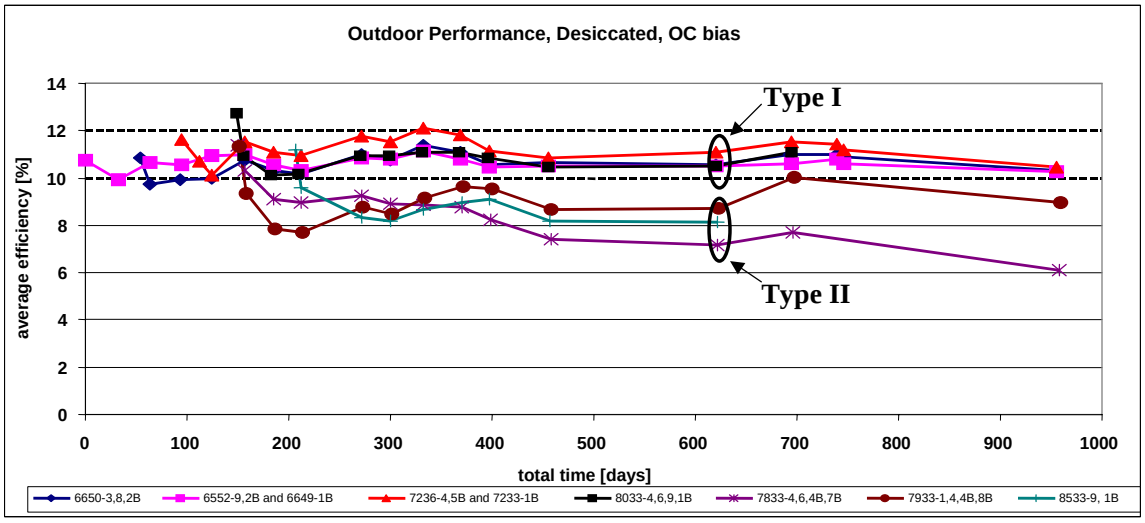


Figure 3 Updated outdoor performance

3.1.3. Indoor Accelerated Stress and Outdoor testing, Correlation of Performance

In order to correlate indoor and outdoor stability, it is beneficial to classify the overall behavior into two types, Type I: small decrease in efficiency versus time for long test time and Type II rapid decrease in efficiency versus time for short test time in both indoor stress and outdoor conditions. Type I behavior as shown in Figure 4 was achieved by running the process at optimal conditions.

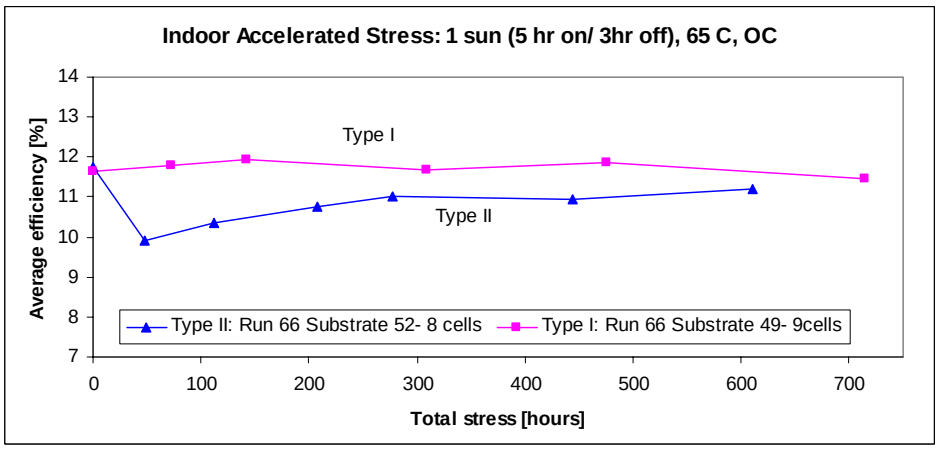


Figure 4: Comparison of Type I and Type II behavior for indoor accelerated stress testing

For Type II behavior, devices exhibit a decrease in efficiency in the early stages of both indoor accelerated and outdoor tests. The magnitude of the decrease is much higher

outdoors than indoors as shown in Figure 5. Type II device performance degradation is primarily due to a loss in J_{sc} for both indoors and outdoors. Tape peel tests demonstrated no loss of film or metallization adhesion in the stressed Type II devices. The loss of J_{sc} is due to a significant decrease in quantum efficiency at shorter wavelengths. Capacitance/voltage (C-V) analysis indicated that the doping in the CdTe had decreased significantly. In Type II behavior, the efficiency did recover in indoor stress testing, whereas such a recovery is not observed in outdoor conditions. It is important to note that the comparison of indoor to outdoor Type I and Type II behavior (Figures 4 and 5) show substrates from a single process run. These devices exhibiting Type II behavior had lower amounts of copper and lower substrate temperature during back contact formation. These variations were introduced intentionally during the processing.

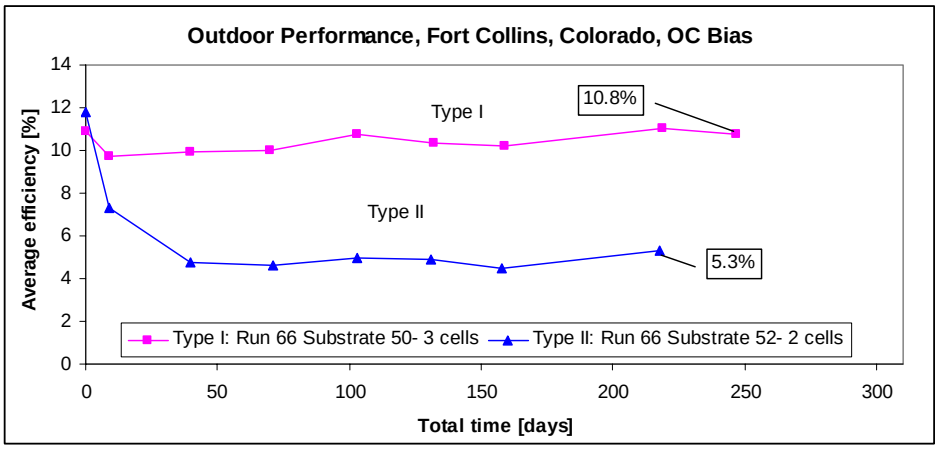


Figure 5: Type I and Type II behavior for outdoor exposure

For Type I behavior it may be possible to obtain an empirical acceleration factor between indoor testing and outdoor performance. But at the present time, the change in efficiency outdoors is insufficient to determine such an empirical acceleration factor. The indoor tests are useful to identify process conditions that do not result in Type II behavior [Barth 2002].

3.1.4. Performance of Devices Subjected to 100° C Stress

Many devices processed at different conditions have also been subjected to 100° C, 1 sun and open circuit stress conditions. It was observed that processing devices at optimum conditions can lead to good stability at both 65° C and 100° C. Figure 6 is an overlay J-V plot which shows the effect of 100° C stress. Initial efficiency for this cell was 10.9% and the final efficiency after 964.5 hr of stress was 9.4%. Other cells from the same process run showed similar stability. Thinner cells had a higher incidence of shunting when stress tested at 100° C versus 65° C or 77° C stress conditions. It was found that the Type II behavior was not observed during 100° C stress tests. Furthermore, the 100° C tests did not have the sensitivity to the differences in the $CdCl_2$ processing effects (please see section 3.4.1). As a result, 65 ° C, 1 sun illumination stress conditions are used to optimize the process.

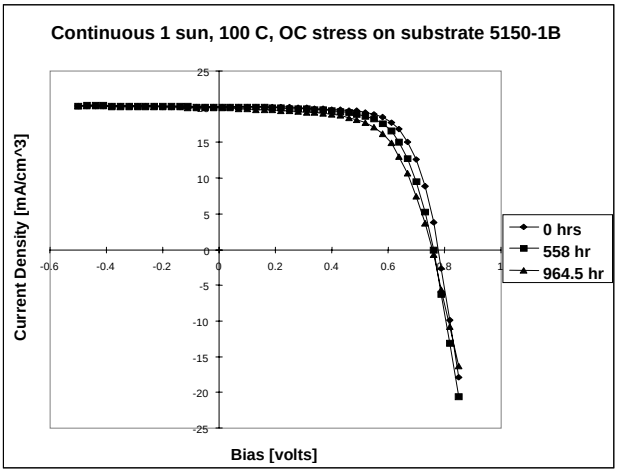


Figure 6: Overlay J-V plot of device performance under accelerated indoor stress

3.2. Development of a Quality Control Metric to Ensure Consistent Stability

The development of a quality control methodology to ensure consistent stability has been the focus of significant effort in this program. A relationship between initial, unstressed device performance and long-term stability has been established. The stability of devices with intentional copper under accelerated stress can be qualitatively predicted using light JV data from devices processed identically but without the intentional addition of copper. This relationship (shown in Figure 7) fits all relevant data for devices processed with the pilot system.

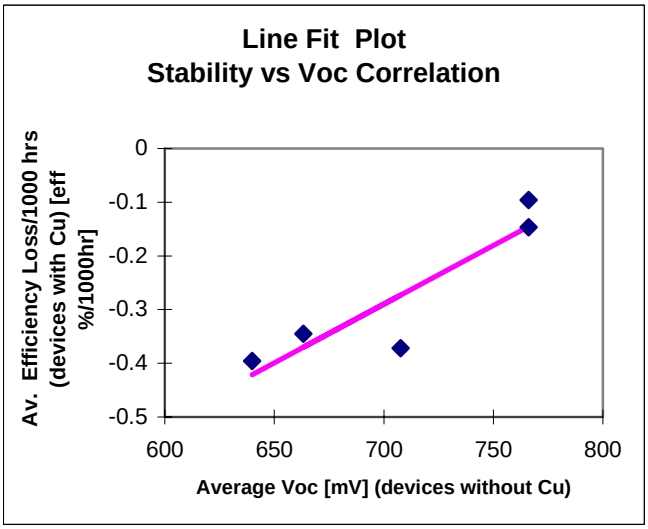


Figure 7: Stability (efficiency loss/1000hrs.) of devices with intentional Cu vs. open circuit voltage (Voc) (no stress) of similarly processed devices without intentional Cu. Devices are stressed at 65°C, open circuit bias, one sun illumination with 5 hours of illumination out of a 8 hour cycle. 5 process conditions and 24 devices are represented. Linear correlation coefficient for line fit is 0.91.

Figure 7 shows the relationship of the stability of fully processed devices (with intentional Cu) versus open circuit voltage for similarly processed devices without intentional copper. Higher open circuit voltage leads to better stability. The lower Voc indicates defects in the device cause device instability, probably through defect migration or defect transformation.

The voltage measurements can be performed directly on the CdTe surface. Good results have been obtained without metallization. A carbon pad and simple digital voltmeter

are utilized. This is a very advantageous quality control metric. This technique could be automated for manufacturing to ensure the production of devices with consistent stability (<10% efficiency drop at 65 °C, one sun, open circuit bias conditions for 1000's hours).

Figure 8 shows the plot of short circuit current vs. open circuit voltage for devices processed without intentional copper and measured before application of stress. The devices denoted by the blue diamonds (6430 and 31) show the highest combined Jsc and Voc. Figure 9 shows the stability of devices processed nearly identically to those in Figure 8 except for the intentional addition of copper to form the back contact. (Similar process conditions are denoted by the same color and point shape in both Figures 8 and 9) As seen in Figure 9, the most stable devices are those with the blue diamonds (6652 and 6549) which, except for the intentional addition of copper, are nearly identical to 6430 in Figure 8. Similarly, the Jsc and Voc for other devices in Figure 8 are predictive of the stability performance shown in Figure 9.

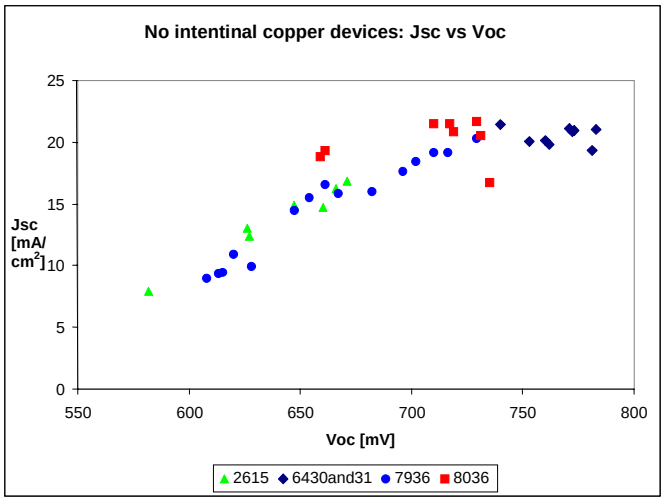


Figure 8: Short circuit current (Jsc) vs. open circuit voltage (Voc) of devices without intentional copper measured at simulated AM 1.5 illumination. All measurements were taken before stress.

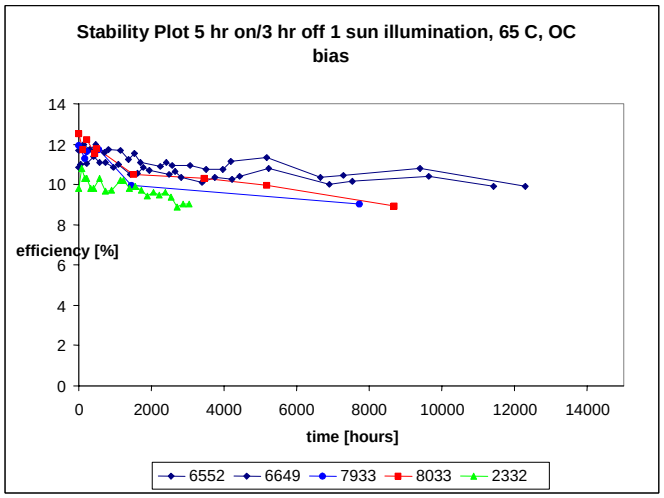


Figure 9: Stability of devices with intentional Cu but otherwise identical to devices shown in Figure 8. Devices are stressed at 65°C open circuit bias, one sun with a cycle of 5 hours of illumination out of an 8-hour cycle.

In contrast, the initial performance of devices made with intentional copper is not as predictive. Figure 10 shows the Voc vs. Jsc of devices processed at similar conditions with the devices of Figure 8 except with intentional copper. Similar process conditions are denoted by the same color and point shape in Figures 8, 9 and 10. Comparing Figure 8 and Figure 10 demonstrates that the Voc and Jsc of the devices without intentional copper are more effective at predicting device stability.

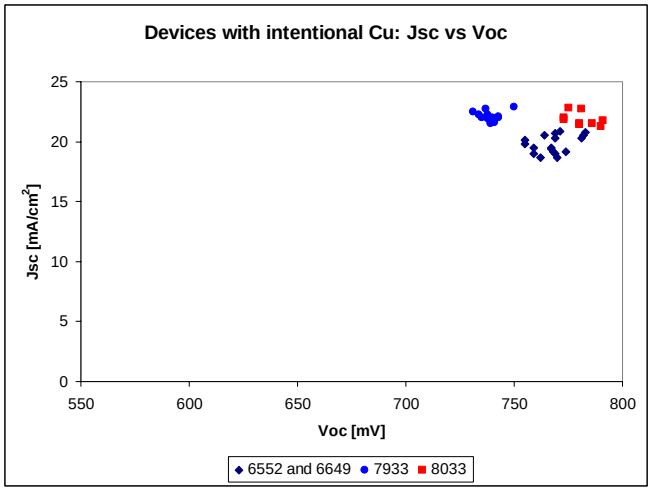


Figure 10: Short circuit current (Jsc) vs. open circuit voltage (Voc) of devices WITH intentional copper measured at simulated AM 1.5 illumination. All measurements taken are before stress.

3.3. Very Long Term Stability Testing

Some of our devices have undergone accelerated stress testing for almost 3.5 years. The stress conditions are 65° C, ~ 1000 W/m^2 illumination (cycled 5 hr. on/ 3 hr. off), open circuit bias, with a desiccated ambient. The efficiency loss follows an exponential decay described by the function:

$$\eta = \alpha \cdot \exp\left(\frac{-t}{\lambda}\right) + \eta_{level} \qquad [1]$$

For the first ~10,000 hours of light soaking the efficiency loss over time is relatively rapid. At approximately 20~25,000 total hours, the efficiency loss levels. The data of average efficiency vs. stress time is shown in Figure 11 along with the calculated exponential decay curves. The curve fits are statistical and no degradation mechanism is assumed. The curve fit correlation parameters (a measure of how accurately the curve approximates the data) ranged from R = 0.86 ~ 0.99 for the fits shown. Calculated constants for the exponential decay function [1] are listed in Table I.

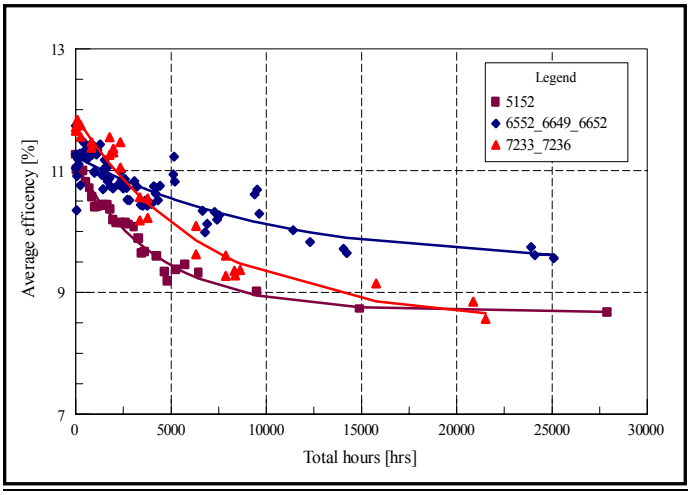


Figure 11: Long term stability plot. Each curve represents an average of at least six devices (total of 45). The data was smoothed using a Savatzky-Golay 4th order polynomial routine.

Substrate	α	λ	η level [%]	Δη [% of initial]
5152	2.43	4329	8.7 ± 0.17	-21.9
6552,6652, 6649	1.78	10140	9.5 ± 0.57	-14.3
7233, 7236	3.37	6853	8.5 ± 0.44	-28.3

Table I: Calculated constants for exponential decay

The very long term performance depends on device processing conditions. The different curves in Figure 11 show the results for three different $CdCl_2$ process conditions. JV parameters for selected devices shown in Figure 11 are given in Table II. As can be seen, the main changes in JV parameters are an increase in Roc and a decrease in fill factor. There is also a slight decrease in Jsc but essentially no change in Voc. Analysis of dV/dJ vs. 1/J+JL curves (not shown) presents no evidence of curvature of formation of a blocking contact.

Cell	Voc [volts]	Jsc [mA/cm^2]	ff [%]	eff [%]	Roc [ohm cm]	Stress hours [total hours]
6649-7B	768	20.33	73	11.34	0.87	0
6649-7B	763	19.80	63	9.53	2.76	23908
7233-2	729	22.67	69	11.33	0.42	0
7233-2	726	20.44	56	8.37	2.80	20866

Table II: JV parameters of selected devices from Figure 11 before and after stress of 65° C, one sun illumination (5 hr. on/ 3 hr. off), open circuit

Maintaining devices at open circuit during stress testing (the condition of the devices in Figure 11) is generally considered to be the most severe condition; it is expected that devices operating in the field (at max. power conditions) will have superior performance [Hiltner 1999]. The stability of devices in outdoor conditions continues to be monitored. However, the degradation outdoors after over 2.5 years is too small to develop a statistically valid correlation between the accelerated stress and outdoor conditions (if any).

3.4. Effect of Processing Parameters on Device Performance and Stability

It has been observed that small changes in processing conditions can have a significant effect on initial device performance and stability. During the course of this research it was found that the $CdCl_2$ process had a very significant influence on device performance.

3.4.1. $CdCl_2$ Processing Effects on Device Initial Performance and Stability

The effectiveness of the $CdCl_2$ treatment has a very strong effect on initial efficiency and long-term device performance under stress. In our chloride treatment process, a $CdCl_2$ film is deposited, annealed, and then the film is removed by precise control of the substrate temperature. Careful control of the substrate temperature to reduce substrate heating after removing the $CdCl_2$ film has been found to be critical to stability.

During the course of this research over 50 separate processing runs were performed to determine the optimal chloride process conditions and to increase the understanding of how the chloride process relates to stability mechanisms. Figure 12 shows the range of initial device performance that can be seen for devices processed similarly except for changes in the chloride processing.

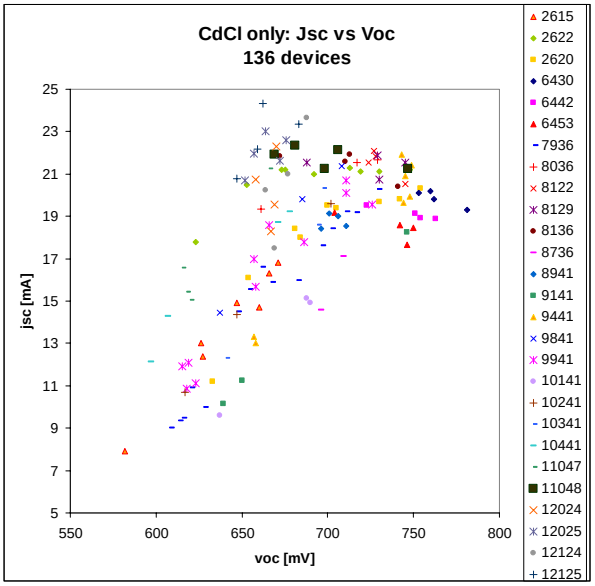


Figure 12: Short circuit current (Jsc) vs. open circuit voltage (Voc) of devices without intentional copper showing the effect of the $CdCl_2$ processing on initial device performance.

Figure 13 shows the effect of $CdCl_2$ treatment on device stability. A significant increase in series resistance is seen over time with non-optimum $CdCl_2$ treatment. All the devices in Figure 13 have similar back contact but slightly different $CdCl_2$ treatments. The differences in the stability were due to changes in $CdCl_2$ flux during processing due to a subtle alteration of the source charge conditions and minor changes in processing temperatures. The better devices received higher $CdCl_2$ vapor flux. However, higher flux is beneficial only to a certain level.

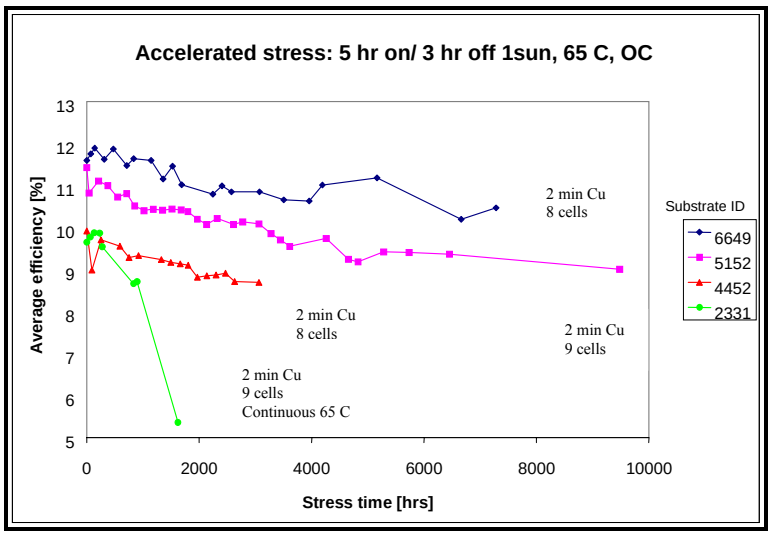


Figure 13: Effect of $CdCl_2$ treatment on stability, each line is an average of at least 8 cells all with the same back contact; stress condition: 1000 W/m^2 (5 hrs on out of 8 hr cycle) illumination, OC bias, 65 C temperature.

3.4.2. Back Contacting Processing Effects on Device Stability

Figure 14 shows the effect of back contact processing variation on stability. Non-optimum conditions lead to a significant increase in the series resistance and JV rollover is seen under light. As can be seen in Figure 14, the higher starting efficiencies do not always

correlate to better stability. Furthermore, we have observed that there is an optimum amount of copper for producing stable devices.

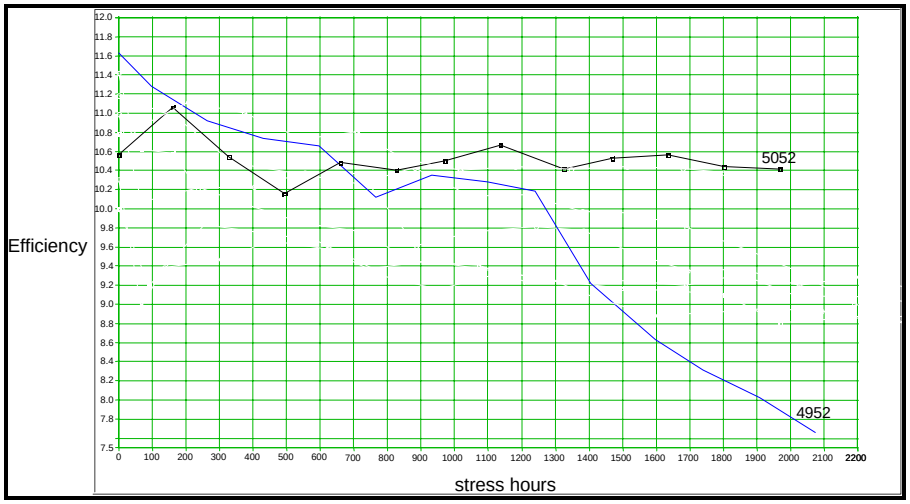


Figure 14: Effect of copper based back contact processing conditions on otherwise similarly prepared and stressed devices. Each line is average of 9 devices from same substrate, stress condition: 1000 W/m^2 (5 hrs on out of 8 hr cycle) illumination, OC bias, 65 C temperature.

3.4.3. Effect of Adsorbed Gasses on Device Stability

As demonstrated above in Figures 2 and 3, when processed at optimal conditions, good efficiency and stability can be obtained with Cu based back contacts. However, very controlled processing is critical for obtaining these results. In one example with our devices, processing was halted after the chloride treatment (before back contact formation) and the device was exposed to air briefly (a few minutes). Following this, our standard contact was fabricated in vacuum. The initial efficiency and the subsequent stability of these devices was significantly worse than the results without the exposure (other deposition parameters were held constant). Starting efficiency (average of 9 devices) with air exposure was 9.6%, compared to average starting efficiency of 11.2% for devices with no air exposure. Adsorbed gases and oxides modify the formation of the back contact.

3.4.4. Effect of Film Thickness on Device Performance

In addition to controlling the $CdCl_2$ treatment and the processing conditions for the back contact, it has been observed that controlling and optimizing cadmium telluride thickness is critical. Variations in CdTe thickness can alter the effectiveness of the $CdCl_2$ treatment due to changes in the film volume needed to be treated. Variations in CdTe thickness can also change the doping profile in the device. Table III shows how, for our process, decreasing the device thickness improves efficiency. However, too small a thickness can cause current losses and device shunting. The only change in processing for the substrates 8433 and 8633 was variation in the CdTe thickness.

Substrate ID: 8433		*Substrate ID: 8633*	
Number of Devices	3	Number of Devices	3
Device Thickness	25 kA	Device Thickness	17 kA
Standard Deviation	0.4	Standard Deviation	0.74
Mean Efficiency	10.9	Mean Efficiency	11.7

Table III: Variation in average device efficiency with film thickness

4. ANALYTICAL STUDIES TO BETTER UNDERSTAND DEVICE BEHAVIOR

In order to develop a detailed understanding of the performance of our devices, the constituent films continue to be studied by X-ray diffraction (XRD), glancing angle XRD, XPS, and SEM SEM-EDS, ellipsometry, surface profilometry and UV-VIS-IR spectrometry at CSU. Devices produced by our process have been studied by SIMS, CL and DLTS at NREL; DLTS at Lawrence Berkley Lab; and glancing angle XRD at IEC.

The electrical properties of the devices are characterized through current/voltage (J-V), capacitance-voltage (C-V) and capacitance-frequency (C-F) techniques in our laboratory. A closed loop temperature controlled cryostat has been installed for measuring capacitance and other device properties in the dark at temperatures from 76K to 320K. This system has been used for measuring device capacitance as a function of temperature and applied voltage (C-V-T).

The most significant finding from these studies is that our back contact processing dopes the CdTe which assists in producing a low resistance back contact. Our back contact fabrication process utilizes no etching. Most other back contacts using copper have a separate p^+ layer, such as Cu_2Te or ZnTe:Cu. Analysis with glancing angle x-ray diffraction (GAXRD) and x-ray photoelectron spectroscopy (XPS) does not show the presence of a separate phase or a Cu_xTe layer at the back of our devices.

4.1. Copper Distribution Within the Device by SIMS

Secondary Ion Mass Spectrometry (SIMS) analysis of three of our devices was performed at NREL by Sally Asher. Two of the devices were fabricated during the same process run and fabricated under identical conditions including back contact copper processing. One of these devices was subjected to a significant amount of accelerated stress; the other saw no accelerated stress. The third device was from a different run but was processed similarly, except no copper was used in processing. The copper distribution of these three devices is shown in Figure 15. The SIMS analysis shows that there is copper in the CdS even when there is no intentional copper added during the processing. There is an increase in the Cu throughout the device with the sample containing intentional addition of copper. The largest increase is in the back approximately 0.4μm. Furthermore, Figure 15 shows that there is little change in the distribution of the copper profile after stress.

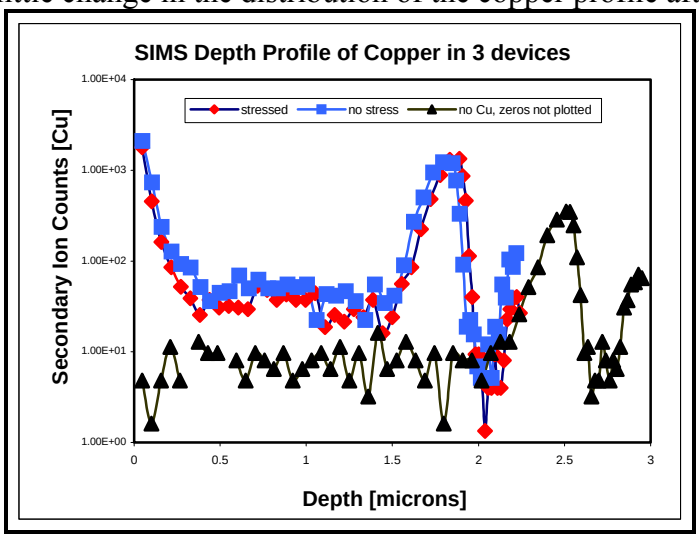
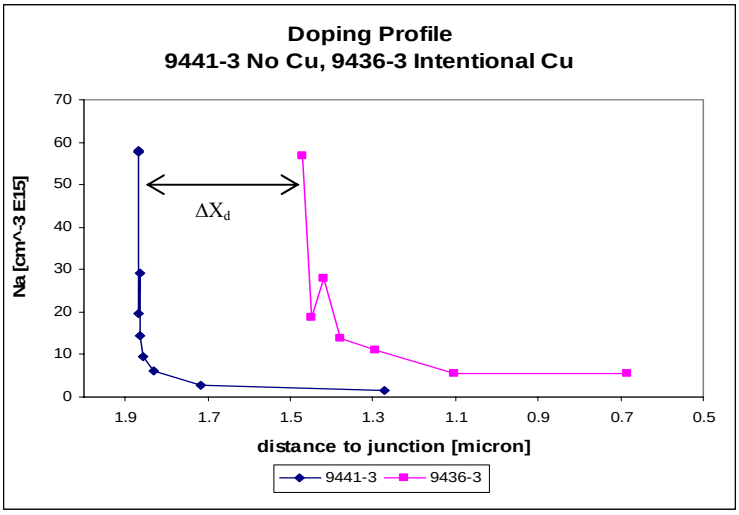


Figure 15: SIMS depth profile of nearly identical devices with and without stress. Stress condition: 3300 hours at 1000 W/m^2 illumination (5 hrs on out of 8 hr cycle), OC bias, 65 C temperature.

4.2. C-V Results for Devices With and Without the Intentional Addition of Copper

The doping profile from C-V analysis for devices with and without the intentional addition of copper is shown in Figure 16. The two devices were fabricated in the same process run. Surface profilometry measurements demonstrated that the samples within the run had the same thickness, within the error of measurement (0.05 μm). The decrease in the depletion width at reverse bias (ΔX_d) is a measure of the thickness of the doped region. This increase in dopant at the back of the CdTe is attributed to the large copper concentration near the back of the CdTe seen by SIMS analysis. The estimate of ΔX_d from Figure 16 is approximately 0.3 μm. This estimated thickness is similar to the thickness of the region with high copper concentration at the back of the device shown by SIMS in Figure 15. A similar variation in depletion width with the change in copper concentration for our devices has been reported previously [Sites 2002, Pudov 2002].



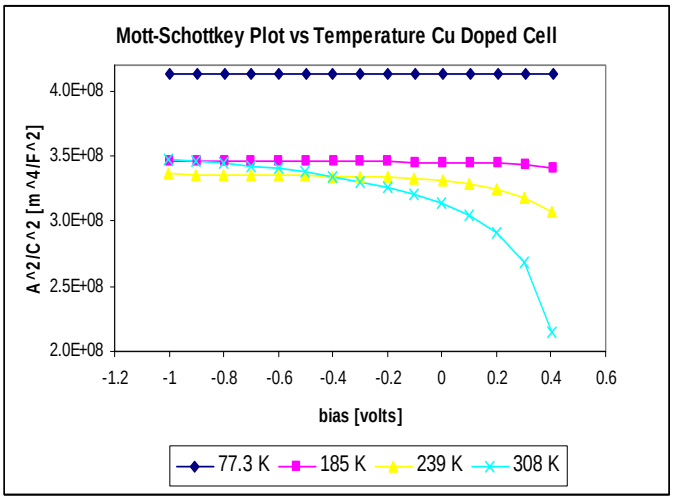
Figures 16: Doping profile of devices with and without copper

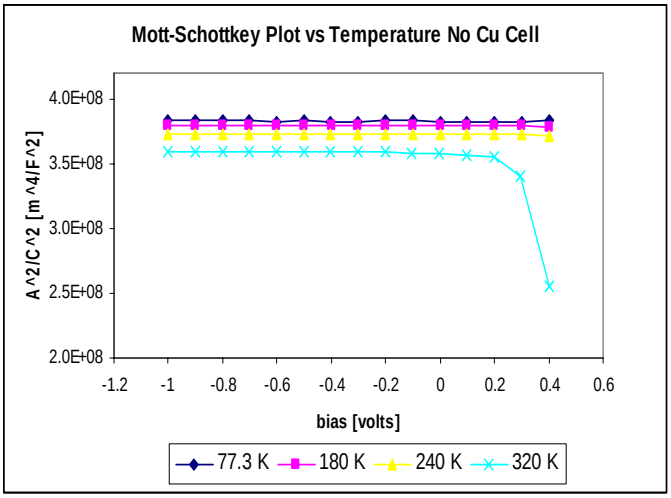
The total device capacitance is a combination of the junction and contact capacitance [Niemegeers 1997]. By assuming that the measured capacitance is attributed only to the junction capacitance (assuming no contact capacitance), the thickness of the CdTe region doped with copper (ΔX_d) is an underestimation. All C-V measurements are performed at the highest frequency where minimal frequency dispersion is detected in order to minimize or eliminate the contribution of traping states [Blood 1992, Mauk 1990].

4.3. C-V-T Results for Devices With and Without the Intentional Addition of Copper

In order to further understand the role of copper in our devices, capacitance-voltage profiling as a function of temperature (C-V-T) was performed on our devices. The Mott-Schottky plots as a function of temperature is shown in Figures 17 and 18. The depletion width in reverse bias at 77 Kelvin matches the thickness of the CdTe film measured through profilometer measurements. The capacitance measurements were done at 100kHz. Higher frequencies could not be used due to inductance of the relatively long leads of the cryostat. However, when the device with copper was tested outside the cryostat (with short leads attached directly to the device to minimize inductance), the difference in capacitance readings between 100kHz and 2.5MHz was only 6%. This validates the use of the lower frequency measurement. Capacitance vs. frequency measurements also show the device

capacitance is not strongly dependent on frequency at the 100kHz range. The increase of capacitance with temperature for the device with copper at the back of the cell is due to the activation of copper based dopants.





Figures 17 and 18: Mott-Schottky plots showing activation of copper based dopants with temperature

4.4. C-V Profile after Stress

The doping profile obtained by C-V measurements on the **same** device after different amounts of accelerated stress is shown in Figure 19. The CdTe thickness in this device, estimated from profilometry measurements, is 1.8 µm. The thickness of the doped region is approximately 0.35µm and as seen in Figure 19 there is very little change in the copper doped region with stress. (The differences are within the limits of measurement accuracy.) These results correlate with the SIMS result in Figure 15, which shows very little change in copper distribution with stress.

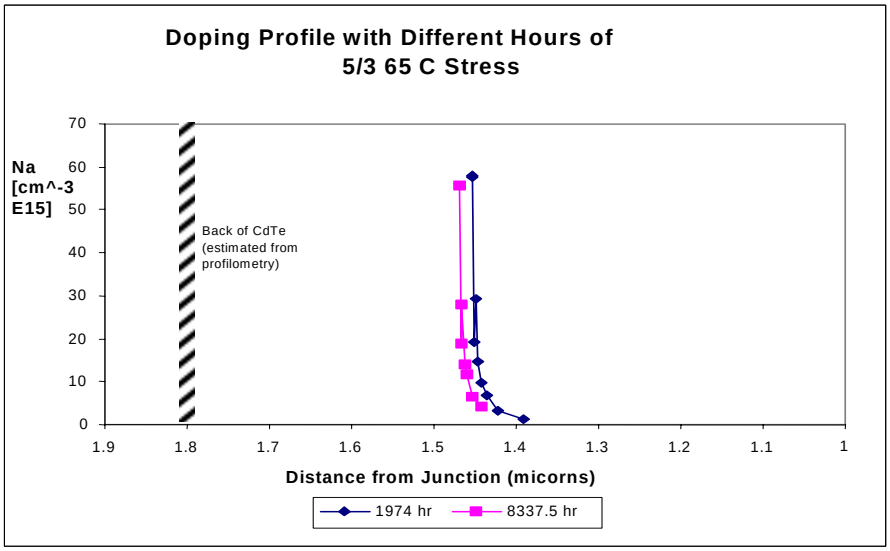


Figure 19: Acceptor density vs. distance from junction for a device with different hours of stress. Stress condition: 1000 W/m^2 (5 hrs on out of 8 hr cycle) illumination, OC bias, 65 C temperature

4.5. DLTS Studies

Analysis of our devices with deep level transient spectroscopy (DLTS) has been performed at both NREL and Lawrence Berkeley Lab. As shown in Table IV only electron type traps were detected at levels below $3x10^{13}$ cm^{-3}. According to Steven Johnston [Johnston 2002] of NREL these levels are a lower bound estimate. This is due to the possible incomplete filling of all of the traps and to the limited temperature range explored (100-300 Kelvin). Concentrations of traps where the trap peak was outside of the measurement temperature range were unresolved. The analysis of our devices using thermal admittance spectroscopy (TAS) has been more fruitful and TAS studies are described in the next section.

Substrate	Trap ID	Doping Density, Na [cm^{-3}]	Activation Energy, Ea [eV] Ec= energy of cond. band	Trap Density, Nt [cm^{-3}]	Technique
5151	E1	7.00E+13	Ec-0.39	3.00E+12	ODLTS
5151	E2	7.00E+13	Ec-1.5	8.00E+11	ODLTS
5151	Trap seen, peak beyond temp range studied		--	--	
7232	E3	1.00E+14	Ec-0.49	3.00E+10	DLTS
7232	E4	1.00E+14	Ec-0.75	6.00E+11	ODLTS
8734	Trap seen, peak beyond temp range studied		--	--	

Table IV: Trap density by DLTS and ODLTS

4.6. TID and TAS Studies

An automated technique for measuring Transient Ion Diffusion (TID) has been developed in our laboratory. The TID technique utilizes changes in devices capacitance in order to measure free ion density. The device capacitance is measured while the applied bias is varied. A Labview program has been developed to carry out the measurements and to calculate the free ion density and diffusion coefficient. This allows repeatable measurements of the density of free ions in the devices and to determine the diffusion coefficient of the ions [Lyubomirsky 1997].

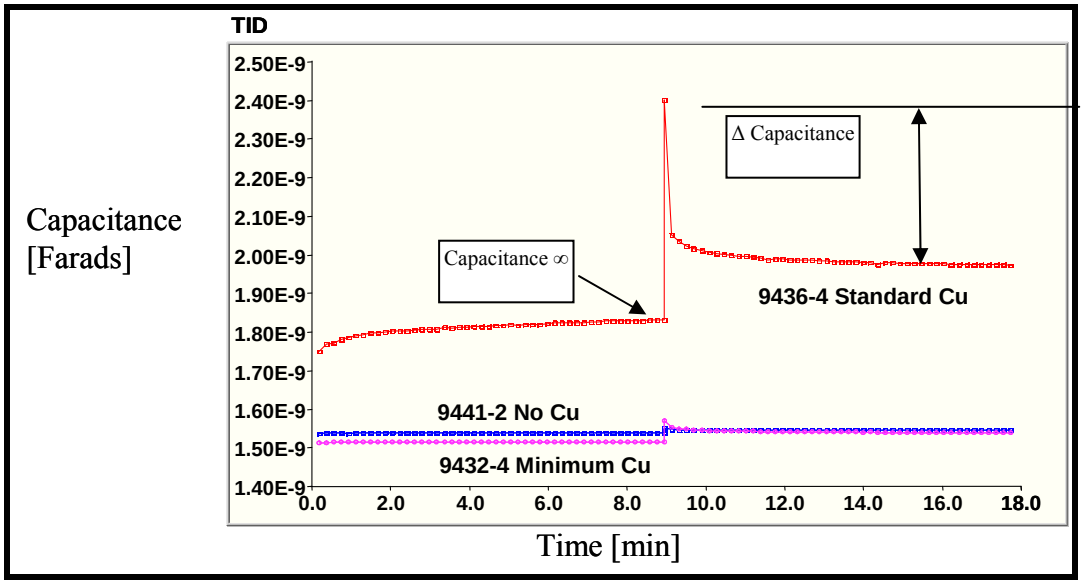


Figure 20: Transient ion diffusion measurements on devices with different amounts copper. Measurements taken at -2 V @ reverse bias, 0.02 V OSC voltage, 100 kHz frequency. The step in the capacitance occurs when the reverse bias is removed.

Figure 20 shows TID measurements for devices processed identically except for variations in copper concentration. The step in the capacitance is proportional to the quantity of copper present as interstitial Cu (Cu_i^+). The fraction of the copper present as Cu_i^+ is a very small fraction of the total copper in the device (< 10^{-4} of the total copper). The significant increase in the transient capacitance with increasing copper concentration indicates that copper can be present in ionic form. Measurement and control of ionic interstitial copper in CdTe is of interest because Cu_i is a donor and diffuses readily. Significant quantities introduced though non-optimal processing can degrade the p-type doping in the CdTe. Table V shows the variation in interstitial copper with different back contact processing.

Cell	$2\Delta C/C_?$	Ncu_i [cm^{-3}]
9441-4 No Cu	0.007	$9.8X10^{11}$
9432-4 Min Cu	0.041	$5.7X10^{12}$
9436-4 Standard Cu	0.47	$6.5X10^{13}$

Table V: Tabular data for Figure 20 and resultant interstitial copper concentration

A TAS analysis has been used to investigate trapping levels within the device. Different processing conditions result in different admittance spectroscopy results. Figures 21 and 22 are representative measurements for a device with less than optimal processing conditions. Figure 21 is a capacitance vs. frequency plot showing three different regions. Region 1 (denoted by the blue curves) is the back contact layer capacitance. This is also seen in Mott-Schottky plots at different temperatures. As temperature increases a "step" forms in the plot (Region 2) indicating a trap level within the device.

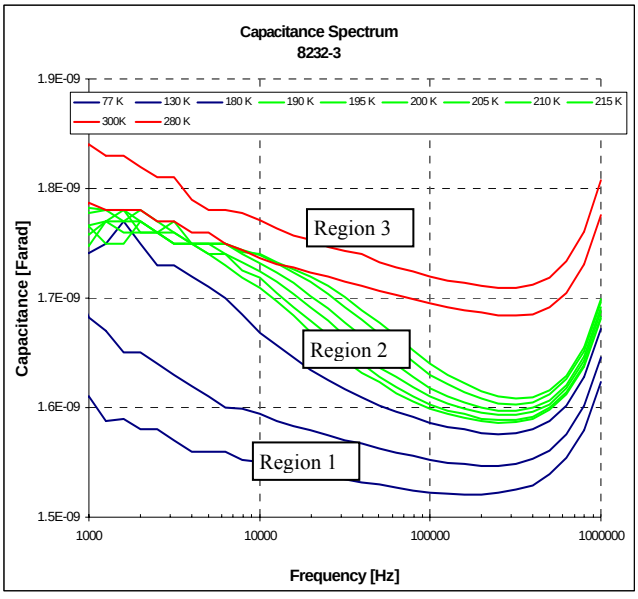


Figure 21: Capacitance vs. frequency plot. The step in region 2 of the plot shows evidence of a trapping state

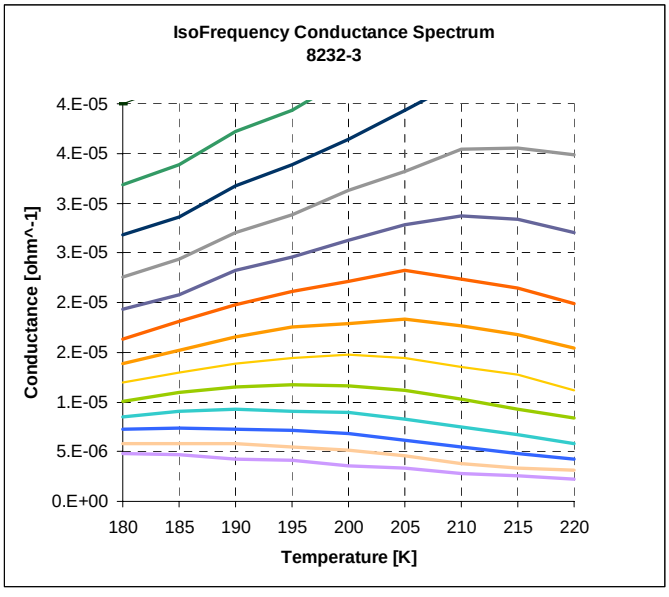


Figure 22: Conductance vs. temperature spectrum for same device as Figure 21. The conductance peaks indicate a trap level.

Further increasing the measurement temperatures leads to curves with a fairly uniform slope. More defects are thermally activated resulting in a more uniform distribution of defects at various energies (Region 3). A peak in the conductance vs. temperature plot (Figure 22)

indicates a specific trap level associated with Region 2. Devices with optimal chloride processing show little or no Region 2 steps and less dispersion in Regions 1 and 3.

The defect levels in our devices have been measured using TAS from 77K to 400K. The TAS technique has been applied to more than 15 devices made with various processing conditions. Data from the capacitance and conductance spectrums have been used to estimate the defect energy levels, apparent capture cross sections and the defect concentrations. Defects at many energy levels have been observed. The method used is outlined in Kneisel and Walter [Kneisel 2000, Walter 1996].

In short, the procedure involves utilizing the peaks from the normalized conductance plot as shown below in Figure 23 to find (temperature, frequency) pairs of peaks and construct an Arrhenius plot as shown in Figure 24.

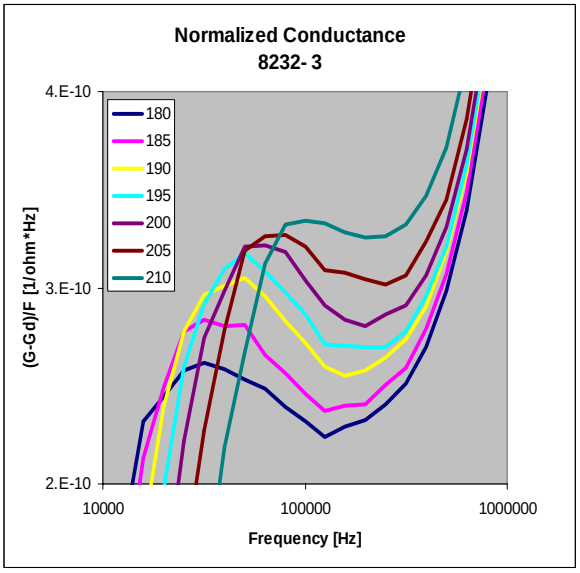


Figure 23: Normalized conductance (G-Gd/F), Gd is the DC conductance, inset shows temperature in °K

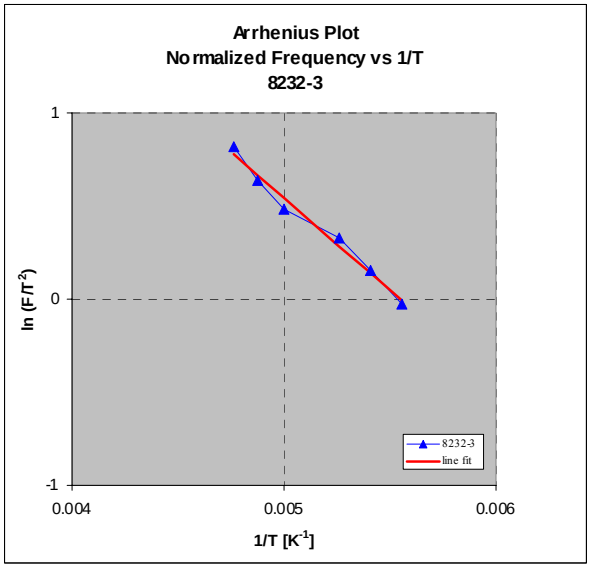


Figure 24: Arrhenius Plot vs. of normalized frequency vs. 1/T

From the Arrhenius plot the defect energy level and the apparent capture cross section can be estimated. Using these two parameters and the original capacitance spectrum it is possible to construct a density of states function (DOS) as shown in Figure 25. There is a clear peak at defect energy level (E_t) of ~ 85 meV.

The defect concentration (N_t) is estimated to be ~1.9 E14 cm^{-3}. A MatLab code has been developed to generate the DOS function. Figures 23, 24 and 25 show defects that result from non-ideal $CdCl_2$ processing. By comparison, the defect shown in Fig. 25 is not present in devices processed at optimum $CdCl_2$ processing. In TAS measurements, optimum $CdCl_2$ treatment leads to a lower density of defects at lower energies. Similar results have been reported [Laurenco 1999]. TAS studies of trap states show a potential Meyer-Neldel relationship (MNR) associated with variation in $CdCl_2$ treatment. In a MNR, the capture cross-section varies exponentially as a function of energy of a trap.

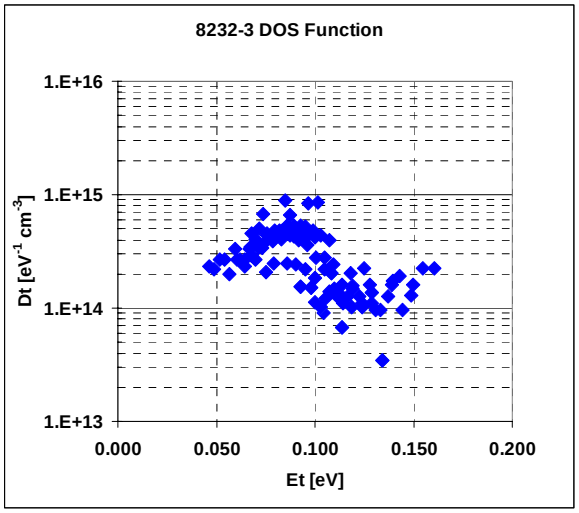


Figure 25: Density of states, D_t, as a function of defect energy, E_t

The results above show that TAS can identify single energy level defects in our devices. There are also signatures of extended defect distributions in the capacitance spectrums. Thus, TAS can be very useful in identifying defects associated with device processing. TAS has shown differences in devices fabricated with different $CdCl_2$ processing conditions, with and without additional Cu, and devices before and after accelerated stress.

Devices with poor $CdCl_2$ treatment and minimal Cu added during processing show a trap level of 140 meV energy, identified as M2. Devices with the complete Cu back contact process and with non-optimal $CdCl_2$ treatment have 4 times the M2 trap concentration. The initial efficiency of this device was approximately 10%. Devices with more optimal $CdCl_2$ processing have no trap levels detectable by TAS. The lack of detectable trap levels on our devices with good chloride treatment was confirmed by F. Seymour of CSM.

5. ADVANCES IN CdS/CdTe DEVICE PROCESSING/INFRASTRUCTURE

Significant effort has been devoted to advancing the process definition and hardware design to consistently fabricate CdS/CdTe devices with high efficiency and good stability over long duration processing.

5.1. Processing Advances

New hardware designs suitable for conditions seen in industrial production (long duration continuous operation of 16+ hours) have been implemented in the pilot system. The new hardware is functioning well. This hardware has been used to process hundreds of devices. A comparison of device performance (without intentional copper) between the new hardware and the old hardware are shown in Table VI. Process conditions, which lead to high Voc and Jsc values for devices without intentional Cu, result in good device stability when processed with intentional Cu (see section 3.2).

	Old hardware		New hardware	
	Voc [mV]	Jsc [mA/cm^2]	Voc [mV]	Jsc [mA/cm^2]
Mean	766	20.5	746	20.9
Standard deviation	13.8	0.7	16	0.4

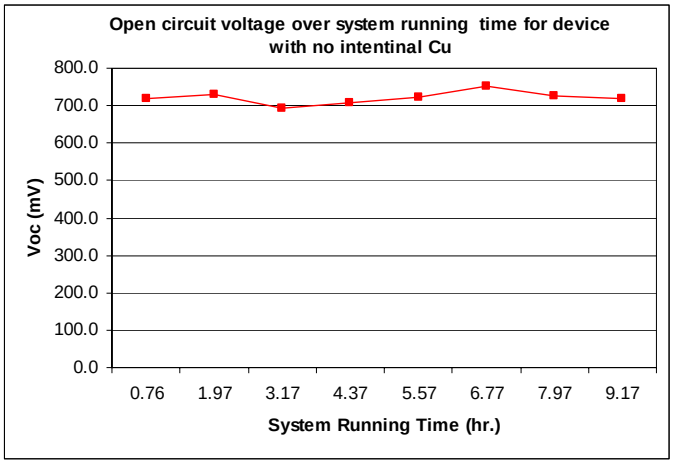
Table VI: Comparison of old hardware to new hardware for devices without intentional Cu. The new hardware is able to maintain processing conditions for 8-10 times longer than the old.

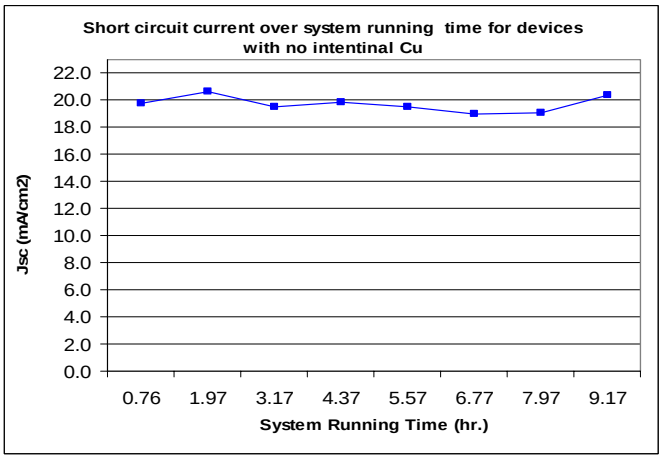
It can be seen from Table VI that the new hardware very closely reproduces the optimal conditions of the old hardware. The optimal conditions of the old hardware resulted in devices with excellent stability at 65°C accelerated testing and devices with no degradation in outdoor conditions (within the error of measurement) for nearly 2 years of exposure. [Barth 2002]. Similar results are expected with the new hardware. This continues to be verified through stability testing of a statistically valid number of devices. The significant advantage of the new hardware is that these optimal processing conditions can be maintained for 8 to 10 times longer during a process run as compared to the old hardware. This ensures fabrication of devices with consistent stability.

5.2. Development of an Optimal Baseline Process

The development of hardware and the determination of optimum conditions for the CdS, CdTe and $CdCl_2$ processing steps, consistently over long duration system operation is a significant accomplishment of this project. This has led to the development of an optimum, baseline process for all PV fabrication steps up to the back contact formation. This baseline process has been repeated for over 9 hours of operation. The Voc and Jsc parameters of devices with no intentional copper (fabricated up to but not including the back contact processing) have remained consistent for over this 9 hour time (Figures 26 and 27). This is a significant result because the $CdCl_2$ process conditions are a dominant factor in determining device performance and stability. As shown in section 3.2, the Voc and Jsc of devices with no intentional copper can be used to predict the stability of fully processed devices. Using this metric, this repeatable, baseline process setup will produce devices with good long term stability. A representative distribution of device efficiencies with back contact processing during the long duration processing is shown in Figure 28.

In this program, many process modules within our system were upgraded for robustness, repeatability and long term operation. These modules have been performing extremely well. The CdS, CdTe and $CdCl_2$ vapor sources have continued to operate very consistently for over 9 hours without replenishment or alteration of the source charge. Additional capability may be available for further long term operation. These process modules have proven to be quite repeatable and easy to control. The target thickness for the CdS/CdTe combined was 1.9 to 1.95 microns. The results of 8 process runs (each run is over an hour) yielded thickness between 0.125 micron below and 0.5 micron above the target. The CdTe vapor source temperature was intentionally varied only 1 °C during this time. The $CdCl_2$ process consistency is demonstrated in Figures 26 and 27. In addition, the chloride deposition thickness (measured by amount of substrate area where resublimation has completely occurred) has been quite repeatable. This repeatability is extremely valuable for CdTe PV process development.





Figures 26 and 27: Open circuit voltage (Voc) and short circuit current density (Jsc) for devices processed over long duration of system operation on same source charge of CdS, CdTe and $CdCl_2$. Each data point is the average of either 4 or 5 devices, no data omitted.

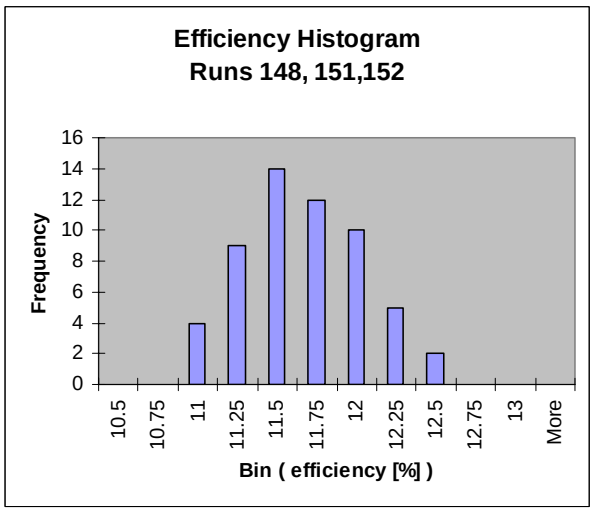


Figure 28: Efficiency distribution of devices processed over long duration of system operation on same source charge of CdS, CdTe and $CdCl_2$

The back contact copper processing is currently being optimized to achieve the same level of consistency, repeatability and long duration running capability as the other processes. The very small amount of copper used in our devices combined with the continuous nature of our system makes direct measurement of the copper deposition very challenging. As a result, controlling the copper back contact processing requires device analysis, and that the preceding processing steps remain repeatable. Additional effort, including SIMS studies, may be required. Initial results show, that for this baseline chloride process, lower substrate temperatures during copper back contact processing improves stability for 65 °C accelerated stress testing. Reducing water vapor partial pressure during device fabrication also has been shown to improve the devices. This optimization is ongoing.

5.3. Improvement in Device Efficiency and Yields

Efforts aimed at improving overall cell efficiencies and reducing the standard deviation within a substrate have resulted in improvements. The best to date efficiency distribution from one substrate are shown in Figure 29. The mean efficiency of the 14 cells is 12.6% with a standard deviation of 0.26%. Five substrates with coatings of 420 Angstroms

of gallium oxide were obtained from IEC and devices with higher Jsc were obtained. Further effort with larger number of substrates will be required for demonstrating higher efficiencies with intrinsic transparent conductor.

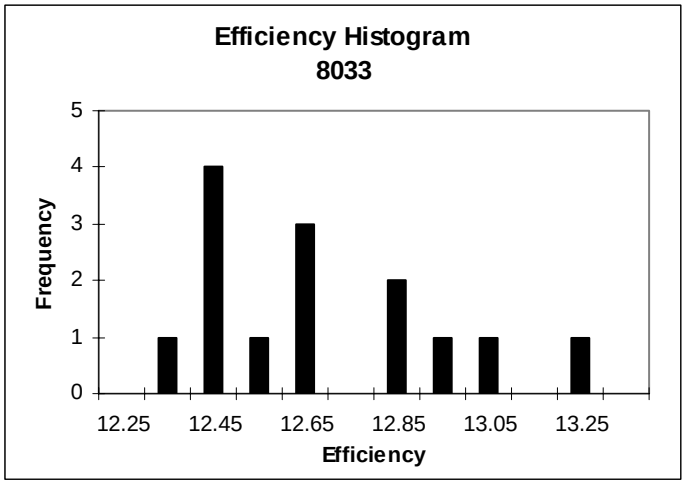


Figure 29: Efficiency histogram

5.4. Improvements to Experimental Infrastructure

Under this program, many of our research facilities including the pilot system have been upgraded. These improvements include:

(a) Design and fabrication of fixtures for testing un-encapsulated cells outdoors,
(b) Design and fabrication of improved indoor stress testers capable of testing a large number (over 600) of cells,
(c) Upgrading the J-V hardware and installing C-V measurement and a cryostat systems,
(d) Writing improved databases for tracking data,
(e) Installation of a residual gas analyzer (RGA) on the pilot system, and
(f) Improving the thermal uniformity of many process modules in the pilot system for long duration (16+ hours of continuous operation).

All these improvements are functioning well. A more detailed description of these activities can be found in the Appendices (Section 7). These improvements have greatly facilitated our research capabilities.

6. LARGE AREA PROCESSING AND JOINT VENTURE DEVELOPMENT

6.1. Processing Larger Substrates

The pilot system described above has been used to determine the optimum process conditions that result in stable, efficient PV devices. Through the support of DOE, the feasibility of processing commercial size modules was demonstrated. This was accomplished through the construction of the system shown in Figure 30. Large area solar cell processing modules (process heads) for the deposition and processing of the semiconductor films have been designed. A significant advantage of our technology is that the process modules are nearly identical for all vacuum process steps. Two stations have been constructed and installed. One has been tested for mechanical, electrical and thermal performance with excellent results. The features of the system shown in Figure 30 include:

- Process stations designed for continuous running for 40 hours or more without reloading

- Six substrate positions, (two installed)
- Phase angle SCR power control for longer lamp life and lower power line electrical transients
- Tested in continuous 8 hour runs
- High thermal efficiency
- Thermal uniformity of +/- 1.5 deg. C was measured for a temperature of 400 °C

A photograph of a 14x14 inch deposition of device quality CdTe on a 16x16 inch Pilkington glass substrates is shown in Figure 31. Estimated film thickness uniformity ~ +/- 5% on the film except at the corners. The system shown in Figure 30 was constructed to demonstrate the ability to scale our technology. In addition, the system was designed to be part of the hardware for a production prototype used for processing 16x16 inch modules. These modules will nominally produce 10 W of power. (10 W modules are an existing commercial product marketed by manufacturers such as BP and Shell.) 10 W modules can be connected together for higher power requirements. The system is designed to operate for long duration and is able to withstand the rigors of full manufacturing. However, this system is only designed to process the devices through the CdS, CdTe semiconductor deposition and the $CdCl_2$ treatment. (Please see schematic in Figure 1.) This system is referred to as the "semiconductor subsystem" and was designed and constructed with support from DOE-EERE. Recently, DOE has provided support to complete the system. This project includes 50% cost share from our industrial partner, National Starch and Chemical (NSC).

Completing this system will result in a full PV manufacturing production prototype system. When operated in full production mode, the production prototype system is capable of producing 2 million watts (2 MW) of PV a year**.**

Thermal and deposition modeling is also being developed in collaboration with professor Roop Mahajan of CU Boulder funded by a UN agency (UNIDO-ICS). These are full 3D models which includes the actual geometry of the process heads, heat lamps and radiation shielding. The results from the simulation match experimental results. Thus the model can be useful for developing advanced process head designs.

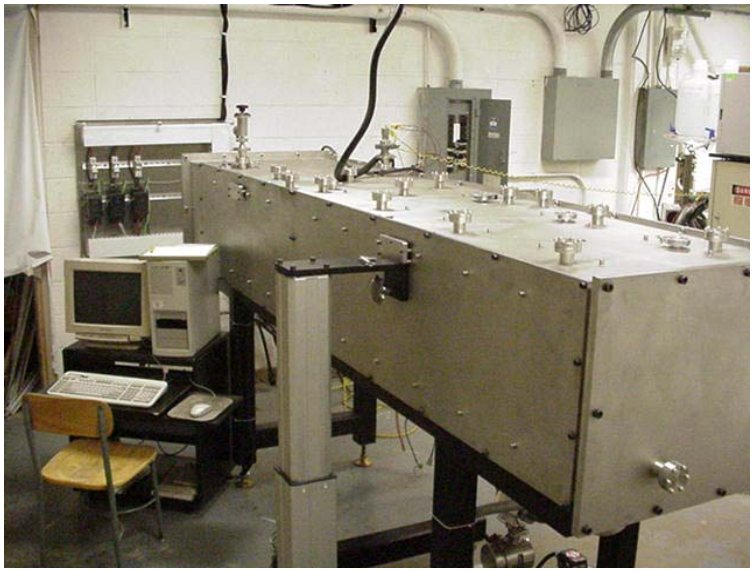


Figure 30: System to demonstrate feasibility of large area processing

Figure 31: Photograph of a large area CdTe PV film on Pilkington TEC 15 glass, ruler at top is 1 foot long.

6.2. Joint Venture Development

Significant progress towards developing a joint venture has been made with National Starch and Chemical (NSC), the US subsidiary of the ICI Group (an international chemical and technology company with approximately $10 billion annual turnover). The joint venture would manufacture and bring CdTe PV to market utilizing our technology. NSC is collaborating and contributing cost share to a project funded by DOE-EERE to complete the production prototype system for processing 10 W modules described above.

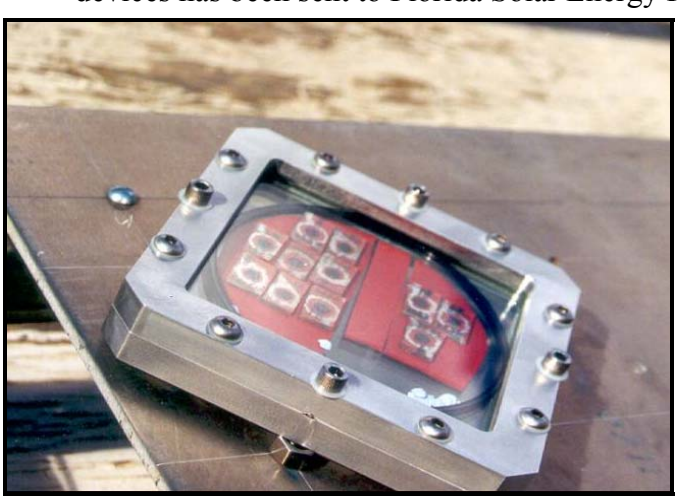
7. APPENDICES

7.1. Description of Improvements to Research Infrastructure

In this section, more details of our activities listed in Section 5.4. are presented.

7.1.1. Outdoor Performance of Cells

In order to develop a correlation between accelerated stress testing and outdoor performance, a unique fixture for exposing devices to outdoor conditions has been developed in our laboratory. This fixture is moisture tight and demountable. Non-encapsulated devices are inserted into the fixture which thermally emulates an encapsulated module. The devices can be removed for testing in the laboratory and then replaced for further exposure. The fixtures were tested for their ability to seal moisture by enclosing granules of indicating desiccant and submerging the fixture in water. After nine days, the desiccant in the fixture did not change color, demonstrating the ability of the fixture to seal against moisture. Fixtures capable of testing 200 cells have been fabricated. One outdoor fixture with ten devices has been sent to Florida Solar Energy Research Center for testing.



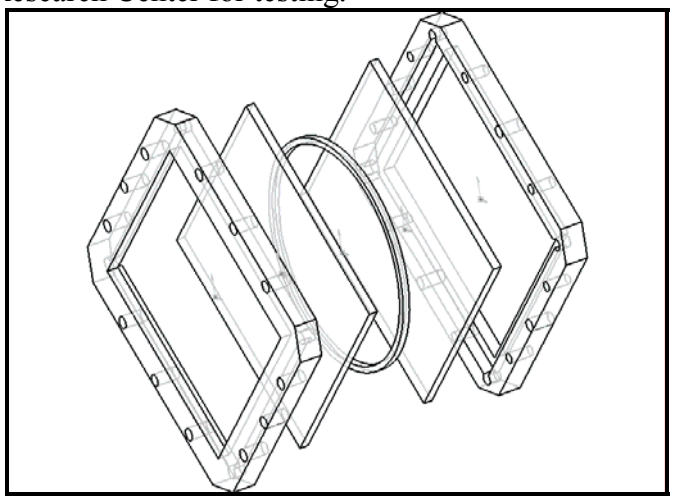


Figure 32 and 33: Photograph and schematic of the fixture for exposing un-encapsulated devices to outdoor conditions

Most of the published results of outdoor performance have been obtained from testing modules. Modules can have additional failure mechanisms such as interconnect degradation, buss bar degradation and encapsulation failure [McMahon 1998]. The use of the outdoor fixture avoids these additional failure mechanisms. This enables accelerated indoor stress tests to be correlated to outdoor performance. Currently, 40 devices are being exposed to outdoor conditions in these fixtures and device performance is being monitored periodically. Some of the results of the outdoor testing are given in Section 3.1.2.

7.1.2. Indoor Stress Testing of Cells

We have significantly expanded and upgraded our capability for indoor stressing of cells. Currently, up to 600 devices can be simultaneously stress tested. Our indoor light soakers enable independent control of illumination and cell temperature. Cell temperature is close loop controlled. A micro-thermocouple was used to confirm and calibrate the control thermocouple readings. The temperatures measured with the micro-thermocouples were within 0-2 degrees C of the control thermocouple readings. The new indoor stress fixtures have an additional control system incorporating redundant sensors. The additional control system has been wired to shut off of illumination (and heat) in case of primary controller failure or excessive device temperatures.

7.1.3. Upgrading IV Measurement

Accurate, repeatable device current-voltage (IV) measurement is critical for process development and evaluating stability. Previously, the IV measurement in our laboratory was performed with an HP 34401A for measuring voltage and a Fluke 8840A for measuring current and an HP 4145A for applying bias. All of this has been replaced by a Keithley 24203A sourcemeter. A Labview program was developed to run the Keithley 24203A using a GPIB interface. The new systems have reduced the time for measuring IV by more than 50% and support the measurement of larger area device including modules. In addition to upgrading the current IV measurement, we have installed a Xantrex XRH 100-10 DC power supply to provide power to the ELH lamps and virtually eliminate variation in illumination due to fluctuations in the line voltage.

7.1.4. Upgrading the Database

All the results from our devices used to be tracked with a database that required manual entry of the data from IV measurement. This has been upgraded to enable the direct entry of cell performance data from IV measurement system. The Labview program for IV measurement has been enhanced to allow direct export of data after IV measurement. The graphical processing has been upgraded to allow better plotting and comparing of results.

7.1.5. Residual Gas Analyzer (RGA) Installation

A Stanford Research System SRS 100 RGA has been installed on the system. Since our operating pressures are in the range of 40 mTorr, a bypass valve assembly was required to reduce the pressure at the inlet of the instrument. A turbopump has been installed to reduce the pressure at the RGA head. The RGA has been interfaced to a computer for data acquisition and control. The RGA system is functioning well. Experiments with the RGA have demonstrated that there is no increase in the partial pressure of oxygen when substrates are transported into the vacuum chamber using our air-to-vacuum-to-air (AVA) transport system. The AVA seals were designed to accomplish this and the tests with the RGA validate the designs.

7.1.6. Upgrading the Pilot System

During this project, significant hardware upgrades have been performed. These include the following:

1. A new air to vacuum to air (AVA) belt has been designed constructed and installed. This new belt is suitable for long duration processing.

2. All internal electrical wiring for the deposition system has been inspected and upgraded where needed.
3. A new substrate heater for the back contact process has been designed, constructed and installed.
4. The primary vacuum pumps for the AVA seals have been rebuilt and a new high vacuum pump has been installed on the system.

Due to the extreme sensitivity of device performance to processing conditions, it is advantageous to perform processing studies with hardware designs suitable for conditions seen in industrial production (long duration continuous operation of 16+ hours). The improved hardware will allow the processing conditions and device results to be directly applied to large scale processing systems. Upgraded systems for CdS, CdTe and $CdCl_2$ deposition have been designed, constructed, installed and successfully tested. The hardware improvements include the development of a unique substrate heating technology which employs both active heating and cooling to maintain set temperatures. This allows precise substrate temperatures to be maintained during CdS and CdTe deposition while allowing long duration operation on our continuous pilot system. These systems were designed with finite element modeling of the radiation heat transfer with non-linear boundary conditions. Excellent correlation was seen between the modeling and the experimental results. Thermometry on the system has been redesigned for greater serviceability and accuracy.
Extensive deposition experiments have been performed with the new CdS, CdTe and $CdCl_2$ hardware to optimize processing conditions for device performance and stability. Most of the vapor sources and substrate heaters in our system are graphite structures heated by quartz IR lamps and have a high degree of thermal uniformity (+/- 2°C). However, three of the heaters in the system utilized other heater designs which did not provide the thermal uniformity of the other sources. These three heaters have been redesigned with the graphite/lamp configuration. Another heater associated with the $CdCl_2$ process has also been redesigned for increase uniformity and for easy removal of the unit for servicing and cleaning. These four heating units have been constructed, installed in the system and tested. They continue to function well.

7.2. Description of Activities with the National CdTe Team

Our group has been actively participating in National CdTe Team activities. The team has had productive collaborations with Prof. Sites's group at Colorado State, as well as with researchers at BP Solar, First Solar, National Renewable Energy Laboratory, Institute of Energy Conversion, Lawrence Berkley Labs, University of Missouri, Pacific Northwest National Laboratory, CU Boulder and others. In addition to attending and presenting talks at the Team Meetings, the following activities were accomplished.

Collaborative research is being performed in conjunction with Photovoltaics Laboratory of CSU under the direction of Jim Sites and Alan Fahrenbruch of ALF. In one study, devices have been fabricated at five different processing conditions incorporating various amounts of copper in the back contact. These devices were characterized through JV as a function of temperature; capacitance vs. voltage and frequency and micro uniformity (LBIC) techniques. AMPS modeling of these devices was performed to gain further insight. These studies have helped in understanding how device performance changes as a function of

the amount of copper introduced during processing. Results were reported [Pudov 2002, Sites 2002].

Larry Olsen of the Pacific Northwest National Laboratory has been a frequent visitor to our laboratory and collaborator on research projects. A collaborative research effort with our group and Larry Olsen is currently in progress. He has investigated applying antimony telluride contacts on our CdS/CdTe. A detailed series of experiments is being conducted to investigate applying barrier coatings over our completed devices. Eight CdS/CdTe devices with a special geometry were provided to his group. After coating, a number of these devices were be subjected to stress and humidity. The barrier coatings do improve the performance over uncoated devices. These positive results have led to a new series of experiments. Twelve new devices will be studied, stability tested and the results published.

Detailed investigations of the effect of water vapor on stability have been conducted. Stress tests were performed in desiccated and un-desiccated conditions indoors and outdoors. The stability of 4 sets of cells (at least 5 devices/set) which have undergone stress under the following conditions: 1) desiccated accelerated indoor 2) desiccated outdoor 3) un-desiccated accelerated indoor and 4) un-desiccated outdoors were studied. Results were reported [Enzenroth 2002].

Many devices have been provided to assist the team. We have provided 51 devices for micrononuniformity studies. Devices were provided to Dr. Dhere of NREL and Maldova University for their collaborative studies with Jim Sites. Devices for capacitance vs. voltage (CV) "round robin" studies have been supplied. The CV measurements performed in our laboratory on these devices closely matches the result obtained by Prof. Sites' group. This demonstrates that CV measurements can be reproduced in different laboratories.

Substrates with CdS deposited in our system have been provided to Dr. X. Wu of NREL for bandgap studies. Additional tin oxide coated substrates were also provided. This collaboration was initiated after Drs. Wu and Dhere were given a demonstration of our technology during a detailed tour of our facilities.

Dave Albin and Tracie Bukowski of NREL visited our facility. The effects of processing conditions on stability were extensively discussed. In support of their efforts, we provided devices processed at both optimal and non-optimal conditions for stress testing at NREL. At the request of D. Albin, we provided details and power point slides showing the effect of the $CdCl_2$ treatment on device stability for our process. He presented this data to First Solar. A research effort between our group and Dr. Y. Yan of NREL to investigate our devices using TEM techniques was initiated. Samples have been provided.

We are continuing our ongoing interactions with B. McCandless of IEC. He reported on the characterization of our CdS films and provided a number of gallium oxide coated Pilkington Tec 15 samples for our research in improving our device efficiency. B. McCandless and Alan Fahrenbruch were also given a tour of our facility and a demonstration of our technology. Substrates processed with and without copper have been provided for characterization of the films.

Graduate students from Colo. School of Mines (CSM) were given a lab tour.

7.3. Description of Interactions with Industry

The activities of our group in interacting with industries are listed below:

7.3.1. Collaborative work with First Solar

A detailed study on $CdCl_2$ treatment was undertaken for First Solar. CSU's research objectives were based on First Solar's interest in evaluating wet vs. vapor $CdCl_2$ treatments. After altering our continuous inline pilot system, vapor $CdCl_2$ treatments were performed on CdS/CdTe material provided by First Solar. An optimization screen was done first and the two best process conditions, chosen by initial device Voc, were used for further study.

The conclusions of the work were as follows: i) devices with good initial efficiencies of 8.5-9.5% and Voc's as high as 829 mV with no back contact processing, and only metallization were fabricated, ii) these devices showed promising stability under accelerated indoor stress and iii) the CdTe back surface after the $CdCl_2$ treatment had no phases other than CdTe as shown by GAXRD. In all samples, the oxides initially present in the as received samples were reduced by our vapor $CdCl_2$ treatment as shown by high resolution XPS scans. Results of these studies were reported at team meetings [Barth 2004] and in a written report to First Solar. P. Meyers of First Solar was given a detailed tour of our facility. The meeting was fruitful and we offered our continued assistance as needed.

7.3.2. Collaborative work with BP Solar

A series of detailed studies on of the effects of the chloride treatment and back contact processing using BP Solar material was performed. Many devices with efficiency values greater than 10% (highest 10.75%) have been fabricated on BP material utilizing our pilot scale processing technology. Results of these studies were presented at the CdTe Team meetings and presented to BP in a series of written reports. (Please see 7.6.2. Additional Reports, Communications.)

A series of detailed XRD studies were performed to characterize the residual stress in BP CdTe films, which had been made using different processing conditions. These studies were part of ongoing quality improvements efforts at BP Solar. Results of these studies were reported at team meetings by D. Cunningham and in written reports to BP Solar (7.6.2. Additional Reports, Communications).

An extended meeting and technology demonstration was performed for V. Palaniappgounder, and D. Cunningham of BP Solar. Extending the current collaboration into technology areas was discussed, but before these collaborative studies could be initiated BP Solar terminated their CdTe efforts.

7.3.3. Collaborative Work with Other Industrial Groups

McMaster Energy was supplied with a number of 3.6 x 3.1 inch substrates with CdS/CdTe films to assist in their investigations of $CdCl_2$ treatments.

B. Stanburry of Helivolt visited our facility. At his request, detailed technical input and design assistance on vapor source design and substrate heating was provided by our group. This technical input will be utilized by him in the design of systems for processing CIS based devices

At the suggestion of Doug Rose, Doug Shultz of Ceramem was contacted and was provided with many 3.6 x 3.1 inch glass substrates with CdS/CdTe films ($CdCl_2$ treated) to further their studies. Our group processed devices from CdS/CdTe material supplied by Canrom. The material was contacted and cells were defined and tested.

. Ingrid Repins of ITN was supplied with a number of 3.6 x 3.1 inch substrates with CdS/CdTe films to assist in her investigations into non-contact temperature measurements for thin film PV processing.

7.4. Additional Activities

We are collaborating with Prof. Roop Mahajan of University of Colorado, Boulder. He is an internationally renowned authority in the field of heat transfer in processing semiconductors. His proposal to ICS (International Center for Science, a UN agency) in collaboration with our group has been selected for funding. The funding will support two students and demonstration projects in Mexico and India. This will provide more opportunity for studying stability under field conditions.

Measurements of the residual stress in the glass substrates after processing through our continuous pilot scale system have been completed as per ASTM C1279. Glass substrates with different levels of residual stress have been sent to the ASU Photovoltaic Testing Lab for hail impact tests. These studies will establish the stress levels needed to pass the hail impact test for modules as per IEEE 1262.

The new CSU president, Larry Penley, in his annual fall address highlighted our PV work. Dr. Penley also visited our lab and was given a technology demonstration.

A meeting with Mr. Rolf Butters of DOE was conducted at our facility. Mr. Butters was a past program manager for some of our projects and he has been familiar with our efforts since 1997.

The president and the CEO of the Everitt Companies toured our facility. The Everitt Companies are some of the largest real estate and commercial development groups in the region. They offered financial assistance, facility space and business/legal help to assist this project.

A detailed lecture, lab tour and technology demonstration was given to the Northern Colorado Chapter of the Colorado Renewable Energy Society (N-CRES). This 2-3 hour event was attended by approximately 30 people and was well received. Representative from the Western Area Power Authority (WAPA) attended and offered their assistance for the project. NREL's support was acknowledged during this event.

Noted author John Perlin visited our facility and given a lab tour at his request. Detailed information concerning our process and CdTe thin film PV was provided. Correspondence will continue.

7.5. Student Activities

Four graduate students, Amit Bindal, Mukul Bhat, Tushar Shimpi and Sachin Vyas were supported through this project. They have assisted in the activities described in this report. Sachin Vyas, Tushar Shimpi and Toru Takamiya are performing their graduate research on this project. Hershel Shelly is conducting his Ph. D. research on this project. His research is to study the pilot scale process from an industrial engineering perspective. Chetan Malhothra of CU Boulder is pursuing his Ph.D. through thermal and deposition modeling of the process. A senior undergraduate student, Marc D. Bucaro, has completed a detailed independent study of the literature of defects in CdTe.

7.6. Publications, Communications and Presentations

7.6.1. Publications and Presentations

Enzenroth, R. A, K. L. Barth and W. S. Sampath; "Continuous, In-Line Processing of CdS/CdTe Devices: Progress Towards Consistent Stability," presented at the 19th European PV Solar Energy Conference in Paris, France, June 2004.

Barth, Kurt L., R. Albert Enzenroth and W. S. Sampath, "Chlorine Issues: The Effect of Vapor $CdCl_2$ Treatment on Device Performance and Stability using First Solar Absorbers" National CdTe Team Meeting, Sponsored by the DOE through the National Renewable Energy Laboratory, Golden, CO, February 26 and 27, 2004.

Enzenroth, R. Albert, K. L. Barth, and W. S. Sampath, "Defects in CdTe PV Devices Fabricated with Varied Process Conditions Measured by Thermal Admittance Spectroscopy " National CdTe Team Meeting, Sponsored by the DOE through the National Renewable Energy Laboratory, Golden, CO, February 26 and 27, 2004.

Sampath, W. S., R. Albert Enzenroth, and Kurt L. Barth, "Accelerated Lifetime Testing: Some Observations" National CdTe Team Meeting, Sponsored by the DOE through the National Renewable Energy Laboratory, Golden, CO, February 26 and 27, 2004.

Sampath, W. S., Kurt L. Barth, and R. Albert Enzenroth, "Continuous In-Line Processing of CdTe Devices: Update" National CdTe Team Meeting, Sponsored by the DOE through the National Renewable Energy Laboratory, Golden, CO, February 26 and 27, 2004.

Mahajan, R; and W. S. Sampath; "CdTe PV Technology: Low Cost Fabrication, Performance and Potential" was presented at ICS in Trieste, Italy, 2004. ICS is part of the UN.

Malhotra. C; R. Mahajan, W. S. Sampath, K. L. Barth and R. A. Enzenroth; "Control Of Temperature Uniformity During The Manufacture of Stable Thin-Film Photovoltaic Device", to be presented at the ASME International Mechanical Engineering Congress.

Sampath, W. S., K. L. Barth and R. A. Enzenroth, "Progress Towards Consistent Stability", National Renewable Energy Laboratory's National CdTe Team Meeting, Golden CO, July 2003.

Barth, K. L., R. A. Enzenroth, and W. S. Sampath, "Progress in Continuous, In-Line Processing of Stable CdS/CdTe Devices", Presented at the National Center for Photovoltaics Program Review Meeting 2003, Denver CO, March 24-26 2003.

Barth, K. L., R. A. Enzenroth, and W. S. Sampath, "Chlorine Issues: The Effect of $CdCl_2$ Treatment on Device Performance and Stability", National Renewable Energy Laboratory's National CdTe Team Meeting, Golden CO, October 31 and November 1, 2002.

Sampath, W. S., Kurt L. Barth, and Robert A. Enzenroth, "Process Uniformity and Stability" National Renewable Energy Laboratory's National CdTe Team Meeting, Golden CO, October 31 and November 1, 2002.

Enzenroth, R. Albert, Kurt L. Barth, and W. S. Sampath, "Effect of Moisture Exposure on CdS/CdTe Solar Cells During Stress", National Renewable Energy Laboratory's National CdTe Team Meeting, Golden CO, October 31 and November 1, 2002.

Chusuei, C. C., K. L. Barth, R. A. Enzenroth and W. S. Sampath, "An XPS and SEM Study of an Efficient, Copper-doped Photovoltaic Cell", 224th ACS National Meeting, Division of Physical Chemistry, Boston, MA, August 18-22, 2002.

Barth, K. L., R. A. Enzenroth, and W. S. Sampath, "Apparatus and Processes for the Mass Production of Photovoltaic Modules" US patent 6,423,565, July 23, 2002.

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7.6.2. Additional Reports, Communications

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