Known Good Die Criteria

For Vendor Input

General Information

Information Type: KGD
Submitted by: Larry Duncan
Part Number: See KGD Products
Part Function: Various
Vendor: Elmo Semiconductor/ELPAQ

	For Vendor Input **KGD ASSURANCE/DATA Test/Screen/Packaging**		***For Vendor Input*** **Performed by Vendor**				***For Vendor Input***
		Level 1	**Level 2**	**Level 3**	**Level 4**	**Level 5**	**Comments**
Wafer Probe	Electrical	Yes	Yes	Yes	Yes	Yes	
	At Speed:						
	DC Parametric						
	Functional (**available**)						
	Margin testing						
	SPC Limits						
	Speed Grading(**available**)						
	Std/Hot Wafer Probe	Std	Std/Hot	Std/Hot	Std/Hot+SPC	Std	
	Voltage Stress:						
Lot Acceptance Test/Charges	Mil-Std-883, Method 5007(**available**)						
NRE/ Charges							
Burn-In	Die Level			Yes	Yes	Yes	
	Wafer Level						Up to 200C
Visual Inspection	Mil-Std-750/2072, 2073; 883/2010/A or	Yes	Yes	Yes	Yes	Yes	
Bond-Pull		Yes	Yes	Yes	Yes	Yes	
Thermal Cycling				Yes	Yes	Yes	
Package Sample		Yes	Yes	Yes	Yes		
SEM Analysis					Yes		
Life Test					Yes		
Other						KGD Coating Process/Co	
Die Packaging/Shipping	Die Form						
	GEL-packs(**available**)						
	Pocketed tapes						
	Sleeves						
	Trays						
	Wafer Form						
	Waffle packs						
Documentation Provided	Characterization Data						
	Charges($)						
	Data Sheet						
	Die Backside Potential						
	Die Backside Surface Material						Au backing is available
	Die Topography(OUTLINE)						
	GDS Files and X, Y Cordinates						
	KGD Die Dimensions						
	Pad /Passivation Openings						
	Pad Metal Composition & Thickness						
	Passivation & Thickness						
	Pin Out						
	Special Assembly Requirements						
	SPICE Modules						
	Wafer Thickness						
Reliability	Life Test Results:						
Yield	Probe/Burn-in:						
Die Shrink Plans							

All COTS information recorded herein is for JPL internal use only.

JET PROPULSION LABORATORY
Electronic Parts Engineering Office 507

Known Good Die Criteria

For Vendor Input
General Information

Information Type: KGD (SmartDie™)
Submitted by: Taken from W W W
Part Number: See KGD Products
Part Function: Various
Vendor: Intel Corporation

	For Vendor Input **KGD ASSURANCE/DATA** **Test/Screen/Packaging**	***For Vendor Input*** **Performed by Vendor** **Standard**		**Comments**
Wafer Probe	Electrical	X		@ hot and cold if needed
	At Speed:	X		for SmartSort products
	DC /AC Parametric	X		for SmartSort products
	Functional			
	Margin testing			
	SPC Limits	X		Statistical bin limits are used
	Speed Grading			
	Std	X		@25C (0-80C for SmartSort products)
	Voltage Stress:			
Lot Acceptance Test/Charges	Mil-Std-883, Method 5007			
NRE/ Charges				
Burn-In	Die Level	X		@125C if required(same as package)
	Wafer Level			
Visual Inspection	100% at 100x	X		
Bond-Pull				
Thermal Cycling				
Package Sample				
SEM Analysis				
Life Test				
Other				
Die Packaging/Shipping	Die Form			
	GEL-packs	X		Carbon conductive
	Tape & Reel	X		used for high volume products
	Sleeves			
	Trays			
	Wafer Form			
	Moistuire barrier bag + desiccant	X		Storage recommended at <40C/90%RH
	Waffle packs			
Documentation Provided	Lot number/qty/ seal date	X		
	Qualification/Quality Validation Data	X		
	Charges($)			
	Data Sheet	X		Called product specificaiton
	Die Backside Potential	X		Most die require bias
	Die Backside Surface Material	X		GOLD/CHROM OR BARE SILICON
	Die Photograph	X		
	GDS Files and or X, Y Cordinates	X		
	KGD Die Dimensions	X		
	Pad /Passivation Openings	X		
	Pad Metal Composition & Thickness	X		
	Passivation type & Thickness	X		
	Pin Out	X		
	Special Assembly Requirements			
	SPICE Modules			
	Wafer Thickness	X		
	Revision Specification History	X		
Reliability	Infant mortality/Life Test Results:	X		Reuirements established by Level
Yield	Probe/Burn-in:			
Die Changes		X		60 day notification prior to change

Known Good Die Criteria

For Vendor Input

General Information

Information Type: KGD
Submitted by: Mike Black
Part Number: See KGD Products
Part Function: SRAM & DRAM
Vendor: Micron Technology

	For Vendor Input KGD ASSURANCE/DATA Test/Screen/Packaging	*For Vendor Input* Performed by Vendor? SRAM 1M	SRAM 2M	DRAM 256K x 16	DRAM 1M x 4, 4M x 1	*For Vendor Input* Comments
Wafer Probe	AC	X(C7)	X(C7)	X(C7)	X(C7)	KGD^{Plus} is C7
	At Speed:	X(C2)	X(C2)	X(C2)	X(C2)	Speed Probe is C2
	DC Parametric	X(C1)	X(C1)		X(C1)	Standard Probe is C1
	Functional	X(C1)	X(C1)		X(C1)	
	Margin testing					
	SPC Limits					
	Speed Grading					
	Temperature(s): 0C to 70C	X(C1)	X(C1)		X(C1)	
	Voltage Stress:	X(C1)	X(C1)		X(C1)	
Lot Acceptance Test/Charges						
NRE/ Charges						
Burn-In	Die Level	X(C3)	X(C3)	X(C3)	X(C3)	Probe^{Plus} is C3
	Wafer Level					
Visual Inspection	Mil-Std-883 method 2010/other					
Bond-Pull	Mil-Std-883 method 2011					
Die Shear						
Gold Back Adhesion Test						
SEM Analysis	Mil-Std-883 method 2018					
Dose Rate Latchup	Method 1020					
Total Dose	Method 1019					
Die Packaging/Shipping	Die Form					C3 & C7 level products only
	GEL-packs	X	X	X	X	
	Pocketed tapes					
	Sleeves					
	Trays					
	Wafer Form	X				C1 & C2 level products only
	Waffle packs					
Documentation Provided	Characterization Data					
	Charges($)					
	Data Sheet	X	X	X	X	Data sheets received
	Die Backside Potential	X				
	Die Backside Surface Material	X				
	Die Topography(OUTLINE)	X				
	GDS Files and X, Y Cordinates					
	KGD Die Dimensions	X				
	Pad /Passivation Openings	X				
	Pad Metal Composition & Thickness	X				
	Passivation & Thickness	X				
	Pin Out	X				
	Special Assembly Requirements	X				
	SPICE Modules					
	Wafer Thickness	X				
Reliability	Life Test Results:					
Yield	Probe/Burn-in:					
Die Shrink Plans						

Known Good Die Criteria

For Vendor Input

General Information

Information Type:	**KGD**
Submitted by:	**Unitec Sales Inc.**
Part Number:	**Various**
Part Function:	**Various**
Vendor:	**Thomson-CSF**

QUALITY LEVELS/SCREENS PERFORMED ON QUAL LOTS

	KGD ASSURANCE/DATA Test/Screen/Packaging	A	V	Qualification lot is assembled. N	T	W	Z	ZP	Comments
Wafer Probe	AC								
	At Speed:								
	DC Parametric								
	Functional	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
	Margin testing								
	SPC Limits								
	Speed Grading								
	Temperature(s):	Yes	Yes	Yes	Yes	Yes	Yes	Yes	25C ONLY
	Voltage Stress:								
Lot Acceptance Test/Charges									
NRE/ Charges									
Burn-In	Die Level				Yes	Yes	Yes	Yes	T,W: 160 H @ 125C; Z: 240 H
	Wafer Level								
Life Test						Yes	Yes	Yes	1000 H
Visual Inspection									
Bond-Pull				Yes	Yes	Yes	Yes	Yes	
Die Shear				Yes	Yes	Yes	Yes	Yes	
Gold Back Adhesion Test									
Die Inspection	100%		Yes	Yes	Yes	Yes	Yes	Yes	
Wafer Inspection			Yes	Yes	Yes	Yes	Yes	Yes	
Stabilization Bake				Yes	Yes	Yes	Yes	Yes	
SEM Analysis								Yes	
Dose Rate Latchup									
Qualification Lot				Yes	Yes	Yes	Yes	Yes	Electrical test @ 3 temperatures for N,T,W,Z; Electrical test after BI @ 25C for T,W,Z; Electrical test after life testr @ 25C for W,Z
Total Dose									
Die Packaging/Shipping	Die Form								
	GEL-packs								
	Pocketed tapes								
	Sleeves								
	Trays								
	Wafer Form								
	Waffle packs								
Documentation Provided	Characterization Data								
	Charges								
	Die Backside Potential	Yes	Yes	Yes	Yes	Yes	Yes	Yes	If applicable
	Die Backside Surface Material								
	Die Topography	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
	GDS Files and X, Y Cordinates								
	KGD Die Dimensions	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
	Pad Metal Composition & Thickness	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
	Passivation & Thickness	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
	Pin Out								
	Special Assembly Requirements								
	SPICE Modules								
	C of C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Reliability									
Yield	Probe/Burn-in:								
Die Shrink Plans(Change Notification)									
Minimum Buy Qty.									

Known Good Die Criteria

For Vendor Input

General Information

Information Type:	**KGD**
Submitted by:	**Mont Taylor**
Part Number:	**Various**
Part Function:	**Various**
Vendor:	**Texas Instruments**

For Vendor Input

	KGD ASSURANCE/DATA Test/Screen/Packaging	**KTD**	**CKGD**	**MKGD**				**Comments**
Wafer Probe	AC	Functionality	Guaranteed to Datasheet	@ Datasheet				
	At Speed:	Min Clock	Yes	Yes				
	DC Parametric	25C	0 & 70C	-55C & 125C				
	Functional							
	Margin testing							
	SPC Limits							
	Speed Grading							
	Temperature(s):	25C	Data Driven	Data Driven				
	Voltage Stress:							
Lot Acceptance Test/Charges								
NRE/ Charges								
Burn-In	Die Level		Data Driven	Data Driven				PDA = 5
	Wafer Level							
Visual Inspection		40X	40X	40X				
Bond-Pull								
Die Shear								
Gold Back Adhesion Test								
SEM Analysis								
Dose Rate Latchup								
Total Dose								
Die Packaging/Shipping	Die Form							
	GEL-packs							
	Pocketed tapes							
	Sleeves							
	Trays							
	Wafer Form							
	Waffle packs							
Documentation Provided	Characterization Data							
	Charges							
	Die Backside Potential							
	Die Backside Surface Material	Silicon	Silicon	Silicon				Die thickness = 15 mils
	Die Topography							
	GDS Files and X, Y Cordinates	Yes	Yes	Yes				
	KGD Die Dimensions	Yes	Yes	Yes				
	Pad Metal Composition & Thickness	Cu doped Al	Cu doped Al	Cu doped Al				Die have Au bumps
	Passivation & Thickness	Compressive Nitride	Compressive Nitride	Compressive Nitride				
	Pin Out	Yes	Yes	Yes				
	Special Assembly Requirements							QMI 2569F Die attach material; Bond wire size =1.0 to 1.25 mil.; Max die attach temp. = 440C.
	SPICE Modules							
	C of C	No	No	Yes				
Reliability		Available	Available	Available				Life & Miosture-resistance data
Yield	Probe/Burn-in:							
Die Shrink Plans(Change Notification)		No	Commercial Practice	Yes				
Minimum Buy Qty.		100 PC Minimum	1000 PC Minimum	25 PC Minimum				