Simulation and Analysis of Three-Phase Rectifiers for Aerospace Power Applications

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Due to the nature of planned planetary missions, fairly large advanced power systems are required for the spacecraft. These future high power spacecrafts are expected to use dynamic power conversion systems incorporating high speed alternators as three-phase AC electrical power source. One of the early design considerations in such systems is the type of rectification to be used with the AC source for DC user loads. This paper address the issues involved with two different rectification methods, namely the conventional six and twelve pulses. Two circuit configurations which involved parallel combinations of the six and twelve-pulse rectifiers were selected for the simulation. The rectifier's input and output power waveforms will be thoroughly examined through simulations. The effects of the parasitic load for power balancing and filter components for reducing the ripple voltage at the DC loads are also included in the analysis. Details of the simulation circuits, simulation results, and design examples for reducing risk from damaging of spacecraft engines will be presented and discussed.

Nomenclature

ALTR.V	Line-to-line output voltage of Alternator, Volt
D1 to D24	Power Diodes
E1, 2, 3	Alternator
L1, 2, 3	Phase inductances of Alternator, Henry
PLC	Filter capacitor for Parasitic Load, Farad
PLK	Parasitic Load Circuit
PLR	Parasitic load resistor, Ohm
PLP	Parasitic load power, Watt
R1, 2, 3	Phase resistances of Alternator, Ohm
ULC	Filter capacitor for User Load, Farad
ULK	User Load Circuit
ULL	Filter inductance for User load, Henry
ULP	User load power, Watt
ULR	User load resistor, Ohm
ULR.I	User load DC current, Amp
ULR.V	User load DC voltage, Volt
Y-to-Delta	Y to Delta transformer
Y-to-Y	Y to Y transformer

I.   Introduction

Due to the nature of planned planetary missions, fairly large and advanced power systems are required for the spacecraft. These future high power spacecrafts are expected to use dynamic power conversion systems incorporating high speed alternators as the three-phase AC electrical power source. A typical block diagram for such a system is shown in Figure 1. Basically, from Figure 1, the Dynamic Power Converter drives the Alternator which generates the three-phase AC power source. This AC power is then routed through the Power Management and

Distribution (PMAD) sub-system for overall control of the system, including the 3-Phase Rectifier, the Alternator's speed and voltage via the Parasitic Load. This Parasitic Load is designed to maintain a constant load on the Alternator regardless of power demand by the Spacecraft Engine. More detailed descriptions of the system can be found in Reference #1. In general, the power system of this kind is compact and isolated. Its impedance is expected to be higher than that of a normal utility system and the distribution voltages may not be clean sinusoids. One of the early design considerations is the type of rectification for use by the spacecrafts electrical propulsion system. It is known that the electric propulsion engine intermittently, unpredictably and momentarily shorts during its recycle event [1]. During this short circuit event, the inrush current spike from the rectifier's output filter capacitor could permanently damage the spacecraft engine if it's not properly designed. Therefore, the design issue is for a given power quality requirement at the spacecraft engine power supply bus (rectifier's output voltage bus), the maximum allowable value for the filter capacitance at this bus must also be satisfied for the safety reason of the engine as mentioned.

Thus, this paper addresses issues involved with two conventional rectification methods, namely the six and twelve-pulses, to be used with such AC power source for the DC user loads. Two circuit configurations which involved parallel combinations of the six and twelve-pulse rectifiers were selected for the simulation. The rectifier's input and output power waveforms will be thoroughly examined through simulations. The effects of the parasitic load for power balancing and filter components for reducing the ripple voltage at the DC loads are also included in the analysis. Details of the simulation circuits and results will be presented and discussed. Examples of using simulation results for proper design of the rectifier's output filter capacitance which is a key solution to reduce risk from damaging spacecraft engine during its recycles will also be given.
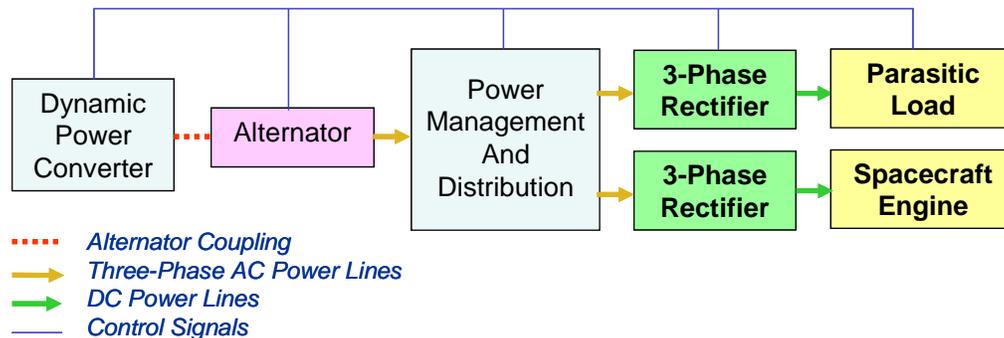

Figure 1: A Typical Block Diagram of a Thermal Dynamic Electric Power System for Aerospace Applications.

II.   Simulation Overview

To simplify the system for study purposes, the simulation was done without the Dynamic Power Converter and the PMAD system (Fig. 1). In addition, the Spacecraft Engine name was replaced or interchangeable with the name "User Load" in the simulation. Two circuit configurations have been selected for this reduced model shown in Figures 2 and 3.

Due to its isolated nature and the characteristics of the heat source, a spacecraft's turbine alternator power source is normally designed as a constant power source. Therefore, a parasitic load (PLR, Figs. 2 and 3) is needed for dissipating the unused power from the source. The parasitic load serves as power or load balancing for the power source to regulate the system voltage and/or speed. One of the key design parameters for a rectifier is the maximum *ripple* magnitude of the output DC voltage (ULR.V, Fig's 2 & 3) that is acceptable for the user loads (ULR, Figs. 2 and 3), such as spacecraft engine (Fig. 1), for a specific range of power. The goal is to design for a specific ripple or power quality requirement while optimizing the rectifier output capacitance to minimize the impact on the thruster grids.

Thus, for the hardware design aid, the simulation is mainly focused on observing the ripple magnitudes of the output DC voltages (URL.V) for a range of filter capacitance values (ULC). This ripple observation at the User/Spacecraft Engine Load is done with and without the influences of the Parasitic Load's filter capacitance (PLC, Figs. 2 and 3) which also plays an important role in reducing the User Load's filter capacitance while maintaining the same power quality at this bus.

The drawings and more detailed descriptions of the two selected circuits are being described in the following.

1. Circuit Configuration #1 (CC #1)

The first circuit configuration, Figure 2, is a conventional six-pulse rectifier with isolation transformer for the User Load Circuit (ULK) and a six-pulse rectifier for the Parasitic Load Circuit (PLK). Note there is no isolation transformer for the PLK. The PLC and PLR are variable names for the filter capacitor and load resistor in the Parasitic Load Circuit. Likewise, ULC and ULR are used in the User Load Circuit. The variable name ULR.V is used for the output DC voltage at the User Load (ULR, or Spacecraft Engine load).
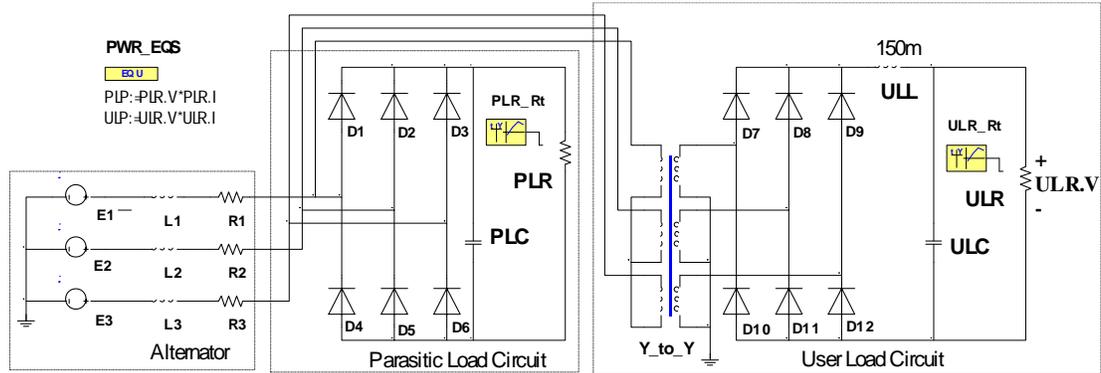
Figure 2: CC #1, six-pulse rectifier for both Parasitic and User Load Circuits.

2. Circuit Configuration #2 (CC #2)

This second circuit configuration, Figure 3, is a conventional twelve-pulse rectifier with isolation transformers for both ULK and PLK. Note that the two six-pulse rectifiers used for twelve-pulse rectification are connected in series. In this series connection, the voltage ratios of the transformers were accordingly stepped down by half for equalizing the DC output voltages in both circuits. The transformers are required in the PLK also to get 12-pulse rectification. The same (CC #1) convention of variable names PLC, PLR, ULC, ULR, and ULR.V are also used here.
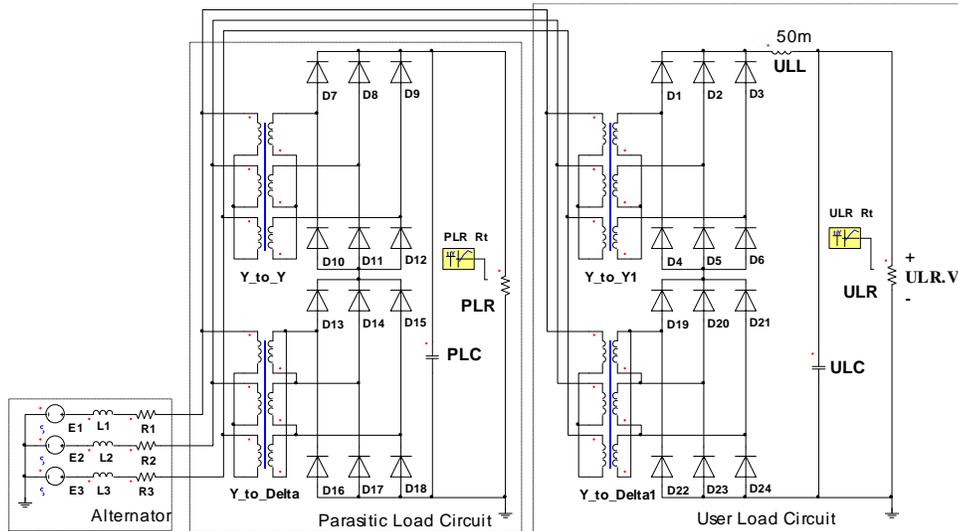

Figure 3: CC #2, twelve-pulse rectifier for both Parasitic and User Load Circuits.

Both of Figures 2 and 3 are obtained from a simulation tool called Simplorer [2] that is currently used for all the simulations.

III. Simulation Parameters

The model properties/parameters described below were taken from the report of a test performed on a 2 kW Brayton power conversion unit [1] at NASA Glenn Research Center in December, 2003 and they are as follows:

Transformers:

Y-to-Y Transformer:	Y-to-Delta Transformer:

Primary winding, per phase
  Leakage inductance: 8 µH.
  Resistance: 1 m Ω.
Secondary winding, per phase
  Leakage inductance: 0
  Resistance: 1 m Ω
Main inductance: 0.1 H.
Resistance for iron losses: 1.0e+018 Ω.
Winding ratio:
1:1 for 6-pulse rectifier.
2:1 for 12-pulse rectifier.
	Primary winding, per phase
	  Leakage inductance: 4 µH.
	  Resistance: 1 m Ω
	Secondary winding, per phase
	  Leakage inductance: 2.31 µH.
	  Resistance: 1 m Ω.
	Main inductance: 0.1 H.
	Resistance for iron losses: 1.0e+018 Ω.
	Winding ratio: $[(\sqrt{3})/2]{:}1$

Alternator:

    Constant average output power: 2 kW.   RMS voltage: 60 V, L-N
    Frequency: 866 Hz.   Resistance, per phase: 10 mΩ.
    Inductance, per phase: 250 µH

Filters:

    Parasitic load filter capacitance, PLC: Variable.
    User load filter capacitance, ULC: Variable.
    User load filter inductance, ULL: 150 mH for CC #1, 50 mH for CC #2.

Rectifier Diodes:

    Forward drop voltage: 0.8 V.   Bulk forward resistance: 1 mΩ.
    Bulk reverse resistance: 100 k Ω.

User and Parasitic Electrical Loads:

    Total constant average power for both Parasitic (PLP) and User (ULP) Loads: 2 kW.

IV. Simulation Cases

The simulations were performed for both circuit configurations at five levels of User Load's power (ULP): 0.2, 0.5, 1.0, 1.5, and 1.8 kW. Since a constant 2 kW (Sec. III) of power is output from the Alternator, the parasitic load consumes the balance of the energy. At each level of the power, ULC values are set at 0, 30, 50, 100, and 180 µF. For each of ULC values, PLC is also set at two values: 0 and 80 µF. Total of 120 simulation runs were executed. The simulation cases and their associated values are summarized as in Table 1:

Table 1: The Simulation Cases.

Cases	ULP, kW	PLP, kW	ULC, µF	PLC, µF
1	0.2	1.8	0, 10, 30, 50, 80, 180	0, 80
2	0.5	1.5	Same as above	0, 80
3	1.0	1.0	Same as above	0, 80
4	1.5	0.5	Same as above	0, 80
5	1.8	0.2	Same as above	0, 80

V. Simulation Results and Design Examples

With the defined scope and given conditions, simulation results and design example will be presented and discussed in the following sections.

A. Simulation Results

Two evaluation parameters were selected for the design references: the *percent peak-to-peak ripples* and *averages* of the User Load voltages (ULR.V). The values of these variables are extracted and calculated from the *steady state* waveforms of ULR.V. They're plotted and presented in the following sections for all simulation cases in Table 1.

1. *Simulation Results for Circuit Configuration #1*

Figures 4, 5, 6, and 7 show the simulation results of the percent peak-to-peak ripple magnitudes and averages of ULR.V for CC #1 at PLC equals 0 and 80 µF, respectively.
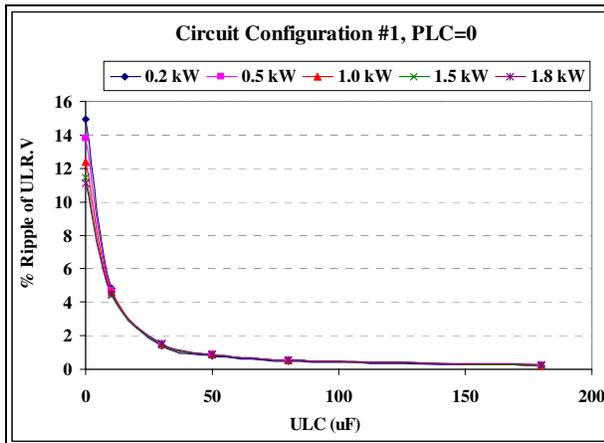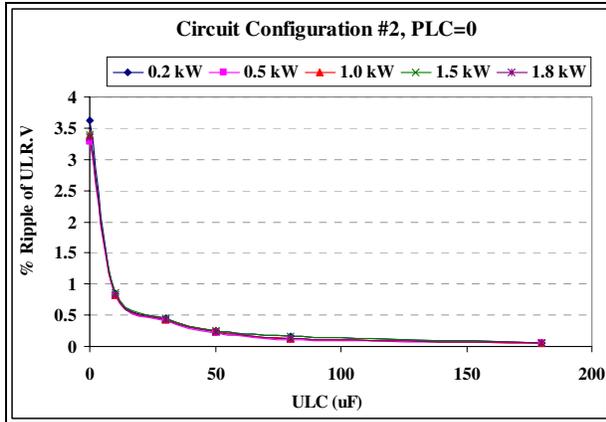

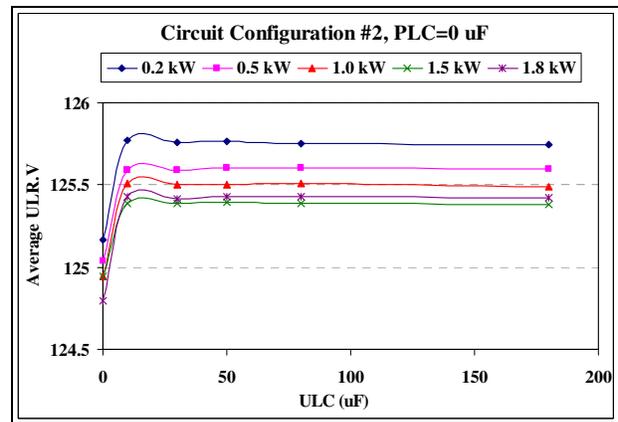**Figure 4: Percent Ripple Magnitude of User Load Voltage for CC #1 with PLC=0.**
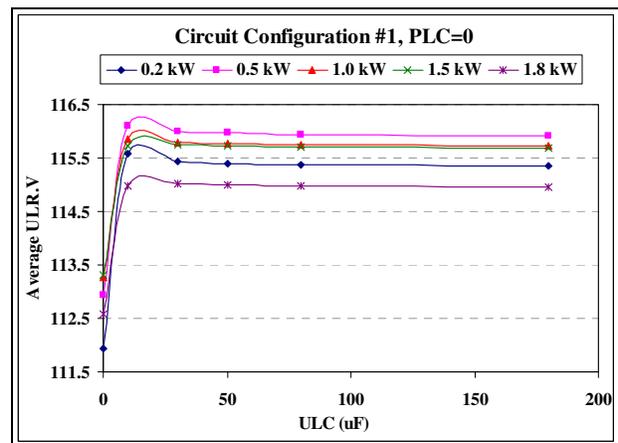
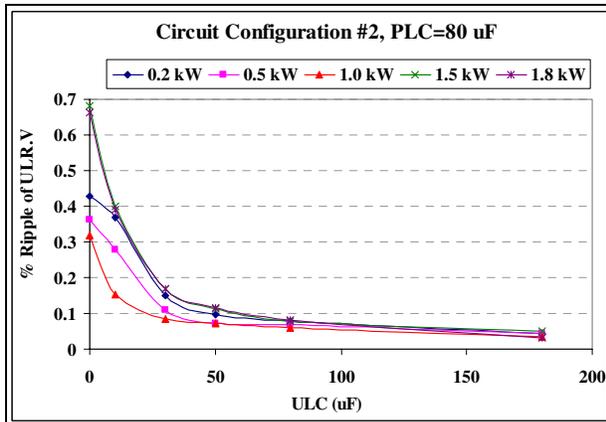**Figure 5: Average of User Load Voltage for CC #1 with PLC=0.**
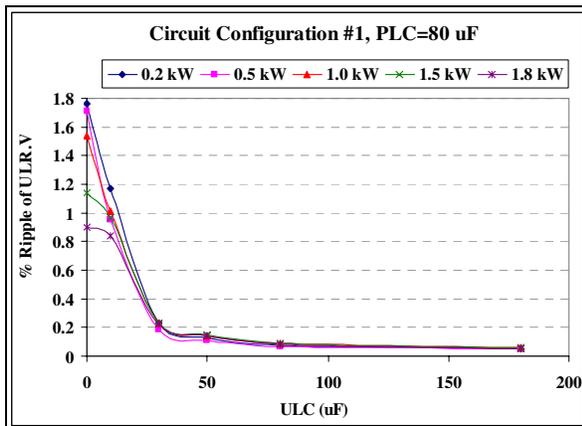
Figure 6: Percent Ripple Magnitude of User Load Voltage for CC #1 with PLC= 80 µF.
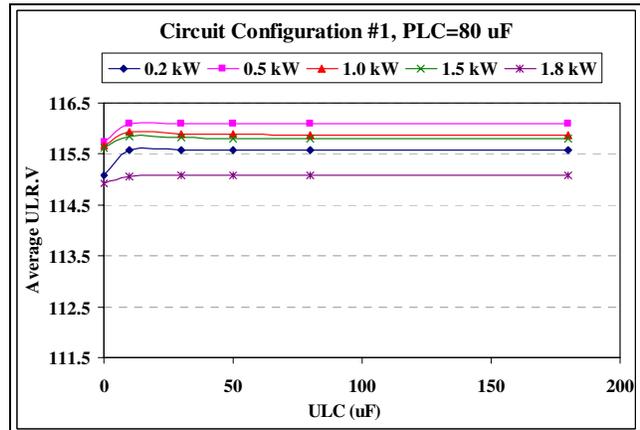
Figure 7: Average of User Load Voltage for CC #1 with PLC=80 µF.

2. *Simulation Results for Circuit Configuration #2*

Figures 8, 9, 10, and 11 show the simulation results of the percent peak-to-peak ripple magnitudes and averages of ULR.V for CC #2 at PLC equals 0 and 80 µF, respectively.

Figure 8: Percent Ripple Magnitude of User Load Voltage for CC #2 with PLC=0.

Figure 9: Average of User Load Voltage for CC #2 with PLC=0

Figure 10: Percent Ripple Magnitude of User Load Voltage for CC #2 with PLC=80 µF.
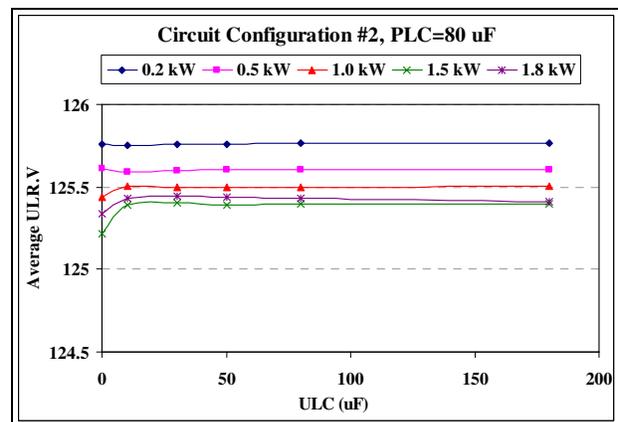

Figure 11: Average of User Load Voltage for CC #2 with PLC=80 µF.

B. Design Examples

The simulation results as shown in Figures 4 to 11 are very useful for engineers/project managers in early phases of the hardware design. For example, if a design requirement is called for *0.25% or less peak-to-peak ripple* of the output voltage, then from the figures, we can easily identify the minimum values for ULC and the deviation of average ULR.V for the full range of power. Thus, key values for this example are extracted from the figures and shown in Table 2.

Table 2: Selection of ULC for ULR.V's Ripple less than 0.25% with PLC=0 and 80 µF.

CC #	PLC, µF	Minimum ULC, µF	Deviation of Average ULR.V, V
1	0	180	115.35 – 115.92
	80	30	115.08 – 116.09
2	0	50	125.34 – 125.76
	80	20	125.40 – 125.75

Notice from Table 2, without PLC, ULC has taken on values as large as 180 µF in CC #1 and 50 µF in CC #2. These large capacitance values might not be compatible with the engine design requirement.

Now let's look at the effects of PLC at 0 and 80µF, with ULC equals zero. The comparison results for this purpose are extracted from Figures 4 to 11 and shown in Table 3.

Table 3: Comparing ripple and average deviation of ULR.V for PLC=0 and 80 µF at ULC=0 µF.

CC #	PLC, µF	% Ripple of ULR.V at 0.2, 0.5, 1, 1.5, & 1.8 kW	Deviation of Average ULR.V, V
1	0	*14.94*, 13.77, 12.35, 11.47, 11.08	111.90 – 113.30
	80	*1.76*, 1.71, 1.53, 1.14, 0.9	114.90 - 115.92
2	0	3.62, 3.28, 3.38, 3.38, *3.36*	124.79 – 125.16
	80	0.42, 0.36, 0.32, 0.68, *0.66*	125.38 – 125.74

From Table 3, we can see that the ripple magnitude is significantly reduced/improved, 88.23% (worst case at 0.2 kW) for CC #1 and 81.21% (worst case at 1.8 kW) for CC#2, when PLC goes from 0 to 80 µF. The deviation of average ULR.V is not very significant. The simulation waveforms of URL.V and ALTR.V for this comparison at 1.8 kW power level for both circuits are shown in Figures 12, 13, 14, 15, 16, 17, 18, and 19.
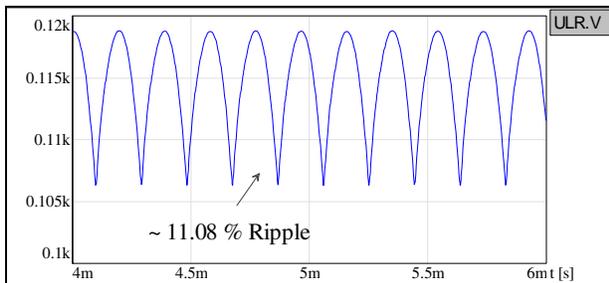

Figure 12: ULR.V (V) Waveform with <u>PLC=0</u>, ULC=0, and ULP=1.8 kW for <u>CC #1</u>.
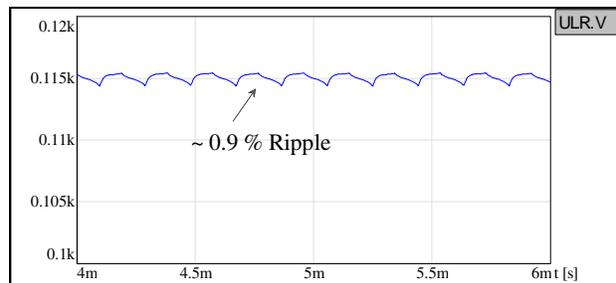

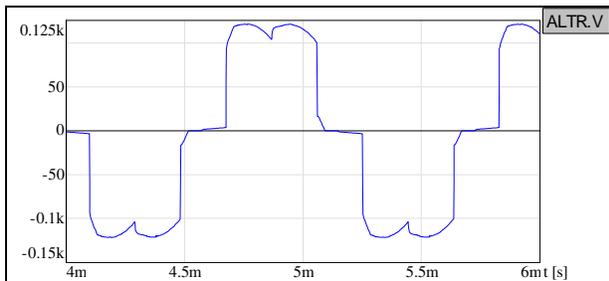**Figure 13: ULR.V (V) Waveform with <u>PLC=80 µF</u>, ULC=0, and ULP=1.8 kW for <u>CC #1</u>.**

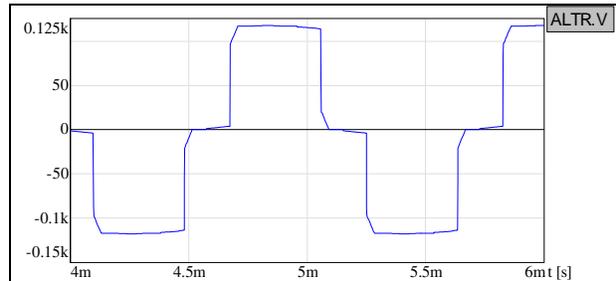**Figure 14: ALTR.V (V) Waveform with <u>PLC=0</u>, ULC=0, and ULP=1.8 kW for <u>CC #1</u>.**

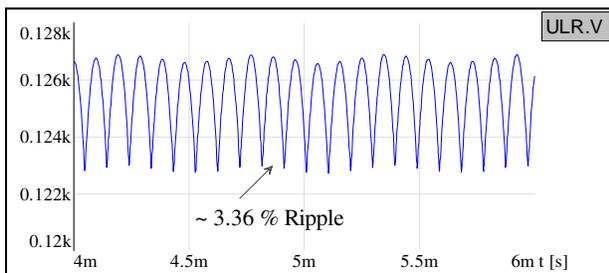**Figure 15: ALTR.V (V) Waveform with <u>PLC=80 µF</u>, ULC=0, and ULP=1.8 kW for <u>CC #1</u>.**

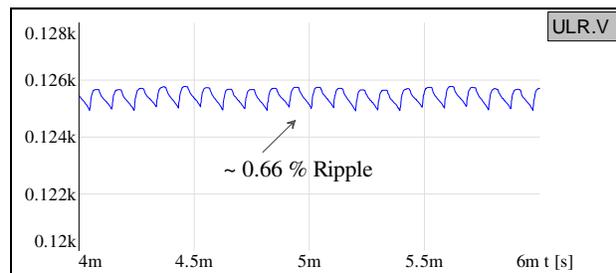**Figure 16: ULR.V (V) Waveform with <u>PLC=0</u>, ULC=0, and ULP=1.8 kW for <u>CC #2</u>.**

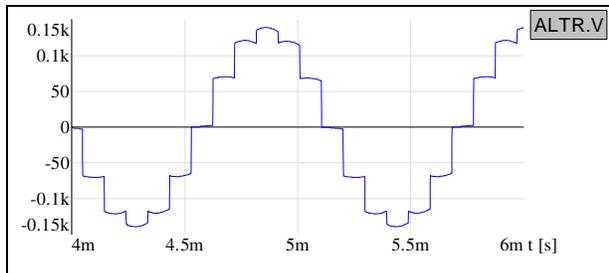**Figure 17: ULR.V (V) Waveform with <u>PLC=80 µF</u>, ULC=0, and ULP=1.8 kW for <u>CC #2</u>.**

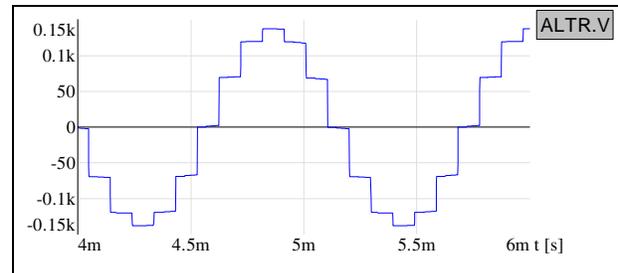**Figure 18: ALTR.V (V) Waveform with PLC=0, ULC=0, and ULP=1.8 kW for CC #2.**

Figure 19: ALTR.V (V) Waveform with PLC=80 µF, ULC=0, and ULP=1.8 kW for CC #2.

This comparison shows an important result: PLC can be properly designed to minimize ULC for the benefit of the spacecraft engine during its recycles (Sec. II). Thus, it is an essential fact which should be seriously considered by the hardware designers.

VI.   Summary and Conclusion

Due to the nature of planned planetary missions, fairly large and advanced thermal dynamic energy conversion systems are expected to be a prime AC power source for the future spacecrafts. Early design considerations of the 3-phase rectifiers for DC user loads of such AC system were discussed:

1) The selection of two targeted circuit configurations (Figs. 2 and 3) which utilize parallel combinations of the six and twelve- pulse rectification methods.

2) The conditions and data collection of 120 simulation cases (Sec. IV) for both selected circuits.

3) The extraction and plotting of two key variables, rectifier's DC average output voltage and its percentage ripple (Figs. 4-11), from the simulation results for design references.

4) The design examples (Sec. IV.B) show how to use the simulation results (Figs. 4-11) to select the value of rectifier's output filter capacitor to reduce risk from damaging spacecraft engine during its recycles.

The simulation results have shown that the waveform of the distribution voltage in a parasitically loaded AC power system can be significantly affected by the amount of capacitance associated with the parasitic load, reducing the filter requirements of the user loads. In a 6-pulse rectifier system, the unfiltered user load ripple can be reduced by an order of magnitude. In a 12-pulse system the reduction is only half as great, but the ripple magnitude is inherently less due to the 12-pulse rectification. The reduced filter requirements for the user loads are particularly significant when using ion engine propulsion systems to reduce the damage to the engine during recycle events, where energy stored in the filter is discharged thru the engine.

The simulations were performed to determine the relative advantages of 6 and 12-pulse systems. Both systems can offer low ripple without extensive filtering. A major disadvantage of the 6-pulse system is the high harmonic content of the distribution voltage, but it may be very applicable in small specialized power systems. A 12-pulse which is heavier and more complex, but the distribution voltage is more nearly sinusoidal, which is desirable in a larger power system with less specific loads and wider distribution.

The system model performed well for this study. Simulation data can be easily obtained for a variety of cases as a design aid.

References

[1] D. Hervol, L. Mason, A. Birchenough, an L. Pinero, "Experimental Investigations from the Operation of a 2 kW Brayton Power Conversion Unit and a Xenon Ion Thruster," Space Technology and Applications International Forum (STAIF-2004), Albuquerque, New Mexico, Feb. 8–12, 2004.

[2] Simplorer V6.0 is a trademark of Ansoft Corporation, www.ansoft.com [cited 15 July 2004].

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13. ABSTRACT (Maximum 200 words)

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