Pixel Reduced Layout
Rev A

IDSG Meeting

September 7, 2000

Overview of Reduced-Layout Study

- Cope with delays in rad-hard front-end electronics
- Goals and constraints
  - Attempt to maintain current rapidity coverage and number of pixel hits.
  - Respect current envelopes
  - Avoid radical design changes that would add even more delay
  - Increase flexibility to respond to still unforeseen delays or potential background problems commissioning LHC.
- How
  - Reduce overall scope
  - Reduce “fixed” part of system that must be installed into barrel region by Spring 2004 according to current schedule
  - Increase “insertable” part of system that can be installed in 2005 after rest of ID is in place
  - Increase production rate of module components and modules

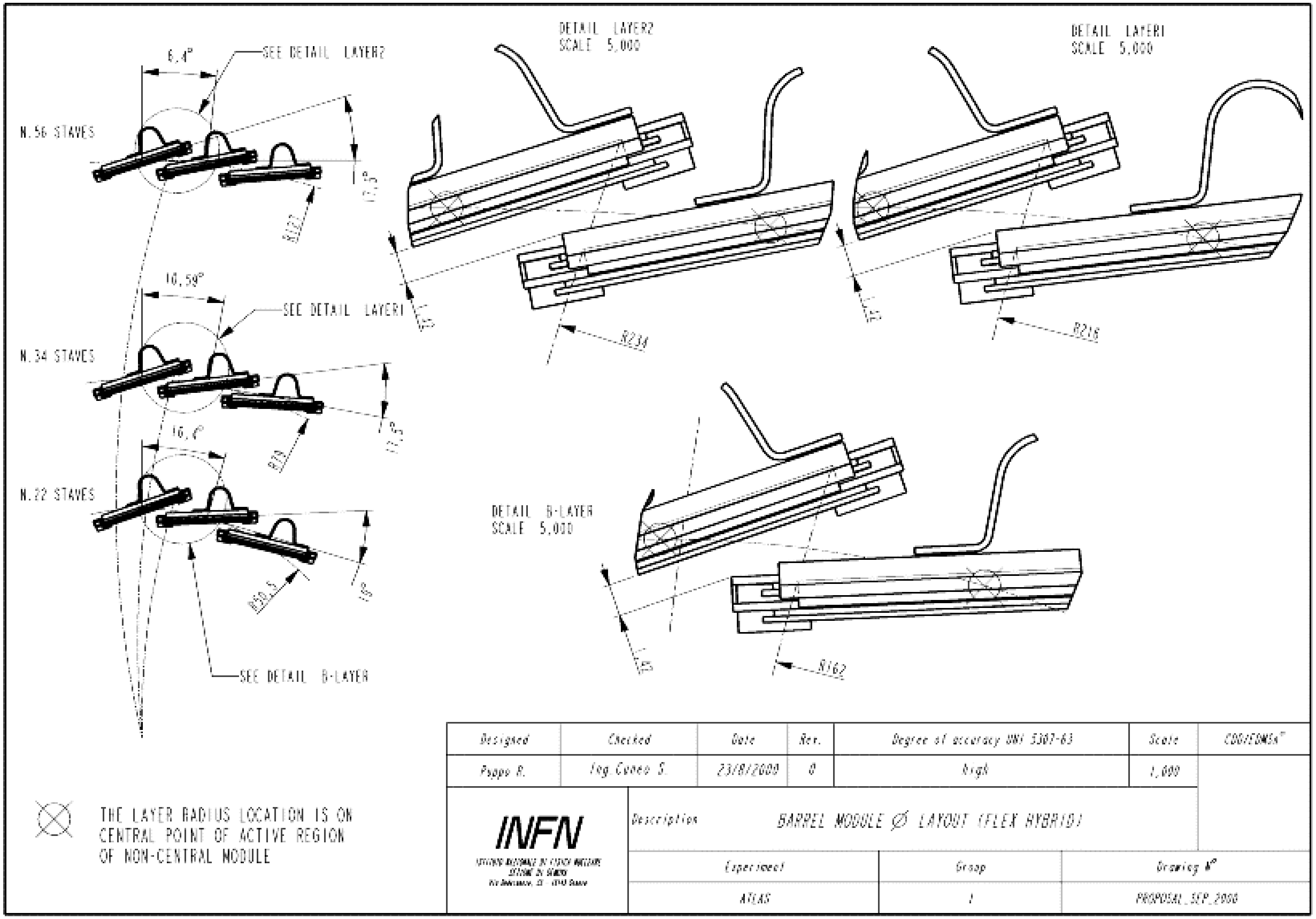
Current Baseline Layout

Barrel						Active	Tilt
	Radius(mm)	Staves	Modules	Chips	Channels	Area(m^2)	Angle(^{o})
B-layer	50.5	22	286	4576	1.76E+07	0.28	-19
Layer 1	93.0	40	520	8320	2.40E+07	0.49	-17.5
Layer 2	127.0	56	728	11648	3.35E+07	0.68	-17.5
Subtotal		118	1534	24544	7.51E+07	1.44	
Disks							
	Inner	Outer				Active	
Z(m)	Radius(mm)	Radius(mm)	Modules	Chips	Channels	Area(m^2)	Sectors
495	121.4	182.2	66	1056	3.04E+06	0.06	11
575	121.4	182.2	66	1056	3.04E+06	0.06	11
640	121.4	182.2	66	1056	3.04E+06	0.06	11
705	99.2	160	54	864	2.49E+06	0.05	9
770	99.2	160	54	864	2.49E+06	0.05	9
Subtotal(Both Sides)			612	9792	2.82E+07	0.57	102
GRAND TOTALS			2146	34336	1.0E+08	2.01	
"FIXED" TOTALS			1860	29760	8.6E+07	1.74	
"INSERTABLE" TOTALS			286	4576	1.8E+07	0.28	

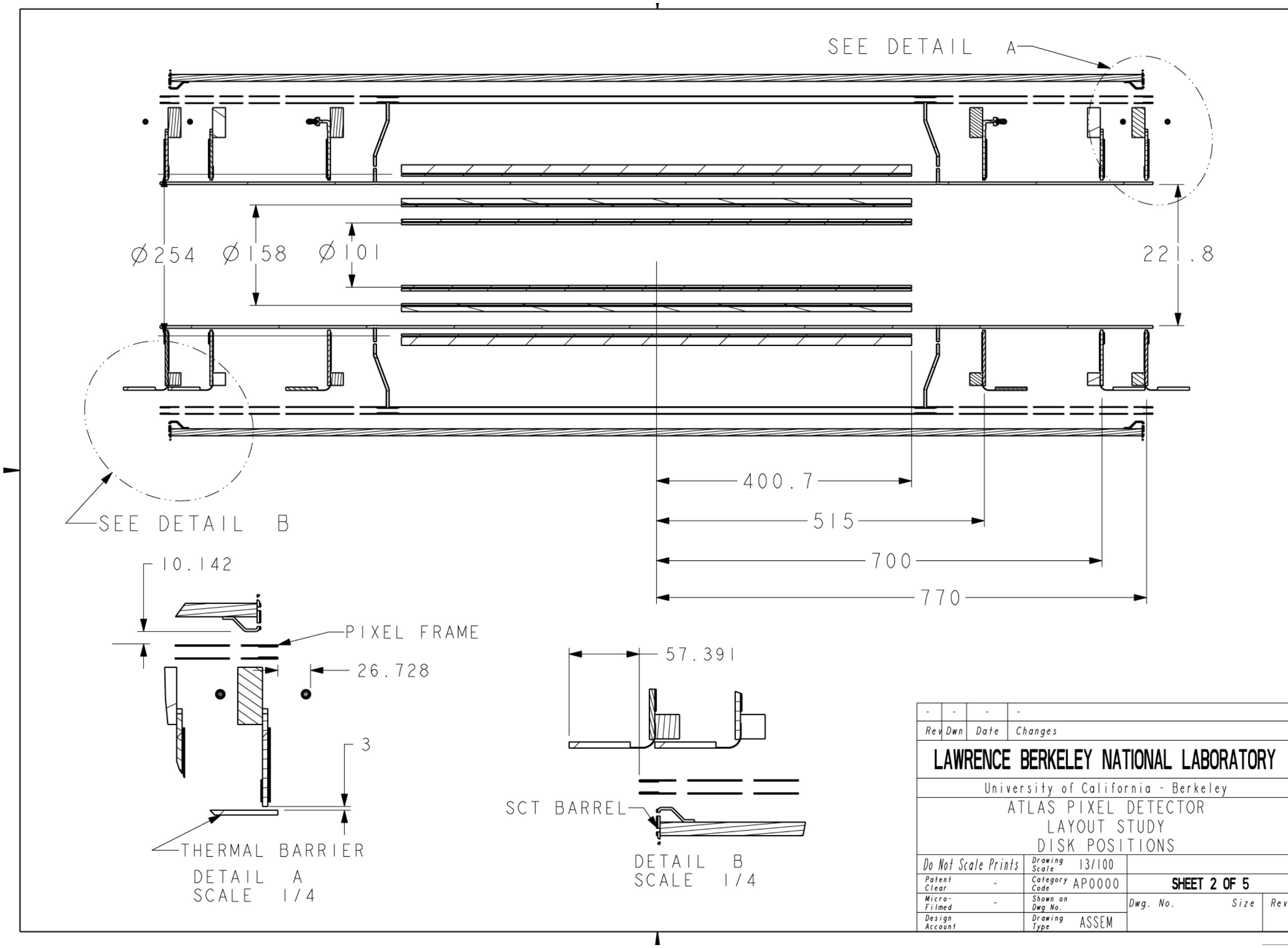
Proposed Reduced Layout

Barrel						Active	Tilt
	Radius(mm)	Staves	Modules	Chips	Channels	Area(m^2)	Angle(^{o})
B-layer1	50.5	22	286	4576	1.76E+07	0.28	-19
B-layer2	79.0	34	442	7072	2.72E+07	0.43	-17.5
Layer 2	127.0	56	728	11648	3.35E+07	0.68	-17.5
Subtotal		112	1456	23296	7.83E+07	1.38	
Disks							
	Inner	Outer				Active	
Z(m)	Radius(mm)	Radius(mm)	Modules	Chips	Channels	Area(m^2)	Sectors
515	121.4	182.2	66	1056	3.04E+06	0.06	11
700	121.4	182.2	66	1056	3.04E+06	0.06	11
770	121.4	182.2	66	1056	3.04E+06	0.06	11
Subtotal(Both Sides)			396	6336	1.82E+07	0.37	66
GRAND TOTALS			1852	29632	9.7E+07	1.75	
"FIXED" TOTALS			1124	17984	5.2E+07	1.05	
"INSERTABLE" TOTALS			728	11648	4.5E+07	0.70	

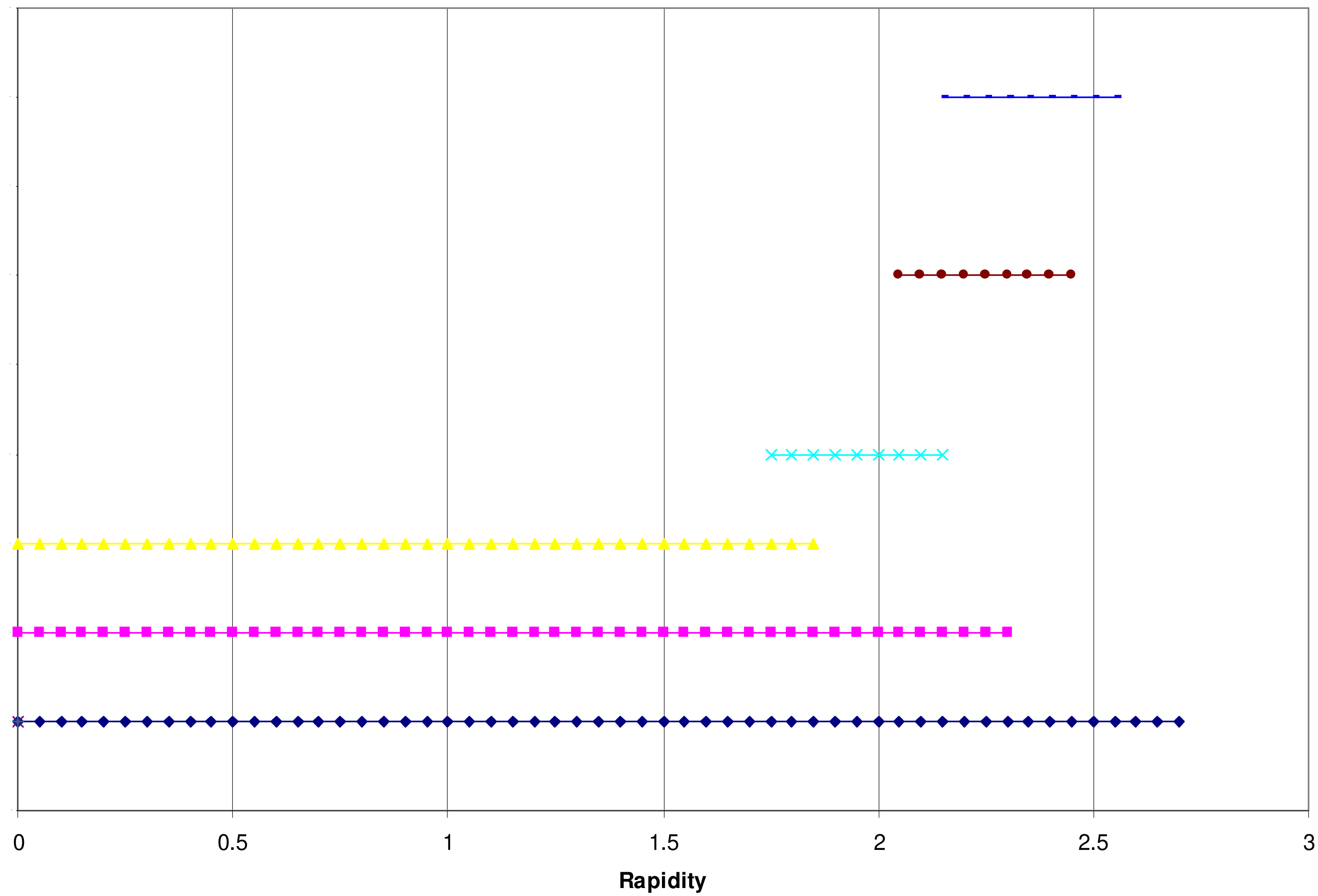
Reduced Layout - Barrel End View



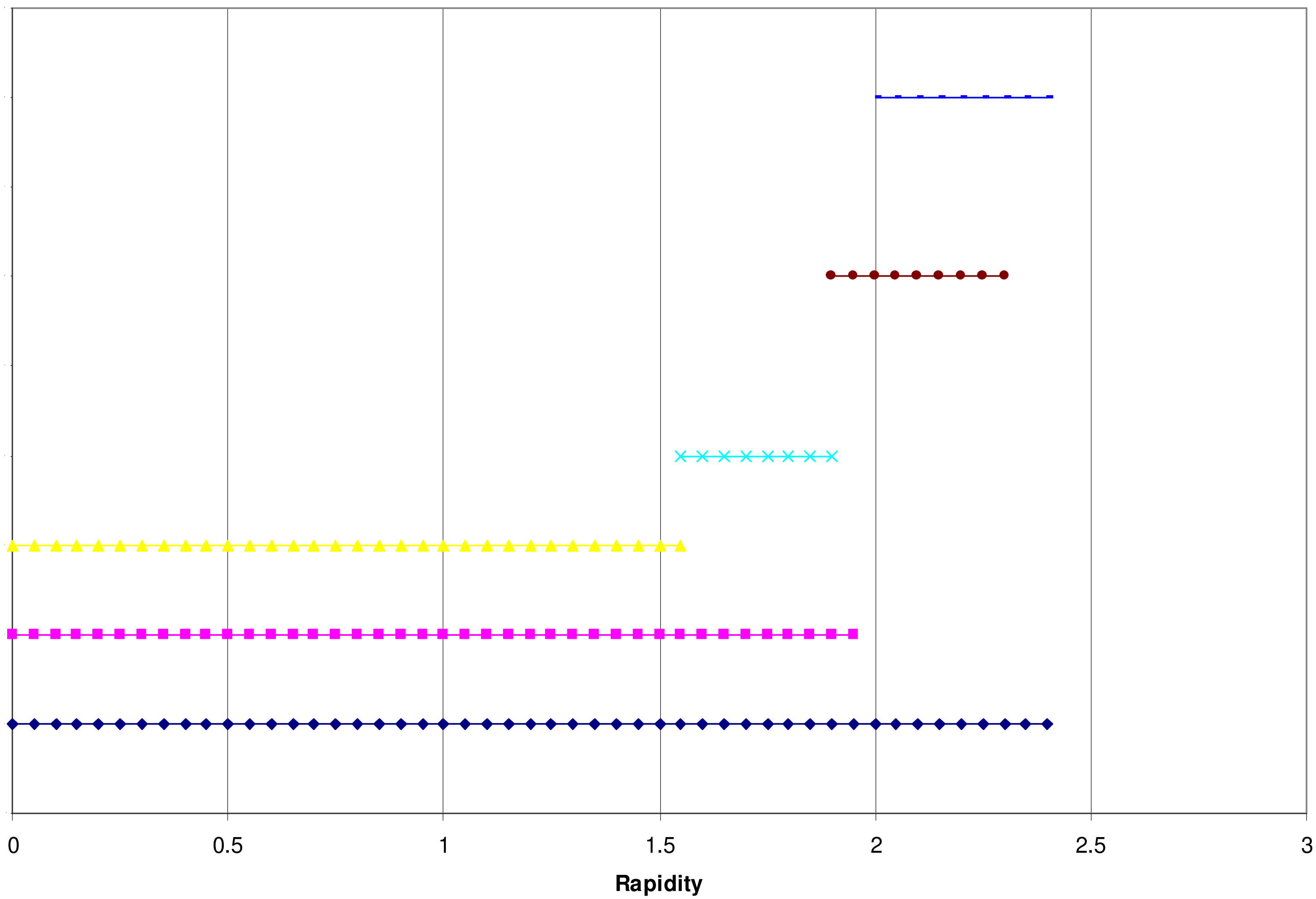
Reduced Layout - Side View



Reduced Layout Rapidity Coverage Z=0



Reduced Layout Rapidity Coverage Z=11cm



Reduced Layout Study - Status

- "Fixed" part of system(modules) is 60% of current baseline => module production schedule for this part correspondingly reduced.
- Minimal changes to mechanical design and services concepts for "fixed" system => no significant additional delays. But greater coordination with ID, forward SCT and beam pipe required to implement larger "insertable" part.
- "Insertable" part of system appears compatible with existing local support(stave/sector) design, but more work on mechanics needed(as would be the case even for a single B-layer).
- Services routing of "insertable" part to be understood in detail, possibility of insertion from both sides,….
- Implementation of reduced-layout in simulation with first results planned for pixel week end of September.
- Increase module component and module production rate - studies underway. Key elements
  - minimize front-end IC full-production time(one year appears possible)
  - faster bump bonding rate eg. by using 3 rather than 2 vendors
- Revised schedule possible by early next year
  - Status of front-end ICs with Temic known by December
  - Simulation results for reduced layout available
  - More known about potential module production rate

Two-Hit-Fallback Options

- Three two-hit fall back options are(in likely order of decreasing performance but increasing ease of the schedule)
  - Option 1 Layer 2 + 2x3 disks + B-layer1
  - Option2 2x2 disks + B-layer2 and B-layer1
  - Option 3 Only B-layer2 and B-layer1
- The number of modules for these are given on the tables on the next pages and summarized below. The rapidity coverage can be determined from the previous plots.

	Numbers of Modules				
	Current	Reduced	Two-Hit Layouts		
	Baseline	Layout	Option 1	Option 2	Option 3
"Fixed"	1860	1124	1124	264	0
"Insertable"	286	728	286	728	728
Total	2146	1852	1410	992	728

Two-Hit Option 1

Option 1							
Barrel						Active	Tilt
	Radius(mm)	Staves	Modules	Chips	Channels	Area(m^2)	Angle(^{o})
B-layer1	50.5	22	286	4576	1.76E+07	0.28	-19
Layer 2	127.0	56	728	11648	3.35E+07	0.68	-17.5
Subtotal		78	1014	16224	5.11E+07	0.96	
Disks							
	Inner	Outer				Active	
Z(m)	Radius(mm)	Radius(mm)	Modules	Chips	Channels	Area(m^2)	Sectors
515	121.4	182.2	66	1056	3.04E+06	0.06	11
700	121.4	182.2	66	1056	3.04E+06	0.06	11
770	121.4	182.2	66	1056	3.04E+06	0.06	11
Subtotal(Both Sides)			396	6336	1.82E+07	0.37	66
GRAND TOTALS			1410	22560	6.9E+07	1.33	
"FIXED" TOTALS			1124	17984	5.2E+07	1.05	
"INSERTABLE" TOTALS			286	4576	1.8E+07	0.28	

Two-Hit Option 2

Option 2							
Barrel						Active	Tilt
	Radius(mm)	Staves	Modules	Chips	Channels	Area(m^2)	Angle(^{o})
B-layer1	50.5	22	286	4576	1.76E+07	0.28	-19
B-layer2	79.0	34	442	7072	2.72E+07	0.43	-17.5
Subtotal		56	728	11648	4.47E+07	0.70	
Disks							
	Inner	Outer				Active	
Z(m)	Radius(mm)	Radius(mm)	Modules	Chips	Channels	Area(m^2)	Sectors
700	121.4	182.2	66	1056	3.04E+06	0.06	11
770	121.4	182.2	66	1056	3.04E+06	0.06	11
Subtotal(Both Sides)			264	4224	1.22E+07	0.25	44
GRAND TOTALS			992	15872	5.7E+07	0.95	
"FIXED" TOTALS			264	4224	1.2E+07	0.25	
"INSERTABLE" TOTALS			728	11648	4.5E+07	0.70	

Two-Hit Option 3

Option 3							
Barrel						Active	Tilt
	Radius(mm)	Staves	Modules	Chips	Channels	Area(m^2)	Angle(^{o})
B-layer1	50.5	22	286	4576	1.76E+07	0.28	-19
B-layer2	79.0	34	442	7072	2.72E+07	0.43	-17.5
Subtotal		56	728	11648	4.47E+07	0.70	
Disks							
	Inner	Outer				Active	
Z(m)	Radius(mm)	Radius(mm)	Modules	Chips	Channels	Area(m^2)	Sectors
Subtotal(Both Sides)			0	0	0.00E+00	0.00	0
GRAND TOTALS			728	11648	4.5E+07	0.70	
"FIXED" TOTALS			0	0	0.0E+00	0.00	
"INSERTABLE" TOTALS			728	11648	4.5E+07	0.70	