FEM to DCM Specification
(Revision 1)

(March 26, 1997)

Packet Header

Sequence No.	20 bits word format (for DC,PC,TEC)	16 bits word format (for TOF,EMCAL, MVD,RICH,BB)	CAV	DAV	Comments
1	all bits "ON"	all bits "ON"	on	off	
2	Detector ID	Detector ID	off	on	* following PHENIX Naming convention (TBD)
3	Event number	Event Number	off	on	* 16 bits L1 accepted event number
4	Module address	Module address	off	on	* following PHENIX Naming convention (TBD)
5	Flag word bit 0 -- zero suppression bit 1 - alternate format	Flag word bit 0 - zero suppression bit 1 - alternate format	off	on	* 0 -- Off 1 -- On
6	FEM Beam Clock Counter(8 bits)	FEM Beam Clock Counter(8 bits)	off	on	

AMU Cells Number Data Block

Sequence No.	20 bits word format (for DC,PC,TEC)	16 bits word format (for TOF,EMCAL, MVD,RICH,BB)	CAV	DAV	
	Not Applicable	AMU Cell Numbers	off	on	* for **TOF, EMCAL,RICH, MVD.** only

Raw Data Block
(Length depend on the sub-system modularity & running condition)

Sequence No.	20 bits word format (for DC,PC,TEC)	16 bits word format (for TOF,EMCAL, MVD,RICH,BB)	CAV	DAV	
	Full 20 bits are used for the data	**Lower 12 bits** are used for the data **EMCAL** use **bit 15** to indicate gain range	off	on	* **No Label bits** are required on the data words

User Word Block
(maximum up to 8 words)

Sequence No.	20 bits word format (for DC,PC,TEC)	16 bits word format (for TOF,EMCAL, MVD,RICH,BB)	CAV	DAV	
	user defined word	user defined words	off	on	* *sub-system defined*

Packet Trailer

Sequence No.	20 bits word format (for DC,PC,TEC)	16 bits word format (for TOF,EMCAL, MVD,RICH,BB)	CAV	DAV	
last-1	Longitudinal Parity word (i.e. X-OR)	Longitudinal Parity word (i.e. X-OR)	off	on	* all previous words with **DAV** on
last	all bits “OFF”	all bits “OFF”	on	off	

TEC Raw Data Block Format

data sequence	channel sequence	Data words			
		bit 19-15	bit 14-10	bit 9-5	bit 4-0
1	0	sample 3	sample 2	sample 1	sample 0
2	0	sample 7	sample 6	sample 5	sample 4
3	0	sample 11	sample 10	sample 9	sample 8
. . . .	. . . .	. . . .	. . . .	. . . .	. . . .
20	0	sample 79	sample 78	sample 77	sample 76
21	1	sample 3	sample 2	sample 1	sample 0
. . . .	. . . .	. . . .	. . . .	. . . .	. . . .
1280	63	sample 79	sample 78	sample 77	sample 76

DC Raw Data Block Format

data sequence	channel sequence	Data words	
		bit 19-10	bit 9-0
1	0	sample 1	sample 0
2	0	sample 3	sample 2
3	0	sample 5	sample 4
. . .	. . .	. . .	. . .
10	0	sample 19	sample 18
11	40	sample 1	sample 0
. . .	. . .	. . .	. . .
800	79	sample 19	sample 18

DC Wire readout sequence

Channel readout sequence	channel No.
1	0
2	40
3	1
4	41
. .	. .
79	39
80	79

DCM-FEM Relationship Summary
(Full Bandwidth Configuration)

Detector	No. of channel	channel/ FEM	DCM Type	FEM/ DCM	Transfer Frequency	Word size	Alternative Format	Raw Data Words/DCM
Beam-beam	128	6	A	11	Beam Freq.*2	16	No	18
MVD	34816	256	A	1	Beam Freq.*2	16	Yes	256/512
DC	12800	160	D	1/2	Beam Freq.*4	20	No	800
PC	69120 X3	2160	P	1	Beam Freq.*2	20	No	108
RICH	5120	160	A	1	Beam Freq.*2	16	No	480
TEC	29312	64	T	1	Beam Freq.*4	20	No	1280
TOF	2048	16	A	8	Beam Freq.*2	16	No	384
EMCAL	24768	144	A	1	Beam Freq.*2	16	Yes	432/720

FEM to DCM Data transfer *Rule*:

(1) All data packet should have ***header + trailer + raw data*** block,
FEM that uses AMU type readout should include ***AMU cell data*** block.
User data block are *optional* for all sub-system FEM.

(2) DC, TEC have to arrange **raw data** block according to DCM specific format as listed above.
For all other detectors **raw data** + **user word** data block can be arranged by FEM.

(3) FEM-DCM communication has exclusive use of **CAV** and **DAV** to indicate data transfer.
CAV and **DAV** must be **off** when not transferring data

(4) FEM ***does not*** have to transmit data continuously but ***do***es have to observe max. event transmission time limit.

(5) ***Max. average event transfer rate*** for FEM to DCM needs to be set to 25 kHz to ensure proper data buffer and bandwidth allocation. This rule will be properly enforced by ***ENDAT bit*** from master timing system.

(6) FEM will use ***ENDAT bit***, distributed by the Master timing system, as the data transfer token.
The FEM holding the token will transmit data.

(7) In ***Half Bandwidth*** mode (DAY-1), we will double the number of FEM's into each DCM.
The maximum average L1 trigger frequency will be reduced to half.

(8) FEM to DCM data format should be the same in the ***Full Bandwidth*** mode and the ***Half Bandwidth*** mode (DAY-1). ***ENDAT bit*** will be used to enforce the proper spacing between two FEM data packets.

(9) In ***Half Bandwidth*** mode, the first FEM to transfer data should be the FEM with the even numbered address, followed by the odd address numbered module. These two addresses have to be consecutive.

(10) Bits ordering of the data following ***HP GLINK transmitter***, HDMP 1012 or 1022, bit ordering.

(11) When FEM has been initialized, FEM clock counter should be set to zero. FEM clock counter should increment at each beam clock after initialization. When FEM receives L1 accept, FEM should store the corresponding clock counter and pack it into the data packet. This implies for multiple L1 accepts, FEM needs to buffer the clock counter. The DCM will use this number to cross check against the Global Level 1 time stamp to ensure that there are no missing clocks at FEM level. The offset between FEM counters and Global L1 time stamp will be determined in the first event at the beginning of new data run.

(12) PHENIX does not have any generally agreed upon recommendation at present as far as "Detector ID" or "Module Address". These two numbers should be treated as if they will be downloaded by ARCNET.

Recommendation

(1) All FEM's should arrange the data in increasing channel number. Data within the same channel should be arranged in increasing timing order.