Electrostatically gated Si devices: Coulomb blockade and barrier capacitance

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Using a device resembling a nano-charge-coupled-device and measuring the Coulomb blockade, we show how the Coulomb blockade degrades with increasing barrier conductance. To explain this behavior, we identify a new parameter, the "barrier capacitance." This parameter can be used to elucidate information about the energy barrier under a gate with a size of a few tens of nanometers. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2240600]

In recent years, the study of devices based on the Coulomb blockade[1] has been pursued by a variety of groups. Among other classes, there has been a fair amount of study in Si-based single electron (SET) devices.[2] These devices have been demonstrated in a variety of geometries and architectures. One basic device is the single-electron tunneling transistor (SETT) which is comprised of two junctions on either side of a central island, with a separate capacitive gate to the island (see Fig. 1).

We have recently[3,4] been fabricating devices that resemble nano-charge-coupled-devices (CCDs), in which the barriers to conduction (tunnel junctions) are formed by fine gates (Fig. 1). This device is similar in its operation to a standard *n*-channel enhancement mode metal-oxide-semiconductor field effect transistor (MOSFET): the heavily doped source and drain regions have electrons as their majority carriers, but the wire does not. Thus, in the absence of applied gate voltages, this device does not conduct between source and drain.

When we apply a positive voltage to the upper gate, this inverts the silicon surface, thus making possible conduction between source/drain and the wire. If we then apply negative voltages to one or more of the lower gates, we can form barriers to conduction along the wire. At low temperatures, where the electrons cannot thermally excite over these barriers, the dominant conduction mechanism is tunneling.[4,5] We note that, in particular, the lower gates do not overlap the heavily doped regions, unlike standard MOSFETs. This difference between these nano-CCDs and standard MOSFETs drives one of the main themes of this letter: by performing Coulomb blockade studies of these devices, we can obtain parameters and elucidate information about the energy barriers that form the junctions. In particular, we can obtain the capacitance of these junctions, a determination which appears possible *only* with Coulomb blockade measurements. We note that previous studies of electrostatically gated SETTs (Refs. 6 and 7) have been performed; one of the advantages of our devices is that, by gating the device with the middle lower gate, we get SET oscillations (see Fig. 3) which are much more periodic than the previous results. This periodicity allows us to do the analysis to obtain the capacitance of the junctions.

One of the common topics of study in MOSFETs has been that of the electrostatics and energetics of the MOS capacitor structure. In particular, the shape of the Fermi energy as a function of lateral position is of great interest; the usefulness of the present work is that the studies in this letter provide an experimental way to gain information about the electrostatics of devices with electrostatically gated barriers.

Devices were fabricated using standard complementary metal-oxide semiconductor (CMOS) processes[2] and measured between 0.2 and 3 K, as noted below. Referring to the device in Fig. 1, we held the upper gate at a voltage of +2 V; the two outside lower gates were held at voltages near −2 V, to form conduction barriers. The middle lower gate LG-C was typically used to control the island potential and varied between −2 V and +2 V.

We performed measurements on three similar devices on three different Si dies, and all results shown in this letter were essentially the same for all three devices.

Figure 2 shows a typical transistor control curve for a single lower barrier. We measured the source-drain current $I_{S\text{-}D}$ and voltage $V_{S\text{-}D}$, and we have plotted the average conductance represented by $I_{S\text{-}D}/V_{S\text{-}D}$. The minimum value of about 1 nS corresponds to our measurement noise floor of about 1 pA. At gate voltages $V_{LG\text{-}D}$ above −2.1 V, the barrier conductance rapidly rises as electrons are able to tunnel through the barrier. We see an exponential dependence over

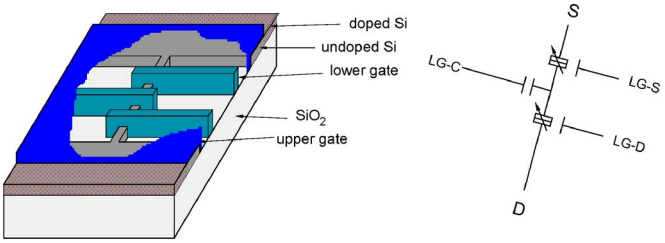

FIG. 1. (Color online) Left side: schematic representation of the device as fabricated. The Si wire runs between two pads which are heavily doped outside the region covered by the upper gate. Right:circuit diagram representing the effect of the three lower gates LG-S, LG-C, and LG-D, but not the upper gate. The two outside lower gates form the tunnel junctions; the middle lower gate is used to modulate the potential of the island and therefore forms the capacitive gate to this transistor.

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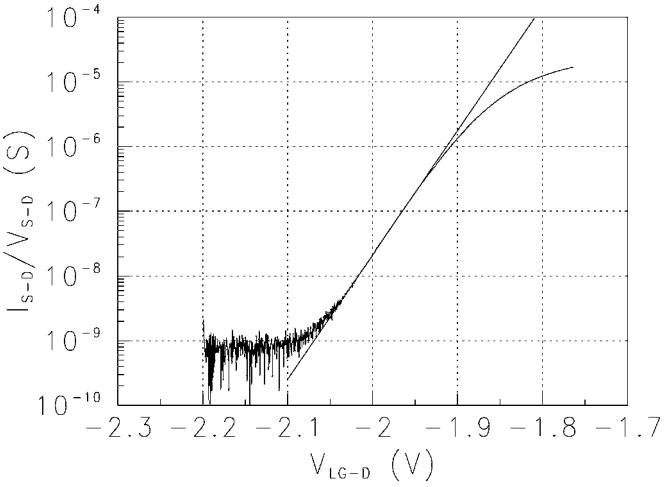

FIG. 2. Measurement of conduction through a single barrier. With the other upper and lower gates set to be conducting, this shows the dependence of the conductance of the single barrier due to the gate closest to the drain. The applied bias voltage $V_{S\text{-}D}=1$ mV and we measure the bias current $I_{S\text{-}D}$. $T=2.3$ K. This curve shows the standard features for a MOSFET: exponential subthreshold dependence and linear dependence above threshold; the threshold voltage is approximately −1.9 V. We have subtracted a parasitic resistance of 67 kΩ.

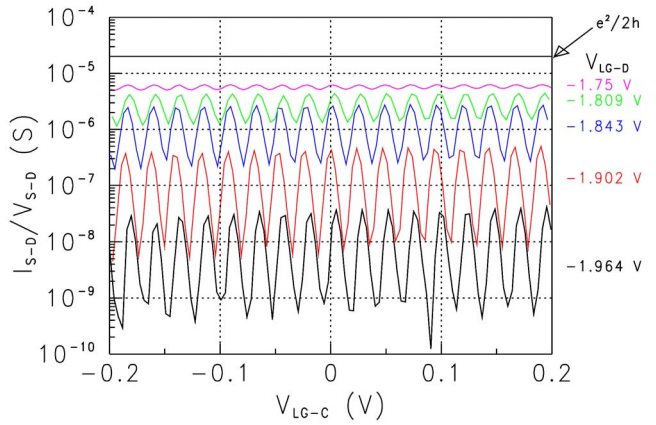

FIG. 3. (Color online) Measurement of SET oscillations for the same device as in Fig. 2. Here, the device is operating as a SET transistor, with the two outside lower gates set to have approximately the same conductance. The five curves shown have a range of conductances from approximately 1 nS to 10 μS. The voltage applied to the drain gate is as indicated; we know that from Fig. 2, the threshold voltage for conduction of this gate is approximately −1.9 V. The horizontal line represents the conductance quantum for two junctions in series, $e^2/2h$. Note that the SET oscillations are reduced in size by a large factor at conductances well below the quantum value. $T=1.5$ K.

several decades of conductance, which could be due to either thermally activated motion or tunneling. In devices with a single lower gate with gate lengths ranging between 8 and 100 nm,[5] the transport switched over from drift to tunneling at temperatures between 10 and 50 K; the data showed herein were for a device with gate length of 40 nm. Thus, we know that the motion is indeed tunneling. At less negative voltages still, as the energy barrier completely disappears and electrons are classically allowed, the dependence weakens to an approximately linear one. The "threshold voltage" where this occurs is approximately −1.9 V in this figure; in the standard MOSFET model, this would be the point at which the barrier disappears (more precisely, at this point, the barrier is low enough that there is significant thermal activation), and thus the transport changes from tunneling to drift.

In Fig. 3, we show the standard SET oscillations of $I_{S\text{-}D}$ versus $V_{LG\text{-}C}$. For each curve, both outside gates LG-D (near the drain) and LG-S (near the source) are set to voltages so that both conductances are approximately the same. Working from the bottom curve to the top curve, the gate voltages to the two outside lower gates are set consecutively less negative, to increase their conductances.

A striking result of this figure is that the size of the oscillations (peak to valley ratio I_{max}/I_{min}) decreased by about a factor of 100 from less conductive to more conductive barriers. We wish to know why this degradation occurs; one obvious answer is that the conductance is getting large enough (near the conductance quantum $e^2/2h$ for two barriers) that quantum fluctuations degrade the Coulomb blockade. We do not believe this to be the dominant cause of the degradation. The horizontal line at the top of the figure represents the value $e^2/2h$, and we note that all curves lie at substantially smaller values than this. Our belief is numerically supported by theoretical predictions for the degradation in the Coulomb blockade due to increasing junction transmission.[8] Using the results of this theory, we estimate that the size of the oscillations should decrease from $I_{max}/I_{min}\approx 100$ for the lowermost curve to $I_{max}/I_{min}\approx 25$ for the uppermost curve; the data show a much larger degradation.

The next most obvious cause for the degradation is that the capacitance of the conduction barriers is increasing. In order to test this, we wish to measure the effective capacitance of the single barriers as unambiguously as possible. In the context of Coulomb blockade measurements, the most straightforward way to do this is with a "diamond diagram." Figure 4 inset shows measurements similar to those in Fig. 3. In contrast to Fig. 3, lower gate LG-S was held fixed, and the three curves shown in the figure correspond to three different values of the other lower gate LG-D. The highest curve corresponds to the two barriers having the same conductance, and successively lower curves correspond to the drain barrier having more conductance. A striking feature of these curves is that the negative slope of the oscillations, indicated by the straight line fits, gets successively less steep as the conductance of the drain barrier increases.

From simple electrostatic arguments,[9] one can show that the slope on this side of the curves is equal to $C_{LGC\text{-}isl}/C_{isl\text{-}D}$; $C_{LGC\text{-}isl}$ is the gate capacitance from the center lower gate to the SET island and $C_{isl\text{-}D}$ is the "barrier capacitance" from the island to the drain. Given that the periods of all curves in Figs. 3 and 4 inset are unchanged, it is obvious that $C_{LGC\text{-}isl}$ is unchanged. Thus, the fact that the slope shown decreases as the drain barrier conductance increases indicates a corresponding increase in drain barrier capacitance $C_{isl\text{-}D}$. This is qualitatively in agreement with the degradation of the Coulomb blockade shown in Fig. 3.

If we quantitatively plot curves, as shown in Fig. 4 inset, and measure the slope, we can obtain the effective barrier capacitance of the drain barrier. We show this in Fig. 4. The major result is as discussed above: the barrier capacitance increases in value as the height of the energy barrier decreases. We emphasize that, rather than fitting to the curves showing the degradation of the SET oscillations, we are using the diamond diagram to derive the capacitance. Because this is based only on a simple electrostatics argument, it is

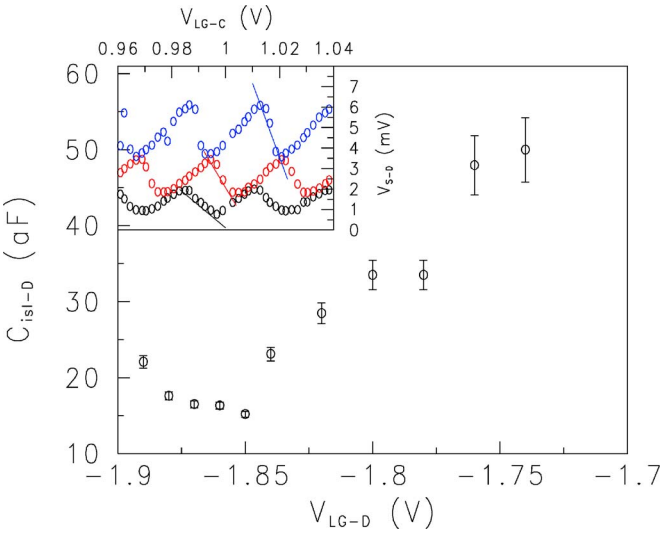

FIG. 4. (Color online) Inset: "diamond diagram" to obtain barrier capacitance. This figure is for a second device, different from the device shown in the previous two figures. The range of V_{LG-D} was over slightly less negative voltages than in the previous two figures. By interpolating a large number of curves of the type shown in Fig. 3 at different bias voltages V_{S-D}, we can obtain the dependence of the bias voltage on the gate voltage at fixed current $I=100$ pA. The curves are offset vertically for clarity, by 0.7 and 2.2 mV. From bottom to top, the values of V_{LG-D} are −1.74, −1.82, −1.86 V, corresponding to drain barrier conductances of 3.1 μS, 770 nS, and 140 nS. Lines are straight line fits to the negative slopes. Main: the barrier capacitance for the drain barrier versus the gate voltage for the drain barrier. These data are derived from the slopes of the lines as shown in the inset and other curves not shown. $T=0.2$ K. The error bars come from the numerical uncertainty in the fitting of the slope. As described in the text, these Coulomb blockade measurements appear to be the only way to measure this effective "barrier capacitance" due to an electrostatically produced barrier.

the most unambiguous way of deriving the capacitance in our opinion. We are unaware of any other technique in Si devices for deriving the capacitance of this barrier formed solely electrostatically by a gate; this result forms the main theme of this letter.

We note another qualitative difference between this device with electrostatically produced barriers and standard MOSFETs. In standard MOSFETs, the gate capacitance dominates, and therefore the potential of the conducting channel is controlled by the gate voltage. In contrast, in these devices where the upper gate capacitance is about 22 aF,[4] the barrier capacitances dominate the total capacitance of the island, and thus the potential of the island is mostly controlled by the bias voltage V_{S-D}.

Finally, we now return to the question: how we can interpret the dependence on barrier height of the capacitance associated with this region?

Full answers to these questions will require a detailed set of comparisons between simulations and experimental results. However, we can obtain basic information about the energy barrier from a very simple consideration. If the energy barrier underneath the lower gate is of a square shape, then as the the gate voltage is increased (conductance increases), the barrier capacitance would remain constant (because the gap between the two conducting regions would remain constant). In contrast, if the upper gate or neighboring lower gates have electrical fringe fields that partially affect the potential under the edges of the lower gate, then the barrier will have a triangular or parabolic or similar shape. In that case, as the peak height of the barrier is lowered, the width of the barrier will also decrease, and concomitantly the barrier capacitance will increase.

From the data in Fig. 4, we can estimate that the width of the energy barrier decreases by about a factor of 3 over the given range of gate voltage. As an example, if we assume that the width at the most negative gate voltage is the geometrical width of the gate (about 20 nm after oxidation), then the width of the energy barrier is about 6 nm at the most positive gate voltage.[10] With modeling and comparison to measurements, we believe that such measurements will be able to elucidate the shapes of the energy barriers under these very short depletion gates.

In summary, we have demonstrated some of the details of a nano-CCD (Ref. 4) which operates in the Coulomb blockade regime. We have shown that there is a "barrier capacitance" when we deplete the minority carrier under the lower gates and have shown empirically how this capacitance depends on the gate voltage. We have also discussed simple estimates one can make of the width of the energy barrier from these measurements.

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[10] We note that the island length is approximately 70 nm and changes by about 4 nm (or twice that). The gate voltages in Figs. 3 and 4 inset are from the middle LG-C which has very little cross capacitance to the outer edges of the island; this is why the period of the oscillations does not change in Fig. 3 and 4 insets.