The HyperCP Trigger-OR Self Inhibit Module

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August 6, 2003

The Trigger-OR Self Inhibit Module (TSIM) is an interface between the essentially asynchronous stream of triggers in a fixed target experiment and the DAQ system. Although the logical operations it performs could be implemented with several standard NIM modules and interconnecting cables, by combining this logic in a single module one can save 50 ns or more of trigger latency. This was crucial in the HyperCP experiment which had $\sim 19,000$ channels whose delays were limited by available cable.

The TSIM fans-in streams of trigger pulses from up to six sources, optionally synchronizes them to an RF clock, outputs a single pulse to the front-end modules (*e.g.* for ADC gates), and then waits for the DAQ system BUSY to end before allowing another output pulse to be produced. A schematic of the main part of this gating logic is shown in figure 1. Detail of the CAMAC and front panel control is given in figure 2 and the output drivers in figure 3. The L1 inputs are first synchcronized to the RF and then hardwire-Or'ed to trigger an ungated one-shot. This ungated one-shot output is available on the front panel (figure 4) for scaling and also triggers a one shot which is gated by the condition INHIBIT.OR.BUSY . The gated one-shot output appears on five outputs on the front panel. The INIHBIT latch is set by this output pulse and cleared at the end of BUSY. Two additional means of clearing are via CAMAC and a front panel pushbutton. For debugging purposes one can force the gated one-shot to be continuously un-INHIBITed by FREE RUN which is generated via CAMAC or a front panel toggle switch. The sequence of operations is shown in the top half of figure 5. This module performed flawlessly at a trigger rate of ~ 100 kHz for two years in the HyperCP experiment.[1]

It would be relatively easy to add level-two (L2) trigger logic with either additional circuitry or, perhaps an external gate generator. In the former case the gated one-shot output would start an L1 timer. A clear pulse would be generated at the end of this L1 timing interval unless a L2-accept pulse was received. The proposed sequence of operations is shown at the bottom of figure 5. These circuit modifications would likely require another circuit board layout.

[1]For a brief period of the 1997 run module forming the DAQ system BUSY signal was malfunctioning and the system would lock-up

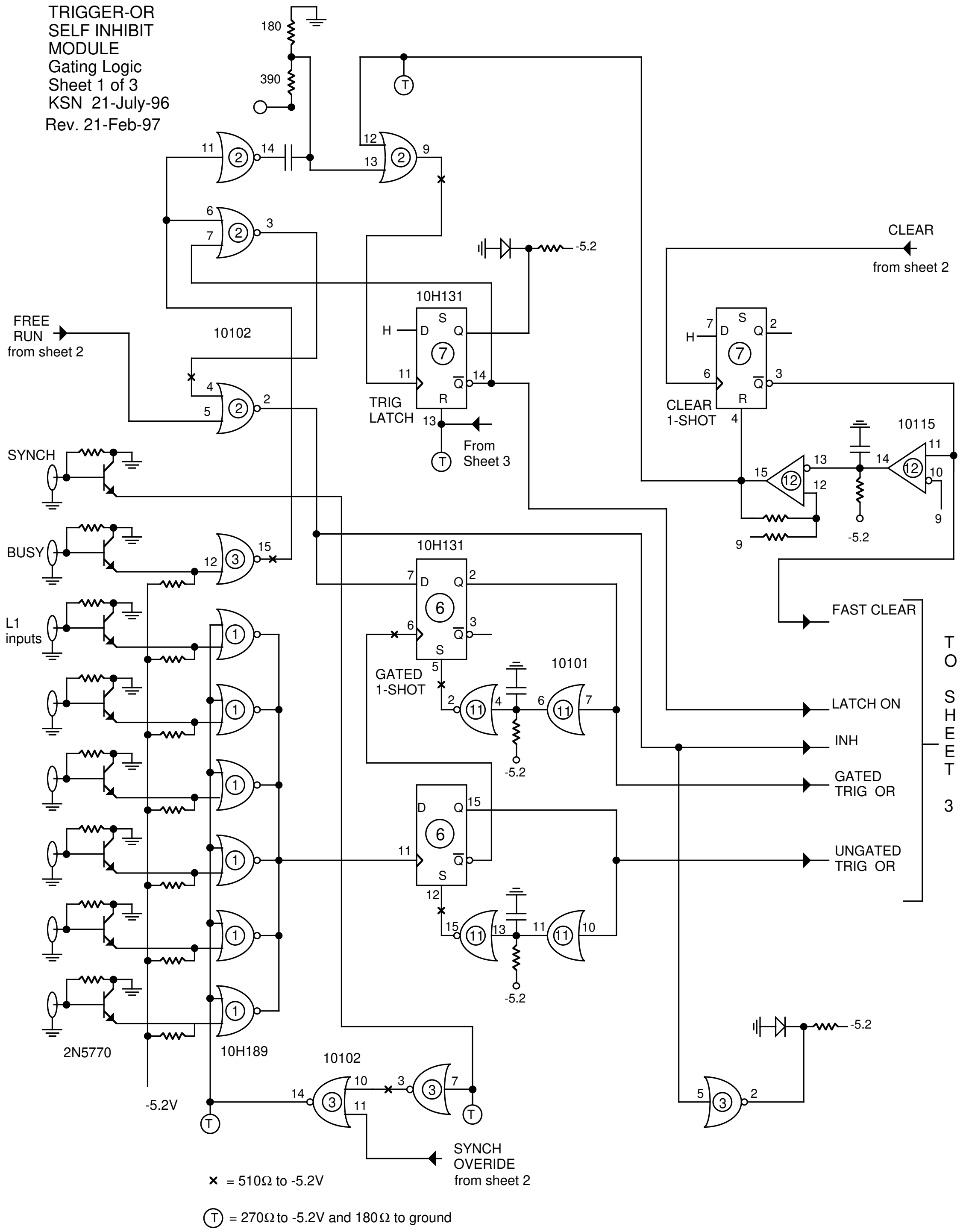

Figure 1: TSIM Gating Logic

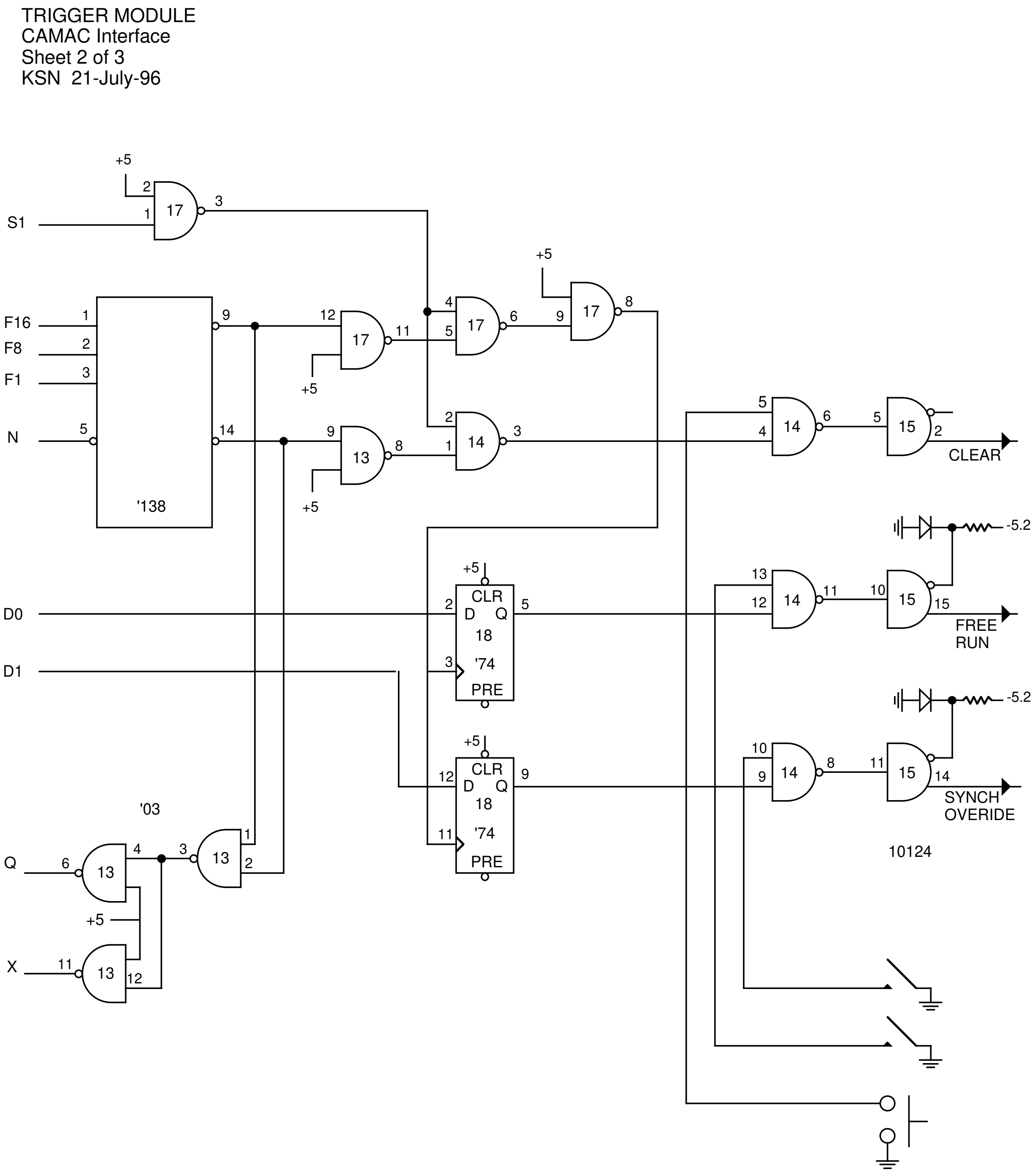

Figure 2: CAMAC and front panel control of the TSIM

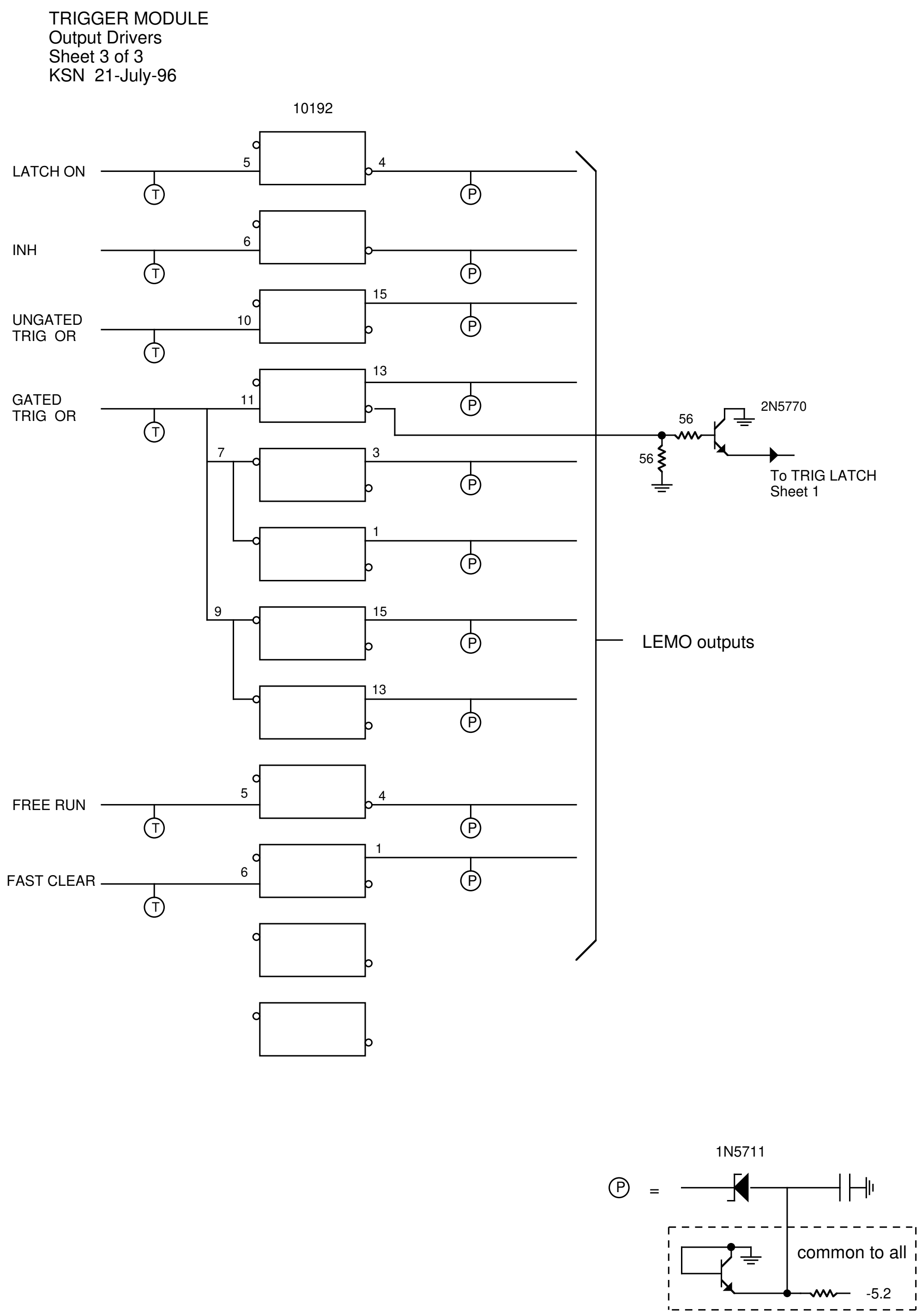

Figure 3: TSIM output drivers

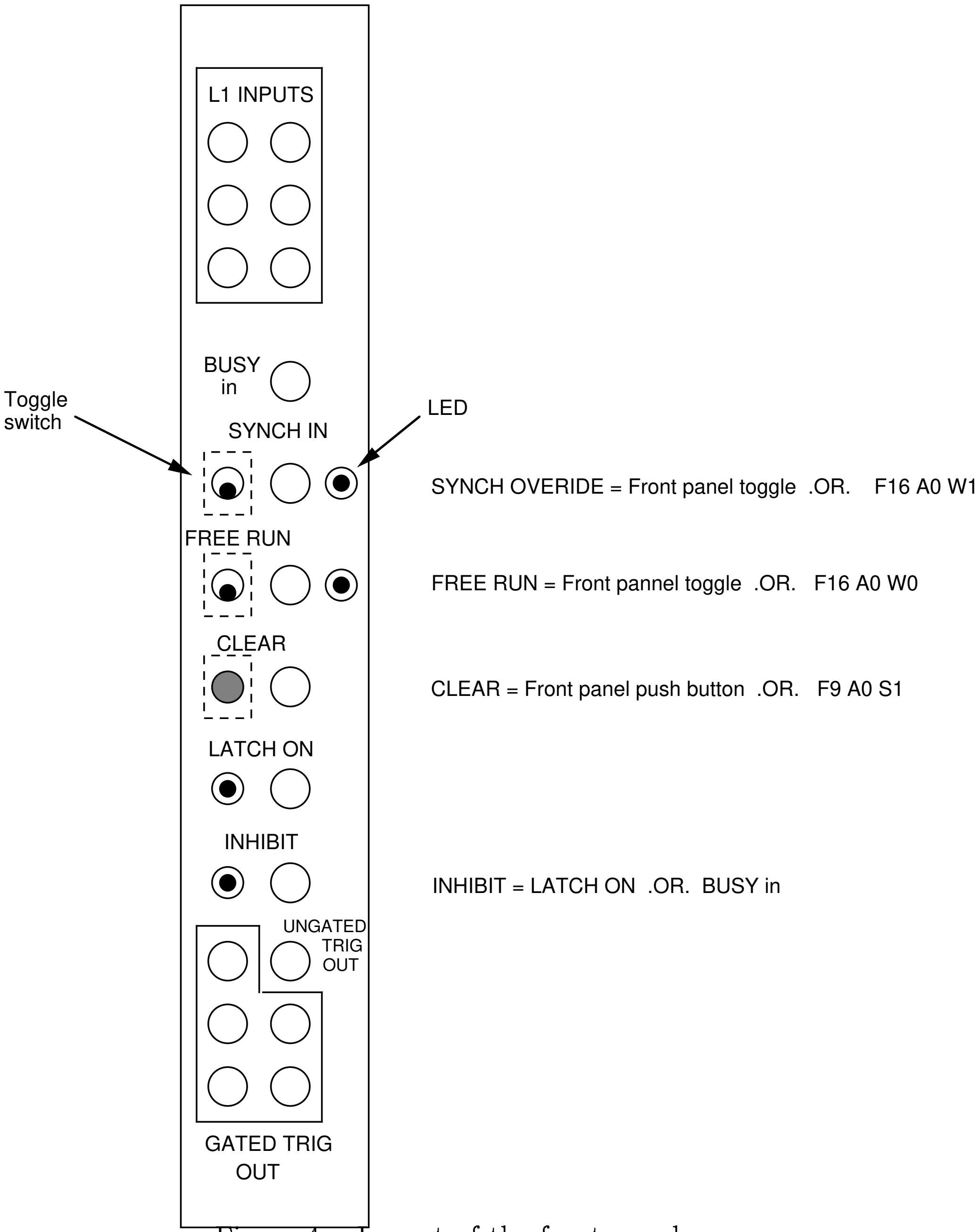

Figure 4: Layout of the front panel

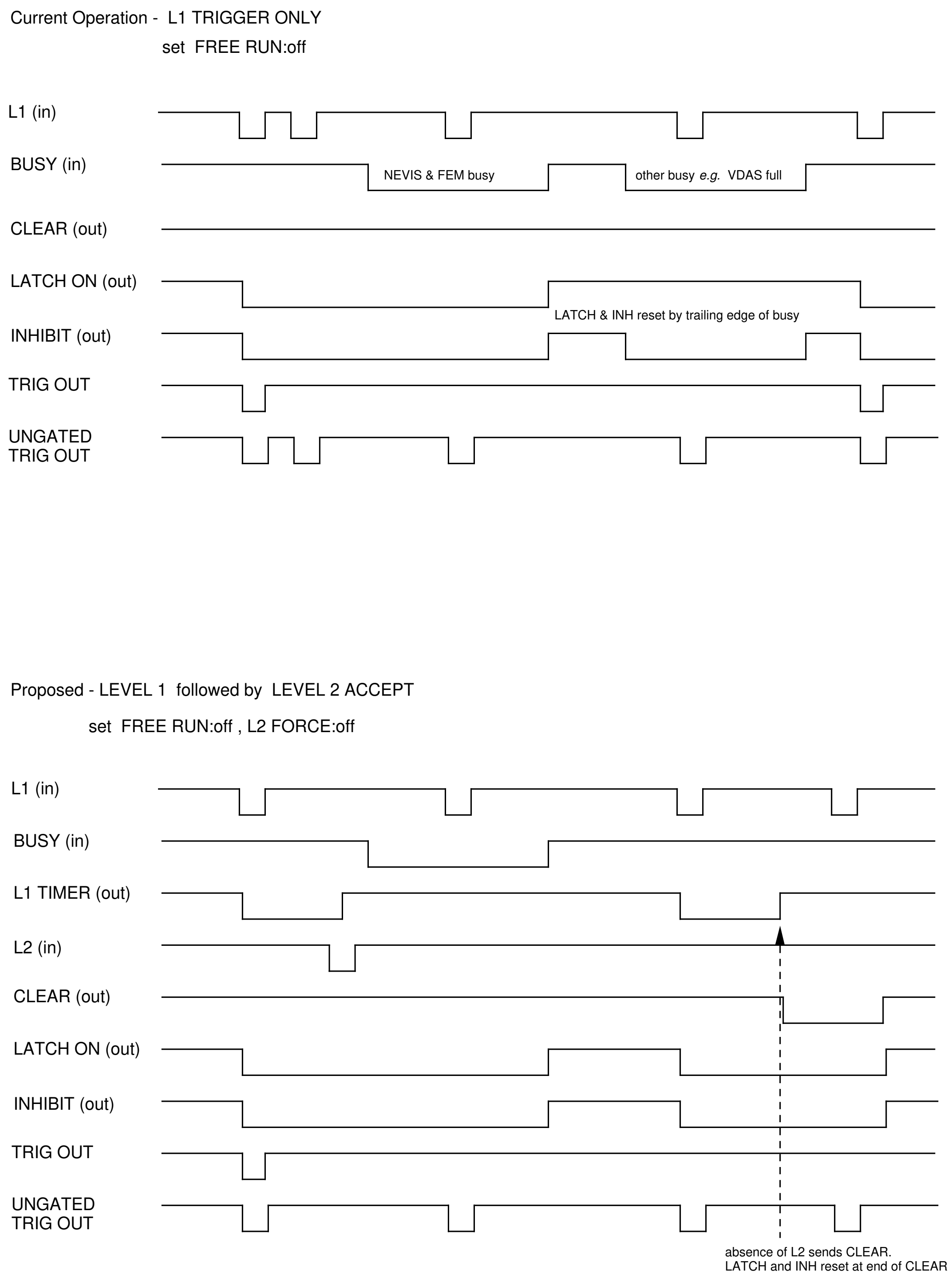

Figure 5: Top:Current TSIM operating sequence, Bottom: sequence with L2 logic