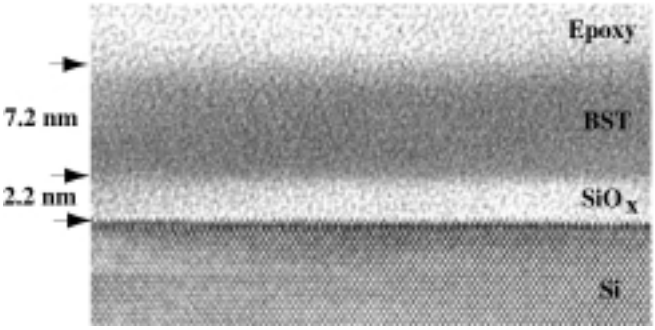
Deposition and Properties of Ultrathin Dielectric Oxide Films

Debra L. Kaiser, Igor Levin

The International Technology Roadmap for Semiconductors projects that traditional silicon dioxide gate stacks will need to be replaced by higher• dielectric materials by the year 2005 to meet the industry's device scaling goals. As a result there has been intensive research on alternative gate dielectric materials. We have developed spin coating processes for the deposition of ultra-thin (< 5 nm) films of ZrO_2 and $(Ba,Sr)TiO_3$, two alternative high• materials. The films are being used to develop nano-scale compositional metrology tools and to investigate processing/structure/property relationships.

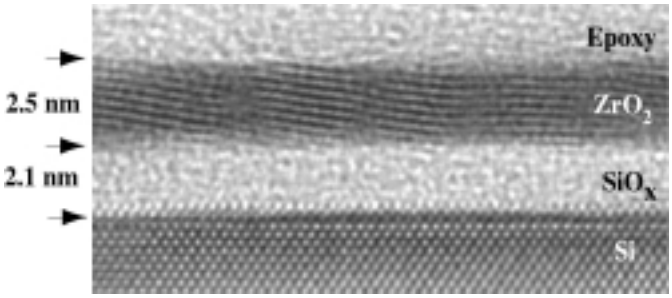
It is projected that oxide equivalent thicknesses below 1.5 nm will be required for the gate dielectric layer in complementary metal oxide semiconductors transistors within the next 5 years[1]. Predictions of unacceptably high tunneling currents in sub-1.5 nm SiO_2 dielectric layers have spurred research into alternative higher dielectric constant gate materials. Candidate materials under consideration are unary oxides such as Ta_2O_5, TiO_2, ZrO_2, and HfO_2, complex oxides such as $(Ba,Sr)TiO_3$ and $LaAlO_3$, and silicates. Characterization of ultra-thin layers of these materials requires the development and application of electrical, structural and compositional metrology tools.

In collaboration with the CSTL, we initiated a project in FY99 on compositional metrology for alternative gate stack materials. Initial efforts focused on developing capabilities to analyze the composition of a model material, chosen to be $(Ba,Sr)TiO_3$ (BST), with film thickness ranging from hundreds of nm (where metrology tools exist) down to a few nanometers. A spin coating process was developed to deposit BST films of precisely known composition from a highly stoichiometric [(Ba+Sr)/Ti = 1.00 ± 0.01] liquid precursor solution onto 50.8 mm (100) Si wafers. By optimizing the solution composition and spinning conditions, films with thicknesses down to 2 nm as measured by x-ray reflectometry and high resolution electron microscopy (HREM) have been fabricated. BST films deposited directly on silicon have an SiO_x interfacial layer, as seen below in the image of one of our films. Analytical methods and correction procedures have been developed to measure the composition of BST films by electron probe microanalysis.



HREM image of a BST thin film (• 7 nm)

Subsequent work by groups outside NIST indicated that BST is not a viable gate dielectric material because it is unstable on Si and has unacceptable electrical properties. Our efforts in FY2000 have shifted to ZrO_2, a promising unary oxide gate dielectric for the 100 nm and 70 nm technology nodes. We have developed a process for spin coating ZrO_2 films onto (100) Si wafers from solutions containing zirconium acetate, propylene glycol, isopropanol and glacial acetic acid. The coated wafers are dried at nominal temperatures of 80 °C, 200 °C, 450 °C and 580 °C in air. By varying the processing conditions (solution composition, ramp rate and spin rate), ZrO_2 films with thicknesses ranging from about 40 nm to 2 nm have been fabricated. Although the silicon wafers are subjected to an HF strip before coating to remove the native oxide, an amorphous SiO_x layer is formed between the film and substrate as illustrated in the HREM image below. The ZrO_2 layer is crystalline with a preferred <111> orientation. The films appear to be smooth and have uniform morphology.



HREM image of a ZrO_2 thin film (• 2.5 nm)

Electrical contacts of Cr (5 nm)/ Au (100 nm) have been deposited onto BST and ZrO_2 spin-coated films. Capacitance and leakage current measurements are in progress in EEEL. Planned work includes exploring alternative processing approaches to reduce the SiO_x layer thickness and determining the effect of structure (amorphous vs. crystalline) on the electrical properties of ZrO_2 films.

[1]*International Technology Roadmap for Semiconductors, 1999 Edition, p. 110.*

Contributors and Collaborators

Chuck Bouldin and Joe Ritter, Ceramics Division
Ryna B. Marinenko, John T. Armstrong, Eric Steel, Chemical Science and Technology Laboratory (CSTL)
Curt A. Richter, Electronics and Electrical Engineering Laboratory (EEEL)