

Adv. Modulation, Coding, Processing and Compression Work Area-5610

GSFC/SOMO Technology Development Program FY01 Annual Review

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Agenda

- Overview
- 5611- Channel Coding at U. of Notre Dame, UC Davis, UH
- 5612- Telemetry at NMSU
- 5613- Data Compression
- 5614 Reconfigurable Data Path Processor
- 5615 Next Generation Digital Receiver
- 5616 Next Generation Level Zero Processor
- 5617 Trellis Coded Modulation Feasibility Study
- Work Area Accomplishments and Plans

Work Area Overview

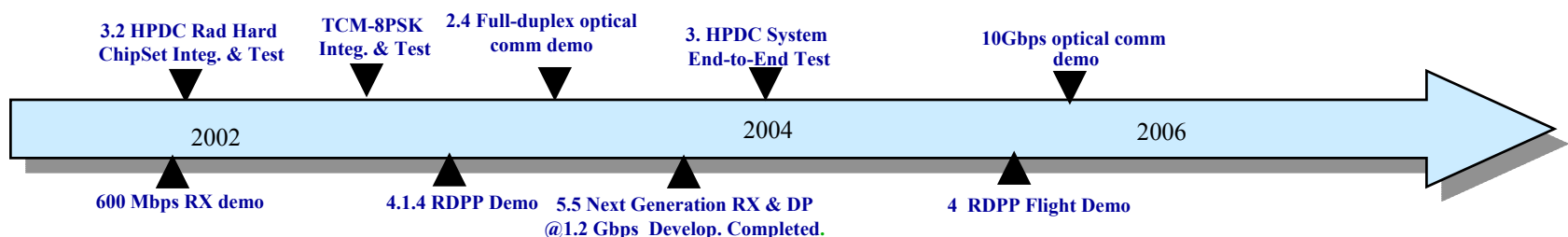
This Work Area strives to return the maximum possible scientific information from instruments onboard a spacecraft to the user/principle investigator (PI) on Earth.

•Objectives

- reduce onboard storage, bandwidth requirement, contact time, quick-look -- high performance data compression and onboard processing
- increase the number of reliably transmitted bits per Hertz of available channel bandwidth -- bandwidth efficient channel coding, modulation, equalization scheme
- provides data transport mechanism-- protocol testing, low-power telemetry
- provides flexibility to ground processing architecture-- low cost high throughput digital receiver and level-zero processing

•Reason-for-Being

- New science instruments produce data volume that require higher bandwidth than currently available, compression and bandwidth-efficient coding/modulation is a “must” for future NASA missions.
- Future missions planning requires “portable” ground stations to receive direct-broadcast data and to provide cross-support -- new communication techniques, protocols, low-cost receiver, level zero processor help to meet requirements



5611-Channel Coding Research Overview

- Goal - **Develop bandwidth efficient channel coding technology for near Earth missions.**
- Benefit- **increase bandwidth utilization with added data protection, high-throughput for encoding/decoding for Ku, Ka bands.**
- Potential Customers -- **All near Earth missions. Previously developed channel coding techniques (CCSDS standards) have been used on HST, TRMM, EOS, MAP, EO-1, ..., and on most international missions. Commercial use includes ---**

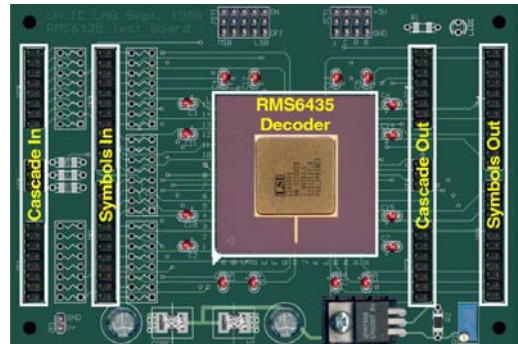
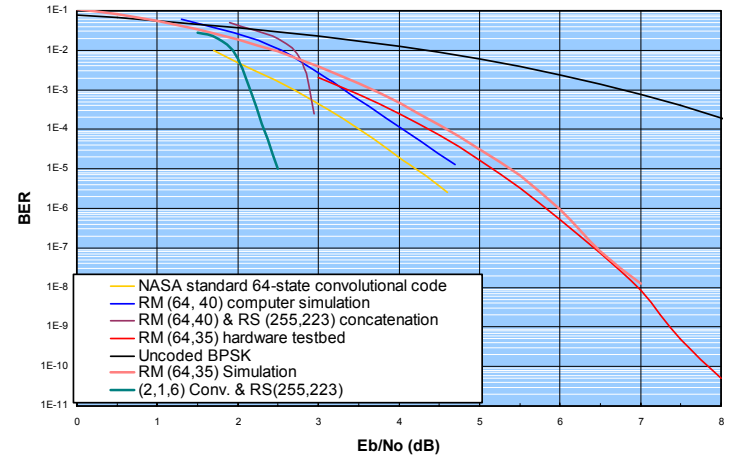
Approach

- **High Rate Channel Coding (HRCC) for a 600 Mbps Viterbi Decoder (UH)**
- **Basic Coding Research at the University of California at Davis and U. of Notre Dame.**

Status- 600 Mbps Reed Muller decoder

- **Accomplished ASIC design and development with LSI Logic, Inc., support. RM(64,35) ASIC tested at 755msps. Block synchronization algorithm developed with FPGA testbed, system tested at 100 Msp.**

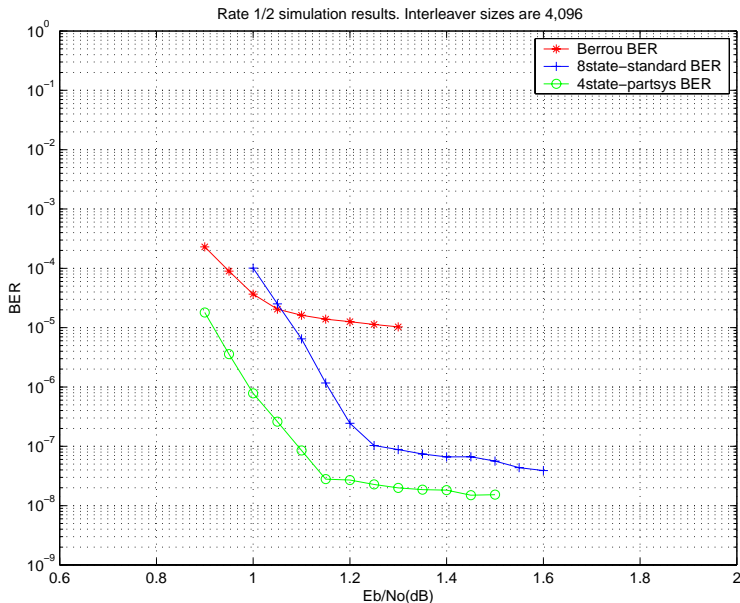
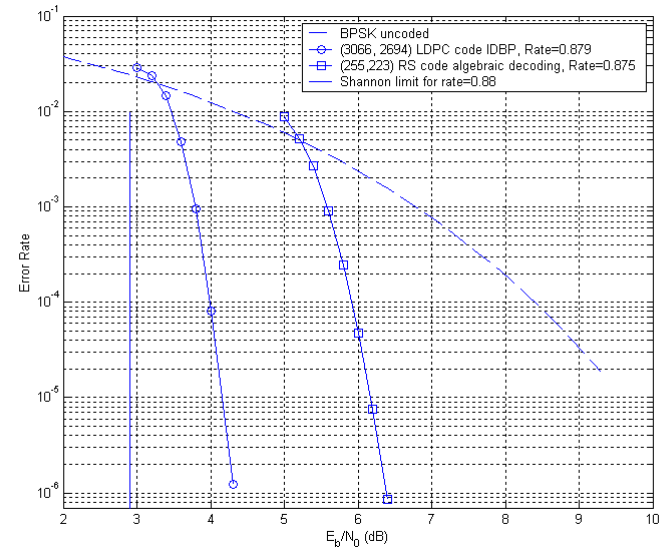
BER Curves for Various Codes



5611-Channel Coding Research Overview

Status - Coding research

- Devised systematic (algebraic) method to construct Low Density Parity Check Code (LDPC) which has performance within 1 db of Shannon limit .
- Devised iterative decoding algorithms for LDPC: multi-stage decoding has potential for very high speed applications.
- Analyzed several concatenated coding schemes
- Devised/analysed several improved Turbo-like code



<u>Concatenated Codes</u>		
<u>Codes</u>	<u>Rate</u>	<u>E_b/N_0</u>
<u>@10^{-6}BER</u>		
RS+Turbo	0.75	3db
LDPC+Turbo	0.75	2.3db
TDRSS	0.44	2.5db

5611-Channel Coding Research Overview

Plans

Reed Muller decoder - **Complete report**

Coding research

- **Continue analytical study of LDPC and Turbo codes**
- **Continue study of concatenated coding system**
- **Investigate higher order coded modulation schemes**

Partnership/Collobration - **LSI logic, NSF**

Infusion/Tranfer/Commercialization - **LDPC has been presented to CCSDS and is pursued by optical communication companies.**

Other information on the coding research by Prof. Shu Lin and Prof. Dan Costello

Total papers presented/published in FY01: 25

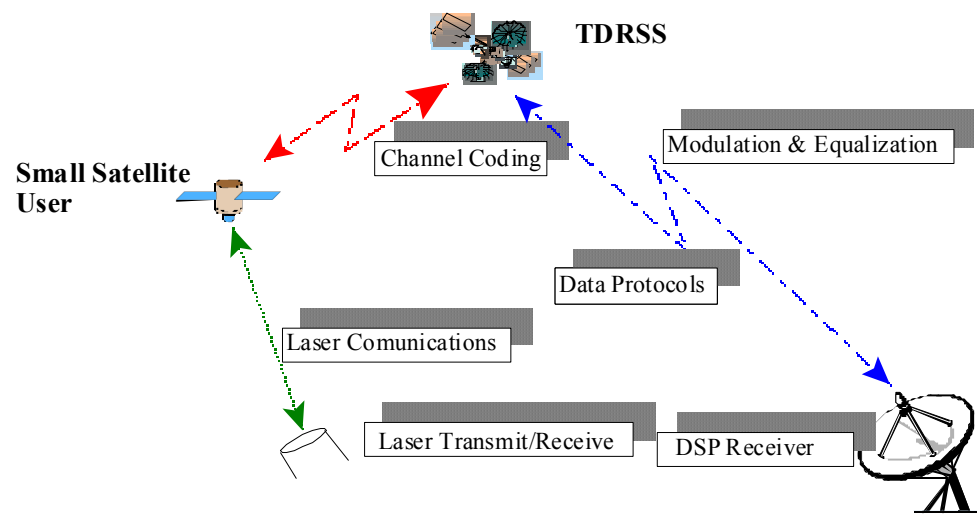
Number of Associates/PostDocs: 3

Number of graduate students:8

5612-Communications and Telemetry Systems at NMSU Overview

Goals/Objectives

- Development of space communications technology to better enable small spacecraft users to access TDRSS and other communications services
- Evaluation of options for more bandwidth-efficient communications via higher-order modulation and non-linear equalization techniques
- Evaluation of space communications protocols by use of channel error simulators and standard software applications
- Evaluation of low-power optical communications techniques for small satellites.



5612-Communications and Telemetry Systems at NMSU Overview

Benefits-

Assist in reducing costs associated with spacecraft antenna system design, communications, and ground network design; assist small satellites obtain support services when high-priority spacecraft are being supported; assists in satellite constellation formation flying.

Reduce bandwidth by a factor of 2 to 4; assist users by evaluating options and techniques and make those results part of the standards development process.

Mitigate user's risk by evaluating protocol for error scenarios; reduce costs associated with Level-Zero Processing.

The potential for the development of spacecraft passive telemetry transmission systems that are lightweight and low power.

Partnerships and Collaborations-

Make study and experiment results available to interested commercial concerns

Working with GRC on FQPSK evaluation

GRC and AFRL for formation flying communications

Arizona State University and University of Colorado for nanosatellite communications

Commercialization Potential/Plan-

Commercial/government CCSDS developers are kept apprised of study results

Space Channel Simulator is of interest to NREN

Patents submitted on optical communications techniques

Other Info: 11 students (8 grad+3under), 6 associates/profs, 11 papers, 6 degrees(2PhD+4MS)

5612-Communications and Telemetry Systems at NMSU Overview

Small Satellite Communications Access

- **Goal:** Develop space communications technology to better enable small spacecraft users to access TDRSS and other communications resources
- **Benefit:** Assist in reducing costs associated with spacecraft antenna system design, communications, and ground network design; assists in satellite constellation formation flying.
- **Potential Customers:** Satellite designers, formation flying designers
- **Approach**
 - Investigating techniques to support formation flying for constellations of nanosatellites, including TT&C and coordination through commercial LEO telecommunications satellites.
 - Examine satellite cluster dynamics to develop constraints on link distance, pointing, and power control requirements
 - Investigate ad hoc and commercial networking techniques to examine cluster configurations and investigate related antenna and power management issues for clusters of small satellites
- **Status**
 - Still looking for LEO telecommunications provider to partner with on using cellular telephone technology for small satellite TT&C from orbit
 - Communications system for 3 Corner Satellite is completed and ready for integration
 - Beginning investigation of communications cluster dynamics and ad hoc networking

5612-Communications and Telemetry Systems at NMSU Overview

- **Plans** Small Satellite Communications Access

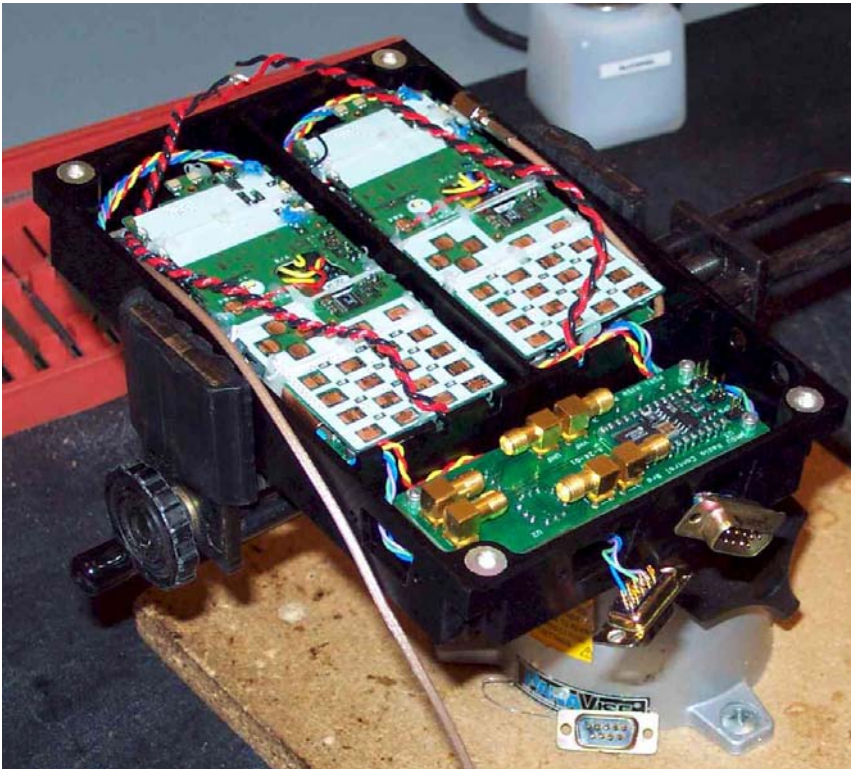
Develop orbital simulations to constrain cluster communications problems

Investigation of ad hoc and commercial networking protocols; communications management

Nanosatellite Communications

- **Development**

- Designed and constructed communications hardware for 3 Corner Satellite communications system
- Passed JSC Phase 0/1 Safety Review
- Working on optimizing radios for allowing TCP/IP support to the satellites in flight



Low-power COTS radio and modem modified for use in a nanosatellite communications system (command, telemetry, and inter-satellite links)

5612-Communications and Telemetry Systems at NMSU Overview

Bandwidth-Efficient Modulation and Equalization

- **Goal** Evaluate options for more bandwidth-efficient communications via higher-order modulation and non-linear equalization techniques.
- **Benefit:** Reduce bandwidth by a factor of 4; assist users by evaluating options and techniques and make those results part of the standards development process.
- **Potential Customers:** Satellite designers, payload designers, CCSDS standards groups
- **Approach**
 - Investigate various CPM waveforms such as GMSK and FQPSK for bandwidth-efficient modulation and make results available to CCSDS committees developing modulation standards
 - Compare overall system performance of non-linear equalization with 16-QAM versus 16-PSK using actual satellite link
 - Investigate synchronization issues with CPM-like waveforms
- **Status**
 - Completed basic FQPSK analysis and reported results
 - Investigating channel equalization techniques that can be applied to satellite channels
- **Plans**
 - Future study will involve: use of higher order modulation, such as the 16-PSK, 16-QAM etc., for spectral and power efficiency study with efficient predistorter design, and nonlinear equalization techniques.

5612-Communications and Telemetry Systems at NMSU Overview

Bandwidth-Efficient Modulation and Equalization

- 1) The CERN processed signals can be applied to higher order modulation such as 8-PSK or 16-PSK. This increases the spectral efficiency significantly (at the cost of BER performance).
- 2) The spectral performance of CERN processed signals can be improved using linearizers or predistorters. Linearizer used along with some backoff==> the spectral efficiency of CERN QPSK becomes better than EFQPSK. (However, it compromises the BER performance). Essentially, it becomes a trade-off between bandwidth efficiency and power efficiency.

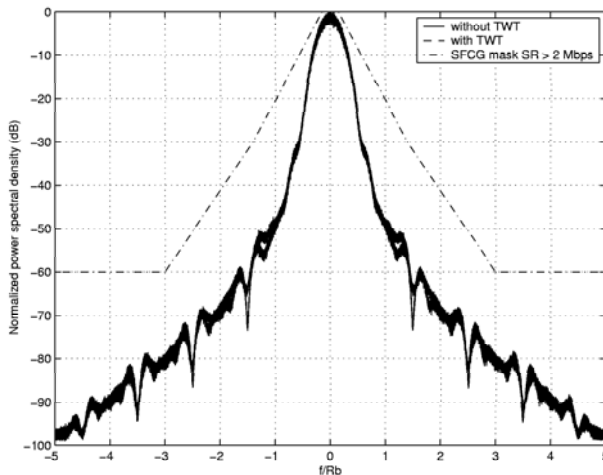


Figure 2: Spectra of EFQPSK. The TWT operates at 0 dB backoff. The figure shows that the effects of the TWT on the spectrum are negligible.

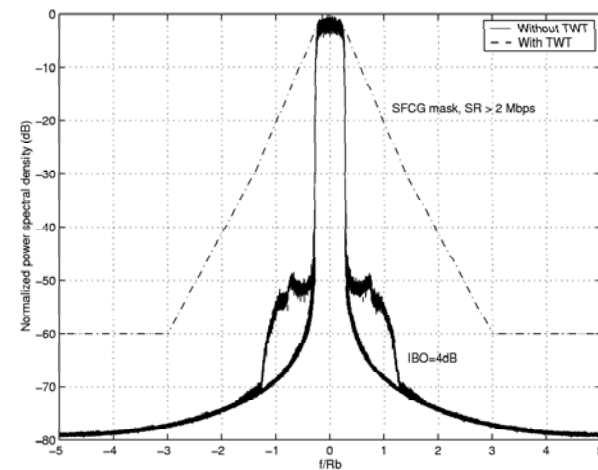


Figure 3: Spectra of QPSK CERN with square root raised cosine filtering (roll-off factor=0.12). The TWT model includes both AM/AM and AM/PM effects and a predistorter is used.

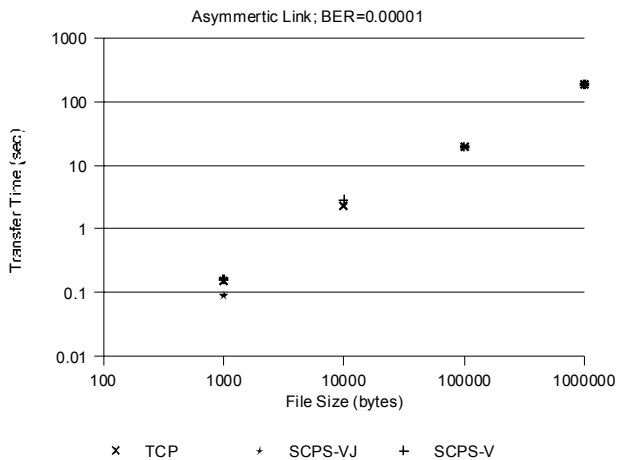
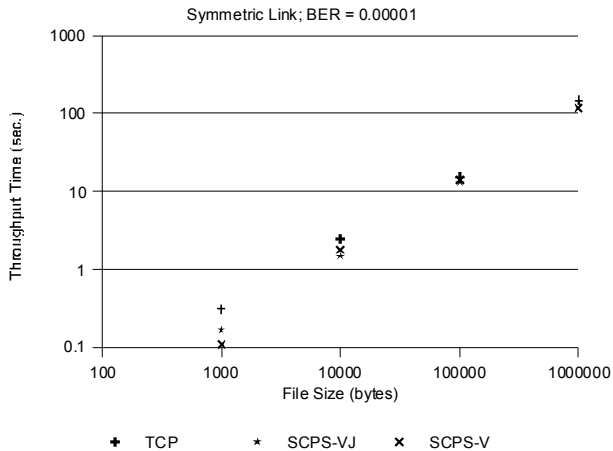
5612-Communications and Telemetry Systems at NMSU Overview

Space Communications Protocol Studies

- **Goal:** Evaluate communications protocols by use of channel error simulators and standard applications.
- **Benefit:** Mitigate user's risk by evaluating protocol for error scenarios; reduce costs associated with Level-Zero Processing.
- **Potential Customers:** Satellite designers, payload designers, CCSDS standards groups
- **Approach**
 - Build upon existing TCP/IP and SCPS protocol testing basis to look at other protocol options, especially those based on UDP.
 - Make channel simulator available over the Internet to groups such as NREN
 - Work with the 3 Corner Satellite program to integrate TCP/IP support into the design of the nanosatellite cluster
 - Integrate other factors such as security into the testbed options
- **Status**
 - Complete TCP/IP and SCPS protocol testing at up to 4Mbps through NRL GEO satellite.
- **Plans**
 - Continue testbed development and increase the number of protocols to be available
 - Plan to incorporate 3 Corner Satellite Internet support to the satellite completed by early 2002
 - NREN has recently expressed interest in having our testbed link with their network

5612-Communications and Telemetry Systems at NMSU Overview

Protocol Testing Result



- For low bandwidth links (< 1 Mbps); GEO hops
 - no difference seen between TCP and SCPS for symmetric links (115 kbps/115 kbps)
 - almost no difference for asymmetric links (115kbps/2.4 kbps)
 - SCPS-VJ 10% better for large files with high BER
- Limited high-bandwidth testing (> 1 Mbps)
 - SCPS-VJ better than TCP/IP
 - TCP/IP better than SCPS-Vegas
 - Flow control algorithm sensitive

5612-Communications and Telemetry Systems at NMSU Overview

Low Power Optical Communications

- **Goal:** Develop low-power optical communications techniques
- **Benefit:** The potential for the development of spacecraft passive telemetry transmission systems that are lightweight and low power with 24-hr coverage
- **Potential Customers:** Spacecraft designers, balloon payload designers
- **Approach**
 - Use circular polarization keying (CPK) on 852nm ground laser for up/down link carrier
 - Use FSK modulation(index 0.1) on beam intensity for sending information forward
 - Conduct ground-based testing of system to provide validation for atmospheric attenuation and interference predictions for low-power optical links
- **Status**
 - Full-up bench testing of both forward and return transmission techniques completed (10kbps rate, <0.5 watt, < 2 pound) -- full duplex on a single optical beam, 'light wire', -- no error detected ovr 10-min link test.
 - Preliminary design for support circuitry to drive modulators and receive data completed and tested in lab
 - Preliminary design for integrating experiment into a Hitchhiker payload underway
 - Testbed for ground "equivalent path length" being assembled

5612-Communications and Telemetry Systems at NMSU Overview Low Power Optical Communications

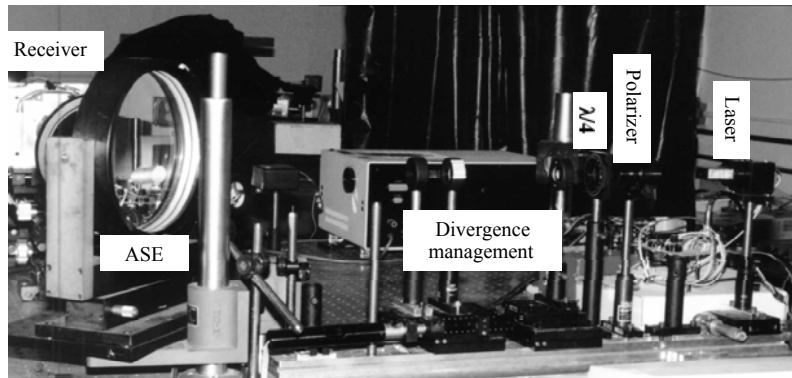


Figure 5.1 The laboratory experiment ground station.

- **Plans**

- The detailed design of Hitchhiker payload to allow for in-flight testing of optical is the basis for a senior-level capstone design class at NMSU during the 2001-2002 year
- Working prototype of hitchhiker prototype to be completed by May 2002 along with basic documentation for Phase 0/1 Safety Review
- Further development contingent on Form 1628 being approved

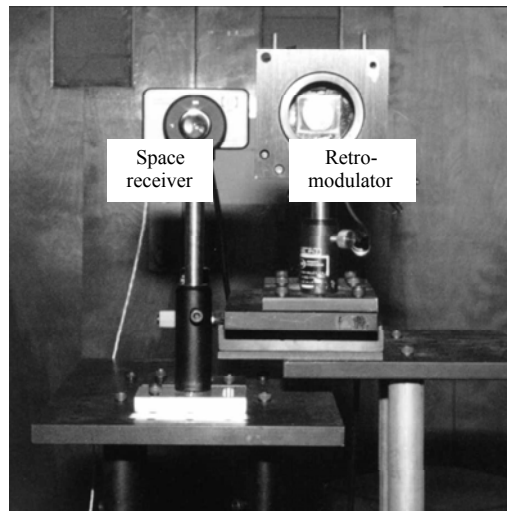


Figure 5.2 The laboratory experiment payload.

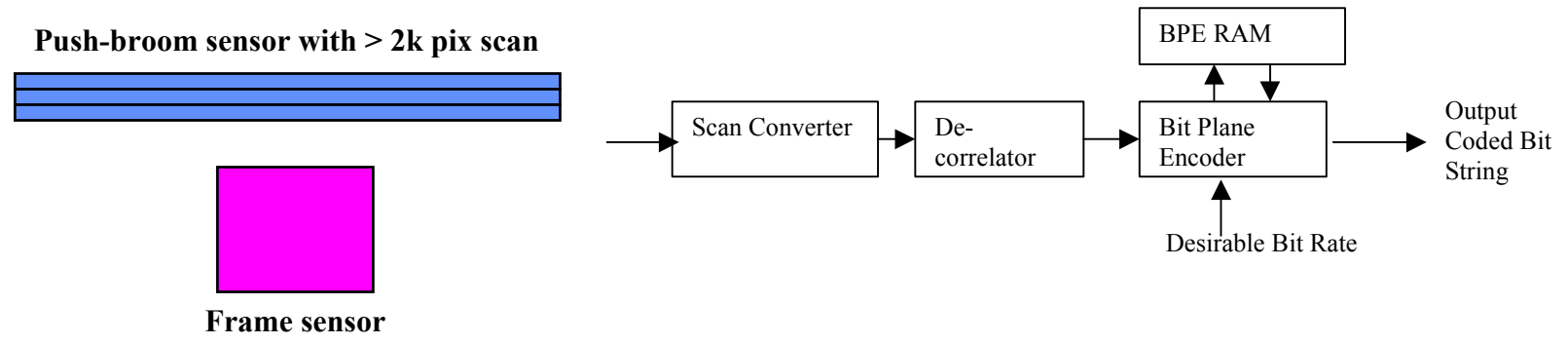
5613-High Performance Data Compression Overview

- **Goal**
 - To develop high speed (> 20 Msamples/sec) onboard data compression technology to maximize scientific information return from space platforms that have either constrained communication channel bandwidth or limited onboard buffer capacity.
- **Benefit**
 - Provides quick look capability for intelligent instrument control, mission planning
 - Provides direct broadcast capability of weather, landscape imaging data for quick assessment of emergency
- **Potential Customers**
 - NOAA LRPT, MOLS/DMSP
- **Approach**
 - Devise algorithms that work well with both push-broom and frame-based sensors and meet requirements for onboard implementation
 - Develop simulation software
 - Develop ASIC chips to implement the algorithm
 - Lab demonstration of hardware

5613-High Performance Data Compression Overview

High Performance Data Compression Algorithm and ASIC Chip Set

- TRL 3
- Features/Performance



- **20 Msamples/sec**
- **8-16 bits/sample input**
- **No external rate adjustment needed**
- **No upload of tables**
- **Progressive decoding for quick look**

• Status 5613-High Performance Data Compression Overview

- Selected by CCSDS standards group as one of the two candidates
- Simulations and comparative study performed on 21 test images
- ASIC chip design (in Radiation Tolerant) at U. New Mexico's MRC:
 - 1st generation de-correlator chip (EDCT) completed in FY00
 - BPE chip (the largest RT chip MRC has ever designed)
 - architecture fixed after several iterations to meet 20 Msamples/sec and ~3W power
 - 0.25u CMOS with 5 metal layers (TSMC), dual voltage(3.3v I/O and 2.5v core)
 - logic design 65% complete
 - on-chip RT RAM design begin (total 240k bit-cell)
 - total logic gates ~ 200k (equivalent commercial RT gates will cost > \$0.5M for initial fab)
 - software simulator co-design 30% complete

• Plans (FY02,FY03)

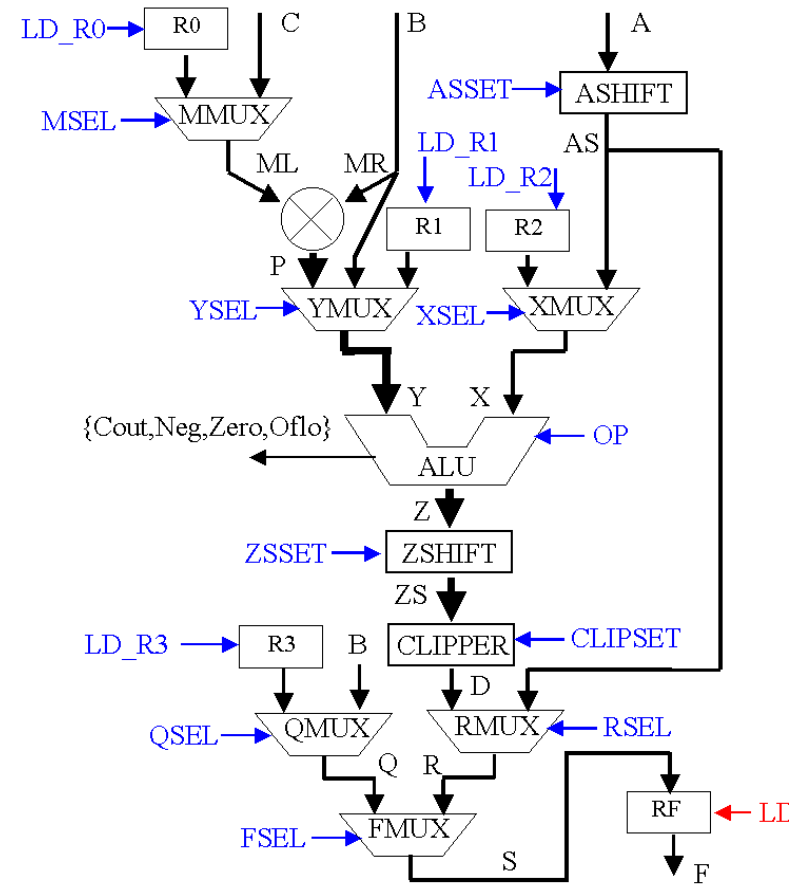
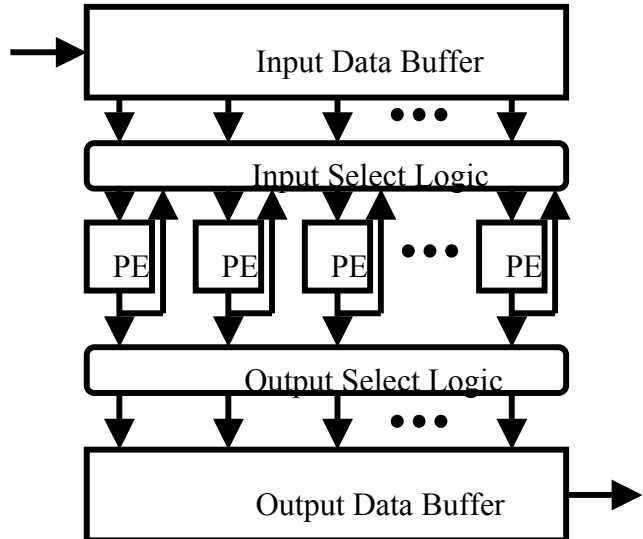
- Complete BPE logic design/verification, layout, fault grading (4QFY02)
- Complete BPE fab/test (2QFY03)
- Begin 2nd generation de-correlator architecture study (3QFY02)
- Begin iBPE design (4QFY02)
- Complete encoder testboard design(2QFY03)
- Demonstrate encoder system (4QFY03)
- Complete iBPE design(4QFY03)

5614-Reconfigurable Data Path Processor Overview

- **Goal**
 - Develop and demonstrate reconfigurable data path processor (RDPP) integrated circuit along with higher level programming language for performing onboard science data processing.
- **Benefits**
 - Provide high-performance, low-power, radiation-tolerant computation (>500MOPS/watt) for data-intensive payloads, especially image and signal processing.
 - Provide capability to extract features from science data, thus reduce bandwidth requirement.
- **Potential Customers**
 - All future science missions
- **Approach**
 - Develop computing methodology based on multiple processing elements (PEs)
 - Analyze onboard processing algorithms to help define PE architecture
 - Develop radiation tolerant (RT) integrated circuit which contain 16 Pes
 - Develop entry level software, compiler, simulator

5614-Reconfigurable Data Path Processor Overview

- **Status**
 - Complete application study in: pixel readout calibration, DFT, FIR filter
 - Complete version 1c spec for processing element (PE)
 - Complete study on data representation scheme within PE.
 - Complete behavior VHDL model for PE
- **Plans(FY02)--SOMO funding \$0k, work proceeds under ESTO funding**



A processing element

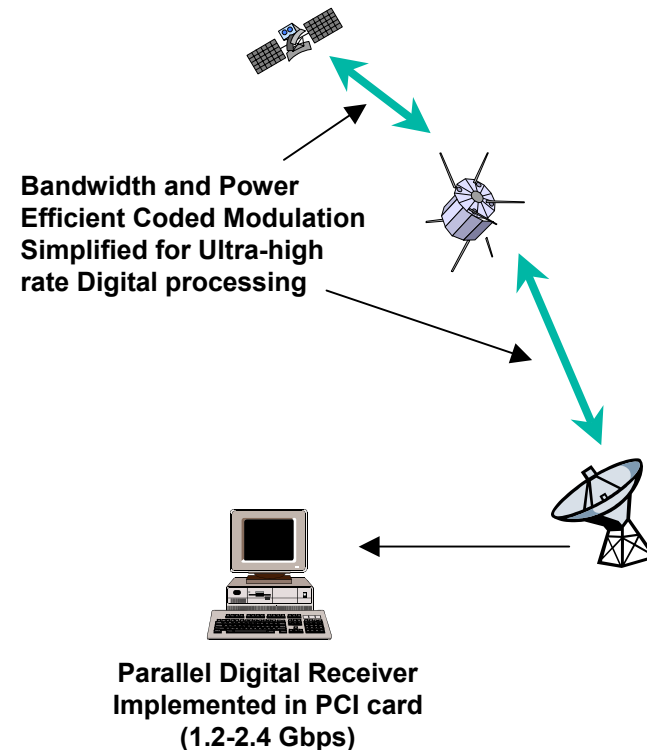
5615-Next Generation Digital Receiver Overview

- **Goal:**

To develop a digital high rate QPSK/QPSK (binary phase shift keying/quadrature phase shift keying) receiver application specific integrated circuit (ASIC) capable of demodulating BPSK, QPSK, FQPSK, and OQPSK(offset QPSK) data rates up to 600 Mega-symbols per second (MSPS). Also, develop a PCI-based prototype high-rate digital receiver board using this custom ASICs, programmable devices and associated components.

- **Benefits:**

- Reduced cost (> 10x) over existing analog processing systems
- Increased data rate (> 10x) over existing digital processing systems
- Demodulates CCSDS-recommended, high rate, bandwidth-efficient modulations for satellite channel



5615-Next Generation Digital Receiver Overview

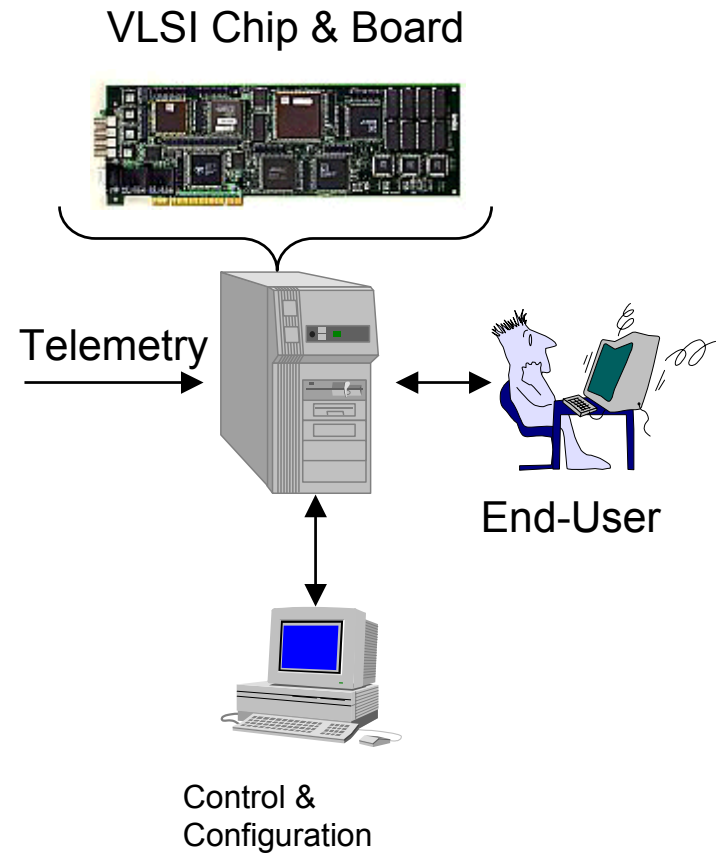
- **Potential Customers:**
 - Supports Next Generation TDRSS
 - VSOP2 and ARISE Space VLBI
 - Numerous present and future earth science missions
 - Terra, AQUA, NPP, NPOES, Landsat 7
 - Missions with hyperspectral imagers
- **Partnerships and Collaborations :**
 - Partnerships with JPL continues to study and implement different modulation/demodulation to address high data rate
- **Approach:**
 - Processing state-of-the-art bandwidth demodulation including 16-QAM
 - Equalizing the very broadband multi-GHz RF channel
 - Performance characterization (BER)
 - Make use of ULSI ASIC approach to address high data rate solution
 - Make use of commercial technology wherever applicable
 - Transfer/license the technology to the commercial sector

5615-Next Generation Digital Receiver Overview

- **Status:**
 - Completed the documentation for HRDD ASIC and technology transfer the HRDD ASIC
 - Demonstrated the current receiver with LANDSAT-7 spacecraft at 150Mbps
 - Tested the Analog Front End board for the down conversion for variable data rates
 - Characterized the performance of the current receiver
 - Started the revision of the current board design and is 75% complete
 - Designed and simulated the Bit Equalizer in SPW tools for the next generation demodulator ASIC
 - Designed 8-Tap parallel equalizer in the Xilinx FPGA
- **FY02 Plans:**
 - VHDL code for next generation digital demodulator (4QFY02)

5616-Next Generation Level Zero Processor System

- **Goal:** Develop an integrated single chip element to perform base-band frame synchronization, Reed-Solomon error correction and service processing functions. The output will be sorted in real time and transferred to a storage media for archiving and retrieval by the end user or via high-speed network interfaces, directly to the end user.
- **Benefits:**
 - Reduced cost (> 10x) over existing solution
 - Increased data rates (> 300 Mpps)
 - Flexibility to process both CCSDS and non-CCSDS data
 - Provide real-time packet level data



5616-Next Generation Level Zero Processor System

- **Potential Customers:**
 - Numerous present and future earth and space science missions
 - Terra, EO-1, AQUA, NPP, and NPOES
- **Approach:**
 - Make use of ULSI ASIC/FPGA approach to address high data rate solution
 - Apply commercial technology wherever applicable
 - Transfer/license the technology to the commercial sector

5616-Next Generation Level Zero Processor System

- **Status:**
 - Investigated new technologies for interface hardware, software and hybrid solutions to implement the high data rate transfer from the ultra high rate data processing element to an I/O device
 - Completed the architectural definition for the next generation Ultra High Rate Telemetry Processing System
 - Obtained a COTS loaner board to evaluate it's capability for the high-speed data transfer from our custom board to a mass storage system. Started running data from the host platform to bench-mark the HW and SW
 - Started the next generation telemetry ASIC/FPGA design and is 50% complete.
 - Worked with the current version of the NT driver to evaluate its performance in a > 1 Gbps Pentium machine
 - Working on obtaining other COTS loaner boards for the ingest and transference of high speed data from the telemetry processing board to the storage device
- **FY02 Plans:** No money no work

5617-Implementation Feasibility Study on TCM-8PSK

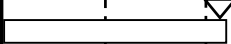

- **Goal:** To determine if 4D Trellis-Coded Modulation 8PSK (now a CCSDS standard) can be implemented in ASIC at high speed ($> 150\text{Mbps}$)
- **Benefits:** to provide increase over 2:1 bandwidth utilization compared to QPSK with rate 1/2 convolutional coding
- **Potential customers:** future missions with high-rate instrument: NPP, Landsat, EOS and small craft with limited bandwidth
- **Approach**
 - Analyze 4D TCM-8PSK specification
 - Identify critical path in computation
 - Perform simulation to obtain initial speed estimate within limited power and real estate

5617-Implementation Feasibility Study on TCM-8PSK

- **Status**
 - **VLSI implementation architecture study at the U. of New Mexico's Microelectronics Research Center.**
 - **Critical path identified in Viterbi decoder, architecture studied.**
 - **Speed bottleneck identified in the adder/select logic, SPICE model simulated**
 - **Conclusion reached: non-optimized architecture cannot achieve 500 Mb/s operation using 0.35u or 0.25u CMOS technology**
 - **It is possible that with 0.35u a decoder can be built at 150 Mb/s (best commercial product is 80Mb/s)**
 - **Study is needed to determine data path width impact on decoding performance**
- **Plan (FY02)**
 - **Complete analytical study of 4D TCM-8PSK (spectral re-growth & decoding accuracy).**
 - **Begin both modulator (in RT library) and demodulator chip design**

Communications and Telemetry Systems - 5612

Milestone Schedule

Work Area Milestones	FY01				FY02		FY03	FY04	FY05	FY06
	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
5611- Channel Coding Research (CCR) Task 1.1 High Rate Channel Coding 1.1.1 Demonstrate inner code decoder in high speed modem (TRW) 1.1.2 Concatenate with Reed-Solomon outer code to build Giga-Hz concatenated coding system										
					<div style="border: 1px solid black; padding: 5px; display: inline-block;">Due to TRW re-org, test plan cancelled.</div>					
						<div style="border: 1px solid black; padding: 5px; display: inline-block;">Lack of funding, analysis performed instead</div>				

Communications and Telemetry Systems - 5612

Milestone Schedule

Work Area Milestones	FY01				FY02		FY03	FY04	FY05	FY06
	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
5611- Channel Coding Research (CCR) Task										
1.2 University of California at Davis/Notre Dame Basic Research										
1.2.1 Devise low density parity check code										
Algebraic method for constructing LDPC codes devised										
1.2.2 Investigate improved Turbo codes and systems at low SNR's										
New Turbo coding system with conv. and LDPC										
1.2.3 Develop efficient soft-decision decoding algorithm										
Error floor lowered to below 10e-10 BER										
1.2.4 Analyze and compare various bandwidth efficient Turbo/new code system, and concatenated coding systems.										
Better than TDRSS code										
1.2.5 Investigate performance of ARQ with Turbo codes and other new codes.										
Outperformed conv. code based scheme by a few dB's										

Milestone Schedule

Work Area Milestones	FY01				FY02		FY03	FY04	FY05	FY06
	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
5612 - Communications & Telemetry Systems (CTS) Task 2.1 Small Satellite TDRSS Access <u>2.1.1 Hitchhiker Payload</u> Development: _____ 2.1.1.1 PDR 2.1.1.2 CDR 2.1.1.3 Fabrication 2.1.1.4 Flight <u>2.1.2 RF Testbed Configuration:</u> 2.1.2.1 Fabrication 2.1.2.2 Test 2.2 Coding Studies <u>2.2.1 Bandwidth-efficient Turbo code design</u> 2.2.1.1 BPSK/QPSK Serial Concatenation Follow-up Study Report 2.2.1.2 Turbo coded partial response Follow-up Study Report	Cancelled!!									

Milestone Schedule

Work Area Milestones	FY01				FY02		FY03	FY04	FY05	FY06
	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
2.3 Bandwidth-Efficient Modulation and Equalization <u>2.3.1 High-Order Modulation Simulation Studies</u> 2.3.1.1 Monitor developments and Report to CCSDS 2.3.2 Higher Modulation Studies: 2.3.2.1 FQPSK Implementation development										
2.4 Space Communications Protocol Testing <u>2.4.1 Protocol Performance Evaluation</u> 2.4.1.1 SCPS & TCP/IP Delay Testing 2.4.1.2 SCPS & TCP/IP >1Mbps Testing										

Milestone Schedule

Work Area Milestones	FY01				FY02		FY03	FY04	FY05	FY06
	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
2.5 Small Satellite Optical Communications										
<u>2.5.1 Ground-based testbed</u>										
2.5.1.1 Fabrication	[Timeline bar from Q1 to Q2]									
2.5.1.2 Test	[Timeline bar from Q1 to Q2]									
<u>2.5.2 Hitchhiker Payload Development</u>										
2.5.2.1 PDR	[Timeline bar from Q1 to Q2]									
2.5.2.2 CDR	[Timeline bar from Q1 to Q2]									
5613 - High Performance Data Compression (HPDC) Task										
3.1 Complete logic design of BPE	[Timeline bar from Q1 to Q3/4]									
3.2 Complete fabrication of BPE	[Timeline bar from Q3 to Q4]									
3.3 Flight Chip set integration/test	[Timeline bar from Q3 to Q4]									
3.4 Demonstrate flight chips	[Timeline bar from Q3 to Q4]									
3.5 Develop inverse BPE ASIC	[Timeline bar from Q3 to Q4]									
3.6 Demonstrate compression system end-to-end	[Timeline bar from Q3 to Q4]									

Milestone Schedule

Work Area Milestones	FY01				FY02		FY03	FY04	FY05	FY06
	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
5614 - Reconfigurable Data Path Processor (RDPP) Task 4.1 Proto-flight ASIC: 4.1.1 Develop ASIC Specification 4.1.2 Design and Fabrication 4.1.3 Test and Evaluate proto-flight ASIC 4.1.4 Demonstration 4.2 Algorithms: 4.2.1 Specs for 2 algorithms for RDPP 4.2.2 Performance data on simulation for software 4.2.3 Report on types of arithmetic operations applicable to data path proc. 4.2.4 Algorithm spec of micro-code library 4.2.5 Micro-code library documentation										

Milestone Schedule

Work Area Milestones	FY01				FY02		FY03	FY04	FY05	FY06
	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
<p>4.3 High Level Software:</p> <p>4.3.1 Spec of high level software</p> <p>4.3.2 First version of high level software</p> <p>4.3.3 Final version of software</p> <p>5615 - Next Generation Digital Receiver Task</p> <p>5.1 HRDR Technology Transfer</p> <p>5.2 Revise the current receiver board design and test</p> <p>5.3 Design the next generation HRDD</p> <p>5.4 Design the next generation receiver board</p>										

Milestone Schedule

Work Area Milestones	FY01				FY02		FY03	FY04	FY05	FY06
	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
5616 - Next Generation Level Zero Processor Task 6.1 Integrated Telemetry ASIC VHDL design 6.2 Platform level software design for data management 6.3 Embedded software for control and monitor 6.4 Integrated Telemetry ASIC (for Technology Transfer) 6.5 Data processing PCB (for Technology Transfer)	Lack of funding									
5617 - Trellis Coded Modulation Feasibility Study Task 7.1 Feasibility Study of High Speed Implementation of TCM Decoder 7.1.1 Modulation Specification 7.1.2 Trellis Block Architecture 7.1.3 VLSI architecture		▼								
			▼							
					Reprogrammed, continued with CS effort					

Milestone Schedule

Work Area Milestones	FY01				FY02		FY03	FY04	FY05	FY06
	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
<p>7.2 TCM Decoder Prototype ASIC</p> <p>7.2.1 Decoder ASIC prototype</p>	Reprogrammed, continued with CS effort									
<p>Note: \triangle = Start</p> <p>∇ = Planned Completion</p> <p>\blacktriangledown = Actual Completion</p>										