THE CONVOLUTIONAL ENCODER UNIT
OPERATIONS
AND
MAINTENANCE
MANUAL

Prepared for:
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1. SCOPE

This manual is intended to provide installation instruction and operational guidance for the Convolutional Encoder Unit.

The information contained herein is provided to assist in general maintenance and troubleshooting.

1.1 INTRODUCTION

The Convolutional Encoder Unit was developed by the Development Engineering Group of AlliedSignal Technical Services, located in Columbia, Maryland. The unit was developed under NASA 31000 contract for the GSFC Code 531. This unit will be installed in South Pole to interface between South Pole Data Server and KSAR Modulator.

1.2 GENERAL DESCRIPTION

The Convolutional Encoder Unit receives KSAR NRZ-L uncoded data and clock and encodes with convolution encoding at the rate of 1/2 with a constraint length of seven. Additionally, the received KSAR NRZ-L uncoded data can be differentially encoded.

The data rate selections and encoding selection can be selected via a front panel thumb-wheel switch and dip switch.

Input signal can be either TTL or ECL and the output will be in ECL compatible signal.

1.3 SPECIFICATION

Electrical and Physical

Input AC voltage	85-135 VAC, 47-63 Hz, single phase
Power Dissipation	20 watts max
Dimensions	17” x 1.5” x 16” (W x H x D)
Weight	7 lb.
Mounting	22” rack slide
Operating Temperature	0 degrees to 50 degrees C
Relative Humidity	20-90% without condensation

Data Interface

Data/Clock In (ECL)	ECL balance or single ended (printed circuit board's jumper configurable), connector type SMA jack , data rate up to 50 Mbps and 50 ohm input impedance
Data/Clock In (TTL)	TTL Balanced, connector type Twinax Trompeter BJ 72, data rate up to 10 Mbps and 100 ohm input impedance
Data/Clock Out (ECL*)	ECL balance or single ended, connector type SMA jack

2. INSTALLATION

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2.1 General

This section details procedures for installation of the Convolutional Encoder Unit. Please read this section in its entirely before applying power to the unit

2.2 Unpacking/Visual Inspection

Remove unit from shipping carton and perform a general inspection of the unit exterior. Check for broken indicator, front panel switches, rear panel connectors, and damage to the chassis in general.

Remove the top cover and examine the unit's interior. Check for loose circuit board, power supply, and cable harness connectors, components, wiring, and connectors.

After visual inspection is completed and all items are found to be satisfactory, replace top cover.

2.3 Mounting

After performing the above unit inspection the unit can be mounted in a standard 19" rack instrumentation rack. The side rack slide is provided with the Convolutional Encoder Unit to provide easy access to the unit's internal area.

2.4 Cooling

There are no special cooling requirements unless the ambient temperature exceeds 50 degrees C.

2.5 Cable Fabrication

Interface cables should be fabricated in accordance with related Engineering Change (EC). Recommended mating pins, and hardware for all cable assemblies are listed below.

ECL Data In+ (J1)	SMA plug
ECL Data In- (J2)	SMA plug
ECL CLK In+ (J3)	SMA Plug
ECL CLK In - (J4)	SMA Plug
ECL Encoded Data Out + (J5)	SMA Plug
ECL Encoded Data Out - (J6)	SMA Plug
TTL Data In (J7)	Twinax Plug
TTL CLK In (J8)	Twinax Plug

2.6 Grounding

An added chassis ground lug is located on the rear panel of this unit for site installation.

3. OPERATIONS

3.1 General

The following section details the operations procedures for the unit's encoding features.

3.2 Pre-Power Up

Before applying power to the Convolutional Encoder Unit insure the data and clock are received to the unit.

Additionally, verify the received data and clock are single ended ECL. The shipped unit's default jumpers are configured as single ended. Remove the top cover and check the printed circuit board's jumpers J1 and J2. Jumper on pins 2 and 3 selects single ended ECL and jumper on 1 and 2 selects balanced ECL.

Table 3-1 contain configuration control switch "jumper" arrangements.

Table 3-2 contain front panel thumb-wheel switch configuration definitions.

Table 3-3 contain front panel dip switch configuration definitions.

Table 3.1 J1 and J2 Jumper Definitions

Jumper Location	Function	Default
J1	ECL Data In Single Ended (J1 pins 2 and 3)	(J1 pins 2 and 3)
	ECL Data In balanced (J1 pins 1 and 2)	
J2	ECL Clock In Single Ended (J2 pins 2 and 3)	(J2 pins 2 and 3)
	ECL Clock In balanced (J2 pins 1 and 2)	

Table 3.2 Front Panel Thumb-wheel Switch Definitions

Thumb-wheel Number	Function
0	Convolutionaly Encoded for the Data rates Data ≤ 10 Mbps
1	Convolutionaly Encoded for the Data rates 10 Mbps < Data ≤ 20 Mbps
2	Convolutionaly Encoded for the Data rates 20 Mbps < Data ≤ 30 Mbps
3	Convolutionaly Encoded for the Data rates 30 Mbps < Data ≤ 40 Mbps
4	Convolutionaly Encoded for the Data rates 40 Mbps < Data ≤ 20 Mbps
5 or 6	Not Used
7	Convolutional encoder Out By-passed Data

Table 3.3 Front Panel DIP Switch Definitions

DIP Switch Location	Position	Definition
SW1-1	OFF	TTL Data In
SW1-1	ON	ECL Data In
SW1-2	OFF	Differentially Encoded
SW1-2	ON	Normal (Differential Encoder Out)
SW1-3	N/A	Not Used
SW1-4	N/A	Not Used

3.3 Control/Indicators

Item	Name	Description
1	AC Power On LED	This is a red LED which indicates the AC power on
2	AC Power Switch	This locking lever toggle switch applies 110 VAC to the Convolutional Encoder Unit

3.4 Power Up Measurement/Adjustment

The unit has no internal adjustment devices. Additionally, internal +5Vdc and -5Vdc power supplies outputs were adjusted properly prior to the shipment. The output voltages should be within +/- .5 volts.

4. DETAILED OPERATIONS

4.1 General

This section provides a general description of the functionality of the Convolutional Encoder Unit.

4.2 Application Hardware

The Convolutional Encoder Unit is a single board application specific design. The Field Programmable Gate Array (FPGA) utilized in this design. A simplified block diagram which identifies the major hardware elements are shown in figure 1.

5. DRAWINGS

5.1 General

The following list of manual, assembly drawings, and logic schematics have been included in this manual to provide additional insight into the operations and maintenance of the Convolutional Encoder Unit.

TDRSS Data Interface and Convolutional Encoder Unit Chassis Operation and Maintenance Manual	Manual No. N/A K & H
Convolutional Encoder Circuit Card Assembly Drawing	1535642
Convolutional Encoder Circuit Card Logic Schematic	1535643

Figure 1. Simplified Block Diagram