The Neolithography Consortium

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The role of process simulation in microlithography is becoming an increasingly important part of process control as wafer feature sizes become smaller than the exposure wavelength, because the pattern transfer from photomask to wafer is nonlinear. An important factor hindering the increased use of simulation applications, however, is their inclination to be standalone applications not easily integrated into the overall process.

These observations have led to the concept of The Neolithography Consortium.

Neolithography is a realization and acceptance that the pattern on the photomask is not replicated exactly on the wafer because of diffraction effects, subresolution mask features and imperfections, and other effects. It is characterized by the full integration of process simulation and metrology into the IC microlithography process, leading to a comprehensive and logical approach to photomask design and wafer exposure. All of the relevant optical projection, resist exposure and development, and etch parameters, and resolution enhancement techniques, are optimized and incorporated into the photomask design before the first wafer is printed.

The Neolithography Consortium is being formed for the purpose of accelerating the adoption of neolithography, by identifying impediments to the integration of simulation and metrology tools into the microlithography process and finding solutions to remove these impediments. It is comprised of companies who create or use commercial IC microlithography simulation software, or who supply metrology or production tools which will interface with simulation software. Any company or organization with a legitimate interest is welcome to join.

KEY WORDS: microlithography, micropatterning, process control, process optimization, simulation, neolithography, photomask, metrology

The role of process simulation in microlithography is becoming increasingly important (and ultimately indispensable[1]) as wafer feature sizes become smaller than the exposure wavelength, because the pattern transfer from photomask to wafer is nonlinear. The effectiveness of optical proximity correction (OPC) and the emerging importance of the mask error enhancement factor (MEEF) attest to this.

This observation has led to the concept of neolithography:[2]

> ***Neolithography*** *n* 1: a realistic photolithographic process in which the pattern on the photomask is not replicated exactly because of diffraction effects, subresolution mask features and imperfections, and other effects. 2: the design and control of such a process.

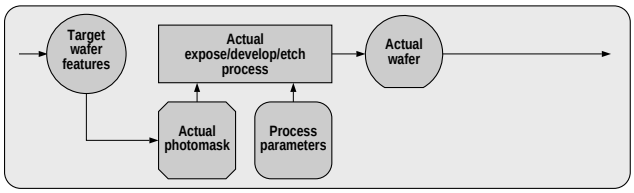
It is characterized by the full integration of process simulation and metrology into the IC microlithography process, leading to a comprehensive and logical approach to photomask design and wafer exposure. All of the relevant optical projection, resist exposure and development, and etch parameters are globally optimized and their effects are incorporated into the photomask design.

There are technical and economic reasons why neolithography is not widely practiced today. These must be overcome for the long term health of the integrated circuit industry and world economy.

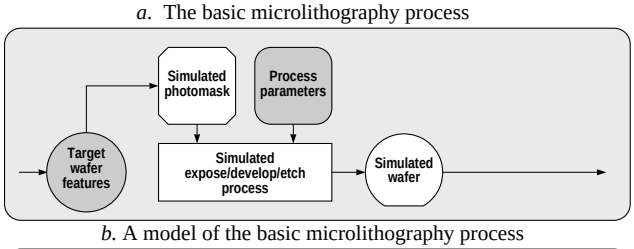
Evolution of microlithography process control

Figure 1*a* shows a simple schematic outline of the IC microlithography process. The objective of this process is to print the *target wafer features* on the wafer so that their sizes and positions are within the wafer feature tolerances specified by the chip designer.[2] The process parameters include such things as wafer exposure wavelength, numerical aperture, coherence parameter, defocus, and exposure dose; photoresist chemical and optical parameters; etch parameters; etc.

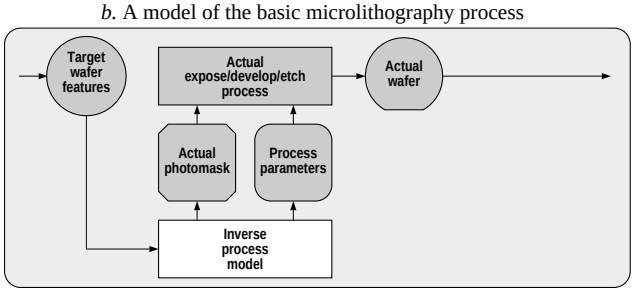
SPIE's 25th Anual Symposium on Microlithography, vol. 3998-54, Santa Clara, Calif. (2000).



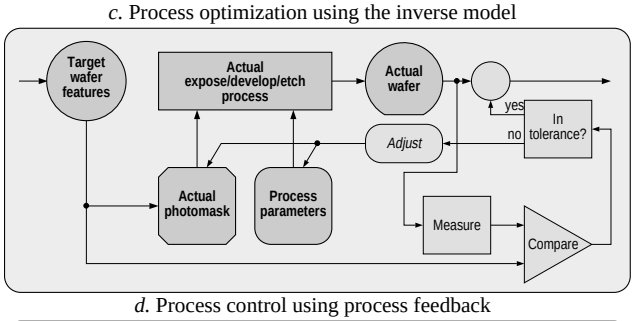
a. The basic microlithography process



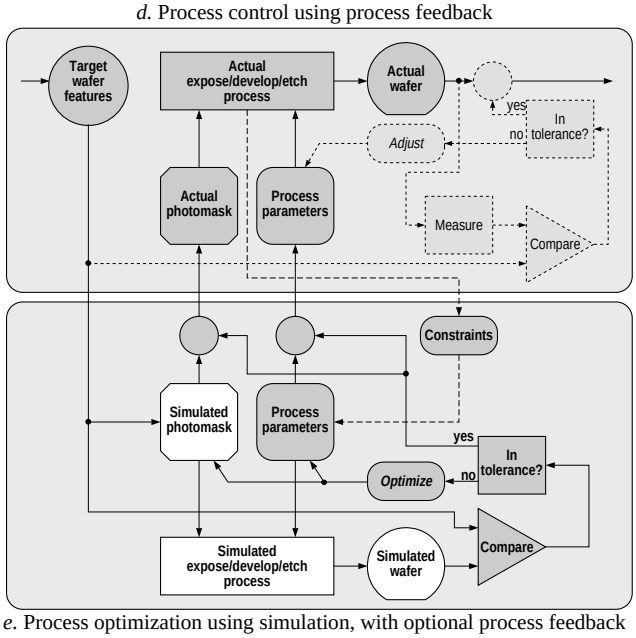
b. A model of the basic microlithography process



c. Process optimization using the inverse model



d. Process control using process feedback



e. Process optimization using simulation, with optional process feedback

FIGURE 1. Simplified block diagram of the microlithography process showing optimization and control methods. Objects shown in white are simulated only.

The process can be understood using a model, or simulation, Fig. 1*b*, typically realized in computer code. Then ideally the inverse model, Fig. 1*c*, can be used to determine the photomask pattern and the values of the process parameters which will produce the desired result in the process. In the days of paleolithography, when the process was approximately linear and the mask pattern appeared to be replicated exactly on the wafer, the inverse process was simply to scale the photomask pattern by the projection reduction ratio.

However, both the optical exposure and resist develop processes are nonlinear. The aerial image of the photomask in the focal plane of an optical projection system can never be an exact replica of the mask pattern, even in a perfect optical system, because of diffraction effects arising from the wave nature of light. The optical response of the photoresist during exposure and its chemical response during development are nonlinear because of saturation and depletion effects. The aerial image and the photoresist are both 3-dimensional objects, and a 2-dimensional model is only an approximation. These and other nonlinearities may be tolerable for larger wafer features with their larger tolerances, but their effects become increasingly apparent as feature sizes become smaller than the exposure wavelength. While the magnitudes of process nonlinearity effects have not changed, these nonlinear effects become more important as wafer feature tolerances become tighter.

As feature sizes began to shrink it soon became apparent that the process was not strictly linear. The solution to this problem was to continue to use the linear process model (simply scaling the mask pattern), but to add feedback control to the process itself, Fig. 1*d*.[2] If the parameter adjustments were small their effects would be approximately linear, and the residual nonlinearities could be absorbed in the wafer feature tolerances. The *measure-compare-adjust* hardware feedback loop (shown lighter in the Figure) adds considerable cost to the process, however. The value added to the product must be sufficient to support this higher cost of

production.

As feature sizes continue to shrink, the effects of the parameter adjustments are no longer linear, the adjustments can interact with each other, and some nonlinear adjustments are now added to the photomask pattern itself (OPC for example). Clearly the cost of this escalating degree of hardware process adjustment will increase at an accelerating rate until it will eventually exceed the value added to the product. It is not pleasant to contemplate the economic consequences.

Neolithography The answer to this dilemma is first to improve the process model by incorporating the nonlinearities and all other known effects, and then to use this model to optimize the process, as shown in Fig. 1*e*. This is basically a combination of Fig. 1*a* and Fig. 1*b*. The ideal solution is to use the inverse model Fig. 1*c*, but the process is so complex that the inverse model is intractable and may not be unique. Consequently the forward model of Fig. 1*b* is used to simulate the process; when placed in the optimization feedback loop as shown this effectively becomes the inverse model. (Since no simulation is perfect, optional hardware feedback for *minor* parameter adjustments is included, shown with dotted lines.) Notice the expensive *Measure* component does not appear in the simulation, because the simulated features are known.

Process optimization While this would appear to add many steps to the process, all of the blocks in the simulation, the lower half of Fig. 1*e*, are executed in software and can be automated, while the processes in the upper part require expensive equipment and labor. In addition, the purpose of the simulation is no longer just to control the process with a few hardware parameter adjustments. The purpose is now to optimize all of the process parameters and the mask pattern design in order to maximize the likelihood that all of the features will be printed within their specified tolerances on the wafer.

The aim is to globally optimize the process using all available degrees of freedom. With a sufficiently sophisticated simulation, all of the (sometimes interdependent) parameters can be simultaneously optimized to maximize the overall process window, while respecting parameter constraints and incorporating all of the focal plane process nonlinearities into the photomask design, All of the available resolution enhancement tools are integrated into the simulation and can be easily incorporated into the mask design as needed.

This is neolithography.

Table I shows a list of some of the lithography process parameters which affect the wafer features and may be subject to optimization. Some of these

Table I
Lithography simulation parameters

Photomask	*Image projection*	*Resist exposure*	*Etch*
specified mask chrome pattern and CDs	magnification	resist thickness	proximity effects
specified mask phase shifters	exposure wavelength	resist sensitivity	etch parameters
optical proximity corrections	numerical aperture	resist index of refraction	other stuff
chrome thickness	coherence parameter	variation in index of refraction of exposed resist	
chrome edge shape	illumination geometry, apodization	position of image focal plane in the resist (focus)	
chrome index of refraction	known projection lens aberrations and distortion	exposure dose	
	wafer substrate reflectivity	wafer substrate reflectivity	
		resist development conditions	
		post exposure bake	

parameters may be beyond the control of the lithographic process engineer, and can be considered external constraints to the process design. All of the remaining process parameters can now be optimized in the simulation to create the largest process window which will center the wafer features within their tolerances. All of this can be done at relatively low cost before the first mask or wafer is printed. Of course, this same reasoning applies to future generation lithography processes (optical or nonoptical). The mask barcode might contain information about the parameter values used for simulation and exposure.

As usual, the process design is a combination of feedforward and feedback. Rules-based OPC, for example, might be applied to the first iteration mask design, then the simulation will indicate whether any OPC adjustments are needed.

Photomask metrology There is no reference to mask metrology in Fig. 1, but Fig. 2 is a more comprehensive diagram showing from a different viewpoint how mask metrology and mask defect detection fit into the overall process.

Process simulation The top left block of Fig. 2 contains the process simulation and photomask design, where the parameter values and the mask pattern, and their tolerances, are derived from the wafer pattern specifications (the positions and sizes, and their tolerances, of the wafer features). All of the components in this block are carried out in software.

The photomask pattern is derived from the wafer specifications as usual, and this pattern (a data file), along with the relevant projection parameters, creates the simulated projected aerial image (a data file of the 3-dimensional distribution of optical intensity in the projected image) in the *Projection tool simulation*. This aerial image, and the relevant exposure and photoresist parameters, create the simulated wafer features in the *Wafer resist and etch simulation*. These simulated features can now be compared with the wafer specifications in *Mask pattern verification*; if the differences are within the specified tolerances, then this mask pattern could be used. Instead, however, the global process window can now be optimized by adjusting the mask pattern and the process parameters (within their limits), to minimize the sensitivity of the process to parameter perturbations. Now the process is optimized and the mask can be fabricated.

The partition of labor here implies that the the entire process--the process parameters and the photomask pattern, including phase shift and OPC features--be designed in the *Process simulation* stage, before the mask specifications are handed to the mask manufacturer. This is because the process tools available, their strengths and weaknesses, their limitations and parameter constraints, and their economic implications, are best understood by the process engineer.

While many elements appear in the *process simulation* block of Fig. 2, the entire simulation and optimization can be viewed as one computer program consisting of snap-together applications from various sources. The design engineer enters his desired wafer feature pattern and the process parameter default values and constraints, and can then go to lunch (or sailing, depending on the processor speed *du jour*), and return to see the optimized parameters and mask pattern.

Photomask fabrication The bottom left block of Fig. 2 shows mask fabrication and testing. After the mask is made (the smaller *Mask fabrication* block), it can be placed in a wafer exposure emulation tool (*CD metrology tool*) to measure the real aerial image which will be formed by this real mask during wafer exposure. This tool is simply a transmission mode optical microscope whose optical parameters (illumination wavelength, objective NA, coherence parameter, and illumination geometry) are adjusted to be the same as the wafer exposure tool to be used. The illumination geometry includes such factors as Kohler or critical illumination, apodization, etc.[2-5] Here the measured aerial image formed by this mask in emulated wafer exposure (a data file) can be compared to the required aerial image which was developed

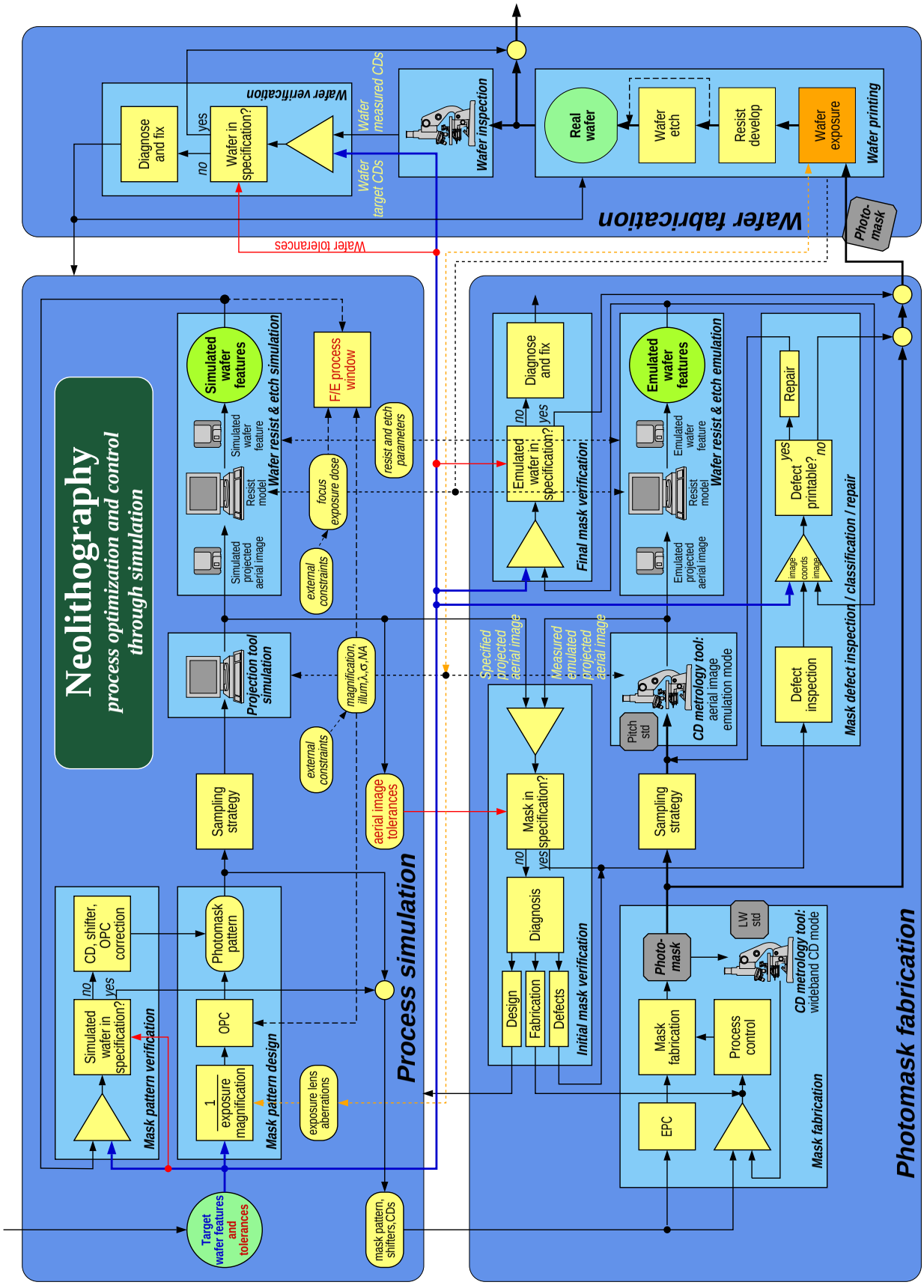

Neolithography
process optimization and control through simulation
Wafer fabrication
Wafer printing
Real wafer
Wafer exposure
Resist develop
Wafer etch
Wafer inspection
Wafer verification
Wafer in specification?
yes
no
Diagnose and fix
Wafer measured CDs
Wafer target CDs
Wafer tolerances
Photo-mask
Process simulation
Photomask fabrication
Wafer resist & etch simulation
Simulated projected aerial image
Resist model
Simulated wafer feature
Simulated wafer features
F/E process window
focus exposure dose
resist and etch parameters
external constraints
Projection tool simulation
magnification, illum,λ,σ,NA
Sampling strategy
aerial image tolerances
Mask pattern verification
Simulated wafer in specification?
CD, shifter, OPC correction
Mask pattern design
Photomask pattern
OPC
1/exposure magnification
exposure lens aberrations
Target wafer features and tolerances
mask pattern, shifters, CDs
Final mask verification
Emulated wafer in specification?
Diagnose and fix
Wafer resist & etch emulation
Emulated projected aerial image
Emulated wafer feature
Emulated wafer features
Mask defect inspection / classification / repair
Defect printable?
Repair
image coords image
Defect inspection
CD metrology tool: aerial image emulation mode
Pitch std
Specified projected aerial image
Measured emulated projected aerial image
Initial mask verification
Mask in specification?
Diagnosis
Design
Fabrication
Defects
Mask fabrication
EPC
Process control
Photo-mask
LW std
CD metrology tool: wideband CD mode

Table II
Mask parameters uncovered in exposure emulation

Mask pattern errors	*Chrome effects*	*Phase shifter errors*	*Mask substrate effects*	*Mask defects*
CD errors	edge runout	dimensions	transmission at exposure wavelength	defect printability
feature placement errors	edge roughness	placement	substrate flatness	defect proximity effects
OPC errors	transmission at exposure wavelength	phase shift at exposure wavelength	mask support effects	success of defect repair
residual optical proximity effects	phase shift at exposure wavelength	image shift from phase errors	tilt of "plane of best focus" relative to substrate	
mean-to-target errors	other subresolution features and artifacts			
across-plate variations				
plate-to-plate variations				

through simulation (the *Initial mask verification* block), revealing the effects of any mask errors and defects, and comparing these effects with the aerial image tolerances. Those errors causing out-of-tolerance regions in the image can then be classified as to their causes, and corrected if necessary before a new mask is made. Some of the mask properties revealed in emulated aerial image inspection are listed in Table II.

Notice how the projection magnification, wavelength, NA, coherence, exposure dose, defocus, and resist parameters couple the simulation and mask fabrication blocks. The mask is an integral part of the process and cannot be designed or tested in isolation from the rest of the lithography process.

Lens aberrations Both the projection lens and the aerial image emulation optical system have aberrations, and the mask pattern can compensate for known projection lens aberrations. These can be properly accounted for in the simulation, but they are difficult to emulate in mask verification because the projection lens aberrations are different from the aerial image emulation tool lens aberrations, and neither can be changed. One way to handle this is to compare the unaberrated simulated and emulated aerial images or the unaberrated simulated and emulated wafer features, by mathematically removing the projection lens aberration corrections from the emulate mask image. The mask inspection microscope aberrations can also be removed if they are known.

Photomask defects In addition to optimizing the entire lithography process in a logical and comprehensive way, neolithography also provides an accurate way to classify mask defects and repairs according to their printability. If a mask defect does not push a wafer feature out of tolerance, the defect is by definition not printable.[6-8]

Defects uncovered in *Mask Verification* or in *Defect inspection* are examined in the *Defect inspection/classification/repair* block, where traditional high resolution defect inspection can supplement the aerial image data. The real mask aerial image creates emulated wafer features in the *Wafer resist and etch emulation* block (identical to the same block above in the *Process simulation,* except here the input data are the real emulated aerial image data instead of the simulated image data). The emulated wafer features at the defect site are compared with the wafer feature specifications; if the emulated wafer features are not out of tolerance, the defect need not be repaired. Otherwise, the repair is made and the site re-examined to confirm that the features are now in tolerance.

The *Final mask verification* block compares the emulated wafer features with the wafer feature specifications. Net MEEF effects will be revealed here. While the MEEF [9-13] is primarily an optical diffraction effect, it may also be influenced by resist develop and wafer etch proximity effects. If

the differences between the emulated wafer features and the wafer specifications are within the specified tolerances, the mask can be released for wafer printing.

Now that the final mask pattern is defined, the process parameters might optionally be re-optimized for this particular photomask by simulating its specific residual errors and defects.

Wafer fabrication The block at the right shows the actual wafer fabrication and inspection, with diagnosis and feedback if any real wafer features are found to be out of tolerance.

The consortium The overall benefit of neolithography is the expeditious fabrication of printed product wafers meeting their design specifications, taking full advantage of all available resolution enhancement techniques as needed, and with minimum of process adjustments or test wafers. The cost is the capital cost of the simulation tools and the design time consumed in the simulation. The capital cost will quickly amortize and the simulation time will improve as the simulations become more efficient and computer speeds increase.

So if neolithography has such a wonderful benefit/cost ratio, why do we not see it widely practiced across the industry? Probably because not all of the simulation software components are yet available, and those that are do not integrate well with each other and with metrology and exposure tools in use. This task is probably too large for any one company, and the group of suppliers is still fragmented. Also, today's computers are only now becoming capable of executing a realistic simulation in a reasonable time.

The nonprofit Neolithography Consortium is being formed to address these issues. It is a group of companies who create or use IC microlithography simulation software. Its purpose is to accelerate the adoption of neolithography by identifying impediments to the integration of simulation and metrology tools into the microlithography process, and finding solutions to remove these impediments. One objective might be a common data exchange format so that, for example, the optical field from the photomask scattering matrix can couple directly into the aerial image-forming projection optics simulation, and that aerial image output will link directly into the resist exposure simulation, even if these tools use different mathematical techniques or are obtained from different companies.

Any company or organization with an interest in this subject is welcome to join.

This consortium is a high leverage project. The cost is low, and the reflexive effect of applying computers to help build better computers compounds the already substantial benefit of logical and comprehensive microlithography process optimization. Someday all of the successful IC fabrication establishments will incorporate neolithography; the most successful will be those who incorporate it first. We can make that day come sooner.

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