Development of a High Density Pixel Multichip Module at Fermilab

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Abstract

At Fermilab, a pixel detector multichip module is being developed for the BTeV experiment. The module is composed of three layers. The lowest layer is formed by the readout integrated circuits (ICs). The back of the ICs is in thermal contact with the supporting structure, while the top is flip-chip bump-bonded to the pixel sensor. A low mass flex-circuit interconnect is glued on the top of this assembly, and the readout IC pads are wire-bounded to the circuit. This paper presents recent results on the development of a multichip module prototype and summarizes its performance characteristics.

I. Introduction

At Fermilab, the BTeV experiment has been approved for the C-Zero interaction region of the Tevatron [1]. One of the tracker detectors for this experiment will be a pixel detector composed of 62 pixel planes of approximately 100x100 mm^2 each, assembled perpendicular to the colliding beam and installed a few millimeters from the beam.

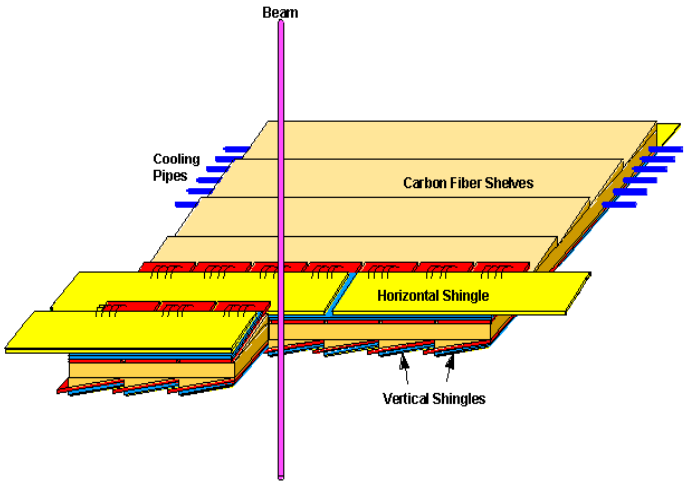

Figure 1: Pixel Station

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The planes in the pixel detector are formed by sets of different lengths of pixel-hybrid modules, each composed of a single active-area sensor tile and of one row of readout ICs. The modules on opposite faces of the same pixel station are assembled perpendicularly in relation to each other (see Figure 1).

The BTeV pixel detector module is based on a design relying on a hybrid approach. With this approach, the readout chip and the sensor array are developed separately and the detector is constructed by flip-chip mating the two together. This approach offers maximum flexibility in the development process, the choice of fabrication technologies, and the choice of sensor material.

The multichip modules must conform to special requirements dictated by BTeV: the pixel detector will be inside a strong magnetic field (1.6 Tesla in the central field), the flex circuit and the adhesives cannot be ferromagnetic, the pixel detector will also be placed inside a high vacuum environment, so the multichip module components cannot outgas, the radiation rates (around 3 Mrad per year) and temperature (-5° C) also impose severe constraints on the pixel multichip module packaging design.

The pixel detector will be employed for on-line track finding for the lowest level trigger system and, therefore, the pixel readout ICs will have to read out all detected hits. This requirement imposes a severe constraint on the design of the readout IC, the hybridized module, and the data transmission to the data acquisition system.

Several factors impact the amount of data that each IC needs to transfer: readout array size, distance from the beam, number of bits of pulse-height analog to digital converter (ADC) data format, etc. Presently, the most likely dimension of the pixel chip array will be 128 rows by 22 columns and 3 bits of ADC information.

II. Pixel Module Readout

The pixel module readout must allow the pixel detector to be used in the lowest level experiment trigger. Our present assumptions are based on simulations that describe the data pattern inside the pixel detector [3]. The parameters used for

the simulations are: luminosity of 2×10^{32} $cm^{-2}s^{-1}$ (corresponds to an average of 2 interactions per bunch crossing), pixel size of 400×50 μm^2, threshold of 2000 e^- and a magnetic field of 1.6 Tesla.

Module 1 →	11	13	17	17	20	18	16	13	8
Module 2 →	11	18	26	31	39	33	25	18	12
Module 3 →	16	20	37	61	76	59	39	26	18
Module 4 →	17	35	63	141	234	130	65	36	16
Module 5 →	23	35	74	234					

Beam

Figure 2: Average Bit Data Rate at Middle Station, in Mbit/s

Figure 2 shows a sketch of the 40 chips that may compose a pixel half plane and the data rate for the station in the middle of 31 stations. The beam passes at the place represented by the black dot. These numbers assume the 23-bit data format shown in Figure 3. Table 1 presents the required bandwidth per module. From this table we see that each half-pixel plane requires a bandwidth of approximately 1.8 Gbit/s.

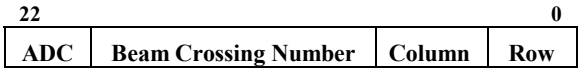

Figure 3: Pixel Module Data Format (23 bits)

Table 1: Half Plane Required Bandwidth, in Mbit/s

	Req. Bandwidth
Module 1	133
Module 2	213
Module 3	352
Module 4	737
Module 5	366
Total	***1801***

We've used simulations of the readout architecture with a clock of 35MHz. This frequency can support a readout efficiency of approximately 98% when considering three times the nominal hit rate for the readout ICs closest to the beam. Efficiency is lost either due to a pixel being hit more than once before the first hit can be read out, or due to bottlenecks in the core circuitry.

A. Proposed Readout Architecture

The readout architecture is a direct consequence of the BTeV detector layout. The BTeV detector covers the forward direction, 10-300 mrad, with respect to both colliding beams. Hence, the volume outside this angular range is outside the active area and can be used to house heavy readout and control cables without interfering with the experiment. The architecture takes advantage of this consideration.

The Data Combiner Board (DCB) located approximately 10 meters away from the detector remotely controls the pixel modules. All the controls, clocks and data are transmitted between the pixel module and the DCB by differential signals employing the Low-Voltage Differential Signaling (LVDS) standard. Common clocks and control signals are sent to each module and then bussed to each readout IC. All data signals are point to point connected to the DCB. Figure 4 shows a sketch of the proposed readout architecture. For more details refer to [6].

This readout technique requires the design of just one rad-hard chip: the pixel readout IC. The point-to-point data links minimize the risk of an entire module failure due to a single chip failure and eliminate the need for a chip ID to be embedded in the data stream. Simulations have shown that this readout scheme results in readout efficiencies that are sufficient for the BTeV experiment.

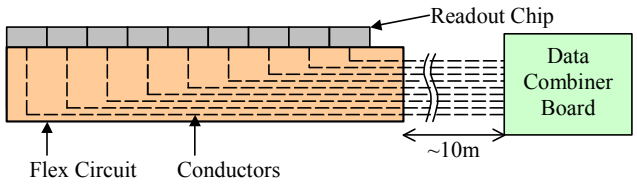

Figure 4: Pixel Module Point-to-Point Connection

III. PIXEL MODULE PROTOTYPE

Figure 5 shows a sketch of the pixel module protoype. This design uses the FPIX1 version of the Fermilab Pixel readout IC [3].

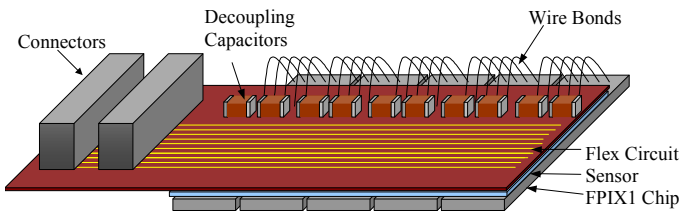

Figure 5: Sketch of the Pixel Multichip Module

The pixel module is composed of three layers, as depicted in Figure 6. The pixel readout chips form the bottom layer. The back of the chips is in thermal contact with the station supporting structure, while the other side is flip-chip bump-bonded to the silicon pixel sensor. The clock, control, and

power pad interfaces of FPIX1 extend beyond the edge of the sensor [2].

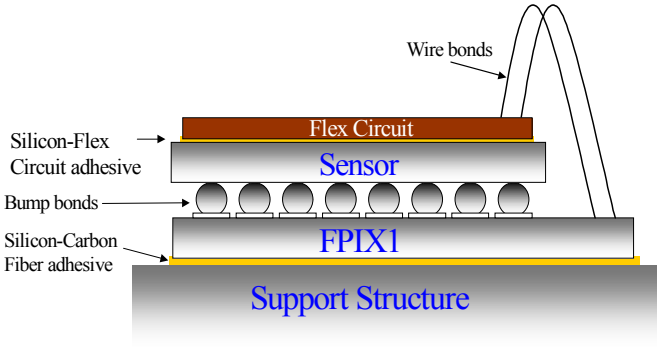

Figure 6: Sketch of the Pixel Multichip Module "Stack"

The interconnect circuitry (flex circuit) is placed on the top of this assembly and the FPIX1 pad interface is wire-bonded to the flex circuit. The circuit then extends to one end of the module where low profile connectors interface the module to the data acquisition system. The large number of signals in this design imposes space constraints and requires aggressive design rules, such as 35 µm trace width and trace-to-trace clearance of 35 µm.

This packaging requires a flex circuit with four layers of copper traces (as sketched in Figure 7). The data, control and clock signals use the two top layers, power uses the third layer and ground and sensor high voltage bias use the bottom layer. The flex circuit has two power traces, one analog and one digital. These traces are wide enough to guarantee that the voltage drop from chip to chip is within the FPIX1 ±5% tolerance. The decoupling capacitors in the flex circuit are close to the pixel chips. The trace lengths and vias that connect the capacitors to the chips are minimized to reduce the interconnection inductance. A picture of the flex circuit made by CERN is shown in Figure 8.

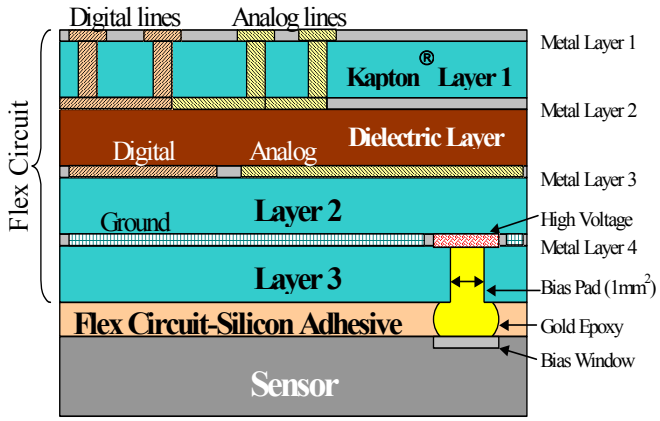

Figure 7: Sketch of Flex Circuit Cross Section

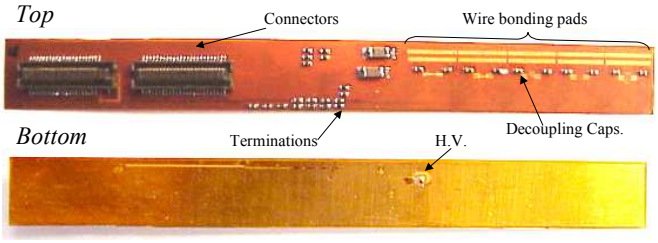

Figure 8: Flex Circuit Picture

To minimize coupling between digital and analog elements, signals are grouped together into two different sets. The digital and analog traces are laid out on top of the digital and analog power supply traces, respectively. Furthermore, a ground trace runs between the analog set and the digital set of traces.

A. High Voltage Bias

The pixel sensor is biased with up to 1000 VDC through the flex circuit. The coupling between the digital traces and the bias trace has to be minimized to improve the sensor noise performance. To achieve this, the high voltage trace runs in the fourth metal layer (ground plane, see Figure 7) and bellow the analog power supply trace. The high voltage electrically connects to the sensor bias window through Gold epoxy. An insulator layer in the bottom of the flex circuit isolates the ground in the fourth metal layer of the flex circuit from the high voltage of the pixel sensor.

B. Assembly

The interface adhesive between the flex circuit and the pixel sensor has to compensate for mechanical stress due to the coefficient of thermal expansion mismatches between the flex circuit and the silicon pixel sensor. Two alternatives are being pursued. One is the 3M thermally conductive tape [7]. The other is the silicone-based adhesive used in [8].

The present pixel module prototypes were assembled using the 3M tape with a thickness of 0.05mm. Before mounting the flex circuit onto the sensor, a set of dummies with bump-bond structures where used to evaluate the assembly process. This assembly process led to no noticeable change in the resistance of the bumps. Figure 9 shows a picture of the dummy.

Figure 9: Dummy Bump Bond Structure

IV. Pixel Module Experimental Results

Two pixel module prototypes were characterized. One of these modules is a single readout IC (FPIX1) bump bonded to a SINTEF sensor (Figure 10) using Indium bumps. In the second pixel module the readout IC is not bump bonded to a sensor (Figure 11). In this prototype the flex interconnect is located on the top of the sensor (as in the baseline design).

The pixel modules have been characterized for noise and threshold dispersion. These characteristics were measured by injecting charge in the analog front end of the readout chip with a pulse generator and reading out the hit data through a PCI based test stand. The results for different thresholds are summarized in Table 2.

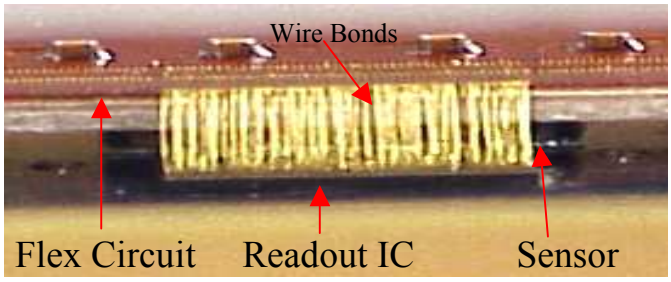

Figure 10: Pixel Module with SINTEF Sensor

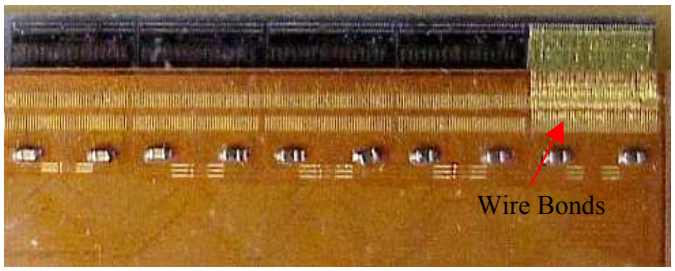

Figure 11: Pixel Module without Sensor

Table 2: Performance of the Pixel Prototype Modules (in e^-)

Without Sensor				***With Sensor***			
μ_{Th}	σ_{Th}	μ_{Noise}	σ_{Noise}	μ_{Th}	σ_{Th}	μ_{Noise}	σ_{Noise}
7365	356	75	7	7820	408	94	7.5
6394	332	78	12	6529	386	111	11
5455	388	79	11	5500	377	113	13
4448	378	78	11	4410	380	107	15
3513	384	79	12	3338	390	116	20
2556	375	77	13	2289	391	117	21

The comparison of these results with previous results (single readout IC without the flex circuit on top) shows no noticeable degradation in the electrical performance of the pixel module [4]. Figure 12 shows the hit map of the pixel module with sensor using a radioactive source (Sr 90), confirming that the bump bonds remain functional.

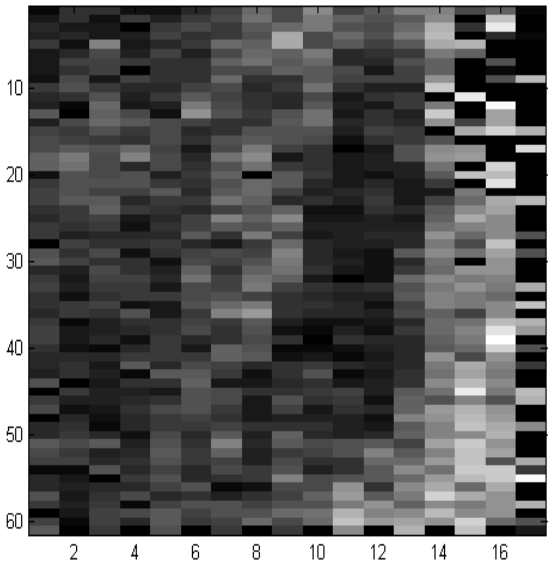

Figure 12: Pixel Module Hit Map

V. Results of the Hybridization to Pixel Sensors

The hybridization approach pursued offers maximum flexibility. However, it requires the availability of highly reliable, reasonably low cost fine-pitch flip-chip mating technology. We have tested three bump bonding technologies: indium, fluxed solder, and fluxless solder. Real sensors and readout chips were indium bumped at both the single chip and at the wafer level by BOEING, NA. Inc (Anaheim, CA) and Advance Interconnect Technology Ltd. (Hong Kong) with satisfactory yield and performance. For more details refer to [5].

VI. Conclusions

We have described the baseline pixel multichip module designed to handle the data rate required for the BTeV experiment at Fermilab. The assembly process of a single chip pixel module prototype was successful. A 5-chip pixel module prototype (Figure 13) will be assembled using the same process. The characterization of the two single-chip modules showed that there is no degradation in the electrical performance of the pixel module when compared with previous prototypes.

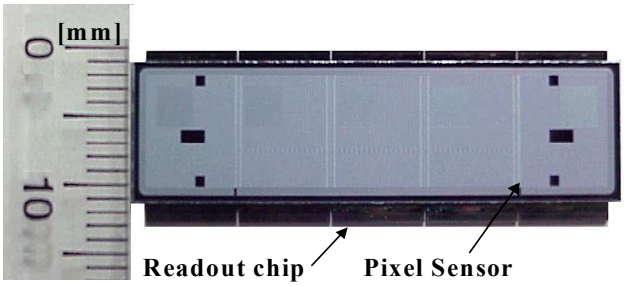

Figure 13: 5-chip Pixel Module with Indium Bumps

VII. ACKNOWLEDGEMENTS

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VIII. REFERENCES

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