Fermilab

Experiment Electronic Systems Group

TESTBOARD CHANNEL LINK

XFT
FINDER DESIGN

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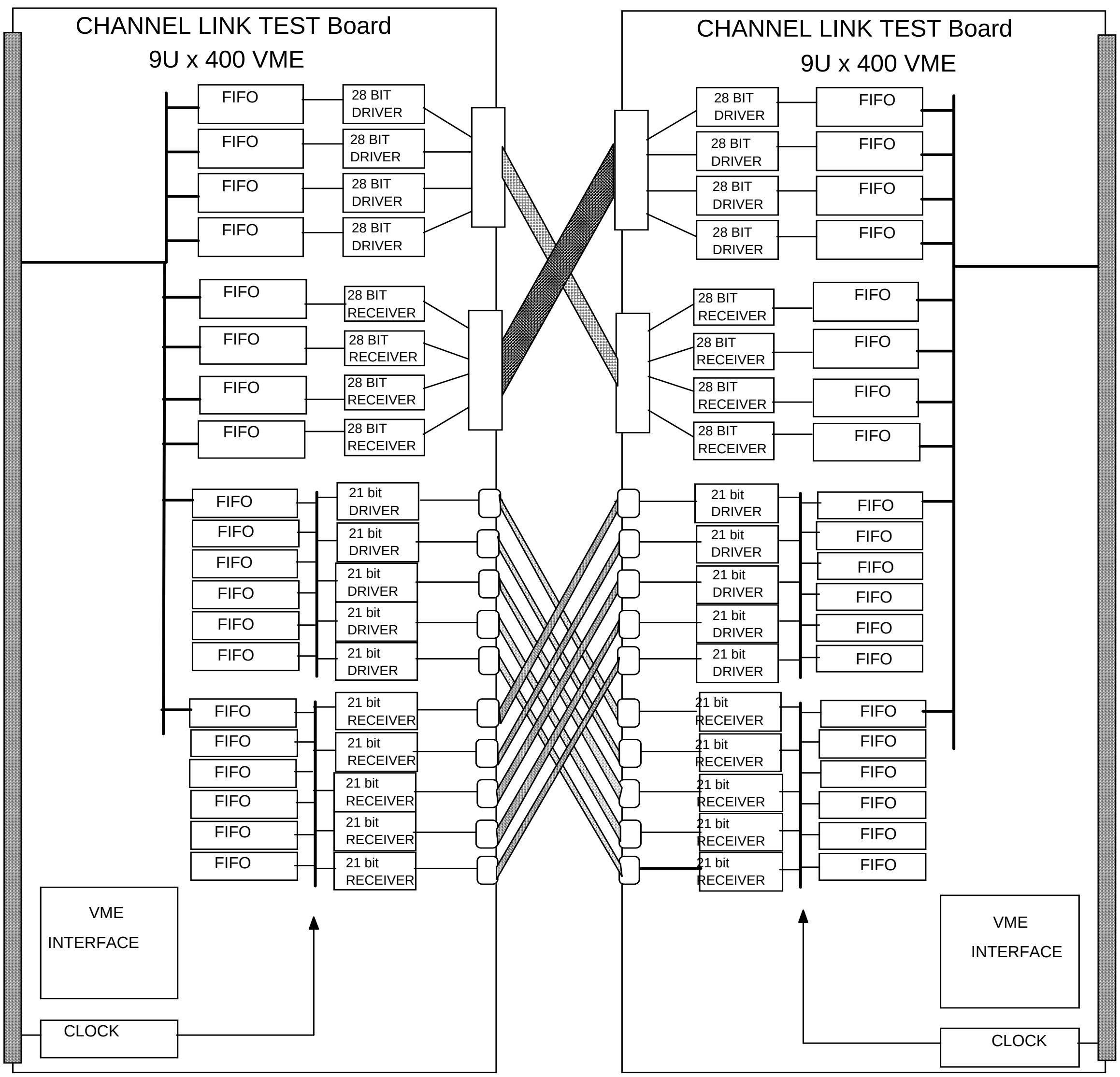
INTRODUCTION:

The purpose of these boards is to test the design of the connection between the FINDER board design and the LINKER board design. These test boards will give us a method to test the NATIONAL Semiconductor DS90CR281/282 28-bit Channel Link and DS90CR211/212 21-bit Channel Link. In addition we would like to find out the type of cable and connectors that will be used in the physical link. Some questions that will be answered by the design work and tests performed on the boards are: Can we gang together the connections of more than one channel link into one cable? What type of cable is needed, size, shielding, length, etc? What type of connectors are available for this type of cable? Is there enough front panel space (length/width) on a 9u board? What happens if all the cables are not the same length?

The following is a block diagram of the Channel Link test board design. Data is clocked into the channel links at a 33ns rate. Maximum cable length is less than 3 meters.



The blocks perform the following functions:

FIFOs- The FIFOS will be read/writeable through VME and will be used to test the data path through the channel link.

CLOCK - Will generate the 33ns clocks from the 132ns CDF clock.

VME INTERFACE- The Interface will contain all necessary logic for interfacing with the rest of the system along with controlling functions within the FIFOS.

What needs to be done!

Decide on the routing of the finder to linker connection.

There are two options: At the present time we are pursuing the 2nd option.

1. Minimize the number of connections between the Finder and Linker. This is done by allowing 6 of the pixels of one finder pair to be transmitted with the pixels of another finder pair, this is for the SL3 board. On SL4 on of the finder pairs only goes to one linker board so it does not have to be redriven**.**

MESSY-(SEE ATTACHED 11x17 DRAWING)

2. Transmit the information of all finders twice.

CLEAN-(SEE ATTACHED 11x17 DRAWING)

PRO's and CON's of each.

A> PRO's of #1.

1. Saves on the number of channel links. (2 on SL1&3 and 1 on SL2&4), for the system of 24 boards of each type plus 24 linkers this saves 144 channel links @ $8 each.

2. The size of the cables and connectors are reduced.

3. Less routing on the Linker board.

4. More space on Linker front panel.

A> CON's of #1.

1. Lose a B0 markers of 2 Finders.

2. Larger inventory of number of connectors and cables.

B> PRO's of #2.

1. All information is presented, including B0.

2. Outputs are duplicated and can go to any of two linker boards.

3. Better for diagnostic purposes the same info is expected out of each link. That is no pixel mapping or offset.

4. Possible to increase the number of pixel of each finder or allows for an additional pixel to be used by a linker if the map is changed.

5. Smaller number of parts to inventory. Price breaks on larger quantities- cable and connectors.

B> CON's of #2.

1. More channel links, cost, space, test, fail.

2. Less front panel space on Linker.

3. Routing on linker.

Can we use the 28 bit channel link with multiple channel links transferring data over one cable? Or do we use the 21 bit channel link with a 4 pair category 5 cable for each link.

National Semiconductor has combined 2 channel links and is doing more tests.

Is there an Application Engineer at National Semiconductor able to answer this question? Yes, Sue Poniatowski and Syed Hud at National, Ph-408-721-4874, 3772(sue).

Has it been done or tested? Syed Hud of National is in the process of doing more tests. One of the tests is crosstalk tests with different cables.

Does National Semiconductor have any recommendations on cable? They have used the 3M 3600 twisted pair cable.

PICK FIFOS

Use the same FIFOS used on the FINDER input test board.

CYPRESS - CY7C4225(1k x 18 bits) & CY7C4221(1k x9 bits) or compatible, I believe the family goes up to a 4k device and is pin compatible with the 1k device.

One 18 bit fifo and one 9 bit fifo will represent two Finders. On this test board we will use 27 bits from the pair of fifos to load the 28 bit channel link.

PICK TRI-STATE BUFFERS

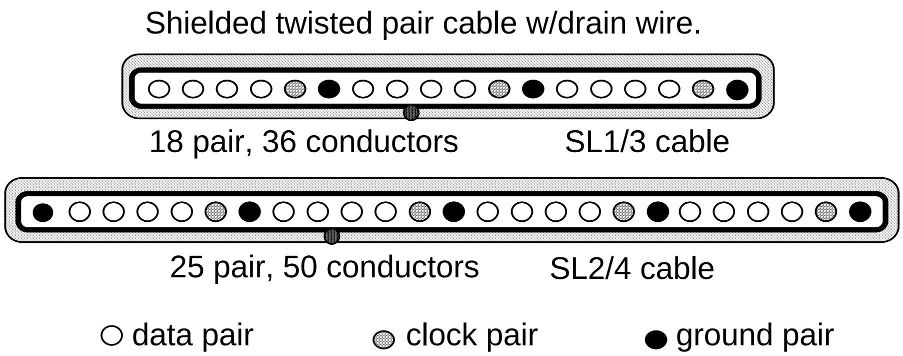
TI has some 18 bit buffers that match up with the 18 bit FIFOS. These 18 bits can also be used as a dual 9 bit.

INVESTIGATE DIFFERENT CABLES

Maximum length of a cable would have to span the width of 3 racks: I would like to keep the length to 10' or less.

21 bit channel link Cables: Category 5, 4 pair, shielded, stranded cables. We would need to use the shield as a current return. They are only a few companies making stranded and shielded 4 pair cables. There would need to be about 450 cable in the system. *VERY MESSY.*

28 bit channel link Cables: If data can be ganged together than there will be two different size cables: 18 pair and 25 pair. For 24 LINKER boards - 48 cables each of the two sizes. I would like to get some general twisted pair cable, some flat to round twisted pair cable and some special cables such as the SKEW CLEAR from AMPHENOL, 3M, BELDEN, HITACHI and fabricate them with the same connectors so that they could all be tested with the boards.



- Flat or Round cable or Flat to Round cable.
- Twisted pair or Twinax.
- Shielded cable or Individual shielded pairs or Both.
- SL2/4 FINDER BOARD:

  28 bit Channel Link- Minimum cable width is 20 pairs(4 channel links @ 5 pairs per) plus a shield grounded at one end and another wire for a ground return. A 25 pair shielded cable would work nicely, allowing up to 5 pairs for ground(return) wires.

  21 bit Channel Link- Use 5 channel links each with its own 4 pair cable.

- SL1/3 FINDER BOARD:

  28 bit Channel Link- Minimum cable width is 15 pairs(3 channel links @ 5 pairs per) plus a shield grounded at one end and another wire for a ground return. A 18 pair shielded cable would work nicely, allowing up to 3 pairs for ground(return) wires.

  21 bit Channel Link- Use 4 channel links each with its own 4 pair cable.

- Impedance: 95 to 120 ohms differential, constant across cable.
- Cable skew + clock jitter will need to be less than 700ps.
- LVDS driver has 0.75ns rise time operating at 210M Hz. data throughput.
- Cable length < 3 meters.
- Low crosstalk.
- Type of connector to be used with cable. It appears that the mini delta ribbon(MDR) connector would work and is available from many suppliers.

COMPANIES:

- SPECS
- SAMPLES
- PRICING

1. 3M: Has supplied us with a cable and connector sample. <$40 per cable.

CABLE: 3600 series, Round, Shielded Jacketed, twisted pair cable, 28 awg 7 x 36 tinned stranded copper, film foil shield w/ copper braid. 91 ohm differential impedance w/ 18.5pf capacitance per foot. 1.69ns/ ft propagation delay. The 3647B series cable is similar with a 100 ohm differential impedance, 15.3 pf capacitance per foot, 1.54ns/ft propagation delay, it only comes in a 18 pair.

CABLE CONNECTOR: 101XX-6000EC series, Mini D ribbon, Shielded

BOARD CONNECTOR: 102XX-series right angle pcb connector: SMT/THRU Hole, 2 row/4 row.

3M used NEP electronics to fabricate the cable and will try to get us a sample of the 3647B cable also.

2. METHODE: Has given a quote on making the 25 & 18 pair cables. < $70 per cable. They have selected a cable(MADISON or CARROL) which is similar to 3M in characteristics and have selected a AMP min- sub-d connector. The contact is trying to get samples of each made and is also trying to get some sample of the AMPHENOL spectra-strip & skew clear able. He is also switching to a MDR connector.
3. HITACHI- The category 5 STP stranded cable is not available as of 4/14/97.
4. BERK_TEK- CAT. 5 cable 540016 4 pr. 26awg stranded with overall tape shield. Tpd=1.4ns/ft, Pair/Pair Skew = 55ps/ft. @$158/1000ft.
5. MONTROSE/CDT - CAT. 5 cable CLD9646 4 pr. 26awg stranded with individually shielded pairs and overall braid. Part of the ALL-LAN system from T&B(Shielded connector cable system rated to 350M Hz.). The CLD9646 has a skew between pairs of 18ps/ft with a cost of $311/1000 ft. T&B has given us a sample of the cable with ALL-LAN connectors installed. 10' ALL-LAN patch cord is $13.30/cord @qty.500 from WESTCO. MONTROSE has said they have a method to bundle cables.
6. BELDEN- Has a round to flat twisted cable, has a low capacitance paired cable.
7. AMPHENOL- Skew Clear cable which is custom orderable in number of pairs and wire size. We are getting a sample of a 22 pair cable. Each pair is individually shielded with an overall shield. 25 pair skew clear @ $16/ft with minimum of 500 ft. Amphenol also has a Round Twist-n-Flat jacketed shielded cable - it has .050 spacing.

INVESTIGATE DIFFERENT CONNECTORS

- Shielded

The MDR (mini delta ribbon) connector seems to be the best fit for the cable. The connectors are available in right angle board mount in 2 and 4 row format. The cable connectors are available in IDC(insulation displacement connector) and in pin/plug format. There are a number of vendors. Also could use a mini sub D with 3 row.

ALL-LAN shielded 4 pair connector from T&B. Will fit on VME board. LINKER would require 18 of these connectors which would use at a minimum 11" of front panel space.

VME interface design

Clock where from

speed

Board trace width and spacing for differential traces,

Differential line impedance: Board layer setup-layer spacing. Try to make similar to final FINDER design.

BOARD OPERATION

The test board will operate in two modes: test and run. During test mode the FIFOS can be tested by writing/reading them through VME. During RUN mode the driver FIFOS are written to through VME, the board is given a 'start' command and the data in the driver FIFOS are transmitted across the channel links into the receiver FIFOS. The data received through the channel link and stored in the receiver FIFOS can then be read through VME and compared to the data transmitted.

TRANSMIT/RECIEVE(T/R) operation

To start a T/R operation the Driver's FIFOS should be loaded and have full flags. The receivers should be empty and have empty flags. A read enable will be issued to all driver FIFOS and a write enable will be issued to all receiver FIFOS. This is done by loading the appropriate information through VME to the 'read enable' and 'write enable' registers. The channel links clock is always operating. This means that data is always being transmitted and received by the channel links.

RECIEVER SETUP: A RECEIVE signal should be issued to enable the tri-state buffers at the output of the receivers and to enable the FIFOS for writing. The VME wclk signal should go to a high state to enable the channel link's clock to proceed to the FIFOS.

DRIVER SETUP: With VME rclk signal low a START signal should be issued. The START signal will enable a dff to register a logic high signal "d27" which is transmitted on the next rising edge of the channel links clock to the receiver board. "d27" is also used to enable the channel link's clock to clock data out of the FIFOS with the same next rising edge of the clock. This allows the "d27" signal to alert the receiver section that the next set of data coming is valid data.

When the 'd27' signal arrives at the receiver it will be registered as a DATA VALID signal which will along with the RECEIVE signal enable the tri-state buffers at the output of the channel link's receiver. This will allow the valid data to be loaded into the receiver FIFOS. When the driver's FIFOS are empty the empty flag will reset the start signal which will reset the DATA VALID signal. The receiver's full flag will also be able to reset the DATA VALID signal.

For the 28-bit link there will be one 'd27' signal input to each driver. This means each 28-bit receiver will operate off of its own data valid signal and the FIFO pair associated with that channel link will receive its write clock signal from the channel links received clock signal.

The 21 bit channel link section operates in the same manner with the 'd104' signal acting as the valid data signal. Due to the nature of the mapping of bits(8*13=104, 5*21=105) when using a 21 bit channel link the 'd104' signal is transmitted through only one channel link. This means that all the receiver FIFOS will use the same write clock. The write clock will come from the same channel link that the 'd104' signal is transmitted with.

TEST MODE

WRITE FIFOS: There are two ways to load the FIFOS: 1. Load all FIFOS with the same data at the same time. 2. Load the FIFOS with different data at different times. Either case involves setting the correct /VME_WE[] bits in the 'write enable' register. The /VME_RE[] signals all need to be logic high and the /RECEIVE and START signals needs to be high and low receptively. A strobe signal /VME_WRT CLK is used to strobe the data into the FIFOS.

READ FIFOS: Similar to the WRITE operation with the difference being that only one FIFO(pair- 18 bit and 9 bit fifo) can be read at a time. The /VME_WE[] bits should all be logic high along with the /RECEIVE and START bits being high and low respectively. Enable the correct /VME_RE[] bit and then a VME_RD_CLK signal will strobe the data onto the 32 bit bus.

The 21 bit channel link operates in a similar manner with the exception that a 9 bit fifo is not paired with a 18 bit fifo.

SEE TWO ATTACHED 11x17 drawings for the 21 & 28 bit diagrams..