D0 Upgrade Electronics

D0Note xxxx

Reasons for a Separate Digital Board

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1. Introduction

The base line design for the Central Tracking Trigger, CTT, Front End board, FE, design prior to December 1998 had the trigger logic located on the same FE board as the multichip modules, MCM. This monolithic FE board;

1. Digitized the analog signals from the VLPC's,
2. Pipelined the L3 data for readout,
3. Produced a fast pick off for the trigger,
4. Latched sorted and forwarded the trigger signals,
5. Processed the trigger signals for a L1 trigger,
6. Processed and pipelined the signals for a L2 trigger, and
7. Passed the L1 and L2 data on.

2. Problems

This large multipurpose FE board caused several problems.

1. Each FE board produced a heat load of between 60 and 100 watts,
2. Each FE crate required several high power sources,
3. A large back plane was required to pass data from board to board.

These three factors proved to be problems.

The large heat load per board was accentuated by the cassette design. Consequently, two adjacent boards were enclosed in an aluminum box, closed on the top and bottom with only a narrow slit in front and back. However, the opening in the back was also blocked because of factor 3. This left only a small area at the backplane to input cooling air and the small front for the air exit. Studies of this indicated that very non-standard techniques and rates of airflow were required for cooling. [1]

The large power load per FE board was a cause for safety concerns. This high powered back plane was located inches from and below the wave guide bundles which bring the signals into the top of the cassettes. These wave guides are believed to be flammable and therefore great care would have to be exercised in designing the power leads, fusing, and connector shielding for the FE crates.

The large back plane placed stringent requirements on the mechanical design of the cassette. Each FE board has connectors not only on the back to the back plane but also along the bottom edge to the cassette itself. These high density, HD, connectors which were the result of considerable R&D, required the FE board to be rigidly mounted along its bottom edge to the cassette. the back plane connectors required very small tolerances as well. These combined requirements translated into a very small tolerance in the placement of each cassette relative to the other 7 in a FE crate.

3. Solution

The solution was to split the monolithic FE board, and move the newly formed board, the digital board, DG to a standard VME crate. The new DG board performs functions 5 through 7 above, while the reduced FE board performs 1 through 4. A slit at this point has two immediate effects.

- Most of the power goes with the DG board.
- Most of the back plane goes with the DG board.

This option had been explored very early in the FE design. At that time which was several years ago it was deemed impractical to move this large amount of digital data. It was possible but very expensive and power hungry.

Each FE board generates 480 fast outputs from the fibers and 64 fast outputs from the central preshower. These 544 bits of data must be passed each crossing or every 132ns. New technology has been developed recently which allows passing this large amount of data for low cost and at low power. The technology is Low Voltage Differential Signal, LVDS. In this technology, the bits are carried as low-voltage-differential-signals on pairs of wires. This low-voltage-differential can be carried on simple twisted pair cables with low loss and low EM noise generation and susceptibility. The data is also serialized and sent at a multiplied clock speed so fewer wire pairs are needed. In the hardware considered, the link is 28 bits wide by 53MHz, multiplexed over six twisted pairs. Five of the pairs are data and the sixth is a clock. Thus, each set of data bits is also sent with its own data valid clock signal. This is a major difference from the other fast serial links used in the D0 Upgrade. Problems such a synchronization loss do not occur. The most common failure mode for these links is that the clock, which is at a different frequency than the data, becomes skewed relative to the data and no longer arrives at the proper time. This failure is a function of the cable length and quality and does not change over time. Therefore once a link is established and seen to work, it continues to work with few errors.

In addition, it should be noted that over this link we are sending raw data not processed data. In processed data, a single bit error can degrade the entire data transmission. For example, one wrong bit in a coded Phi address can make the entire track wrong. In this case, the raw data itself is error prone. The inefficiencies in the singlets are at the 1% level. Multiple interactions and very low Pt tracks cause spurious hits at the few percent level. Therefor any additional error in the raw bit transmission below the 1% level would not be seen.

A side benefit of splitting the FE board is that not only is the back plane gone from the FE crate, it is not necessary on the DG crate either. Those signals from a single FE board which must be sent to two DG boards are sent over two different links. Thus the topology of the backplane mixing is put into the cable plant.

4. Benefits - New Concerns

The split of the Fe boards into two sets of boards has several benefits and gives rise to new, lets call them, concerns.

- Benefits
  - Low heat load at FE - down to about 30 watts
  - Low power at FE
  - No back plane for data passing at FE crates
  - No backplane for data passing at the DG crates
  - Simplifies the FE board design
  - DG crate heat load in standard crate -> standard solutions
  - DG crate high power in electronics rack -> standard solutions
  - *May* lead to single FE board design for CFT and FPS
  - *May* lead to more freedom in wave guide routing
  - DB board could be 6U - more freedom in fabrication
  - Solution is in common with CMS trigger designs
- Concerns
  - Space for new crates
  - Cable runs between FE and DG crates
  - Added latency in trigger, especailly in link to L1 MUON
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Certainly the **benefits** include the solution to the original problems. The FE boards now have a heat load of around 30 watts. And each FE crate requires fewer and lower power supplies. And of course the FE crate no longer has a large back plane. A back plane is still required but now it can be per cassette instead of per crate and is much smaller vertically. An added benefit is that the back plane from the FE is not just moved to the DG crate but disappears. Less obvious is that for the new FE board, which only includes analog processing it, is more possible to use a single layout for all boards. The added flexibility in wave guide routing has been explored for the FPS and seems to lend itself to sending the forward layers to one set of cassettes and the back layers to a second set. This option is described elsewhere and will continue to be studied. [2] A natural question is will this new freedom allow the CFT to dispense with the wave-guide mixing box. This option is also explored in a separate document. [3] A preliminary look, however, indicates that this option is not desirable. Finally, lvds links using the same vendor are under investigation by CMS trigger groups. This was unknown to us when we first developed this plan and picked vendors. Subsequently we learned that our colleagues were on the same path. We plane to share information in the future.

The **concerns** have also been addressed. The first, which is serious for all electronics located on the platform, has been investigated. The DG crates for the CFT trigger could be located in the east platform in space which the L1 MUON may have available. The fall back location is in the center platform one of the center racks. These racks house calorimeter crates and Sequencer crates. Calorimeter expects to be able to consolidate its space needs so that displacing a Sequencer crate will make room for a DG crate. The Sequencer crate displaced would be the one for the CFT L3 readout and can be placed in the west platform. The DG crates for the PS systems can be located in the west platform. A concern here is that the north FPS cassettes are on the east side of the central platform. At least a 40' run is required to the DG crate. Both improved quality cable and repeaters are being investigated for this. It seems the location concern is well in hand. The cable runs are also mostly a space concern. There is space to run these cables under the false floor of the platform between the various FE crates and their matching DG crates. Since they are bundles of twisted pair cables the cable plant is not very large. The added latency is not a result of using the links. Translation onto and off the links takes about the same amount of time as the former multiplexing onto and off the backplane. The added latency is completely in any added cable distance. For the FPS this increase is close to zero. Before the signals from the FE went to the concentrator on the west platform and then to the MCH. Now the signals come from the new FE at the same place as the old FE and go to the DG boards located on the west platform and then to the concentrator located in the same rack. The CFT runs are more of a concern. Here the most time critical path is to the L1 MUON located on the east platform. If we locate the DG boards with the L1 MUON as mentioned above, there is no problem. If we locate the DG bards in the former Sequencer space, the cable run grows by about 20 to 40ns. A time of 40ns is 5% of the allowed 800ns latency so this must be watched closely.

5. Impact on Schedule, Cost and Engineering Resources

The split of the Fe boards into two sets of boards has impacts on the schedule, cost and engineering resources needed. The major effect is where before one board was to be designed and produced there are now two boards. The one to two board change is mitigated to a large extent because the combined functionality remains the same. Also unlike the physical board the design was from the start divided into the two major functionality's of the board (or board pair). What is now the FE board was the responsibility of one EE and the now DG board of another EE. The change in cost has two factors, first many test and production costs are based on the number of board types, and second the lvds links are an added part of the hardware. Because of the first factor many parts of the cost will double. However, some offsetting savings will be realized because the DG board will be smaller. One saving is realized because since it is smaller, the larger and cheaper FPLD chips can be used. These larger FPLD chips simply can not be automatically placed on large boards at this time. The second factor is mitigated because the lvds links are very inexpensive. It appears that the lvds chip sets can be purchased for about the same price as the latching drivers used on the former backplane design. This results in a net null cost change. The cables will be an added cost but the lack of a large backplane will be a reduced cost. In total we estimate that the total cost increase will be less than $50K. This potential increase is less than many of the cost uncertainties at this time.

The effect on the schedule is minimized because the two boards can be developed and produced in parallel. If a single FE board layout is possible, versus one for the CFT and a second for the FPS, (and a possible third for the CFT Stereo, and a possible forth for the CPS Stereo), then the schedule is shortened and the FE boards are ready by the projected start of run.

REFERENCES:

1 - Pat S.'s studies of heat.
2- reference to high and low gain FPS cassettes note
3- wave guide mixing box replaced note