DØ Run 2 Luminosity Monitor Vertex Board Specifications

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This document provides detailed specifications for the Luminosity Monitor Vertex board. In the sections that follow, we provide a brief introduction to the Luminosity Monitor electronics, describe the functionality of the TDC board that generates the input signals processed by the Vertex board, present an overview of the Vertex board functionality, and delineate specifications for the design and construction of the Vertex board. These sections are followed by detailed descriptions of the required FPGA and CPLD programmable logic, a map of VME address space, the connector pin assignments, and a glossary that provides a definition of the signals and internal bits utilized by the Vertex board.

1. Introduction

The DØ Luminosity Monitor (LM) consists of two arrays of scintillation counters mounted on the endcap calorimeters close to the beam pipe. The primary goal of these counters is to measure the Tevatron luminosity by counting the number of proton-antiproton interactions that have at least one charged particle striking each array. Other goals of the LM electronics are to measure the position of the interaction vertex, identify beam crossings with more than one proton-antiproton interaction, and provide information to the Level 1 trigger for further processing.

When a charged particle from a proton-antiproton interaction strikes one of the LM scintillators, a short pulse of light is generated. This light pulse is detected by Hamamatsu fine-mesh photomultiplier tubes (PMTs) to produce a ~10 ns long current pulse. This pulse is amplified a factor of 5.5 by an AD8009 located a short distance from the PMT. The resulting signal is then sent to the Moving Counting House (MCH) on high-quality LMR-400 cable.

Both the north and south LM detectors have 24 scintillation counters, giving a total of 48 readout channels. The vertex position can be obtained by taking the time difference between the PMT hits in the north and south luminosity monitor detectors:

$$z_v = \frac{c}{2}\left(t_N - t_S\right).$$

Multiple interactions can be identified by the increase spread in arrival times at each end due to the interactions having different vertex positions and collision times.

Two types of readout boards are needed for the LM electronics: the LM Timing (TDC) board and the LM Vertex (VTX) board. These boards will also be used for the Forward Proton Detector (FPD) timing scintillator. The TDC board digitizes and processes eight PMT signals. A total of six TDC boards are used to readout the LM, three each for the north and south arrays. Three additional TDC boards are used by the FPD. The VTX board processes signals generated by the TDC board and sends the processed data to the Level 1 Trigger Framework and the FPD Trigger Manager. The processed data is also readout by the DAQ system via the VME Buffer Driver (VBD) board. One VTX board is needed for the LM and one for the FPD.

The TDC and VTX boards reside in two 9U 280 mm deep VME crates that will be located in rack M115, one for the LM and one for the FPD. These crates will have standard muon backplanes. Each crate will also include a 68K processor for control, a VBD that provides the DAQ readout, and a Muon Fanout Controller (MFC) that distributes timing signals and provides readout control. The TDC and VTX boards are designed to emulate Muon Readout Cards (MRC) used by the muon system.

2. Luminosity Monitor TDC Board

The TDC board accepts eight photomultiplier signals and a common stop signal via front-panel LEMO connectors. The primary goal of the TDC board is to precisely measure the time a particle strikes the scintillator. It performs Time-to-Charge Conversion on each channel by switching on a current source when the PMT signal crosses a programmable threshold and switching off the current source when the common stop signal is detected. The charge from the switched current source is integrated and digitized using CAFÉ cards developed for the CDF calorimeter readout. Each PMT signal is fed into a second CAFÉ card to measure the charge of the PMT signal. This charge is used to generate a time-slewing correction to maintain good timing resolution over a wide range of scintillator pulse-heights.

The TDC board uses the timing and pulse-height measurements to select valid timing measurements, and calculates an 8-bit TIME signal by summing the measured time and charge slewing corrections for valid hits. The lsb for the TIME signal is ~50 ps, providing a ±6 ns time range. The TIME signal, as well as the measured time and slewing correction, is readout through the VME bus during event readout.

The TDC board calculates several quantities from the TIME signals. It counts the number of PMT's with valid time measurements, NHIT, and calculates the sum of their times, SUM. It also finds the three largest times, T_H1, T_H2, and T_H3, as well as the two smallest times, T_L1 and T_L2. Finally, it identifies hits that are out-of-time but consistent with being from beam halo, setting the HLOOSE and/or HTIGHT bits if one or more PMT's have a time in the loose/tight halo window.

The LM electronics incorporates a histogramming feature for calibration, monitoring, and diagnostics. For each channel, three different quantities on the TDC board are available for histogramming: the measured time, the charge correction, and the corrected TIME signal. The selected quantity is put on the HIST bus for processing by the VTX board.

The outputs for three TDC boards are combined using a daisy chain approach. The first board in the chain outputs the signals on a 40-conductor flat cable. The second and third boards receive the signals from the previous board and output the combined result. For NHIT and SUM, the results from the TDC board are added to the results from the previous board. For the T_H1, T_H2, T_H3, T_L1, and T_L2 signals, the relevant comparisons are made to provide the 3 latest and two earliest times from all boards in the chain. HLOOSE and HTIGHT are the logical OR of these signals for all boards in the chain. If a quantity on the board is selected for histogramming, it is put on the HIST bus; otherwise, the value from the previous board is passed on. A total of 76 signals are multiplexed onto the cable using the 7.59 MHz beam crossing clock from the MFC, as shown in Tables 13-14 below. Only two 40-conductor flat cables are needed to send signals to the VTX board, one from the three TDC boards serving the "North" LM counters and one from the three TDC boards serving the "South" LM counters.

3. VTX Board Overview

A high-level block diagram of the VTX board is shown in Figure 1.

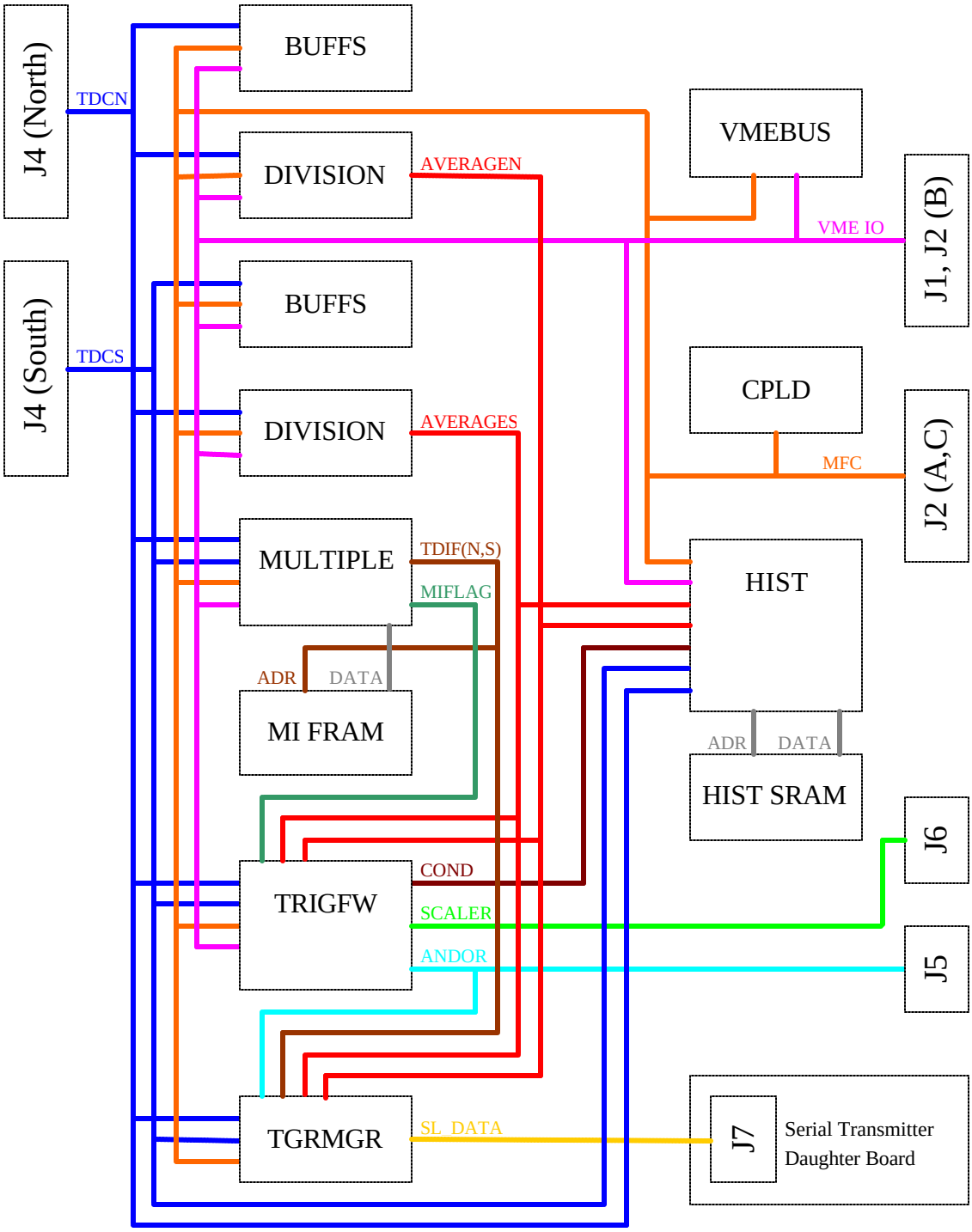

Figure 1: High-level block diagram of the VTX board showing flow of major signals. Signals are generally labeled near their source. In some cases, only a subset of the bus lines may actually be connected to a particular element.

The TDCN and TDCS buses carry input signals from the north and south TDC boards, including the sum of hit PMT times, the number of PMT hits, and two earliest and three latest PMT times, beam halo bits, and histogram input quantities. These signals are buffered for DAQ readout by the BUFFS FPGAs.

The DIVISION FPGAs calculate the average time of the PMT hits in the north and south detectors from the sum of hit PMT times and the number of PMT hits. The DIVISION FPGAs also buffer the average times for DAQ readout.

The MULTIPLE FPGA calculates the north and south time differences using a programmable combination of earliest and latest PMT times. A flash RAM lookup table is used to transform these time differences into the multiple interaction flags. The MULTIPLE FPGA also buffers the time differences and multiple interaction flags for DAQ readout.

The TRIGFW FPGA calculates the z-coordinate of the interaction vertex and constructs the LM and-or trigger terms, the LM foreign scaler quantities, and the histogram condition bits. The TRIGFW FPGA also buffers the vertex position and and-or bits for DAQ readout.

The TRGMGR FPGA multiplexes the past and current and-or bits, the north and south average times, the north and south time differences, the vertex position, the number of north and south PMT hits, and the multiple interaction lookup table used onto a 16-bit bus that feeds the serial transmitter daughter board. This daughter board converts the 96 input data bits into a serial data stream that is fed to the FPD trigger manager.

The HIST FPGA performs a histogramming function that will be use for calibration, monitoring, and diagnostic functions. A variety of data sources can be selected for histogramming. The histogram update can be done selectively based on the histogram condition bits and the beam crossing number. A static RAM is used to store the histogram.

The VME FPGA provides the interface with the VME bus. It also constructs the module header and buffers it for DAQ readout.

The MFC bus carries timing, control, and trigger signals between the VTX and MFC boards. The CPLD decodes an encoded data stream that provides the first crossing, abort gap, and synch gap markers.

4. VTX Board Specifications

The VTX board should emulate an MRC board. Further information on the MRC boards and features of the muon readout electronics can be found at:

http://www-d0.fnal.gov/muon_electronics/#readout.

Note that while the LM and Muon electronics share common infrastructure elements (VME backplane, MFC, VBD, crate processor), the functionality of the VTX and MRC boards is quite different. The MRC board is designed to interface the readout electronics on the platform to a VME crate in the MCH, whereas all the readout electronics for the LM is located in the MCH using TDC and VTX boards.

FPGA and CPLD Considerations

All major logic functions on the board shall be provided by eight FPGAs and one CPLD, as described in Section 5 below.

The VTX board shall incorporate eight Xilinx Spartan XCS40 FPGAs with 240 pin QFP packages to implement the major logic functions performed by the board. Preliminary versions of the FPGA code have been successfully simulated using an XCS40-3PQ240C target device with one exception. The current TGRMGR FPGA design does not meet the timing specification for either the –3 or –4 speed grade of the XCS40. This FPGA either needs further code optimization or a change in the target device to the 3.3V XCX40XL device. The XCS40XL device comes in a faster –5 speed grade and has a 2-1 output MUX, which should allow it to operate at the required speed.

A reasonably fast CPLD is needed to decode the GAP, SGAP, and FC signals. These three signals are encoded on the differential PECL ENC+ and ENC- lines on the VME J2 connector. The CPLD decoding utilizes a 106 MHz clock, which may be obtained from a x8 frequency multiplier (suggested part EXAR ST49C101ACF8-03) of a 13 MHz clock. The CPLD produces the 13 MHz clock by dividing down the 53 MHz RF signal. The Xilinx XCR5064C-7PC44C CPLD was employed on the TDC boards, but this part has been recently discontinued. A decision must be made to: find a few of these chips still on the market, utilize the 3.3V version of this part (XCR3064XL) and perform any necessary level translations, or identify a replacement CPLD.

The board shall have a JTAG header (suggested part 3M 2306-6111TG) that provides a serial JTAG loop for accessing the on-board FPGAs and CPLD (including the FPGA located on the serial transmitter daughter board).

Configuration EEPROMs shall be provided for each type of FPGA (suggested part Atmel AT17C512-10JC). The EEPROMs shall be socketed to allow off-board programming. Where two FPGAs with identical programming are employed (BUFFS, DIVISION), a single EPROM may be used to simultaneously download both FPGAs.

The FPGAs shall be configurable from either on-board EEPROMs or the JTAG interface. To select between these modes, each FPGA INIT signal shall have a jumper that selects between a ground pulldown (JTAG) and a VCC pullup (EEPROM). To help diagnose FPGA download problems, each FPGA DONE signal shall have a jumper that selects between a common VCC pullup for all FPGAs and an individual VCC pullup. The pullup resistors should be sized to provide ~1 ma of current per pin for a 5 volt drop.

Uncommitted FPGA and CPLD input/output pins shall be interconnected for possible future use in a manner to be determined jointly by Brown and Rice personnel.

Memories

The multiple interaction lookup table is an 1Mx8 FlashRam (suggested part AMD AM29F800BB-55SC).

Histogram storage is provided by a pair of 64Kx16 static RAMs (suggested part Cypress CY7C1021V-15C or equivalent). The two static RAMs shall have separate write enable signals to allow the memory to be addressed using either D16 or D32 VME transfers.

VME Interface

The board shall recognize A24 addresses in the range 2x0000-2xFFFF as defined in Section 6 below (the value of x is set by the BOARD_ID switches). Registers and the multiple interaction lookup table shall support D16 transfers, while VBD buffers and histogram memory shall support D32 transfers. While the current FPGA code does not support D16 access to the VBD buffers and histogram memory, the VME_LW signal is made available to the FPGAs to allow possible future support for D16 access.

Register bits that are not defined shall default to “0” at power-on and read back the last value written to them. VBD buffer bits that are not defined shall read back as “0”.

TDC Signals

The signals from the TDC board are brought to the VTX board on two 40-pin ribbon cables. An 80-pin 3M condo header (3M 3432-L202), designated as J4, shall be used to connect these ribbon cables to the board. The condo header is effectively two 40 pin headers stacked on top of each other. Pin 1 of the condo header shall be located a distance 2.6” below pin 1 of the VME J1 connector. The pin assignment for the condo header is given in Table 13 below. Two signals are multiplexed on each pin as shown in Table 14. The CLK=1 signals are to be latched by the FPGAs on the falling edge of CLK; the CLK=0 signals are to be latched on the rising edge of the CLK.

Trigger Signals

The LM provides the Level 1 Trigger Framework with 16 and-or terms on 40-conductor twist-and-flat cable. The TFW_ANDOR, TFW_SGAP, and TFW_STROBE signals must

be converted to differential ECL with pulldown current supplied by the VTX board (suggestion: 510 ohm pulldown resistors to –5V). These signals shall be made available on J5 with the pin assignments given in Table 15 below. Further details may be found at:

http://www.pa.msu.edu/hep/d0/ftp/l1/framework/andor_terms/receiving_l1_framework_input_terms.txt

The LM also provides the Level 1 Trigger Framework with foreign scaler signals. The trigger framework uses these signals to control the updating of the scalers used to determine the luminosity and beam halo rates. The TFW_SCALER signals must be converted to differential ECL with pulldown current supplied by the VTX board (suggestion: 510 ohm pulldown resistor to –5V). The J6 connector shall provide at least 20 pins for the scaler signals. It is suggested that J5 and J6 be combined on a single 80-pin 3M condo header (3M 3432-L202). The proposed pin assignments for this header are given in Table 16 below.

Up to 96 signals may be sent to the FPD Trigger Manager using a Serial Transmitter Daughter Board. These signals are multiplexed onto 16 data lines as shown in Tables 18-19. The J7 connector (SAMTEC TFM-115-02-S-D-LC) provides the data and interface signals required for this daughter board, while the J8 connector (SAMTEC TFM-105-02-S-D-A) provides a JTAG interface to the on-board FPGA. The pin assignments for J7 and J8 are given in Table 17 and Table 20, respectively. Specifications for the Serial Transmitter Daughter Board may be found at:

http://hound.physics.arizona.edu/l1mu/transmitter-070799.pdf.

VME Backplane Signals

The LM electronics utilizes 9U backplanes originally developed for the Run 1 DØ Muon system. These backplanes have three 96 pin connectors (designated J1, J2, and J3) that provide the VME IO bus, power distribution, and interconnections. The J1 connector has the standard VME J1 signals on it. Note that current plans do not include powering the +12V, -12V, and +5STDBY pins. The J2 backplane has standard VME signals on the "B" pins, while the "A" and "C" pins provide a custom bus for communications between the TDC/VTX boards and the MFC controller card. The J3 backplane provides -5V power and additional ground connections. It also provides a direct connection to the J7 and J8 50-pin connectors on the rear of the muon VME backplane. The pin assignments for J1-3 are given in Tables 10-12 below.

The RF+/RF- and ENC+/ENC- differential PECL signals shall be received and converted to TTL levels (suggested part Motorola MC10H350FN). The PECL signals shall have 100 Ohm series damping resistors placed between the PECL-TTL converter and the VME backplane. These signals operate at 53 MHz and are bussed across the VME backplane to several boards. Thus, the stub length of the PECL signals should be minimized and the TTL signals routed using controlled impedance traces with AC termination (suggestion: 100 pf capacitor in series with the termination resistor).

The !DTACK, !SRQ, !L1BUSY, !L2BUSY, !L1ERROR, and !L2ERROR signals shall have open collector drivers located to minimize stub length from the VME backplane (suggested part SN74AS757). The drivers shall be non-inverting to avoid asserting these signals during FPGA configuration, when the FPGA outputs are high.

The VME data lines shall be interfaced to transceivers located to minimize the stub length from the VME backplane (suggested part SN74ABTH16245).

Other VME signals backplane signals not listed above shall have receivers located to minimize stub length from the VME backplane (suggested part SN74ABTH16245).

Power Supply Considerations

The board shall incorporate appropriately sized fuses on all power supply lines. EMI filters shall be placed on each power supply line between the fuse and the digital logic (suggested part Murata BNX002-01). The board will also incorporate over-voltage protection diodes with a current rating that exceeds the fuse rating (suggested part 1N5908).

The board shall generate the 3.3V power needed by the serial transmitter daughter board (and possibly the CPLD and TGRMGR FPGA) from the existing 5V power supply.

Dedicated ground and power planes shall be provided. Ample bypass capacitors shall be employed throughout the board. All IC power pins shall be connected to the appropriate supply and decoupled with a 0.01-0.1 μF capacitor to ground. These decoupling capacitors shall be augmented by larger capacitors on both sides of the EMI filter and elsewhere on the board as deemed appropriate. The fine pitch of the FPGAs and large number of power pins will likely require some bypass capacitors to be placed on the bottom side of the board. All IC ground pins shall be connected to the ground plane.

Mechanical Considerations

The VTX board shall be a 280 mm deep 9U VME board with J1, J2, and J3 connectors. The board shall have a front panel that includes board extraction hardware (suggestion: Schroff 20817-427 for consistency with TDC boards).

Miscellaneous

The VTX board shall have four switches that determine the value of BOARD_ID.

The !GRESET signal shall be asserted at power-up (suggestion: pullup to VCC using a 10K resistor in parallel with a 4.7μF capacitor).

5. FPGA and CPLD Descriptions

This section describes the functionality of the FPGAs and CPLD utilized in the VTX board design and specifies the signals connecting to them. The pin assignments will be established at a future date based on PCB layout considerations and FPGA timing simulations.

BUFFER

This FPGA buffers the TDC board signals NHIT, SUM, T_H1, T_H2, T_H3, T_L1, and T_L2, making them available for VBD readout. There are two BUFFER FPGAs on the VTX board, distinguished by the value of CHIP_ID. The signals on this FPGA are documented below, with x representing N or S, depending on the value of CHIP_ID.

Table 1: Signals connecting to the BUFFER FPGA.

Signal	Bits	Type	Description
A[6:1]	6	In	VME address bus
BOARD_EN	1	In	VME IO for this board
CHIP_ID	1	In	0: N, 1: S
CLK	1	In	7.59 MHz beam crossing clock
D	32	I/O	VME data bus
!G_RESET	1	In	Global reset issued upon power up, board reset
L1ACC	1	In	Level 1 trigger accept
L2ACC	1	In	Level 2 trigger accept
L2REJ	1	In	Level 2 trigger reject
NPERIOD	5	In	Length of L1 trigger buffer
READ_EN	1	In	Enable reading from the VME bus
S_RESET	1	In	Soft reset that clears trigger queues
TDCx	40	In	TDC board signals
VBD_DONE	1	In	VBD readout completed
VME_LW	1	In	VME long word transfer
VME_MODE	2	In	VME IO operation type
VME_WR	1	In	VME write operation
WRITE_EN	1	In	Enable writing to the VME bus

DIVISION

This FPGA calculates the average time of the hits in one LM detector. The FPGA multiplies SUM by 1/NHIT where NHIT must lie in the range 0-24 (the average is set to 0 when there are no hits). The calculation includes compensation for rounding and truncation in the binary representation of 1/NHIT, and gives good agreement with the exact result rounded to the nearest integer. The average is made available on the FPGA output and buffered in the FPGA for VBD readout. There are two DIVISION FPGAs on the VTX board, distinguished by the value of CHIP_ID. The signals on this FPGA are documented below, with x representing N or S, depending on the value of CHIP_ID.

Table 2: Signals connecting to the DIVISION FPGA.

Signal	Bits	Type	Description
A[6:1]	6	In	VME address bus
AVERAGEx	8	Out	Average time of PMT hits
BOARD_EN	1	In	VME IO for this board
CHIP_ID	1	In	0: N, 1: S
CLK	1	In	7.59 MHz beam crossing clock
D	32	I/O	VME data bus
!G_RESET	1	In	Global reset issued upon power-up, board reset
L1ACC	1	In	Level 1 trigger accept
L2ACC	1	In	Level 2 trigger accept
L2REJ	1	In	Level 2 trigger reject
NPERIOD	5	In	Length of L1 trigger buffer
READ_EN	1	In	Enable reading from the VME bus
S_RESET	1	In	Soft reset that clears trigger queues
TDCx[36:32]	5	In	Number of PMT hits (NHITx)
TDCx[28:16]	13	In	Sum of PMT times (SUMx[12:0])
VBD_DONE	1	In	VBD readout completed
VME_LW	1	In	VME long word transfer
VME_MODE	2	In	VME IO operation type
VME_WR	1	In	VME write operation
WRITE_EN	1	In	Enable writing to the VME bus

MULTIPLE

This FPGA determines the Multiple Interaction (MI) flags that are used to identify single/multiple interactions in a beam crossing. Multiple interaction identification is based on the time difference between early and late hits in the north and south LM detectors. An 8Mx8 flash RAM lookup table is used to determine the MI flags for a given pair of time differences. Depending on the setting of the MI_SEL register and the number of PMT hits, the earliest, latest, and/or 2nd latest PMT hits are discarded in the calculation of the time differences. The north and south time differences are concatenated and used as the address in a look-up table. There are effectively 16 different lookup tables, with the choice of lookup table determined by the number of north and south PMT hits (see the definition of MI_TBL in the signal glossary). The MI flags and time differences are buffered for VBD readout. The MI lookup table is redirected to the VME bus when MI_VME = 0 (the upper seven address bits must first be loaded in the MI_SEG register).

Table 3: Signals connecting to the MULTIPLE FPGA.

Signal	Bits	Type	Description
A[13:1]	13	In	VME address bus
BOARD_EN	1	In	VME IO for this board
CLK	1	In	7.59 MHz beam crossing clock
D	32	I/O	VME data bus
!G_RESET	1	In	Global reset issued upon power-up, board reset
L1ACC	1	In	Level 1 trigger accept
L2ACC	1	In	Level 2 trigger accept
L2REJ	1	In	Level 2 trigger reject
MI_DATA	8	I/O	MI lookup table data
MI_FLAG	4	Out	Multiple interaction flags
MI_OE	1	Out	MI lookup table output enable
MI_TBL	4	Out	MI lookup table selector (MI_ADR[19:16])
MI_WE	1	Out	MI lookup table write enable
NPERIOD	5	In	Length of L1 trigger buffer
READ_EN	1	In	Enable reading from the VME bus
S_RESET	1	In	Soft reset that clears trigger queues
TDCN[39:32]	8	In	Time of 2nd earliest north PMT hit (T_L2N) and number of north PMT hits (TDCN[36:32] also carries NHITN)
TDCN[31:24]	8	In	Time of earliest north PMT hit (T_L1N)
TDCN[23:16]	8	In	Time of 3rd latest north PMT hit (T_H3N)
TDCN[15:8]	8	In	Time of 2nd latest north PMT hit (T_H2N)
TDCN[7:0]	8	In	Time of latest north PMT hit (T_H1N)
TDCS[39:32]	8	In	Time of 2nd earliest south PMT hit (T_L2S) and number of south PMT hits (TDCS[36:32] also carries NHITS)
TDCS[31:24]	8	In	Time of earliest south PMT hit (T_L1S)
TDCS[23:16]	8	In	Time of 3rd latest south PMT hit (T_H3S)
TDCS[15:8]	8	In	Time of 2nd latest south PMT hit (T_H2S)
TDCS[7:0]	8	In	Time of latest south PMT hit (T_H1S)

TDIFN	8	Out	North early/late time difference (MI_ADR[7:0])
TDIFS	8	Out	South early/late time difference(MI_ADR[15:8])
VBD_DONE	1	In	VBD readout completed
VME_LW	1	In	VME long word transfer
VME_MODE	2	In	VME IO operation type
VME_WR	1	In	VME write operation
WRITE_EN	1	In	Enable writing to the VME bus

TRIGFW

This FPGA prepares data for use in the L1 trigger decision and generates the signals that are sent to the trigger framework. The z-coordinate of the vertex position (ZVTX) is calculated by taking the difference between the north and south average times. Four interaction trigger bits are formed by requiring |ZVTX| < ZCUTn where ZCUTn are four programmable cuts. Halo trigger bits are formed by requiring a halo bit be set for the north (south) detector with at least one in-time hit detected in the south (north) detector. The four multiple interaction flags and four bits representing the four possible combinations of LM hits (EMPTY, PDIF, ADIF, COIN) complete the set of trigger and-or bits. The and-or bits, a data valid strobe (TFW_STROBE), and a synchronization signal (TFW_SGAP) are made available on J5 and the and-or bits are buffered for VBD readout. Luminosity and halo signals are also derived (TFW_SCALER) and made available on J6. Finally, this module generates the histogram update condition flags (HIST_COND).

Table 4: Signals connecting to the TRIGFW FPGA.

Signal	Bits	Type	Description
A[6:1]	6	In	VME address bus
AVERAGEN	8	In	Average time of north PMT hits
AVERAGES	8	In	Average time of south PMT hits
BOARD_EN	1	In	VME IO for this board
CLK	1	In	7.59 MHz beam crossing clock
D	32	I/O	VME data bus
FC	1	In	First crossing marker
!G_RESET	1	In	Global reset issued upon power
GAP	1	In	Abort gap marker (exclusive of synch gap)
HIST_COND	16	Out	Histogram update condition flags
L1ACC	1	In	Level 1 trigger accept
L2ACC	1	In	Level 2 trigger accept
L2REJ	1	In	Level 2 trigger reject
MI_FLAG	4	In	Multiple interaction flags
NPERIOD	5	In	Length of L1 trigger buffer
READ_EN	1	In	Enable reading from the VME bus
S_RESET	1	In	Soft reset that clears trigger queues
SGAP	1	In	Synch gap marker
TDCN[39]	1	In	Spare north TDC signal (SPAREN[3])
TDCN[38]	1	In	Loose north halo flag (HLOOSEN)
TDCN[37]	1	In	Tight north halo flag (HTIGHTN)
TDCN[36:32]	5	In	Number of north PMT hits (NHITN)
TDCN[31:29]	3	In	Spare north TDC signals (SPAREN[2:0])
TDCS[39]	1	In	Spare south TDC signal (SPARES[3])
TDCS[38]	1	In	Loose south halo flag (HLOOSES)
TDCS[37]	1	In	Tight south halo flag (HTIGHTS)
TDCS[36:32]	5	In	Number of south PMT hits (NHITS)

TDCS[31:29]	3	In	Spare south TDC signals (SPARES[2:0])
TFW_ANDOR	16	Out	Trigger framework and-or bits
TFW_SGAP	1	Out	Trigger framework synch gap marker
TFW_SCALER	10	Out	Trigger framework foreign scalers
TFW_STROBE	1	Out	Trigger framework data strobe
VBD_DONE	1	In	VBD readout completed
VME_LW	1	In	VME long word transfer
VME_MODE	2	In	VME IO operation type
VME_WR	1	In	VME write operation
WRITE_EN	1	In	Enable writing to the VME bus

TGRMGR

The TGRMGR FPGA multiplexes 96 bits of data into six 16-bit frame that are fed to the serial transmitter daughter board. In addition to multiplexing signals from the current crossing, the trigger framework and-or bits from the previous crossing are also provided. The current FPGA code does not meet the speed requirements, so either the code must be further optimized or a faster device selected. One possibility would be to use the Xilinx Spartan XCS40XL-5PQ240C FPGA, which is a faster part operating on a 3.3V supply. Since the XCS40XL inputs are 5V tolerant, and the outputs of this device only drive the serial transmitter daughter board, no level conversion would be necessary.

Table 5: Signals connecting to the TGRMGR FPGA

Signal	Bits	Type	Description
AVERAGEN	8	In	Average time of north PMT hits
AVERAGES	8	In	Average time of south PMT hits
CLK	1	In	7.59 MHz beam crossing clock
FC	1	In	First crossing marker
!G_RESET	1	In	Global reset issued upon power-up, board reset
GAP	1	In	Abort gap marker (exclusive of synch gap)
MI_TBL	4	In	MI lookup table selector (MI_ADR[19:16])
RF	1	In	53 MHz RF clock
SGAP	1	In	Synch gap marker
SL_CLK	1	Out	Serial link clock
SL_ENABLE	1	Out	Enable sending data to trigger manager
SL_FASTOR	1	In	Serial link fast-or bit
SL_DATA	16	Out	Serial link data
SL_PARITY	1	Out	Serial link parity enable
SL_SPARE	1	In	Serial link spare
TDCN	40	In	North TDC board signals
TDCS	40	In	South TDC board signals
TDIFN	8	In	North early/late time difference (MI_ADR[7:0])
TDIFS	8	In	South early/late time difference(MI_ADR[15:8])
TFW_ANDOR	16	In	Trigger framework and-or bits
TFW_SGAP	1	In	Trigger framework synch gap marker

HIST

The HIST FPGA performs a histogramming function that will be used for calibration, monitoring, and diagnostics. The quantity to be histogrammed is determined by the value of the HIST_SRC register. The histogram is accumulated in a 64Kx32 static RAM. Updating of the histogram can be done selectively based on the crossing number and/or the state of bits in the HIST_COND. The HIST_CSR, HIST_TICK, HIST_CONDL, and HIST_CONDH registers control the updating of the histogram. The HIST FPGA controls access to the memory, which can either be in accumulate or VME mode. In accumulate mode, the histogram is accumulated by identifying the bin to be updated, reading the current value in the bin, adding one, and writing the updated value back into the histogram memory. A halt on overflow option is implemented. In VME mode, the histogram memory can be accessed from the VME bus (the upper three address bits must first be loaded in the HIST_SEG register).

Table 6: Signals connecting to the HIST FPGA.

Signal	Bits	Type	Description
A[13:1]	13	In	VME address bus
AVERAGEN	8	In	Average time of north PMT hits
AVERAGES	8	In	Average time of south PMT hits
BOARD_EN	1	In	VME IO for this board
CLK	1	In	7.59 MHz beam crossing clock
D	32	I/O	VME data bus
FC	1	In	First crossing marker
!G_RESET	1	In	Global reset issued upon power-up, board reset
GAP	1	In	Abort gap marker (exclusive of synch gap)
HIST_ADR	16	Out	Histogram memory address
HIST_COND	16	In	Histogram update condition flags
HIST_DATA	32	I/O	Histogram memory data
HIST_OE	1	Out	Histogram memory output enable
HIST_WEH	1	Out	Histogram memory write enable (high 16 bits)
HIST_WEL	1	Out	Histogram memory write enable (low 16 bits)
READ_EN	1	In	Enable reading from the VME bus
SGAP	1	In	Synch gap marker
TDCN[36:32]	5	In	Number of north PMT hits (NHITN)
TDCN[15:0]	16	In	North TDC histogram bus (HISTN)
TDCS[36:32]	5	In	Number of south PMT hits (NHITS)
TDCS[15:0]	16	In	South TDC histogram bus (HISTS)
VME_LW	1	In	VME long word transfer
VME_MODE	2	In	VME IO operation type
VME_WR	1	In	VME write operation
WRITE_EN	1	In	Enable writing to the VME bus

VMEBUS

This FPGA provides the VME and MFC interface logic. The VME address is decoded to see if a valid IO request is being made for the VTX board. If so, BOARD_EN and the appropriate values of VME_LW, VME_MODE, and VME_WR are asserted. The VME transceivers are enabled in the appropriate direction and either READ_EN or WRITE_EN is asserted when an on-board FPGA is required to read from or write to the VME data bus. The VMEBUS FPGA also generates a standard "Muon" format header block that is buffered for VBD readout. A CSR provides the control bits needed by the crate processor to readout the board and generate the VBD_DONE signal. The status of the Level 2 and readout queues are tracked, asserting SRQ when there is an event in the readout buffer, L1BUSY (L2BUSY) when the Level 2 (readout) buffer are full, and L1ERROR (L2ERROR) when L1ACC (L2ACC) is received and the Level 2 (readout buffer) is full. Finally, TICK and TURN are generated and TICK is checked against XING for each trigger accept. If there is a mismatch for a L1ACC (L2ACC), L1ERROR (L2ERROR) is generated.

Table 7: Signals connecting to the VME FPGA.

Signal	Bits	Type	Description
A[31:1]	31	In	VME address bus
AM	6	In	VME address modifiers
!AS	1	In	VME address strobe
BOARD_EN	1	Out	VME IO for this board
BOARD_ID	4	In	Board ID switches
CLK	1	In	7.59 MHz beam crossing clock
D	32	I/O	VME data bus
!DS0	1	In	VME data strobe 0
!DS1	1	In	VME data strobe 1
!DTACK	1	Out	VME data acknowledge
FC	1	In	First crossing marker
!G_RESET	1	In	Global reset issued upon power up, board reset
GAP	1	In	Abort gap marker (exclusive of synch gap)
!IACK	1	In	VME interrupt acknowledge
INIT	1	In	MFC initialize signal
L1ACC	1	In	Level 1 trigger accept
!L1BUSY	1	Out	Level 1 busy condition
!L1ERROR	1	Out	Level 1 error detected
L2ACC	1	In	Level 2 trigger accept
!L2BUSY	1	Out	Level 2 busy condition
!L2ERROR	1	Out	Level 2 error condition
L2REJ	1	In	Level 2 trigger reject
!LWORD	1	In	VME long word transfer
NPERIOD	5	Out	Length of L1 trigger buffer
READ_EN	1	Out	Enable reading from the VME bus
S_RESET	1	Out	Soft reset that clears trigger queues

SGAP	1	In	Synch gap marker
!SRQ	1	Out	Service request
!SYSRESET	1	In	VME system reset signal
VBD_DONE	1	Out	VBD readout completed
VME_DIR	1	Out	VME bus transceiver direction
VME_LW	1	Out	VME long word transfer
VME_MODE	2	Out	VME IO operation type
VME_OE	1	Out	VME bus transceiver output enable
VME_WR	1	Out	VME write operation
!WRITE	1	In	VME write signal
WRITE_EN	1	Out	Enable writing to the VME bus
XING	8	In	Beam crossing number

CPLD

A CPLD is used to decode the ENC signal. A 106 MHz clock is required, which is generated by dividing the RF clock by four followed by a x8 frequency multiplier. The decoding logic was copied from the muon electronics decoder.

Table 8: Signals connecting to the CPLD

Signal	Bits	Type	Description
CLK	1	In	7.59 MHz beam crossing clock
ENC	1	In	Encoded FC, GAP, and SGAP signal
FC	1	Out	First crossing marker
GAP	1	Out	Abort gap marker (exclusive of synch gap)
!G_RESET	1	In	Global reset issued upon power up, board reset
RF	1	In	53 MHz RF clock
RFDIV4	1	Out	RF clock divided by 4
RFX2	1	In	RF clock multiplied by 2
SGAP	1	Out	Synch gap marker

6. VME Address Map

The VTX board is given access to a 64KB block of VME A24 address space. Address bits A[19:16], denoted by x below, are determined by the BOARD_ID switches. Registers are 16 bit and must lie in the address range 2x0000-2x007F. VBD readout buffers are 32 bit and must lie in the address range 2x1000-2x107F. The multiple interaction lookup table is 8 bits wide, but is accessed with using 16 bit transfers (the upper 8 data bits are ignored in write operations, set to 0 in read operations). The histogram memory is 32 bits wide. Both memories are larger than the 16K address range shown below. The high order address bits must be set before accessing these memories by loading MI_SEG or HIST_SEG. All unspecified bits must be set to 0.

Table 9: VME address map.

Address	FPGA	R/W	Xfer	Contents
2x0000	VMEBUS	R/W	D16	CSR1
2x0002	VMEBUS	R/W	D16	CSR2
2x0010	MULTIPLE	R/W	D16	[11:0]: MI_SEL
2x0012	MULTIPLE	R/W	D16	[6:0]: MI_SEG
2x0014	MULTIPLE	R/W	D16	[0]: MI_VME
2x0020	HIST	R/W	D16	HIST_CSR
2x0022	HIST	R/W	D16	[3:0]: HIST_SRC
2x0024	HIST	R/W	D16	[7:0]: HIST_TICK
2x0026	HIST	R/W	D16	HIST_CONDL
2x0028	HIST	R/W	D16	HIST_CONDH
2x002A	HIST	R/W	D16	[2:0]: HIST_SEG
2x0030	TRIGFW	R/W	D16	[7:0]: ZCUT0
2x0032	TRIGFW	R/W	D16	[7:0]: ZCUT1
2x0034	TRIGFW	R/W	D16	[7:0]: ZCUT2
2x0036	TRIGFW	R/W	D16	[7:0]: ZCUT3
2x1000	VMEBUS	R	D32	[15:0]: VBD_WC
2x1004	VMEBUS	R	D32	[31:16]: MODULE_WC [15:0]: MODULE_ID
2x1008	VMEBUS	R	D32	[23:16]: TICK [15:0]: TURN
2x100C	VMEBUS	R	D32	[31:0]: STATUS1 [15:0]: STATUS2
2x1010	BUFFER	R	D32	[31:24]: T_L2N [23:16): T_H3N [15:8]: T_H2N [7:0]: T_H1N
2x1014	BUFFER	R	D32	[25:21]: NHITN [20:8]: SUMN [7:0]: T_L1N
2x1018	BUFFER	R	D32	[31:24]: T_L2S [23:16): T_H3S

				[15:8]: T_H2S [7:0]: T_H1S
2x101C	BUFFER	R	D32	[25:21]: NHITS [20:8]: SUMS [7:0]: T_L1S
2x1020	MULTIPLE	R	D32	[19:16]: MI_FLAG [15:8]: TDIFN [7:0]: TDIFS
2x1024	DIVISION	R	D32	[7:0]: AVERAGEN
2x1028	DIVISION	R	D32	[7:0]: AVERAGES
2x102C	TRIGFW	R	D32	[24:16]: ZVTX [15:0]: TFW_ANDOR
2x8000 – 2xBFFF	MULTIPLE	R/W	D16	[7:0]: MI_DATA
2xC000 – 2xFFFF	VMEBUS	R/W	D32	HIST_DATA

7. Connector Pin Assignments

This section describes the pin assignments for the J1-J8 connectors.

J1 Connector

The J1 connector has standard VME pin assignments, as given below.

Table 10: DØ Muon Backplane J1 Connector.

Pin	A	B	C
1	D00	!BBSY	D08
2	D01	!BCLR	D09
3	D02	!ACFAIL	D10
4	D03	!BG0IN	D11
5	D04	!BG0OUT	D12
6	D05	!BG1IN	D13
7	D06	!BG1OUT	D14
8	D07	!BG2IN	D15
9	GND	!BG2OUT	GND
10	SYSCLK	!BG3IN	!SYSFAIL
11	GND	!BG3OUT	!BERR
12	!DS1	!BR0	!SYSRESET
13	!DS0	!BR1	!LWORD
14	!WRITE	!BR2	AM5
15	GND	!BR3	A23
16	!DTACK	AM0	A22
17	GND	AM1	A21
18	!AS	AM2	A20
19	GND	AM3	A19
20	!IACK	GND	A18
21	!IACKIN	SERCLK	A17
22	!IACKOUT	SERDAT	A16
23	AM4	GND	A15
24	A07	!IRQ7	A14
25	A06	!IRQ6	A13
26	A05	!IRQ5	A12
27	A04	!IRQ4	A11
28	A03	!IRQ3	A10
29	A02	!IRQ2	A09
30	A01	!IRQ1	A08
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

J2 Connector

The J2 connector has standard VME pin assignments on its “B” row. The “A” and “C” rows carry signals needed by the MFC board, which are bussed across the VME backplane to the TDC and VTX boards. The J2 pin assignments are given below.

Table 11: DØ Muon Backplane J2 Connector.

Pin	A	B	C
1	GND	+5V	GND
2	CLK	GND	RF+
3	GND	RESERVED	RF-
4	INIT	A24	GND
5	GND	A25	ENC+
6	L1ACC	A26	ENC-
7	GND	A27	GND
8	L2ACC	A28	XING0
9	GND	A29	GND
10	L2REJ	A30	XING1
11	GND	A31	GND
12	RESERVED	GND	XING2
13	GND	+5V	GND
14	RESERVED	D16	XING3
15	GND	D17	GND
16	!SRQ	D18	XING4
17	GND	D19	GND
18	!L1BUSY	D20	XING5
19	GND	D21	GND
20	!L2BUSY	D22	XING6
21	GND	D23	GND
22	!L1ERROR	GND	XING7
23	GND	D24	GND
24	!L2ERROR	D25	RESERVED
25	GND	D26	GND
26		D27	
27		D28	
28		D29	
29		D30	
30		D31	
31		GND	
32		+5V	

J3 Connector

The J3 connector provides –5V power and additional ground pins. The uncommitted pins are connected to a pair of 50-pin connectors on the rear of the backplane (labeled BP7/8 here). Pins 41-50 of BP8 are tied to GND on the backplane. No use is currently foreseen for the BP7/8 connectors, although they could be used to bring out the trigger framework and-or and scaler signals if necessary. The J3 pin assignments are given below.

Table 12: DØ Muon Backplane J3 Connector.

Pin	A	B	C
1	GND	GND	GND
2	BP8:[2]	BP8:[1]	BP8:[4]
3	BP8:[3]	BP8:[6]	BP8:[5]
4	BP8:[8]	BP8:[7]	BP8:[10]
5	BP8:[9]	BP8:[12]	BP8:[11]
6	BP8:[14]	BP8:[13]	BP8:[16]
7	BP8:[15]	BP8:[18]	BP8:[17]
8	BP8:[20]	BP8:[19]	BP8:[22]
9	BP8:[21]	BP8:[24]	BP8:[23]
10	BP8:[26]	BP8:[25]	BP8:[28]
11	BP8:[27]	BP8:[30]	BP8:[29]
12	BP8:[32]	BP8:[31]	BP8:[34]
13	BP8:[33]	BP8:[36]	BP8:[35]
14	BP8:[38]	BP8:[37]	BP8:[40]
15	BP8:[39]	BP7:[2]	BP7:[1]
16	BP7:[4]	BP7:[3]	BP7:[6]
17	BP7:[5]	BP7:[8]	BP7:[7]
18	BP7:[10]	BP7:[9]	BP7:[12]
19	BP7:[11]	BP7:[14]	BP7:[13]
20	BP7:[16]	BP7:[15]	BP7:[18]
21	BP7:[17]	BP7:[20]	BP7:[19]
22	BP7:[22]	BP7:[21]	BP7:[24]
23	BP7:[23]	BP7:[26]	BP7:[25]
24	BP7:[28]	BP7:[27]	BP7:[30]
25	BP7:[29]	BP7:[32]	BP7:[31]
26	BP7:[34]	BP7:[33]	BP7:[36]
27	BP7:[35]	BP7:[38]	BP7:[37]
28	BP7:[40]	BP7:[39]	BP7:[42]
29	BP7:[41]	BP7:[44]	BP7:[43]
30	BP7:[46]	BP7:[45]	BP7:[48]
31	BP7:[47]	BP7:[50]	BP7:[49]
32	-5V	-5V	-5V

J4 Connector

The J4 connector brings input signals from the TDC boards to the VTX board. An 80-pin 3M condo header (3M 3432-L202) shall be used to receive these signals. The condo header is effectively a pair of 40-pin headers stacked on top of each other, with the header closest to the PCB carrying the north TDC signals (x=N) and the header furthest from the PCB carrying the south TDC signals (x=S). The pin assignments for this connector are given below.

Table 13: Pin assignments for the J4 TDC input connector.

Pin	Signal	Pin	Signal
1	TDCx[0]	2	TDCx[20]
3	TDCx[1]	4	TDCx[21]
5	TDCx[2]	6	TDCx[22]
7	TDCx[3]	8	TDCx[23]
9	TDCx[4]	10	TDCx[24]
11	TDCx[5]	12	TDCx[25]
13	TDCx[6]	14	TDCx[26]
15	TDCx[7]	16	TDCx[27]
17	TDCx[8]	18	TDCx[28]
19	TDCx[9]	20	TDCx[29]
21	TDCx[10]	22	TDCx[30]
23	TDCx[11]	24	TDCx[31]
25	TDCx[12]	26	TDCx[32]
27	TDCx[13]	28	TDCx[33]
29	TDCx[14]	30	TDCx[34]
31	TDCx[15]	32	TDCx[35]
33	TDCx[16]	34	TDCx[36]
35	TDCx[17]	36	TDCx[37]
37	TDCx[18]	38	TDCx[38]
39	TDCx[19]	40	TDCx[39]

Multiplexing of J4 Signals

The signals on the J4 connector are multiplexed and must be properly latched by the receiving FPGA. The CLK=0 signals shall be latched on the rising edge of CLK; the CLK=1 signals shall be latched on the falling edge of CLK.

Table 14: Multiplexing of J4 signals.

Signal	CLK=1	CLK=0
TDCx[0]	HISTx[0]	T_H1x[0]
TDCx[1]	HISTx[1]	T_H1x[1]
TDCx[2]	HISTx[2]	T_H1x[2]
TDCx[3]	HISTx[3]	T_H1x[3]
TDCx[4]	HISTx[4]	T_H1x[4]
TDCx[5]	HISTx[5]	T_H1x[5]
TDCx[6]	HISTx[6]	T_H1x[6]
TDCx[7]	HISTx[7]	T_H1x[7]
TDCx[8]	HISTx[8]	T_H2x[0]
TDCx[9]	HISTx[9]	T_H2x[1]
TDCx[10]	HISTx[10]	T_H2x[2]
TDCx[11]	HISTx[11]	T_H2x[3]
TDCx[12]	HISTx[12]	T_H2x[4]
TDCx[13]	HISTx[13]	T_H2x[5]
TDCx[14]	HISTx[14]	T_H2x[6]
TDCx[15]	HISTx[15]	T_H2x[7]
TDCx[16]	SUMx[0]	T_H3x[0]
TDCx[17]	SUMx[1]	T_H3x[1]
TDCx[18]	SUMx[2]	T_H3x[2]
TDCx[19]	SUMx[3]	T_H3x[3]
TDCx[20]	SUMx[4]	T_H3x[4]
TDCx[21]	SUMx[5]	T_H3x[5]
TDCx[22]	SUMx[6]	T_H3x[6]
TDCx[23]	SUMx[7]	T_H3x[7]
TDCx[24]	SUMx[8]	T_L1x[0]
TDCx[25]	SUMx[9]	T_L1x[1]
TDCx[26]	SUMx[10]	T_L1x[2]
TDCx[27]	SUMx[11]	T_L1x[3]
TDCx[28]	SUMx[12]	T_L1x[4]
TDCx[29]	SPAREx[0]	T_L1x[5]
TDCx[30]	SPAREx[1]	T_L1x[6]
TDCx[31]	SPAREx[2]	T_L1x[7]
TDCx[32]	NHITx[0]	T_L2x[0]
TDCx[33]	NHITx[1]	T_L2x[1]
TDCx[34]	NHITx[2]	T_L2x[2]
TDCx[35]	NHITx[3]	T_L2x[3]
TDCx[36]	NHITx[4]	T_L2x[3]

TDCx[37]	HTIGHTx	T_L2x[5]
TDC[38]	HLOOSEx	T_L2x[6]
TDC[39]	SPAREx[3]	T_L2x[7]

J5 Connector

The J5 connector allows the TFW_ANDOR signals to be sent to the trigger framework via twist-and-flat ribbon cable. In addition to the 16 and-or trigger inputs, the cable also carries the TFW_SGAP synch gap signal, which is used to synchronize the LM signals with the TFW timing, and the TFW_STROBE signal whose rising edge should occur midway between transitions in the and-or terms. All signals are differential ECL with pulldown current supplied by the VTX board. The pin assignments for this connector are given below. Further details of the and/or input cable specifications may be found at:

http://www.pa.msu.edu/hep/d0/ftp/l1/framework/andor_terms/receiving_l1_framework_input_terms.txt

Table 15: Pin assignments for the J5 And-Or connector.

Pin	Signal	Pin	Signal
1	TFW_ANDOR[0]+	2	TFW_ANDOR[0]-
3	TFW_ANDOR[1]+	4	TFW_ANDOR[1]-
5	TFW_ANDOR[2]+	6	TFW_ANDOR[2]-
7	TFW_ANDOR[3]+	8	TFW_ANDOR[3]-
9	TFW_ANDOR[4]+	10	TFW_ANDOR[4]-
11	TFW_ANDOR[5]+	12	TFW_ANDOR[5]-
13	TFW_ANDOR[6]+	14	TFW_ANDOR[6]-
15	TFW_ANDOR[7]+	16	TFW_ANDOR[7]-
17	TFW_ANDOR[8]+	18	TFW_ANDOR[8]-
19	TFW_ANDOR[9]+	20	TFW_ANDOR[9]-
21	TFW_ANDOR[10]+	22	TFW_ANDOR[10]-
23	TFW_ANDOR[11]+	24	TFW_ANDOR[11]-
25	TFW_ANDOR[12]+	26	TFW_ANDOR[12]-
27	TFW_ANDOR[13]+	28	TFW_ANDOR[13]-
29	TFW_ANDOR[14]+	30	TFW_ANDOR[14]-
31	TFW_ANDOR[15]+	32	TFW_ANDOR[15]-
33	TFW_SGAP+	34	TFW_SGAP-
35	GND	36	GND
37	TFW_STROBE+	38	TFW_STROBE-
39	GND	40	GND

J6 Connector

The J6 connector allows the TFW_SCALER signals to be sent to the trigger framework via twist-and-flat ribbon cable. All signals are differential ECL with pulldown current supplied by the VTX board. The J6 connector shall provide at least 20 pins for the scaler signals. It is suggested that J5 and J6 be combined on a single 80 pin 3M condo header (3M 3432-L202). The pin assignments for this connector are given below.

Table 16: Pin assignments for the J6 trigger scaler connector.

Pin	Signal	Pin	Signal
1	TFW_SCALER[0]+	2	TFW_SCALER[0]-
3	TFW_SCALER[1]+	4	TFW_SCALER[1]-
5	TFW_SCALER[2]+	6	TFW_SCALER[2]-
7	TFW_SCALER[3]+	8	TFW_SCALER[3]-
9	TFW_SCALER[4]+	10	TFW_SCALER[4]-
11	TFW_SCALER[5]+	12	TFW_SCALER[5]-
13	TFW_SCALER[6]+	14	TFW_SCALER[6]-
15	TFW_SCALER[7]+	16	TFW_SCALER[7]-
17	TFW_SCALER[8]+	18	TFW_SCALER[8]-
19	TFW_SCALER[9]+	20	TFW_SCALER[9]-
21		22	
23		24	
25		26	
27		28	
29		30	
31		32	
33		34	
35		36	
37		38	
39		40	

J7 Connector

The J7 connector (SAMTEC TFM-115-02-S-D-LC) provides the necessary power and data signals to the serial transmitter daughter board. The pin assignments for this connector are given below:

Table 17: Pin assignments for J7 serial transmitter daughter board connector.

Pin	Signal	Pin	Signal
1	GND	2	GND
3	SL_DATA[0]	4	SL_DATA[1]
5	SL_DATA[2]	6	SL_DATA[3]
7	SL_DATA[4]	8	SL_DATA[5]
9	SL_DATA[6]	10	SL_DATA[7]
11	SL_DATA[8]	12	SL_DATA[9]
13	SL_DATA[10]	14	SL_DATA[11]
15	SL_DATA[12]	16	SL_DATA[13]
17	SL_DATA[14]	18	SL_DATA[15]
19	SL_FASTOR	20	SL_CLK
21	SL_ENABLE	22	SL_PARITY
23	SL_SPARE	24	GND
25	+5V	26	+5V
27	SL_REF	28	GND
29	+3.3V	30	+3.3V

Multiplexing of J7 Signals

The serial transmitter daughter board sends six 16-bit frames of data between each beam crossing. The following tables show the multiplexing for the six data frames.

Table 18: Multiplexing of frames 0-2.

Net	Frame 0	Frame 1	Frame 2
SL_DATA[0]	HISTORY[0]	AVERAGEN[0]	TDIFN[0]
SL_DATA[1]	HISTORY[1]	AVERAGEN[1]	TDIFN[1]
SL_DATA[2]	HISTORY[2]	AVERAGEN[2]	TDIFN[2]
SL_DATA[3]	HISTORY[3]	AVERAGEN[3]	TDIFN[3]
SL_DATA[4]	HISTORY[4]	AVERAGEN[4]	TDIFN[4]
SL_DATA[5]	HISTORY[5]	AVERAGEN[5]	TDIFN[5]
SL_DATA[6]	HISTORY[6]	AVERAGEN[6]	TDIFN[6]
SL_DATA[7]	HISTORY[7]	AVERAGEN[7]	TDIFN[7]
SL_DATA[8]	HISTORY[8]	AVERAGES[0]	TDIFS[0]
SL_DATA[9]	HISTORY[9]	AVERAGES[1]	TDIFS[1]
SL_DATA[10]	HISTORY[10]	AVERAGES[2]	TDIFS[2]
SL_DATA[11]	HISTORY[11]	AVERAGES[3]	TDIFS[3]
SL_DATA[12]	HISTORY[12]	AVERAGES[4]	TDIFS[4]
SL_DATA[13]	HISTORY[13]	AVERAGES[5]	TDIFS[5]
SL_DATA[14]	HISTORY[14]	AVERAGES[6]	TDIFS[6]
SL_DATA[15]	HISTORY[15]	AVERAGES[7]	TDIFS[7]

Table 19: Multiplexing of frames 3-5.

Net	Frame 3	Frame 4	Frame 5
SL_DATA[0]	NHITN[0]	ZVTX[0]	TFW_ANDOR[0]
SL_DATA[1]	NHITN[1]	ZVTX[1]	TFW_ANDOR[1]
SL_DATA[2]	NHITN[2]	ZVTX[2]	TFW_ANDOR[2]
SL_DATA[3]	NHITN[3]	ZVTX[3]	TFW_ANDOR[3]
SL_DATA[4]	NHITN[4]	ZVTX[4]	TFW_ANDOR[4]
SL_DATA[5]	NHITS[0]	ZVTX[5]	TFW_ANDOR[5]
SL_DATA[6]	NHITS[1]	ZVTX[6]	TFW_ANDOR[6]
SL_DATA[7]	NHITS[2]	ZVTX[7]	TFW_ANDOR[7]
SL_DATA[8]	NHITS[3]	ZVTX[8]	TFW_ANDOR[8]
SL_DATA[9]	NHITS[4]		TFW_ANDOR[9]
SL_DATA[10]	MI_TBL[0]		TFW_ANDOR[10]
SL_DATA[11]	MI_TBL[1]		TFW_ANDOR[11]
SL_DATA[12]	MI_TBL[2]		TFW_ANDOR[12]
SL_DATA[13]	MI_TBL[3]		TFW_ANDOR[13]
SL_DATA[14]			TFW_ANDOR[14]
SL_DATA[15]			TFW_ANDOR[15]

J8 Connector

The J8 connector (SAMTEC TFM-105-02-S-D-A) provides JTAG signals to the serial transmitter daughter board. The pin assignments for this connector are given below:

Table 20: Pin assignments for the J8 JTAG connector.

Pin	Signal	Pin	Signal
1	TCK	2	GND
3	TDO	4	+5V
5	TMS	6	n/c
7	n/c	8	n/c
9	TDI	10	GND

8. Signal Glossary

Table 21 provides a brief description of the signals referenced in this document. Descriptions of VME bus and JTAG signals are widely available and thus not included in the glossary. The table also includes definitions of various internal register and VBD readout buffer bits. Register bits that are not defined shall default to "0" at power-on and read back the last value written to them. VBD readout bits that are not defined shall read back as "0". The notation ABCx indicates that there are two ABC signals, ABCN and ABCS, derived from the north and south TDC board signals.

Table 21: Signal glossary.

Signal	Bits	Source	Description
ADIF	1	TRIGFW	"Antiproton diffractive disassociation" trigger term (hits in north LM, no hits in south LM)
AHLOOSE	1	TRIGFW	Antiproton halo, loose cuts
AHTIGHT	1	TRIGFW	Antiproton halo, tight cuts
AVERAGEx	8	DIVISION	Average time of PMT hits
BOARD_EN	1	VMEBUS	VME IO for this board
BOARD_ID	4	Dip switch	Board ID switches – compared against A[19:16]
CLK	1	J2	7.59 MHz beam crossing clock
COIN	1	TRIGFW	Coincidence of hits in both north and south LM counters (no ZVTX cut)
CLR_DONE	1	VMEBUS	Writing 1 to this bit clears VBD_DONE (reads 0)
CLR_SRQ	1	VMEBUS	Writing 1 to this bit clears SRQ (reads 0)
CSR1	16	VMEBUS	Control and Status Register 1: [7]: CLR_SRQ [6]: CLR_DONE
CSR2	16	VMEBUS	Control and Status Register 2: [15]: L2ERROR [14]: L1ERROR [13]: L2BUSY [12]: L1BUSY [11]: SRQ [10]: VBD_DONE
EMPTY	1	TRIGFW	"Empty" beam crossing with no hits in N or S
ENC	1	J2	Encoded FC, GAP, and SGAP signal
FC	1	CPLD	First crossing marker
GAP	1	CPLD	Abort gap marker (exclusive of synch gap)
!G_RESET	1	VCC Pullup	Global reset issued upon power-up, board reset
HIST_ACC	1	HIST	Histogram accumulate mode – when set, the histogram will update (accumulate mode must be off for VME access to histogram memory)
HIST_ADR	16	HIST	Histogram memory address – for HIST_ACC = 1, HIST_ADR is determined by HIST_SRC; for HIST_ACC = 0, HIST_ADR is given by: [15:13]: HIST_SEG

			[12:0]: A[13:1]
HIST_COND	16	TRIGFW	Histogram update condition flags (currently, these are identical to TFW_ANDOR)
HIST_CONDH	16	HIST	Histogram condition hi mask – setting a bit in this mask requires the corresponding condition flag to be high for the histogram to update
HIST_CONDL	16	HIST	Histogram condition low mask – setting a bit in this mask requires the corresponding condition flag to be low for the histogram to update
HIST_CSR	16	HIST	Histogram control register - the following bits are currently defined: [2]: HIST_SPTCK [1]: HIST_OFLW [0]: HIST_ACC
HIST_DATA	32	HIST	Histogram memory data
HIST_OE	1	HIST	Histogram memory output enable
HIST_OFLW	1	HIST	Halt on overflow – HIST_ACC will be set to 0 when the contents of a histogram bin reaches 2^{32}-1
HIST_SEG	3	HIST	Histogram memory segment - HIST_ADR[15:13] are set to HIST_SEG during a VME transfer
HIST_SPTCK	1	HIST	Histogram on specific tick – histogram update restricted to the tick set in HIST_TICK
HIST_SRC	4	HIST	Histogram source. Signals are multiplexed onto HIST_ADR as follows: 0: HISTN 1: HISTS 2: [7:0]AVERAGEN 3: [7:0]AVERAGES 4: [15:8]AVERAGEN, [7:0]AVERAGES 5: [4:0]NHITN 6: [4:0]NHITS 7: [9:5]NHITN, [4:0]NHITS 8: [8:0]ZVTX 9: HIST_COND 10: TICK 11-15: NULL (0)
HIST_TICK	8	HIST	Tick number for histogram on specific tick mode
HIST_WEH	1	HIST	Histogram memory write enable (high 16 bits)
HIST_WEL	1	HIST	Histogram memory write enable (low 16 bits)
HISTx	16	J4	TDC histogram bus (TDCx[15:0])
HISTORY	16	TRIGFW	And-or bits from previous crossing
HLOOSEx	1	J4	Loose halo flag (TDCx[38])
HTIGHTx	1	J4	Tight halo flag (TDCx[37])
INIT	1	J2	MFC initialize signal
L1ACC	1	J2	Level 1 trigger accept
!L1BUSY	1	VMEBUS	Level 1 busy condition

!L1ERROR	1	VMEBUS	Level 1 error detected
L2ACC	1	J2	Level 2 trigger accept
!L2BUSY	1	VMEBUS	Level 2 busy condition
!L2ERROR	1	VMEBUS	Level 2 error detected
L2REJ	1	J2	Level 2 trigger reject
MI_ADR	20	MULTIPLE	MI lookup table address – depends on MI_VME MI_VME = 0 (VME access disabled): [19:16]: MI_TBL [15:8]: TDIFS [7:0]: TDIFN MI_VME = 1 (VME access enabled): [19:13]: MI_SEG [12:0]: A[13:1]
MI_DATA	8	MULTIPLE	MI lookup table data
MI_FLAG	4	MULTIPLE	Multiple interaction flags: [3]: Multiple interaction likely [2]: Multiple interaction favored [1]: Single interaction favored [0]: Single interaction likely
MI_MODE	3	MULTIPLE	Possible choices for calculating TDIFx: 0: use earliest and latest times 1: use 2nd earliest and latest times 2: use earliest and 2nd latest times 3: use 2nd earliest and 2nd latest times 4: use earliest and 3rd latest times 5: use 2nd earliest and 3rd latest times
MI_OE	1	MULTIPLE	MI lookup table output enable
MI_SEG	7	MULTIPLE	MI lookup memory segment. MI_ADR[19:13] are set to MI_SEG during a VME transfer
MI_SEL	12	MULTIPLE	Select time difference used in MI lookup: [11:9]: MI_MODE for MULTx = 0 [8:6]: MI_MODE for MULTx = 1 [5:3]: MI_MODE for MULTx = 2 [2:0]: MI_MODE for MULTx=3
MI_TBL	4	MULTIPLE	MI lookup table select (MI_ADR[19:16]): [3:2]: MULTS [1:0]: MULTN
MI_VME	1	MULTIPLE	MI VME access bit: 0: VME access prohibited (MI_FLAG bits valid) 1: VME access allowed (MI_FLAG bits are 0)
MI_WE	1	MULTIPLE	MI lookup table write enable
MINBIAS	4	TRIGFW	Minimum bias triggers: [3]: |ZVTX| < ZCUT[3] [2]: |ZVTX| < ZCUT[2] [1]: |ZVTX| < ZCUT[1] [0]: |ZVTX| < ZCUT[0]

MODULE_ID	16	VMEBUS	Module ID – 1 for VTX board
MODULE_WC	16	VMEBUS	Module word count, including the count itself (identical to the VBD word count since there is always an even number of 16-bits words)
MULTx	2	MULTIPLE	PMT hit multiplicity bin: 0: NHITx <= 6 1: 6 < NHITx <= 12 2: 12 < NHITx <= 18 3: 18 < NHITx <= 24
NHITx	5	J4	Number of PMT hits (TDCx[36:32])
NPERIOD	5	VMEBUS	Length of L1 trigger buffer
PDIF	1	TRIGFW	"Proton diffractive disassociation" trigger term (hits in south LM, no hits in north LM)
PHLOOSE	1	TRIGFW	Proton halo, loose cuts
PHTIGHT	1	TRIGFW	Proton halo, tight cuts
READ_EN	1	VMEBUS	Enable reading from the VME bus
RF	1	J2	53 MHz RF clock (7x crossing clock)
RFDIV4	1	CPLD	RF clock divided by 4
RFX2	1	Freq. mult.	RF clock multiplied by 2
S_RESET	1	VMEBUS	Soft reset that clears trigger queues
SGAP	1	CPLD	Synch gap marker – indicates crossing is in the abort gap containing the first crossing
SL_CLK	1	TGRMGR	Serial link clock
SL_ENABLE	1	TGRMGR	Enable sending data to the trigger manager (should be off during the synch gap)
SL_FASTOR	1	Serial Link	Serial link fast-or bit
SL_DATA	16	TGRMGR	Serial link data
SL_PARITY	1	TGRMGR	Serial link parity enable
SL_REF	1	Power	Serial link input level reference (3.3V or 5V)
SL_SPARE	1	Serial Link	Serial link spare signal
SPAREx	4	J4	Spare TDC signals: [3]: TDCx[39] [2:0]: TDCx[31:29]
!SRQ	1	VMEBUS	Service request - used to request VBD readout
STATUS1	16	VMEBUS	VTX status word 1: [5]: L2 crossing mismatch [4]: Readout buffer full [3]: L1 crossing mismatch [2]: L2 buffer full
STATUS2	16	VMEBUS	VTX status word 2: no bits currently defined
SUMx	13	J4	Sum of PMT times (TDCx[28:16])
T_H1x	8	J4	Time of the latest PMT hit (TDCx[7:0])
T_H2x	8	J4	Time of the 2nd latest PMT hit (TDCx[15:8])
T_H3x	8	J4	Time of the 3rd latest PMT hit (TDCx[23:16])
T_L1x	8	J4	Time of the earliest PMT hit (TDCx[31:24])

T_L2x	8	J4	Time of the 2nd earliest PMT hit (TDCx[39:32])
TDCx	40	J4	TDC board signals
TDIFx	8	Multiple	Early/late time difference - used in MI calculation, MI_MODE selects which PMT times are used
TFW_ANDOR	16	TRIGFW	Trigger framework and-or bits: [15]: MINBIAS[3] [14]: MINBIAS[2] [13]: MINBIAS[1] [12]: MINBIAS[0] [11]: MI_FLAG[3] [10]: MI_FLAG[2] [9]: MI_FLAG[1] [8]: MI_FLAG[0] [7]: PHTIGHT [6]: PHLOOSE [5]: AHTIGHT [4]: AHLOOSE [3]: EMPTY [2]: ADIF [1]: PDIF [0]: COIN
TFW_SGAP	1	TRIGFW	Trigger framework synch gap marker
TFW_SCALER	10	TRIGFW	Trigger framework foreign scalers
TFW_STROBE	1	TRIGFW	Trigger framework data strobe
TICK	1	VMEBUS HIST	Tick number – increments by one for each beam crossing clock, set to one when FC is asserted (ranges from 1-159)
TURN	16	VMEBUS	Turn number – incremented by one when FC is asserted, reset to 0 by S_RESET
VBD_WC	16	VMEBUS	VBD word count – number of 16-bit words that follow (fixed at 22)
VBD_DONE	1	VMEBUS	VBD readout completed
VME_DIR	1	VMEBUS	VME bus transceiver direction
VME_LW	1	VMEBUS	VME long word transfer
VME_MODE	2	VMEBUS	VME IO operation type: 0: VBD data transfer 1: Access register 2: Access MI lookup table 3: Access histogram memory
VME_OE	1	VMEBUS	VME bus transceiver output enable
VME_WR	1	VMEBUS	VME write operation
WRITE_EN	1	VMEBUS	Enable writing to the VME bus
XING	8	J2	Beam crossing number for trigger decision – ranges from 1-159 with FC signaling XING=1 (should match TICK)
ZCUTn	8	TRIGFW	Cuts on |ZVTX| for TFW and-or terms (n=0-3)

ZVTX	9	HIST TGRMGR TRIGFW	Vertex z coordinate – calculated by subtracting AVERAGES from AVERAGEN, giving an lsb for ZVTX that is c/2 times the TDC lsb (2's complement representation)