D0 Upgrade Electronics

Technical Design Report

for the

Upgrade L1/L2 Tracking Trigger - CTT

Includes

Central Fiber Tracker,
Central Preshower Detector,
Forward Preshower Detector,
Forward Proton Detector

DRAFT - Version 5 - DRAFT

by CTT Group*

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Thankyou.

2. Central Fiber Tracker and Central Preshower Axial Trigger, CFT/CPS

The Central Fiber Tracker Axial and Central Preshower Axail Front End Electronics, CFT/CPS FE, and Trigger system includes all of the Central Fiber Tracker Axial channels and the Central Preshower axial channels. Some of the main features of the system are as follows.

The CFT/CPS System

1. Includes all of the Central Fiber Tracker axial channels.
2. Includes Central Preshower axial channels.

L3 Readout

1. The analog signal from the CFT axial is input into an MCM channel. The analog signal from each CPS axial strip is split and input into a HIGH and a LOW gain channel. Digitized values are available to L3 only. Discriminator outputs are used for L1 and L2.
2. The HIGH and LOW gain channels for a given CPS strip are input into a single MCM, the CFT fibers are input into 7 other MCM's. The HIGH gain channels can have different SIFT thresholds and gains than the LOW.
3. The HIGH and LOW gain channels each have one discriminator output.

CFT/CPS Trigger System

1. Provides the means for triggering at level 1 on the information from the CFT axial and CPS axial detectors.
2. Supplies information for the level 2 CFT Trigger Preprocessor, CFTpp, the PSpp, and for the proposed STTpp.

For the L1 FPS Trigger

1 Tracks are found in the CFT axial layers from 1.5 GeV to infinity.
2 Clusters are found in the CPS axail for two threshold settings.
2 Each cluster is matched to a track. Tracks are tagged with cluster matches and clusters are matched with track matches.
4 Seventeen numbers are forwarded to the CFT Trigger Manager, CFTTM, for the global L1 decision. Sixteen number are sent for four Pt threshold bins by matched/ non-matched by isolated/non-isolated. Another number is the count of hits fibers in the sector.

For the L2 PS preprocessor

1. Pipelines track and cluster information.
2. Upon the receipt of a L1 accept forwards information to the CFTpp.

A block diagram of the components of the system is shown in Figure 1. There are two sets of front-end electronics boards, FE, in several crates located above the VLPX cryostat in the detector platform. These boards receive the analog signals from the VLPC's and process them for the L3 readout, shown as the Sequencer and VRB crates, and for the L1 and L2 triggers. In the center of figure 1 is the Concentrator system. This receives the L1 and L2 information from each of the FE boards, concentrates it and sends it on to the L1 and the L2 triggers.

The location of the VLPC cassettes for the CFT system is shown in Figure 2. The FE boards are located in five crates on the platform.

2.1 CFT/CPS Axial Trigger System Overview

The CFT/CPS Axial trigger system provides the means for triggering at level 1 on the information from the CFT and CPS axial channels, forms counts for a L1 multiple interaction veto, sends seed information to the muon level 1 trigger, and supplies information for level 2 trigger preprocessors. It also supplies, from the FE boards, the raw data from the VLPC channels for the level 3 read out.

For the L1 CFT/CPS Trigger it counts the number of tracks found in sixteen categories from all the FE boards and allows for a L1 trigger if any of these counts exceed a required minimum. For the L1 miltiple interaction veto it counts the number of fibers hit in each sector and compares this number to a minimum. It then looks at how many sector exceeded this minimum to decide the most probable number is interactions for this crossing. For the level L1 muon system it supplies from each FE a list of tracks indexed by Pt and ϕ. For the L2 preprocessors the system pipelines track and cluster information indexed by Pt and ϕ, and upon the receipt of a L1 accept compresses, sorts and forwards this information.

2.1.1 Functional Description

During normal running the operation of the system can be separated into four function blocks as shown in figure 2-1. In the FE the raw hit data is shared across the back planes between neighboring boards to form a seamless trigger. The raw hit data is then formed into bins for the fibers and clusters for the preshower. The bins are then compared to possible track roads and track candidates identified. The track candidates are then converted into lists of tracks indexed by Pt and ϕ. There are four lists of six tracks each where each of the four lists is for tracks in one of the four Pt threshold bins. Also the number of tracks in each of the four Pt threshold bins is saved. At this point the first six track candidates from the four lists are formed into another single list and passed to the L1 MUON. The six tracks sent to L1 MUON are taken from the four Pt threshold bin lists in order of the bin Pt, highest to lowest. Thus the tracks are not guaranteed to be but will very probably be the six highest Pt tracks. Concurrently with the above the number of single fibers hit in the sector is found and stored. In parallel with the track finding the strip information from the CPS Axial layer is formed into clusters. The location and width of the cluster is found. Next the tracks are matched with CPS clusters and those tracks, which point to a CPS cluster have their match bit set. Finally each track is checked to see if it is isolated and its track isolation bit set. A track is isolated if it is the only track in the home sector and both neighbor sectors have no tracks. There must not be any track in any of the four Pt threshold bins. A track, which has a cluster match, is isolated if it is the only matched track in the three sectors. A second, match isolation bit is set for this. A single sector can have only one isolated track or only one isolated matched track, but it can have both. At this time the track and cluster candidates are loaded into pipelines for transfer to L2 and the count of the track candidates found are forwarded to the CFT Receiver boards for the L1 trigger.

The CFT receiver boards, the second box in figure 2-2, are located in the Broadcaster Crates. Each receives information from several FE boards over a 1-bit wide fast serial link and translates it onto 16-bit wide parallel links for transmission through the crate back plane to the CFT L1 Concentrator boards. These boards which are the third box in figure 2-2, receive the individual counts and sum them into a single set per board, count the number of multiple interaction flags set, and send all this information out over another serial link to the CFT Trigger Manager, the bottom box. The trigger manager sums the several sets it receives into a single global set over the entire CFT/CPS detectors. At this point the individual sums are compared to cuts set by the host and are used to set bits in the AND/OR cable to the trigger manager.

Whenever a L1 accept for the system is issued it stops normal processing and shifts to L2 readout mode. The functional description for this can be divided into three blocks as shown in figure 2-3. First in each FE the data for the correct crossing is pulled out of the pipeline and sent to the CFT receiver boards. Also at each FE the raw data is pulled out of each SVX pipeline, digitized and read out for the L3. Most of the L3 readout system is shared with the silicon system and is not detailed in this document.

The CFT receiver boards operate in the same manner as for normal readout but now a different board, the CFT L2 concentrator board pulls the data off the back plane busses. The L2 concentrator board sorts the tracks from several front ends into a single list, sorts by Pt and sends a truncated list to the L2 preprocessors. It also sorts the clusters by ϕ, forms them into a single list and sends the list to the PSpp.

2.1.2 System Architecture

2.1.2.1 Geometry and Definitions

To ensure consistent results between the FE trigger, the online, the offline and the Monte Carlo processing a unified coordinate system and system of definitions must be adopted. This section describes the coordinate system and definitions. A detailed geometry of the detector is given elsewhere.

The D∅ standard coordinate system is used. In this system the +z-axis is along the proton direction, which is south. The x-axis is horizontal with the +x direction pointing towards the outside of the Tevatron ring (i.e., east). Figure 2-4 shows the South face of the detector. The y-axis is vertical with the +y orientation pointing towards the zenith. Azimuthal angles, ϕ, are measured with respect to the +x-axis such that $\phi = 0$ coincides with the +x-axis, $\phi = \pi/2$ coincides with +y and $\phi = \pi$ coincides with the -x-axis. The range of ϕ is $[0, 2\pi)$. Polar angles, θ, take values in the range $[0, \pi]$ and are measured from the +z-axis.

The CFT consists of 32 concentric layers of scintillating fibers, each layer at the same radial distance from the z-axis. That is on imaginary cylinders concentric with the z-axis. The 32 layers are arranged in 16 ‘doublet’ layers. Half of the layers have fibers parallel to the z-axis (axial layers) and the other half are at an angle to the z-axis (stereo layers). For the CFT trigger system, only the 8 axial doublet layers are used and are referred to as layer A through H with A the innermost layer.

In the rϕ plane, the CFT is divided into 80 trigger sectors with sector 1 subtending angles from 0 to $2\pi/80$. The number of fibers inside each sector in each of the 8 axial doublet layers is given by [16 + 4(j-1)], where j is the j-th layer and the 1st layer is the one at the smallest radii. Each doublet layer consists of one inner and one outer ``singlet'' layer and the numbers of fibers in these two singlet layers are the same. There is an offset between the inner and outer layers in ϕ by one-half of a fiber pitch. The exact geometry is detailed elsewhere.

The indices of the fibers are counted in the counter-clockwise direction if one stands at the south end of the D∅ detector. For each layer j, the fiber indices range from 0 to {[16 + 4(j-1)]*80 - 1}. The center of inner layer fiber 0 is at $\phi = 0$. Figure 2-5 shows an expanded view of a doublet layer. Note that ‘up’ for figure 2-4 corresponds to ‘to-the-right’ for figure 2-5.

A doublet bin is a logical combination of inner and outer fibers. DOUBLET[k] is defined logically as follows:

DOUBLET[k] = { NOT(OUTER[k]) .AND. INNER[k] } .OR. OUTER[k+1],

where OUTER[k] and INNER[k] correspond to the outer and inner singlet fiber indices respectively. Note that is important that exactly the above equation and the exact meaning of the indexes be used in the FE Trigger software, the M. C. simulation software, and the online and offline analysis software.

In the above definition, the width of a doublet bin depends on the diameter of the relevant singlet fibers and the gap between them, which is slightly different from layer to layer. Also the exact ϕ position of the bin boundaries depends on the 'active' diameter of the fibers. The total diameter of a fiber is 0.835 mm in which 0.060 mm is occupied by two layers of cladding to make sure that the light is internally reflected and 0.775 mm is the scintillator. A charged particle, which passes through the fiber center with normal incidence, generates about 12 photoelectrons on average. The average number of photoelectrons generated by a traversing particle is linearly proportional to the length of the track inside the scintillating fiber. The CFT is likely to operate at a threshold that corresponds to about 1 photoelectron. Then by simple geometric calculations, the thickness of the area of a fiber which on average generates more than 1 photo-electron in terms of the fraction of the fiber diameter is for this case $(1 - (1/12)^2)^{1/2}$ or 99.7% of the diameter. Therefore, under the above assumption, it is reasonable to claim that the "active" diameter of a fiber is equal to (0.775-0.060)mm or 0.715mm. Therefore the bin boundaries are approximately defined by the fiber geometry but can vary as the threshold used for the trigger or the light output from the fibers varies.

The CFT trigger system is inside a solenoid magnet, which bends all charged tracks in the $r\phi$ plane. A charged track is said to have positive momentum if its ϕ coordinate increases in value when its r coordinate increases in value. Whether this track is that of a positively or negatively charged particle depends on the sign of the magnetic field. If the positive magnetic field is orientated along the +z-axis, a positive momentum would correspond to a positively charged track, and vice versa.

2.1.2.2 Trigger Sectors

The level 1 trigger must accept a new event every 132ns (396ns) and send found tracks to the Muon L1 within 500ns. Therefore it is necessary to have all the data needed to make a trigger decision concentrated at one location. The trigger achieves this by dividing the global trigger into a series of local triggers each of which are independent of one another. The trigger finds tracks that propagate through all eight layers in small sectors or ϕ wedges of the detector. Each of these sectors contains all or most of the fibers transited by a track. The detector is divided into eighty trigger sectors each of which has 480 axial fiber channels and 32 axial central preshower strips for a total of 512 channels per FE board. Eighty trigger sectors result in a sector size which can contain a track below 1.5GeV and at most requires fiber information sharing between two sectors to reconstruct all possible tracks.

The trigger sectors are numbered in a counter-clockwise direction when viewed on the South face of the detector with sector 1 just above the positive x-axis. Since the fibers are built in ribbons, which extend over the ϕ direction, and the trigger sectors extend in the r direction, five mixing boxes, MB, are used to map from the ribbons to trigger sectors. Each MB contains 16 trigger sectors, with the first, MB-1, containing sectors 73 through 80 and 1 through 8. Figure 2-4 shows the South face of the detector with the sector numbering.

The sectors are arranged in 5 FE crates in a special order to meet two requirements. First the channels in a mixer box must all go to the same crate. Second, data is passed between FE boards so that the trigger does not have any cracks. If all the sectors were placed in one line starting with 1 and ending with 80, then passing data from sector 1 back to sector 80 would require that the signals be passed over a cable of about 8 feet. But the signal propagation time for this, about 12ns, is too long. If the sectors are packed into the five crates as shown in figure 2-6, then there are 5 jumpers between back planes, but now each of is about the same 16" length.

2.1.2.3 Hardware Inventory

The CFT/CPS Trigger system has;

1	GS with SCL
1	VRB Crate
1/2	Sequencer Crate
5	Front End Crates
80	FE Boards, 40 RHB & 40 LHB
2	Broadcaster Crates
1*	MTM Crate

Each VRB crates has;

1	VRB Controller board with SCL receiver
10	VRB Boards
10	VEPA Boards
40	Optical link receivers (from Seq)

Each ½ Sequencer crate has;

½	Sequencer Controller Board with SCL receiver
10	Sequencer boards
40	Optical link transmitters (to VRB), 4 per board
40	50-Conductor Cables, 4 per board

Each FE crates has;

8	Right Hand FE Trigger Boards
8	Left Hand FE Trigger Boards
8	BP Connectors for 50-Conductor Cables
8	BP Connectors for Cryo I/O

Each FE board has;

1(2)	Serial link transmitters to Muon L1
1	Serial link to broadcaster crate
1	1553 Node to receive download
1	SVX String
½	50-Conductor Cable from Sequencer
1	Analog and Serial Clock generator
8	MCM, each with 1 SVX and 4 SIFT chips

Each Broadcaster crate has;

1	Controller board
3	L1 Concentrator Board
6	L2 Concentrator Boards, 3 for STT/CFTpp & 3 for CPSpp

10	Receiver Boards
40	Copper Serial link recievers (from FE)
6	Optical Serial link transmitters to STT/CFTpp
6	Optical Serial link transmitters to PSpp
3	Copper Serial link transmitters to L1

Each Controller Board has;

1	50-conductor cable receiver
1	1553 Node

Each Receiver Board has;

4	Copper Serial link receivers

Each L1 Concentrator Board has;

1	Copper Serial link transmitter

Each L2 Concentrator Board has;

2	Optical Serial link transmitter

2.1.2.4 Hardware description

Figure 2-1 shows the overall data flow of the system. It could also be considered a crate level diagram of the system since each box corresponds to one or more crates.

The data starts in each of the 80 FE boards located on the VLPC cryostat in the center platform. During L1 live time each FE continuously transmits information for each crossing, within the time of one crossing, to two different destinations. One link is to the muon L1 located on the east platform and consists of 80 fast serial copper links. The other link, which serves a dual function, uses the same type of hardware and goes to eight crates on the west platform. During L1 live time this second link carries track counts from the CFT FE. And from each of these crates fast serial links transmit data to the CFT Trigger Manager, CFTTM, in the same crate as the Muon Trigger Manager on the east platform. When a L1 accept is received this link transmits track lists from each FE to the same four crates. And from there the track lists are transported to L2 preprocessors located in the mobile counting house over a fast optical serial link. Figure 2-2 is a functional diagram of the system during L1 times and figure 2-3 is a functional diagram of the system upon a L1 accept.

2.2 CFT/CPS Axial Trigger Front End, CFT FE

2.2.1 Functional Description

The CFT/CPS Axial Trigger Front End boards are mounted on the VLPC cassettes which are in turn inserted into the top of two VLPC cryostats located in the center aisle of the detector platform.

Each of the 80 FE boards has several functions. The principle functions are supporting the VLPCs, VLPC signal processing and producing a fast logic signal within the MCM, finding the track, and reporting out the trigger information. Figure 2 is a schematic of the data flow on each FE.

2.2.1.1 VLPC Support

Visible Light Photon Counters, VLPC, are used to convert the light produced in both the scintillating fibers of the CFT and the scintillating strips of the CPS to electronic signals. Each VLPC chip contains a two by four array of 1mm diameter photo sensitive areas and operates at from 6 to 14 degrees Kelvin and at a bias voltage of 6.5 volts. The VLPC chips are mounted in 1024 channel cassettes that are inserted from the top into a special cryostat. The tops of the cassette assemblies when placed in the cryostat form an electronics crate. This crate contains special back planes and holds the front end electronics boards, CFT FE. For space reasons 1/2 of the FE boards must have their components mounted on the left hand side of the boards when viewed from the front of the crate while the other half are the VME standard right hand side. Therefore each type of FE board has two handedness versions.

The bias voltage is routed from the crate back plane to the VLPCs over the FE boards. Each VLPC chip has a single bias supply line but each of its eight pixels has a bias return line. The bias supply is -6.5V and the return is at 0V. A dominate failure mode of a VLPC pixel is for the output to latch up and draw a large current. This excess current can warm the entire chip and cause the entire chip to fail. To guard against this a current restricting resister is placed in series with the bias return. After this resister all the bias returns are tied together. All the VLPCs in a single cassette share a common bias supply and return.

The VLPC output signal is superimposed on the bias return. Therefore the input into the MCMs must be AC coupled to the bias return. This isolation capacitor is located just before the protection resistor on the FE board. Each FE board receives 512 VLPC signals and therefore has 512 sets of capacitors and resistors. To keep the space required down the capacitors are small surface mount types and the resistors are in surface mount packages.

The monitoring of the cassette temperature and the power for heaters for each group of 64 channels is routed over the FE boards also. These services are only routed on the right hand boards.

2.2.1.2 Analog signal processing

The expected mean signal level from the VLPC is 30,000 electrons per photoelectron and the longest charge collection time is about 70ns. The number of photoelectrons varies widely from roughly 10 at the center of the fiber tracker to 1500 for the preshower detectors. The signal needs to be both digitized and discriminated. The fiber tracker needs only a few bit ADC while the pre shower detectors need 11 bits because of their larger dynamic range and the discriminator threshold needs to be programmable over a factor of 10 range. Because of radiation damage expected during the running and downward fluctuations of the signals, the minimum discriminator threshold is 4 fC (24,000 electrons) for the fiber tracker while the maximum is around 5000 fC for the preshower. The signal processor must also provide for up to a 32 crossing delay for forming the L1 trigger. Also 512 channels are needed per circuit board.

The ADC is the SVX IIe chip, which was developed for the silicon detector. It has an 8 bit ADC with programmable gain so that the full scale charge ranges from 25 fC to 150 fC. The fastest rise time is 90ns (42ns charge collection time for 132ns crossing intervals). This does not meet all the requirements mentioned above. To meet these demands, another custom chip (called SIFT) which fits in front of the SVX IIe was designed. It has a selectable gain of 0.25 or 0.5 and a discriminator with a variable threshold of either 3 to 50 fC or 30 to 300 fC. Both the discriminator range and gain are selectable on the chip. The SIFT charge acquisition time is 70ns.

The 11 bit ADC requirement is met by using 2 SIFT-SVX channels for each of the preshower channels. A 3 way capacitor charge divider (figure n) is used so that one channel will get one tenth of the charge of the other giving slightly more than 11 bits of range. The third capacitor shunts the excess charge to ground so that the large amplitude signals are within the range of the SIFT and SVX IIe. For example, by shunting 90% of the charge, the 5000 fC preshower signal will is reduced to 500 fC at the SIFT input. If the SIFT has a gain of 1/4, 125 fC is sent to the SVX IIe which is well within its range. The 300 fC discriminator threshold is on the input charge so this signal is above the highest discriminator setting. At the other end of the scale, a few fC signal is reduced by only a factor of 2 which is also well within the range of the SVX IIe.

Each SIFT chip has 18 useable channels. Four SIFT chips and one SVX IIe are packaged together in a multichip module (MCM) where only 72 of the 128 channels in the SVX IIe are used. There are 8 MCMs on each board and all the SVX chips on each board are connected together into one readout string (the equivalent of one high density interconnect in the silicon system) and read out with a D0 sequencer module.

The output of the discriminator stage is latched to an output driver and therefore remains high for about 100ns. This signal is TTL, which is suitable for driving the following trigger logic.

2.2.1.2.1 Charge Pileup

The preamplifier in the SVX chip is not reset every crossing since it needs a large fraction of a microsecond to settle. Therefore it is only reset during a time when beam crossings are not seen by the detector. Initially there will be three super-bunches in the Tevatron and eventually there may be only one. Between preamplifier resets it sees all of the charge from all particles traversing a given scintillation fiber. The average amount of charge into the SVX per turn can be calculated. This value is important because the digitized output of the SVX is the difference of the integrated charge after a pipeline stage minus the integrated charge before that stage. The SVX preamplifier saturates at about 450 fC and once it has reached saturation all subsequent pipeline stages will digitize to zero, the pedestal value. Also as the preamplifier approaches saturation a single hit may push the preamplifier into saturation resulting in a truncated digitized value.

Luninosity	20	E+31		
Bunches	36		108	
Ave. # of Int	5.13		1.71	
Occupancy per interaction	8%		8%	*100tracks/80/16*
pe per hit	15		15	
Charge from VLPC	96	38 fC	96	13 fC
SIFT Gain	0.4	15 fC	0.4	5 fC
Crossings	36	554 fC	108	554 fC
	12	185 fC	36	185 fC

In the above table the average amount of charge into an SVX in the innermost layer is calculated. The table assumes that there are 100 tracks per interaction, each track deposits 15 photo electrons in the fiber, and that the VLPC gain is 40K. Then each track sends 96 fC of charge from the VLPC to the MCM and SVX. From the table it is clear that at the highest luminosity the SVX will need to be reset three times per turn. Only at 8 E+31, the luminosity at the end of run I, could the SVX be reset only once per crossing.

2.2.1.3 CFT Track Finding

2.2.1.3.1 Hit Transfer

Each of the 80 FE sectors subtends about 4.5 degrees. At the lowest Pt envisioned, 1.5 GeV, all tracks which cross the outer detector layer, H layer, are completely contained within the sector, called the home sector, or are partly in the home sector and one of the adjacent sectors, called the neighbor sectors. To form a seamless trigger for all tracks which intercept the H layer, called the anchor layer, within the home sector, hit information from the two neighbor sectors must be imported.

When the logic signal for each of the home sector fibers exits the MCM it is latched into a PLD. The latching action removes the time scatter of the signals due to particle eta value, light path length differences and other sources. This latching PLD then distributes the home signals to the track finding logic on the home board and to the logic on each of the two neighbor sectors. In order to minimize the number of traces on the FE boards, the number of pins on the latching PLDs and the number of back plane lines the data out of the latching PLDs is 4 to 1 multiplexed.

Four latching PLDs are used for the CFT signals and a fifth is used for the CPS signals. A special sorting of the fiber layers into the latching PLDs equalizes the size for each and allows for the different timing of the two inner layers, which are shorter.

2.2.1.3.2 Track Finding

The track finding is performed in parallel within 4(or6) large FPLDs. Figure 2 shows the data flow for the track finding in the CFT FE. Each of these FPLDs gets the entire set of input fiber signals which, consists of 480 fibers from the home sector and 192 fibers from each neighbor. Since each gets all the input information and has identical output connections, which part of the track finding is performed in any PLD is simply a matter of programming. This allows the greatest flexibility for evolving the tracking algorithm as experience is gained with MC and real data or as physics goals change. It is also possible to use different algorithms in each PLD. Details of the baseline algorithm are given below.

2.2.1.3.3 Track Indexing

Finding the track candidates is only half of the problem. The found tracks must be reported out to clients in a meaningful way. Each track candidate is represented by a 16 bit word into which is packed its momentum and its phi value at the outer layer of the CFT.

Sorting through the track candidates and assigning an index to each is resource intensive within the PLD, and in fact requires about the same resources as the track finding itself. The track indexing is contained in the same PLD as the track finding for information handling reasons. At the point in the algorithm where the track candidates are found the information content of the problem is at its maximum. Transferring that information out of one PLD and into another is not possible. Indeed if it were possible the track indexing itself would be trivial.

Since the track indexing is located in the same PLD as the track finding, possible algorithms are not restricted by the hardware external to the PLD and may continue to be optimized, or to be re-optimized to different goals as the run proceeds. The combined track finding and track indexing portions of the problem require the largest and fastest PLDs available and represent a major component in the expense for the trigger.

2.2.1.4 Transfer to L1 Muon

The L1 Muon system uses the CFT track candidates as seeds for finding candidate muon tracks. Since these are the seeds for its track finding the list must arrive at the muon trigger crates before the muon chamber information. The muon drift time is about 800ns, thus the timing specification for CFT tracks to muon is within 800ns. Figure 5 shows the timing of the different tracking stages up to reception at muon. (A transmission distance to muon of 90ns was used.) These times are based on simulations of the PLD code and detailed studies of the signal timings.[1]

As the list of six tracks exit the four track finding PLDs they are collected in another PLD which orders them from highest to lowest Pt threshold group and transmits the first six to muon. The list of six tracks is transmitted from the FE's each crossing over a fast serial link that sends 16 bits of information every 53MHz clock cycle. This fast serial link over copper was developed for the muon trigger.

2.2.1.5 CPS Cluster Matching

The Central Preshower, CPS, axial strips are included in the trigger. The VLPC signals from each strip is passively split into two and each is input to a SIFT channel with separate thresholds. As the CFT logic signals are being input into the tracking FPLDs the CPS logic signals are input into a separate FPLD. This FPLD pipelines the strip information while the track candidates are being found. It then forms the CPS clusters in parallel to decoding the CFT track indexes. A combination of two/three center strips above a high threshold, about 4 mips, with strips on either side below a low threshold, about 1 mip, constitutes a cluster. Then it compares the clusters to the CFT track information to form a track match. If a match is found a bit is set in the original track list for that track. A more detailed note on CPS cluster matching can be found in the references.[1]

2.2.1.6 Isolation

The logic next determines if the tracks in the list from each FE should be tagged as isolated. As stated above a track is isolated if it is the only track in the home sector and the two neighbor sectors within a Pt threshold bin.

If there are one or more tracks in the home sector the logic raises the level on a line, which via the back plane terminates in the neighbor logic to either side. There is one line per Pt threshold bin and per CFT or CFT/CPS for a total of eight lines. The logic then looks at the corresponding input lines from each of its 2 neighbors, 16 lines. If neither neighbor found a CFT track the CFT track isolation bit is set, and if neither found a CFT/CPS track the CFT/CSP track isolation bit is set.

2.2.1.7 Track Counting

The L1 muon and L2 preprocessors require a list of tracks, the CFT L1, however, requires a count of the number of found tracks. A by product of the track indexing described above is a count of the number of tracks. This number is transferred to the cluster matching where a second count is created, the count

[1] PLD simulations - FB, Detailed studies – MM

of CFT/CPS tracks, and passed on to the isolation stage. At that stage two more counts are added, isolated CFT and isolated CFT/CPS. This completes the set of 16 counts.

These 16 numbers are moved to an output buffer for transmission to the CFT L1 trigger. This link is the second copper fast serial link mounted on each FE board, which sends 96 bits each crossing. The 16 numbers, each of which is 6 bits wide are packed into this data block and transmitted.

2.2.2 System Architecture

2.2.2.1 L2 Pipeline

The track lists are stored in a pipeline for retrieval upon a L1 accept. There are 4 pipelines, one for each Pt threshold bin. Each is 6 tracks by 16 bits wide, 96 bits wide, by 32 deep. These pipelines are implemented in fast FIFO chips.

2.2.2.2 FE Controller

The control and coordination of all the functions of the FE board requires a sophisticated controller. The controller must receive the 53MHz clock, the crossing signal, the L1 accept and an external reset and must monitor the mode of the on board SVX chips. From these it must generate the clock signals used to move the data between PLDs on the board and internal clock signals for the many PLDs. It must also generate the clock signals used by the SIFT chips and keep those chips in phase with the SVX chips which for technical reasons must be clocked external to the FE board. The controller is not a single chip but a master chip and several subordinate chips located near the chips they support.

2.2.2.3 Download Support

Each of the large PLDs requires about 250Kbits of information for its programming. Programming that is lost on any power interruption. A download system is located on each FE board consisting of non-volatile memory, which stores a copy of the programs for all chips on the board and a download controller, which is a non-volatile PLD. Upon power up or reset the download controller resets itself and then downloads all the FPLDs from non-volatile RAM. During operation an external host reads the contents of the FE RAM and compares it to a master copy. If any differences are found the master copy is again downloaded to the FE board(s). Note that for the as-built detector each tracking PLD may have different tracking programming which has been customized to the surveyed fiber locations.

2.2.2.4 Tracking Algorithm

2.2.2.4.1 Introduction

The goal of the track finder is to achieve the highest efficiency for finding the real tracks while maintaining the largest possible rejection factor for fake tracks. In the fiber tracker the main source of fake tracks is a random fiber hit near a real track that when included with the real track hits results in a fake track of higher Pt than the real track. When this occurs for real tracks just below a Pt threshold the fake track promotes it into a found track. Another significant source when the occupancy is high is the overlap of two or more lower Pt tracks which mimic a single higher Pt track.

The greatest rejection is achieved in the trigger if a hit is required on all of the eight layers of the tracker and the road width at each layer is one fiber pitch wide, about 1mm. Wider roads result in too many extra fake tracks. Particles too often scatter out of narrower roads. The base line set of roads used in the MC show the tracker to be about 97% efficient for muons above 5 GeV and over 95% efficient for electrons over 10 GeV. There are over 850,000 roads in the tracker.

The axial trigger uses field programmable logic devices, FPLD's, to implement the trigger logic. Each road is converted into a logical equation within the device consisting of an eight fold AND of the doublet hit in each layer. Since the doublet hit is a logical OR of two singlet layers its efficiency is over 99.5%. Thus the eight fold efficiency is above 96.5%. The major advantage of using these devices is that, since the trigger logic can be programmed into them when they are in place in the detector, they can be reprogrammed as required by changes in Physics interest or detector geometry at any time during a running period. The hardware design of the boards was purposely kept as general as possible and the specific design choices are implemented in the firmware as much as possible. Thus design changes require only a new software download, not a hardware fix. FPLD's are also extensively used in the commercial market and market forces are expected to both drive down their price and drive up their performance.

The basic geometry of the tracker is discussed in several places.[2] Some of the basic features which are important for discussions of forming the trigger are presented here.[3, 4, 5] Each layer is made up of two single layers. The outer of these two layers is staggered by ½ a fiber so that there are no gaps, all tracks either pass through the inner, the outer or both layers. There are 8 doublet layers. The fibers are routed to the electronics so that the signals from all 8 layers for exactly 1/80th in phi of the detector go to one board. This 1/80th phi slice of the detector is called a sector and each sector contains 4 cells. A cell is the smallest phi slice that has a non-repeating geometry. A sector is 16 fibers wide at the innermost or A layer, increases by 4 fibers for each layer until it is 44 wide at the 8th and outermost layer, the H layer. A cell is 4 wide at the inner, 1 wider on each layer and 11 wide at the outer layer.

2.2.2.4.2 Finding Track Candidates

2.2.2.4.2.1 Doublet Finding

The first part of finding a track is forming a hit in each doublet layer. The individual fiber hits of each pair of singlet layers must be formed into a hit bin in the doublet layer. For the base line design the doublet bin size is the same as the fiber size of each layer. The doublet bin can be formed in the most basic manner possible, just an OR of an inner singlet fiber with one other outer singlet fiber. In equation form this is:

hl [k] = hi [k] OR ho [j];

where k and j are the k'th and j'th fibers on the ribbon. The indexes are such that the inner and outer fibers are adjacent, but whether the outer fiber is to the right or the left of the inner is arbitrary. This manner of forming a doublet doesn't distinguish if a particle transited one or both fibers. Also a particle which transits an inner fiber of one doublet pair and the outer fiber of the adjacent doublet pair will generate two doublet bins hit.

The doublet formation was expanded to eliminate the possibility of a single track forming two adjacent doublet bin hits. The doublet equation is then:

hl[k] = (NOT(ho[j -1]) AND hi[k]) OR ho[j];

Now if a track passes through hi[k] and ho[j - 1], hl[k] will be FALSE and only hl[k - 1] will be TRUE. Due to the architecture of the PLD this modification does not take any more logic cells, LC's, but it does require more interconnects.

2.2.2.4.2.2 Track Finding

The eight doublet layer bins are then combined to form a track. The list of roads, which are found both analytically and with a special Monte Carlo, are translated into equations and loaded into the trigger logic. The base line requires that all 8 of 8 possible doublet layers be hit for any equation to be satisfied. There are about 11,000 equations in each sector and 2,600 in each FPLD. These equations are of the form:

T1013172227323945 = al[10] AND bl[13] AND cl[17] AND dl[22]
AND el[27] AND fl[32] AND gl[39] AND hl[45];

The several terms that share the same A layer doublet number, here 10, and the same H layer number, here 45, are then OR'ed together:

Trig_a10h45 = T1013172227323945 OR T10…45 OR …

A strait line corresponding to an infinite momentum track drawn from the center of the detector and through the <u>center</u> of an H layer bin passes through just one A layer bin which is defined as the zero offset bin for the H layer bin. The different Pt bins can then be defined with respect to the relative offset from the zero A layer bin. For the above example the zero A layer for an H layer bin value of 45 is 17. Therefore the offset for A layer bin 10 is -7. Table 3 gives a calculation of the Pt for tracks of differing offsets from the H layer bin.

The output from this stage is a matrix of pins which is 44 phi bin rows, the H layer bins, by 24 Pt bin columns, the A layer offset bins. Each pin in this matrix will be TRUE (1) if a track was found or FALSE (0) if it wasn't.

2.2.2.4.2.3 Serializing the Found Tracks

The track finding stage outputs a matrix of pins. The array must be searched in decreasing Pt order looking for any pins that are TRUE. As each TRUE pin is found the phi bin address and Pt bin address for that pin are loaded into a register. This is basically a serial problem that must be solved in parallel hardware. If it were done serially the process would take at least 44 x 24 = 1056 steps. To get a result every crossing this processor would have to make 1056 steps times the 27 MHz crossing frequency which requires a clock rate of 30 GHz. Alternatively the problem can be solved using PLD's using a tree structure with many parallel branches in a very short time. However, this method requires significant resources. Most of the pins or elements in this matrix are FALSE since the occupancy of the 1056 pins is expected to be less than 1%. Thus some short cuts can be taken in solving the problem, which are very efficient in their use of logic resources.

The equations are sorted by Pt value into 24 bins and by Phi index into 44 bins giving 1056 2d bins. Each 2d bin is assigned an index number that codes its phi bin value and its Pt bin value. It should be noted that this sorting criterion is arbitrary. The equations could be sorted, for example, according to the mean Pt of the equations and the mean phi value at a particular radius instead of by H value and A offset. Or they could be sorted by outer fiber bin and inner fiber bin. All that is required is that 2d bins of 44 phi units by 24 Pt units are formed.

Next the matrix is subdivided into 4 Pt groups corresponding to the 4 Pt threshold groupings of the L1 trigger terms. Each of these 4 groups is contained within a separate PLD. Each of these sub-matrixes are then 44 phi bins by 6 Pt bins. Then, for each of the 44 phi bins, the 6 Pt bins are input into a priority encoder which outputs the index of the highest priority Pt bin that is TRUE. The order of inputs into the priority encoder is arranged so that the highest Pt TRUE is output. Information about any other bin that may have been TRUE is lost. However, information should be lost less then 1/4% of the time.

At this point the matrix is reduced to a single column of 44 index numbers. The next step scans this list and puts the first six non-zero values into an output buffer. This step is done in a mixed parallel/serial mode to reduce the latency for the process to its minimum. Any information about any tracks beyond six is lost in this stage.

2.2.2.4.2.4 Robustness of the Design

The finding of track candidates discussed above is done in a set of four FPLD's where each FPLD is used to find the tracks in one Pt threshold range.

The board hardware is designed to hold six and laid out such that the extra two can be added if the necessity arises and the resources are available.

There are many things with would require the number of equations to be increased and hence more FPLD resources needed and few that would allow a decrease. The minimum Pt is a case in point. The number of equations doubles in lowering the minimum Pt threshold from 3.0 GeV to 1.5 GeV. (It scales almost exactly as the inverse ratio of the Pt.) Therefore the low Pt threshold bin requires by far the most equations. The equations used for this design assumed that the fibers were exactly placed on the detector. Studies show that systematic placement errors starting as small at 50 um significantly increase the number of equations[6]. The interaction vertex in R-Phi for this design is assumed to be a point source. We know from the accelerator that the beam spot will be about 50 um. The size of the beam spot has the same effect on the number of equations as fiber placement error[7]. Think of it as a fiber at r = 0. The CFT trigger starts to be inefficient for displaced vertex tracks. Recovering that efficiency requires more equations. Also it is believed that while the efficiency of each doublet layer will be over 99.5% at the start of the run, this efficiency will drop with aging and radiation damage especially if we see high luminosity for much of the run. As the doublet efficiency drops below 99% the base line trigger which requires all eight layers drops below 90%. This can be remedied by only requiring 7 of 8 layers, but a 7 of 8 trigger requires four times the logic resources. All of these argue that the track finder stage should be implemented in as many of the largest FPLD's that fit the budget.

Since the board is set up for 4(6) FPLDs in parallel, tuning of the algorithm independently within each Pt threshold bin is possible. A 7 of 8 trigger could be implemented in the highest Pt bin for example to maintain its efficiency. While the logic for the other Pt bins could be tuned for other criteria.

2.2.2.5 L3 Readout

The L3 readout should include the data from the detector and all data created at each stage of the trigger. Only the FE sees the raw data but both the FE and concentrators create trigger information.

2.2.2.5.1 The FE L3 Readout

The CFT/CPS raw data is digitized and pipelined in eight SVX chips on each FE board which are connected into one string and read out by the SERIAL board located in crates located elsewhere on the platform. Each FE string has eight SVX chips for the raw data plus a virtual SVX chip located within a PLD chip for the data created by the trigger. This virtual SVX chip collects the readout information discussed below, pipelines it, and passes it on in a format imitating a single SVX chip. This virtual SVX chip receives the same mode controls as the other SVX chips but interprets them differently. The SVX mode is loaded into each SVX independently during an SVX chip download. The real SVX chips send the data byte by byte. The first byte is the channel address and the second byte is the ADC counts. The first bit of the address has a special meaning so only 15 bits of information are passed per channel. The virtual SVX receives the data as 16 bit words. It drops the msb and sends the remaining 15 bits with the high byte in the address position and the low byte in the data position.

The input into the FE boards is the analog VLPC signal which in addition to being digitized by the SVXIIe chip is discriminated by the SIFT20a chip. The discriminated signal is then presented to the trigger logic where track lists and track counts are formed. These track lists are then sent off board to the triggers. Within the track logic intermediate objects are formed and discarded. The candidate information for transmission to the L3 includes; the discriminator output bits, the resulting track lists, the track counts and information from intermediate logic stages.

Sending all the above information all the time would result in an unduly long readout time and too much L1 dead time. To keep the dead time minimal and to allow for detailed diagnostic ability four levels of readout are formed. They are NORMAL, INPUT, DIAGNOSTIC and TEST.

2.2.2.5.1.1 NORMAL

The NORMAL mode is the minimum length readout and is designed for use in normal running. (SVX Sparsify Mode.) For this mode the L3 readout for the virtual SVX consists of the list of 24 found tracks, the 16 count numbers, and a 16bit status word. Table xxx shows the contents of each byte of the readout string. The added length is 496bits and adds about 0.58usec to the SVX readout time. *Note that a string of eight SVX chips is 16Kbits long and takes up to 19usec to read out at full occupancy. So the added length is comparable to about 3% occupancy.*

2.2.2.5.1.2 INPUT

The INPUT mode includes the NORMAL mode data plus the discriminated signals from the home and neighbor sectors for both the CFT and CPS fibers. (SVX Read Neighbors Mode.) This readout adds 1408bits and 1.65usec. While this mode does not add much to the readout length it adds a considerable amount of resources to the logic because logic must be converted to a pipeline fifo to store the hits from each of up to 32 crossings until L2 readout time. Therefore when running in this mode the CFT and CPS trigger PLDs are re-programmed to use less resources, thereby freeing up logic to pipeline the input bits.

2.2.2.5.1.3 DIAGNOSTIC

The DIAGNOSTIC mode includes the INPUT data plus an extra Kbit of diagnostic information. (SVX Read All Mode.) This readout adds 2448bits and 2.88usec. As above the trigger PLDs are re-programmed in this mode to pipeline the input bits and also to intercept the results of intermediate steps within the logic and output diagnostic information. Note that the diagnostic information for each crossing must also be pipelined, so extra resources are needed to both create the output diagnostics and to pipeline them.

2.2.2.5.1.4 TEST

The TEST mode adds 2Kbits of information plus a 16bit status word, adding 2.43usec to the readout time. (The undefined SVX Mode.) In this mode any of several test processes are loaded into one or more of the trigger PLDs. For this case the raw data into the trigger logic is ignored so the data read out of the virtual SVX chip is independent of the data read out of the real SVX chips. Therefor in this mode the readout of the real SVX chips is turned off.

2.2.2.6 FE Board IO

The FE board is an I/O intensive board. It has three back plane connections of 160 pins each, plus 8 bottom edge connections of 88 pins each for a total pin count of about 1200. Each of the bottom edge connectors recieves 64 new signals every 132 ns for a bit rate of 3.88 Gbits/sec. 320 of the back plane pins transfer data every 25ns for a bit rate of 12.8 Gbits/sec.

2.2.2.7 Transfer to L1 Muon

The transfer of track information from the CFT FE board to the Muon Trigger System is done through a pair of serial transmitter and receiver daughter

CFT/CPS Trigger FE Board I/O Types
Back Plane

- 1553 Link
- Sequencer Link
- TCL Input
- Isolation Flags
- PS Signal Transfer
- Fiber Signal Transfer
- Cryo Support I/O
- Power & Grounds

Bottom Edge Connector

- VLPC Bias Supply
- VLPC Bias Return / Signal Source
- Cryogenic Services

Front Pannel Connections

- Muon L1 Copper Link Transmitter
- Broadcaster Crate Copper Link Transmitter

Front Pannel Displays

- Bottom Edge Connection Indicator
- Serial Link Status Indicators
- L1/L2 Mode indicator Light
- Download Status Indicator Light
- Hex Status Display

Front Pannel Probe Points

- Power Sense
- 16-bit Status

boards. The detailed I/O specification of these boards can be found in [1].

In each octant, CFT trigger information from 10 CFT FE would be transferred to a MTC05 (Muon Trigger Card “05”) located inside one of the three Muon Trigger Crates. Each MTC05 card accepts 16 inputs but only 10 are from the CFT FE whereas the others are inputs from the scintillator hits.

From each CFT FE, data of 6 tracks each with 16 bits and a reference clock are fed into a serial transmitter daughter board which is plugged into the CFT FE board. From this transmitter board, the CFT information is sent to the serial receiver daughter board imbedded in the MTC05 over coaxial cable (RG58 or equivalent) using the AMCC Gbit/s serial link chipset [1], in which data is transferred in groups of 96 bits.

There are seven RF clock cycles per 132 ns and data is transferred as six data words plus a parity word during each bunch crossing. During the Synch Gap, Fiber Channel synch characters (K28.5) are sent instead.

In each coaxial cable, the necessary inputs from the CFT FE to the MTC05 are as follows:

10 sets of CFT track information, each from a CFT FE board and having a maximum of 6 tracks;
RF Clock
Enable
Parity_Enable

“RF clock” is the clock running at the accelerator RF frequency. All other inputs, including “Enable”, are referenced to this clock. “Enable” indicates the end of Synch Gap and the start of real beam crossing. Data is transmitted when "Enable" is high, and odd parity is transmitted when both "Enable" and “Parity_Enable" signals are high. The parity word is typically added as the 7th word after the 6 data words sent for a bunch crossing.

The following figure shows the relationship among the terms described above.

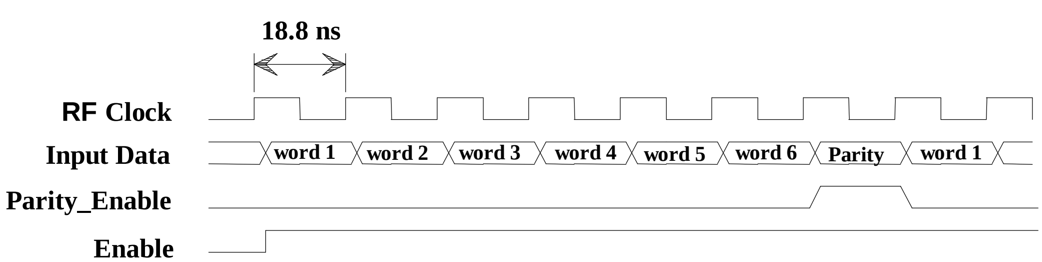


Figure 1: The input timing relationship among the RF Clock, input data, "Parity_Enable" and "Enable".

At the receiver daughter board, there will be two clocks, "Ref_Clock" and "Receive_Clcok". "Ref_Clock" is input from the motherboard (MTC05) and should be at the accelerator RF frequency. "Receive_Clock" is the extracted from the input signal, i.e. the above-mentioned RF_clock from the transmitter. These two clocks have the same frequency but may not be in phase with each other and the phase difference depends on the length of the cable carrying the serial input data. A FIFO can be used to switch the parallel data from the "Receive_Clock" to "Ref_Clock".

Format of Data Words from CFT Front End

Bit #		Field Bit #	Use
15	Most Sig.	0	Track Found Flag [1=found]
14		3	spare
13		2	spare
12		1	spare
11		0	spare
10		0	Sign of the Pt for Track
9		3	Inner (A) Layer Offset from Outer Layer Bin
8		2	
7		1	
6		0	
5		5	Outer (H) Layer Phi Bin
4		4	
3		3	
2		2	
1		1	
0	Least Sig.	0	

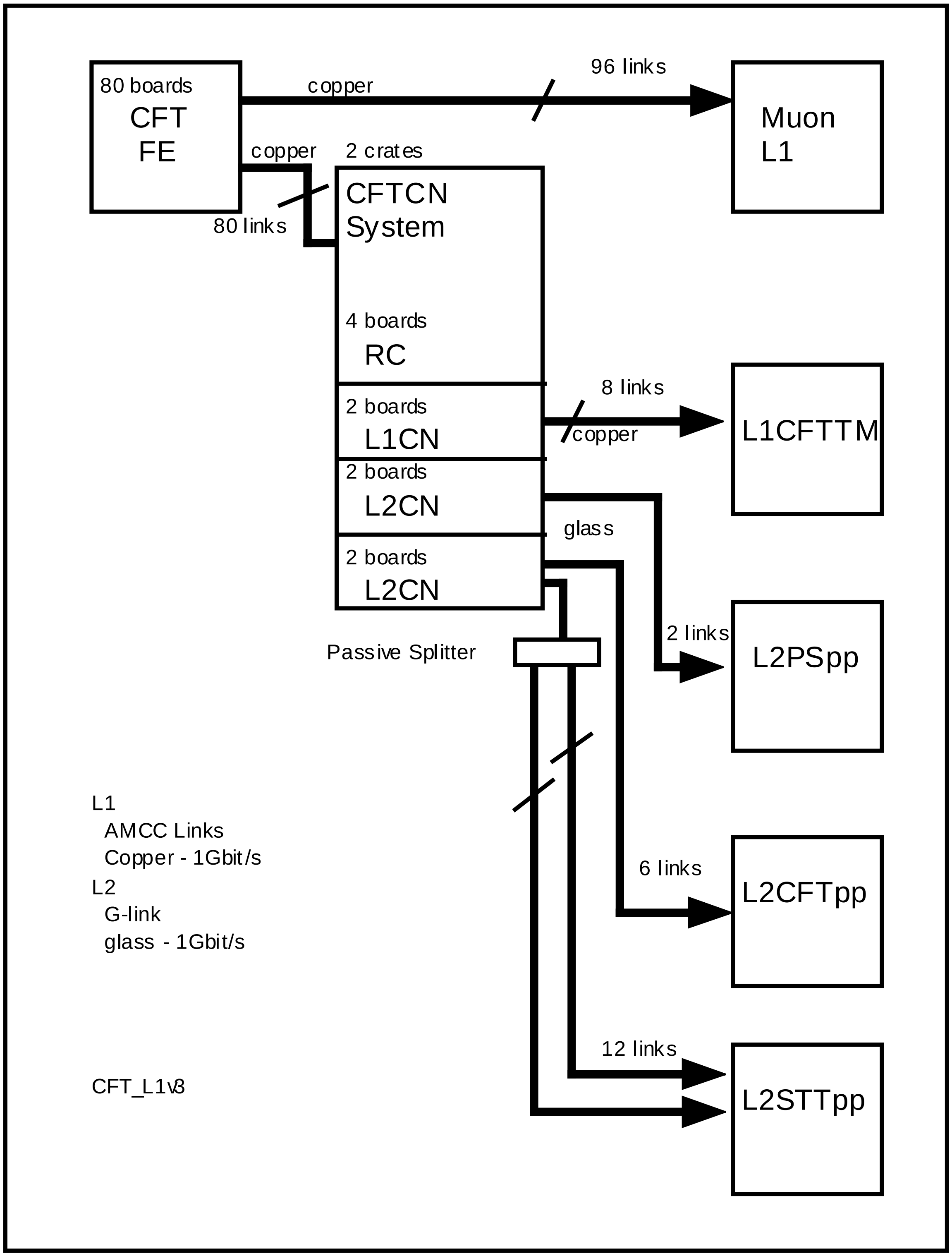
Table 1. Definition of bits for L1 MUON track word. Six bits are used to identify the phi position. Five bits are used to identify the momentum including its sign. And one bit is used to tag the word as containing valid track information.

Term Number	Description of Term			
Term_15		CFT above	Highest	Pt Threshold
Term_14		CFT above	High	Pt Threshold
Term_13		CFT above	Medium	Pt Threshold
Term_12		CFT above	Low	Pt Threshold
Term_11		CFT/CPS above	Highest	Pt Threshold
Term_10		CFT/CPS above	High	Pt Threshold
Term_9		CFT/CPS above	Medium	Pt Threshold
Term_8		CFT/CPS above	Low	Pt Threshold
Term_7	isolated	CFT above	Highest	Pt Threshold
Term_6	isolated	CFT above	High	Pt Threshold
Term_5	isolated	CFT above	Medium	Pt Threshold
Term_4	isolated	CFT above	Low	Pt Threshold
Term_3	isolated	CFT/CPS above	Highest	Pt Threshold
Term_2	isolated	CFT/CPS above	High	Pt Threshold
Term_1	isolated	CFT/CPS above	Medium	Pt Threshold
Term_0	isolated	CFT/CPS above	Low	Pt Threshold

Table 3. The definition, version 1.0, of the AND-OR terms from the L1 CFTTM.

Luminosity	Crossings	Other	Av per 5	Ratio of 4	Ratio of 8	Ratio of 16
2.00E+32	108		4.72	0.4896	0.9483	1.0000
2.00E+32	108	1/40	1.19	0.9552	0.9998	1.0000
2.00E+32	36		7.07	0.1669	0.7202	0.9989
2.00E+32	36	1/40	4.53	0.5255	0.9581	1.0000
2.00E+33	108		13.54	0.0025	0.0774	0.7940
2.00E+33	108	1/40	10.00	0.0293	0.3330	0.9730

Table showing the number of tracks per event per 5 sectors for all tracks down to 1.5 GeV. This table is based on numbers for one trigger event plus dijet MC data for the background interactions. The MC backgrounds are weighted by relative cross section for parton energy and are weighted for number of events by a Poisson distribution for the luminosity. The trigger event is arbitrarily assigned 15 global tracks on average and either 0.6 or (15/40) per sector on average. Under the assumptions that went into this table, keeping 4 tracks per Pt bin per 5 sectors (Ratio of 16) is 100% efficient for run II even at 36 bunches. It is also close to efficient for run III with this low trigger threshold.


80 boards
CFT
FE
copper
96 links
Muon
L1
copper
2 crates
CFTCN
System
80 links
4 boards
RC
8 links
2 boards
L1CN
copper
L1CFTTM
2 boards
L2CN
glass
2 boards
L2CN
2 links
L2PSpp
Passive Splitter
L1
AMCC Links
Copper - 1Gbit/s
L2
G-link
glass - 1Gbit/s
6 links
L2CFTpp
12 links
L2STTpp
CFT_L1v3

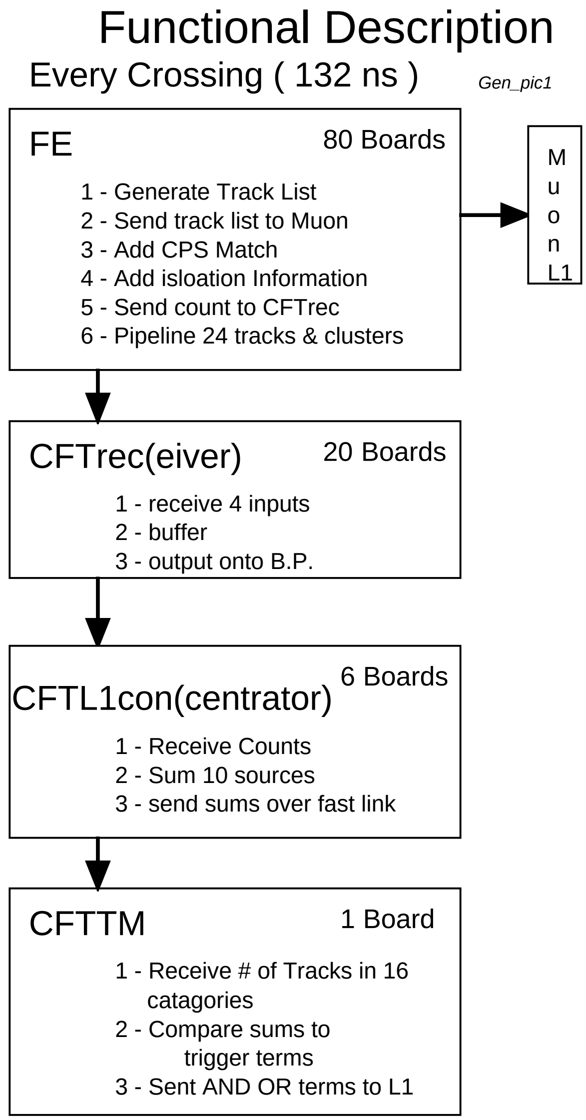


Figure 1. Functional description of the main blocks of the CFT L1 Trigger system. This figure shows the functions carried out for each crossing cycle during L1 live time.

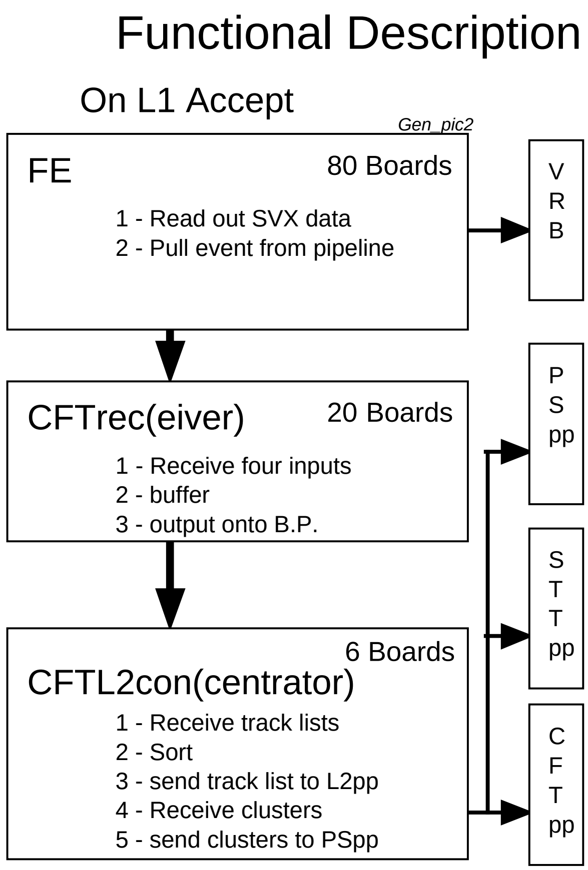


Figure 2. This figure shows the functional description of the main blocks of the CFT L1 Trigger system. These functions are carried out after an L1 accept is received.

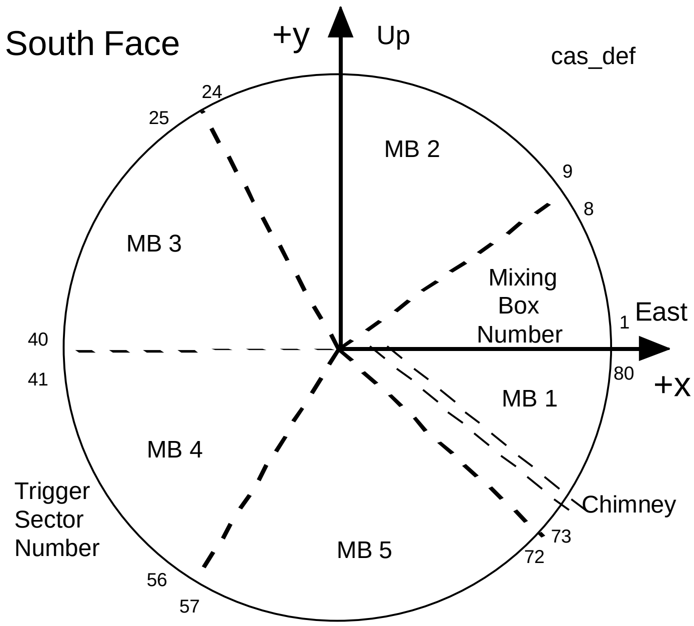


Figure 3. South face of the detector end showing areas subtended by each mixing box and the position of each trigger sector.

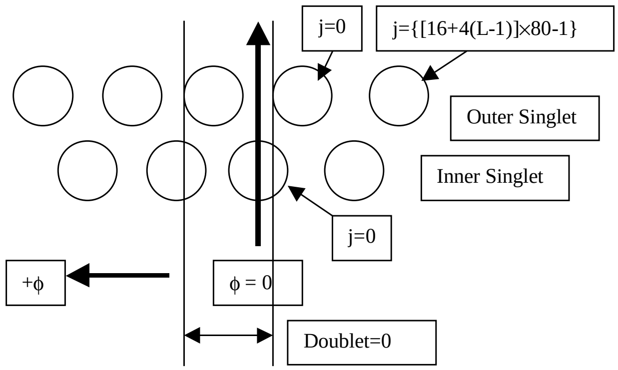


Figure 4. This view shows the numbering system for the singlet fibers and the doublet bins. Note that the inner singlet fiber j=0 is centered at ϕ=0, but the outer j=0 fiber is at -ϕ. Note also that doublet bin 0 starts at a -ϕ value.

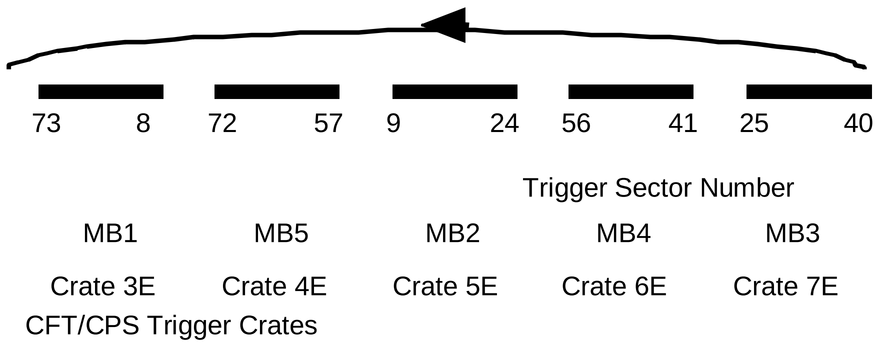
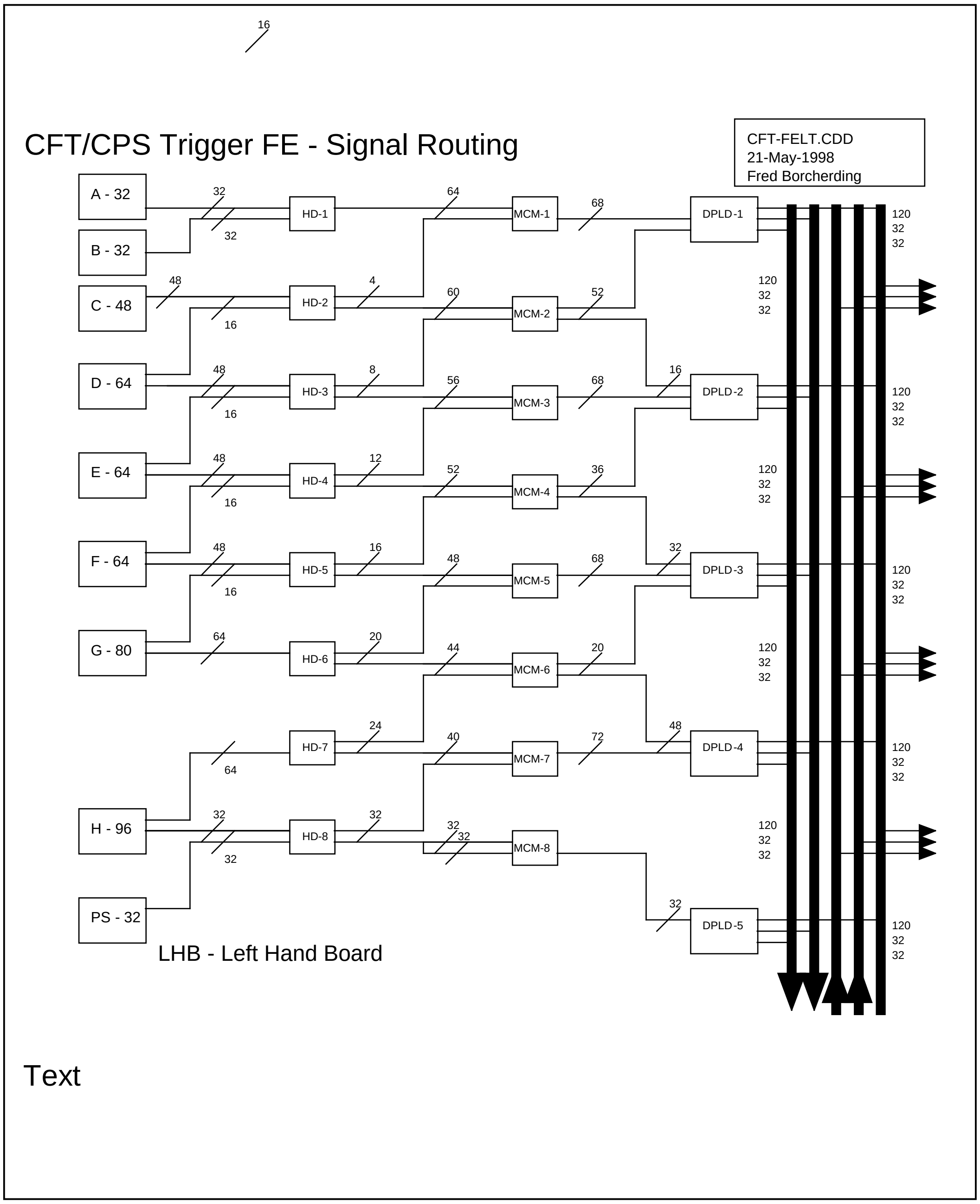
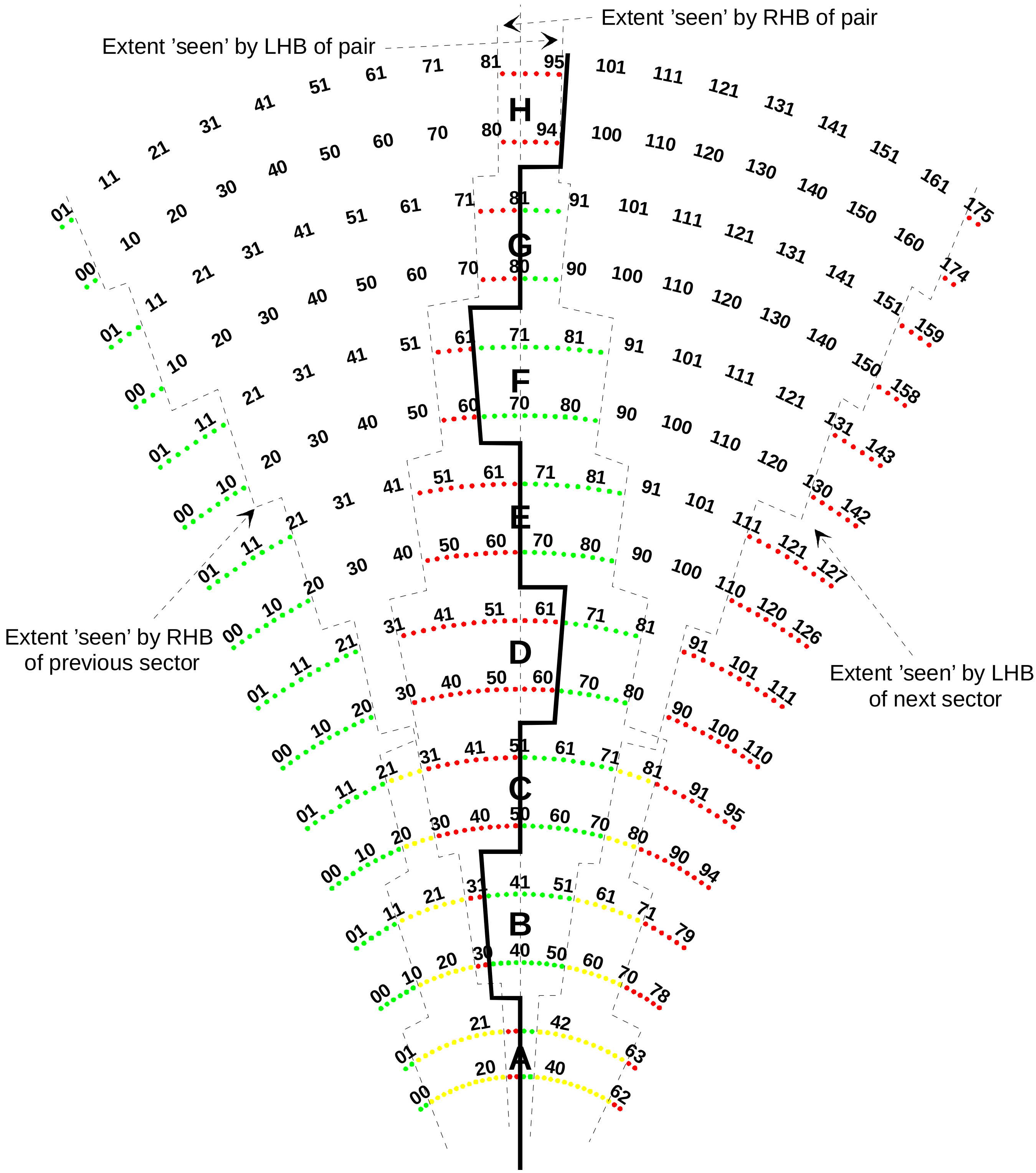
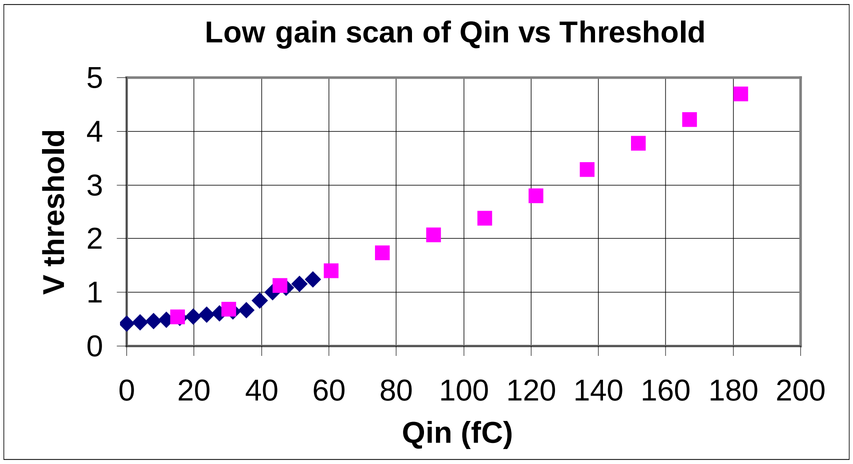


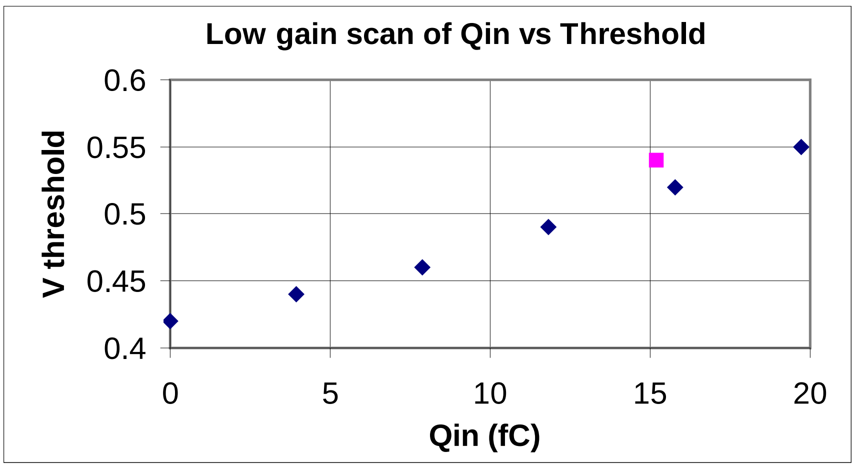
Figure 5. Shown are the five FE crates with their contents in terms of mixing box and sector. The arches represent back plane jumpers between crates, which connect adjacent sectors for a seamless

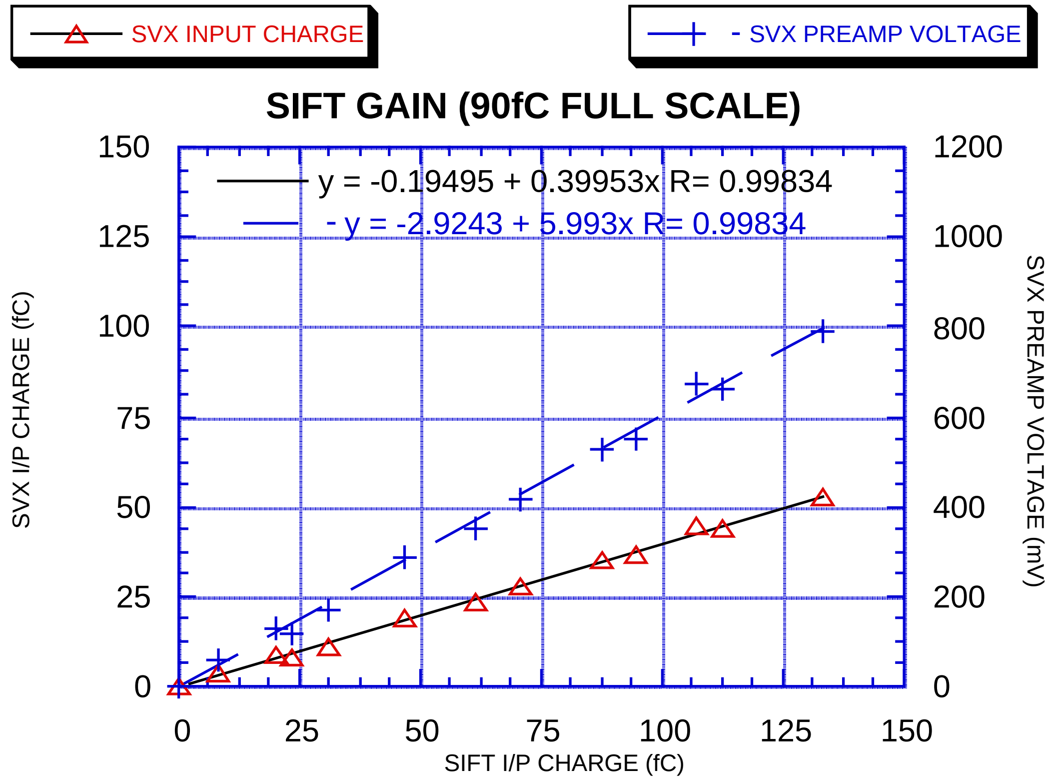
Figure 1. Schematic of the overall data flow in the CFT L1 and L2 Triggers.



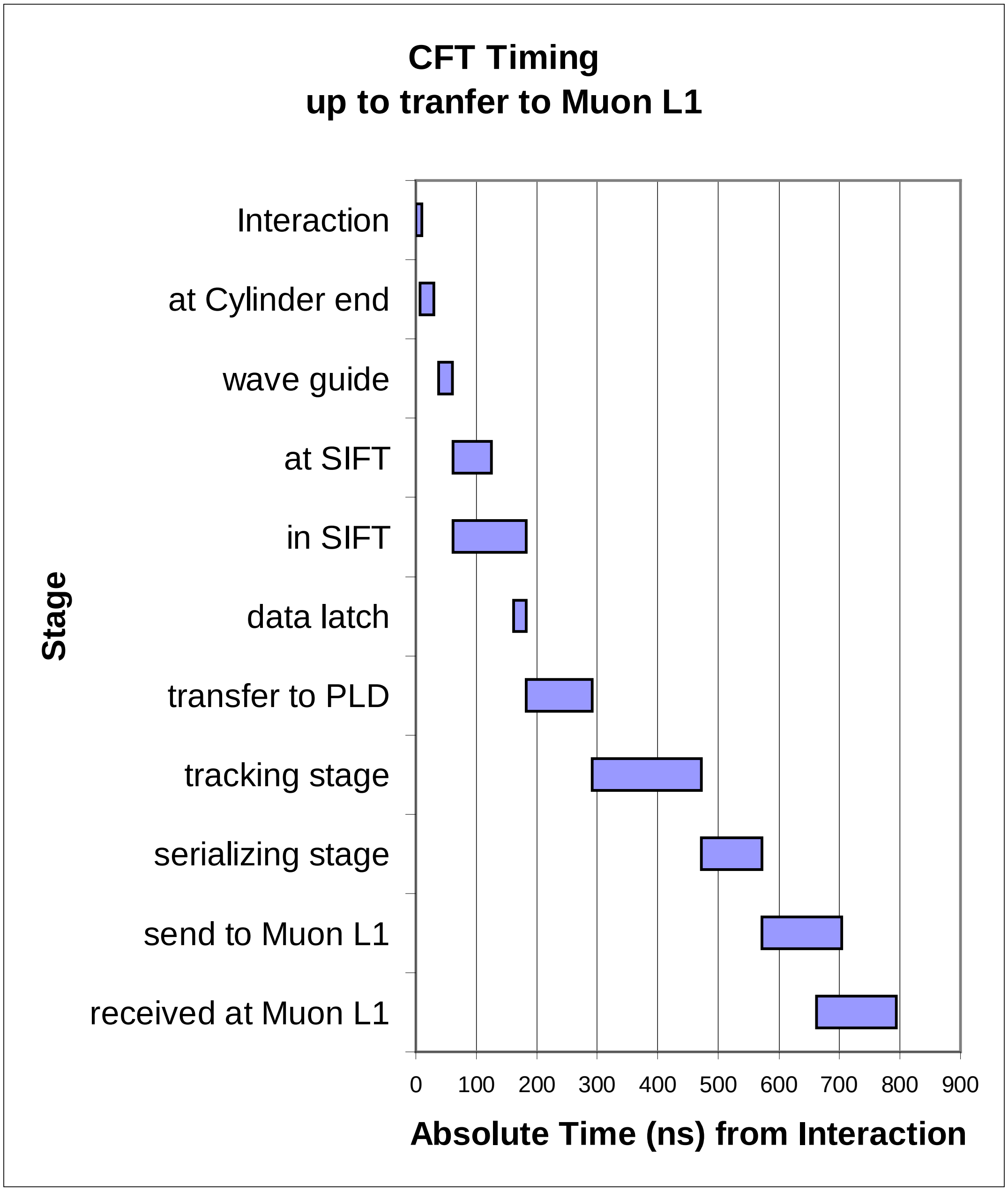

Extent 'seen' by RHB of pair
Extent 'seen' by LHB of pair
H
G
F
E
D
C
B
A
Extent 'seen' by RHB of previous sector
Extent 'seen' by LHB of next sector


Low gain scan of Qin vs Threshold
V threshold
5
4
3
2
1
0
0 20 40 60 80 100 120 140 160 180 200
Qin (fC)


Low gain scan of Qin vs Threshold
V threshold
0.6
0.55
0.5
0.45
0.4
0 5 10 15 20
Qin (fC)


SVX INPUT CHARGE
- SVX PREAMP VOLTAGE
SIFT GAIN (90fC FULL SCALE)
y = -0.19495 + 0.39953x R= 0.99834
- y = -2.9243 + 5.993x R= 0.99834
150
125
100
75
50
25
0
1200
1000
800
600
400
200
0
SVX I/P CHARGE (fC)
SVX PREAMP VOLTAGE (mV)
0
25
50
75
100
125
150
SIFT I/P CHARGE (fC)

Offset	Pt Index	Min	Mean	Max
0	0000	18.00	21.40	
1	0001	9.00	16.90	
2	0010	6.50	11.00	21.00
3	0011	4.50	6.80	10.50
4	0100	4.00	5.00	7.00
5	0101	3.25	3.90	5.00
6	0110	2.75	3.30	4.00
7	0111	2.50	2.80	3.50
8	1000	2.20	2.40	2.80
9	1001	1.80	2.20	2.50
10	1010	1.80	1.90	2.20
11	1011	1.60	1.76	2.00
12	1100	1.50	1.62	1.80
13	1101	1.40	1.53	1.60
14	1110	-	-	-
15	1111	-	-	-


CFT Timing
up to tranfer to Muon L1
Stage
Interaction
at Cylinder end
wave guide
at SIFT
in SIFT
data latch
transfer to PLD
tracking stage
serializing stage
send to Muon L1
received at Muon L1
0
100
200
300
400
500
600
700
800
900
Absolute Time (ns) from Interaction

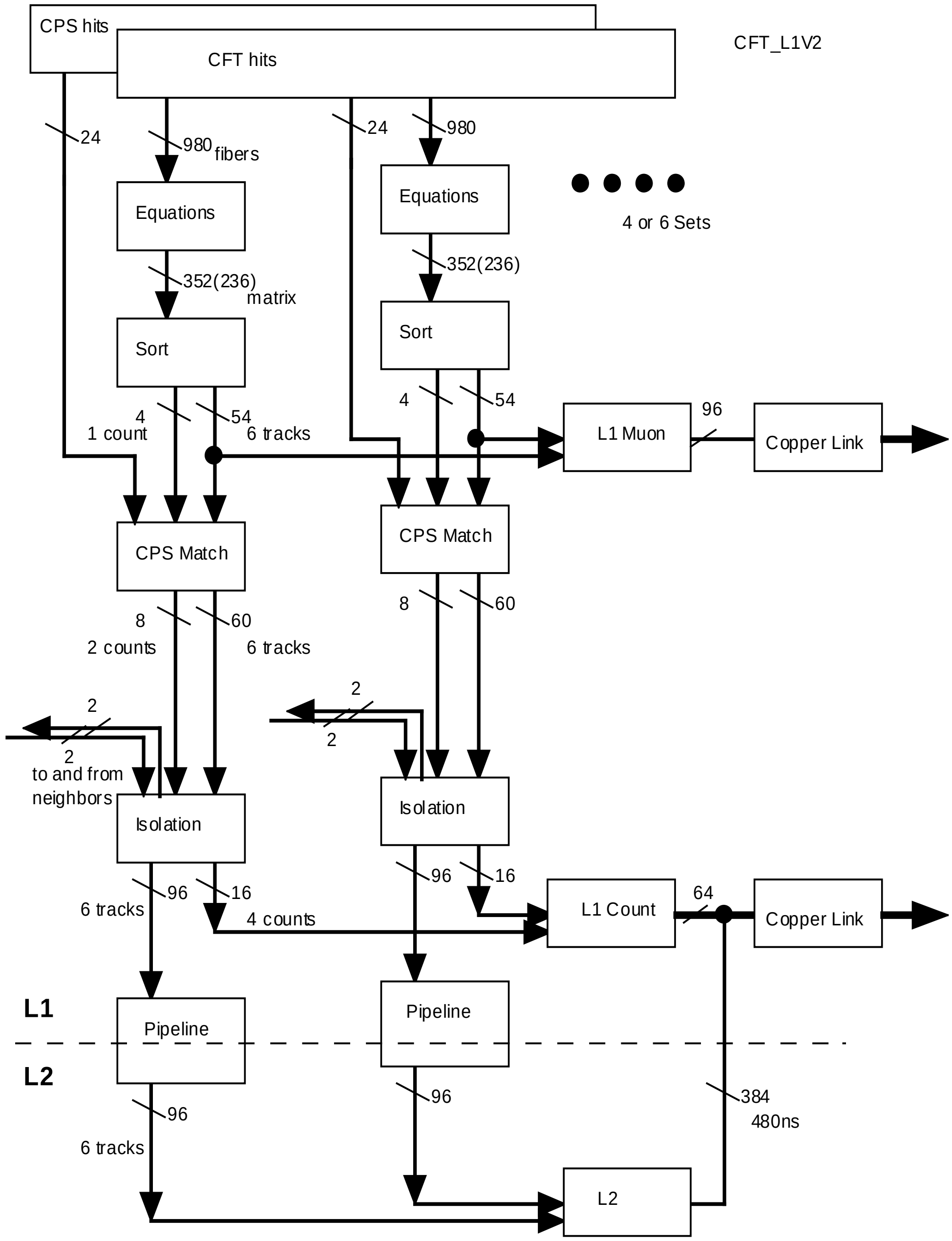


Figure 2. Schematic of the data flow in the FE. The raw hit information enters at the top. The track list for Muon L1 is sent over a copper serial link. The track count values for CFT L1 are sent over a second copper serial link. This second link is also used at L2 time to transfer track lists to the preprocessors.

Configuration of Concentrator Crates

conc_crates_1098

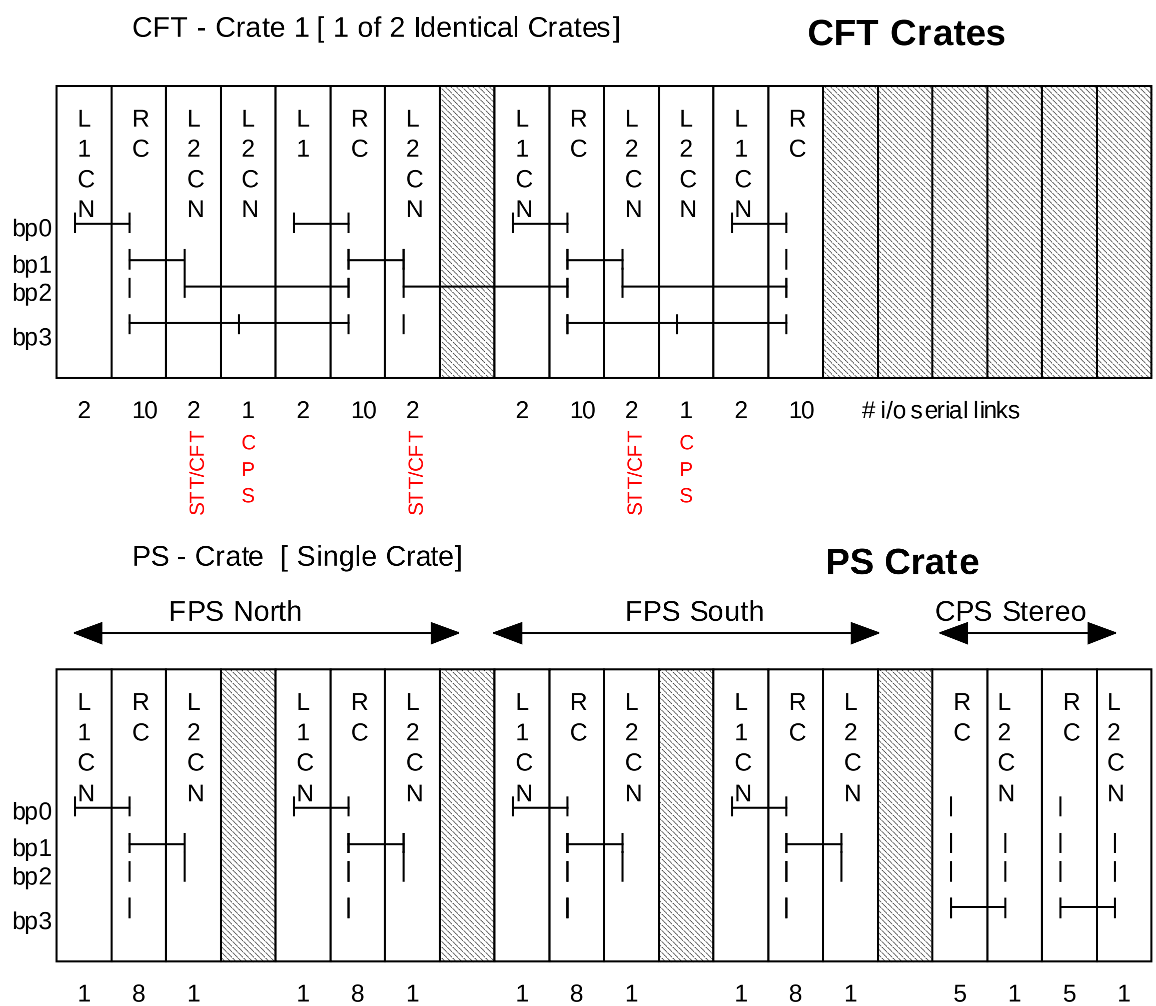


Figure 2. Crate layout for the CFTCN System and the PSCN System. Because of the arrangement of busses in the back plane each slot is board type specific. The different board types are used.

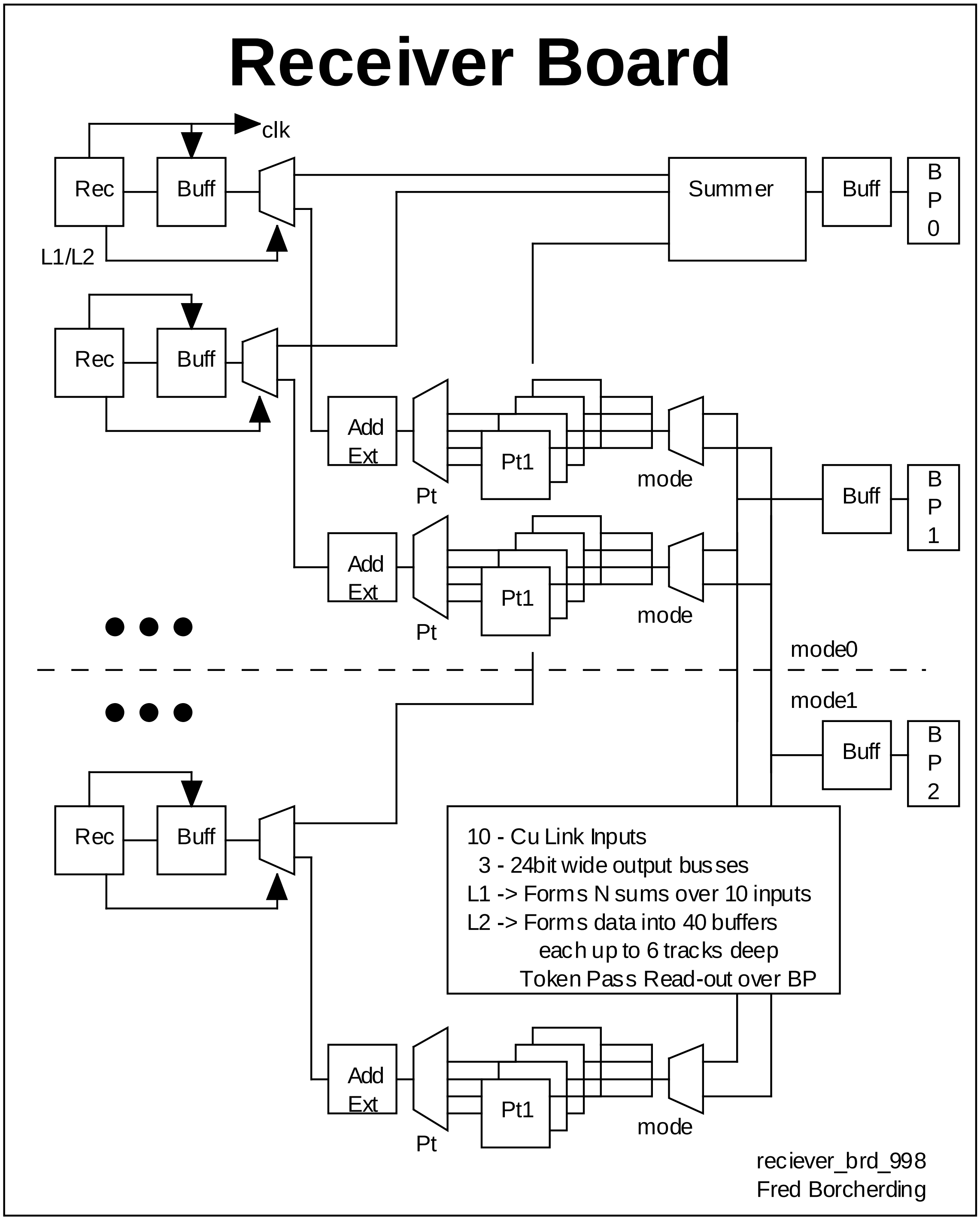
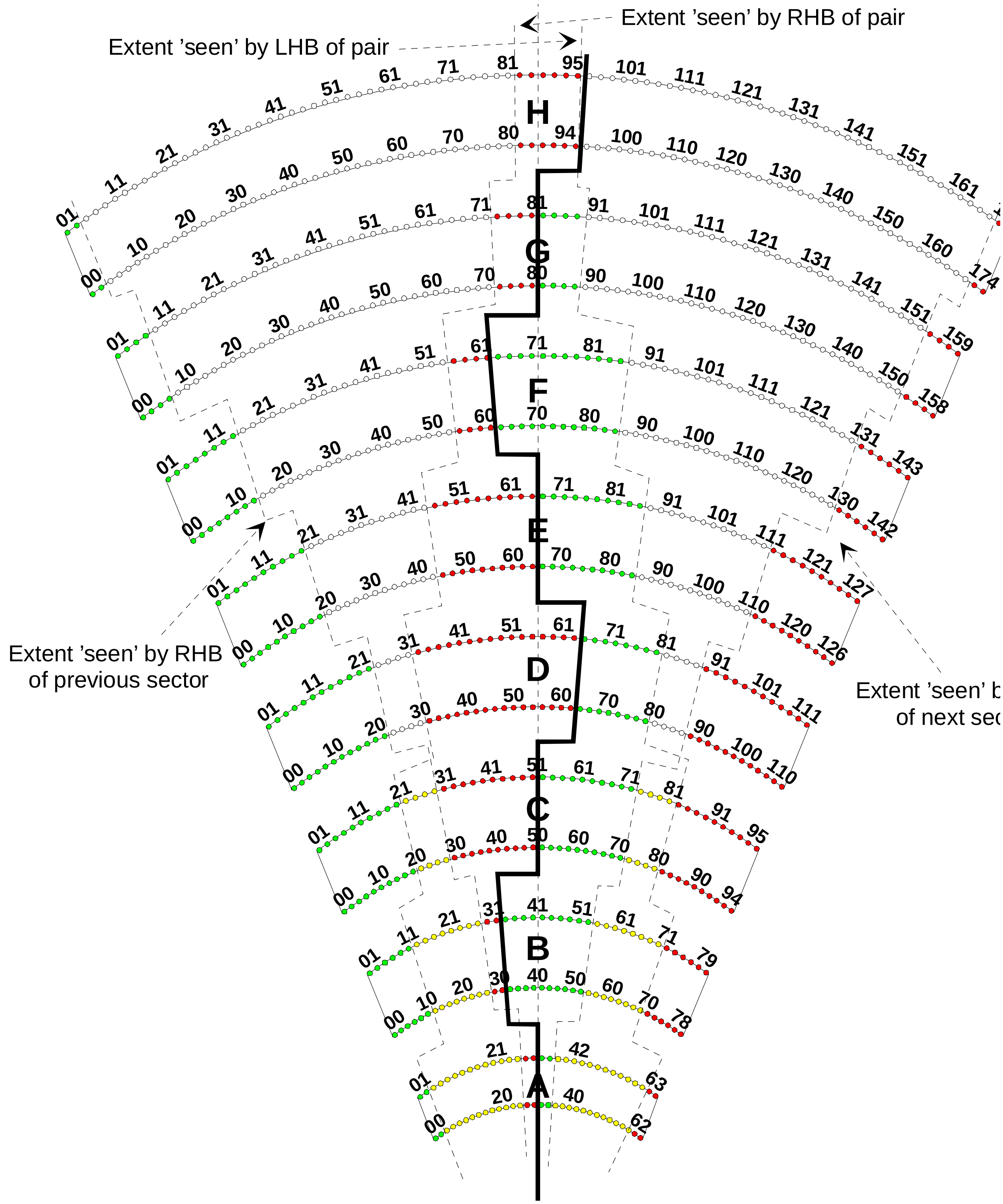
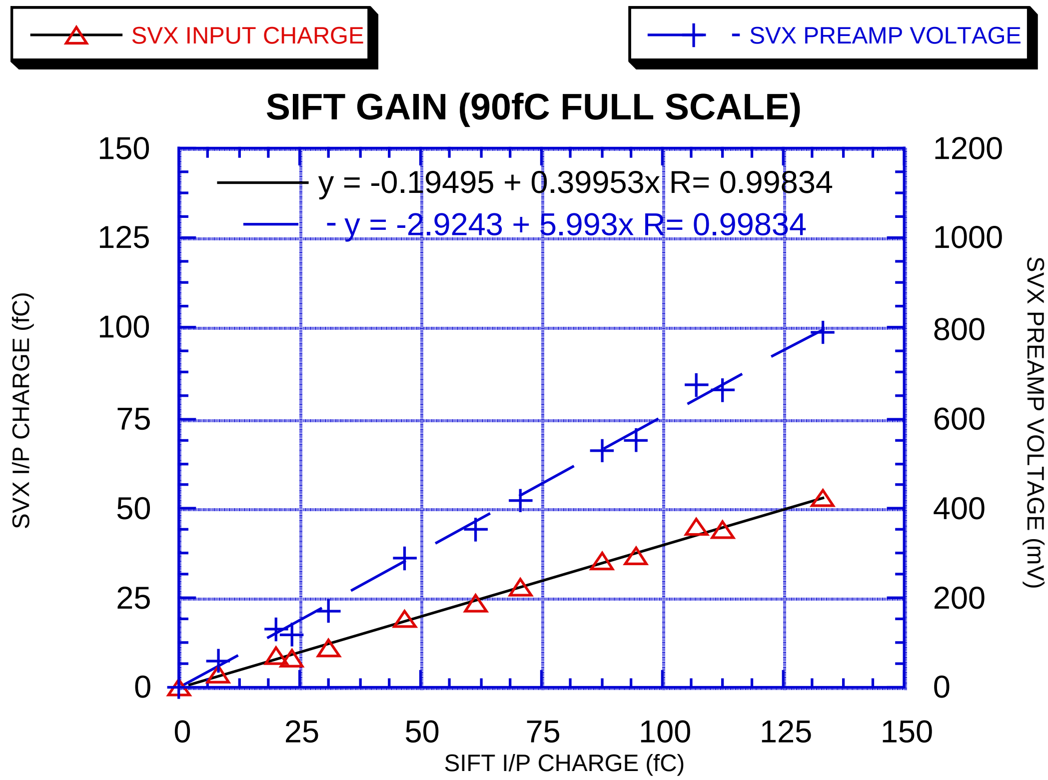
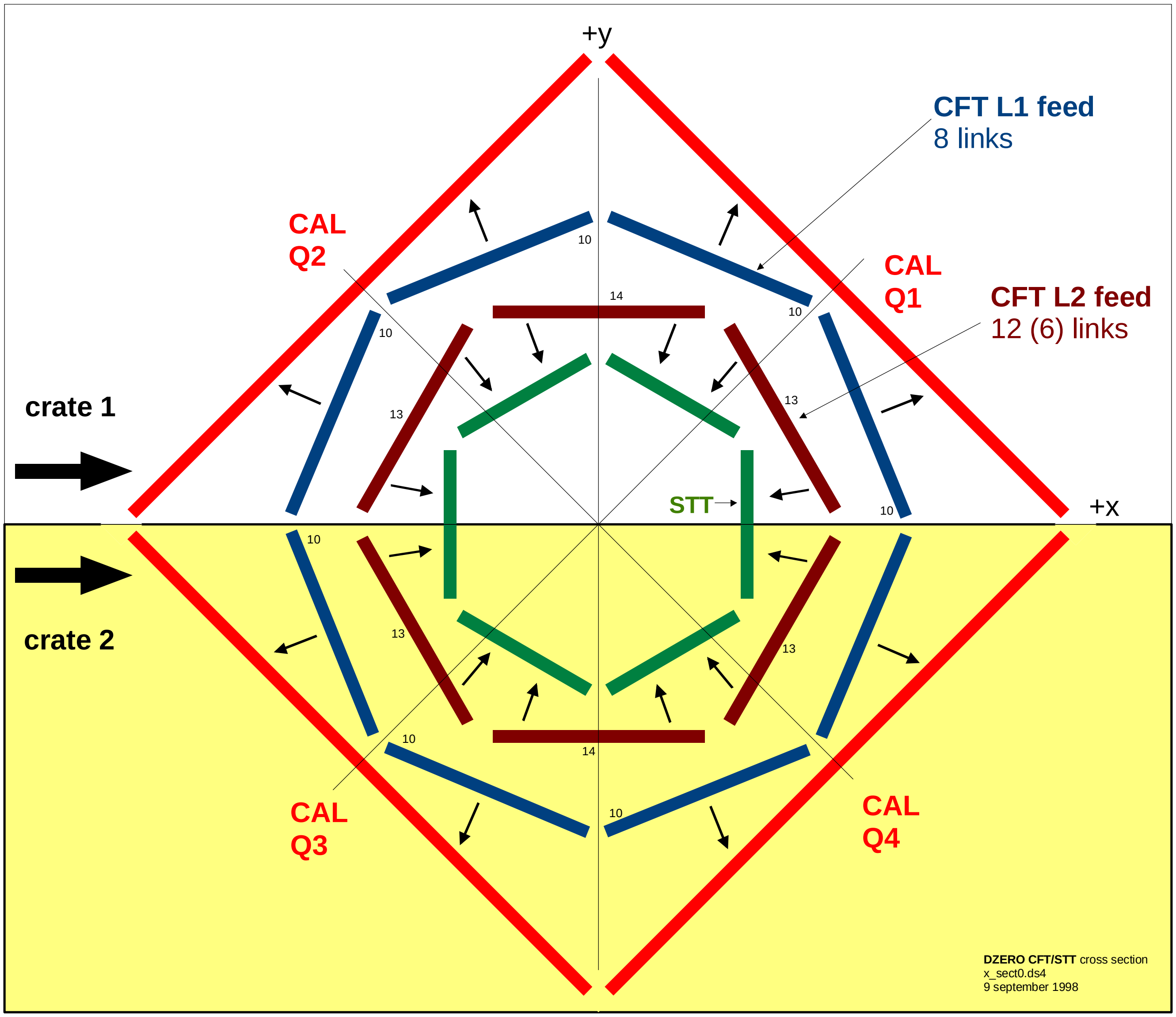


Figure 3. Block diagram of RC board. Each board has 10 input channels. Each input channel feeds data to nay of 3 processes. Each process has one or more back plane busses for transfer of data out.


Extent 'seen' by RHB of pair
Extent 'seen' by LHB of pair
H
G
F
E
D
C
B
A
Extent 'seen' by RHB
of previous sector


SVX INPUT CHARGE
- SVX PREAMP VOLTAGE
SIFT GAIN (90fC FULL SCALE)
y = -0.19495 + 0.39953x R= 0.99834
- y = -2.9243 + 5.993x R= 0.99834
SVX I/P CHARGE (fC)
SVX PREAMP VOLTAGE (mV)
SIFT I/P CHARGE (fC)
0
25
50
75
100
125
150
200
400
600
800
1000
1200


+y
CFT L1 feed
8 links
CAL
Q2
CAL
Q1
CFT L2 feed
12 (6) links
crate 1
STT
+x
crate 2
CAL
Q3
CAL
Q4
10
14
10
10
13
13
10
10
10
13
13
10
14
10
DZERO CFT/STT cross section
x_sect0.ds4
9 september 1998

[1] Note on CPS

[2] The 'Official' Detector parameter files are on the Web at: http://d0server1.fnal.gov/www/Upg_CFT/base_line.html

[3] D0 Note 2139, Electronics Design Specifications for the D0 Upgrade Scintillating Fiber Detector with a Level 1.0 Trigger, Alan Baumbaugh, Fred Borcherding, Marvin Johnson, Jesse Costa, Lourival Moreira, Sudhindra Mani, Steven Glenn and David Pellett, 19-July-1994

[4] D0 Node 2359, Level 1 Trigger Design for the D0 Upgrade Central Fiber Tracker, Fred Borcherding, 21-November-1994

[5] D0 Note 3058, D Zero Central Hardware Trigger Preliminary Implementation Studies of the "Base Line Design", R. Angstadt and Fred Borcherding, 15-August-1996.

[6] D0 Note 2504, A study of the Effects of Fiber Placement Errors on the Level 1 CFT Trigger, Fred Borcherding, 17-March-1995

[7] Addendum to: D0 Note 2504, A study of the Effects of Fiber Placement Errors on the Level 1 CFT Trigger, Fred Borcherding, 12-April-1995