Charge-Coupled Devices (CCDs)

What they are

Why they are ubiquitous

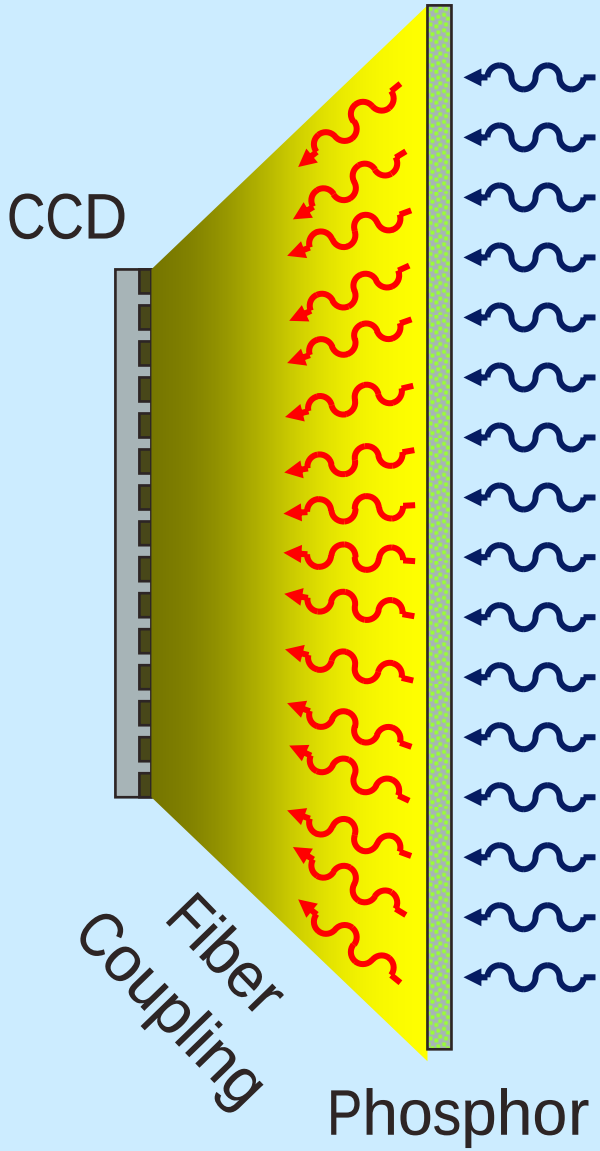
And who's the competition

How they can be improved

CCDs – just keep going and going and going…

P. Denes
Engineering Division
Lawrence Berkeley National Laboratory

Standard Detector

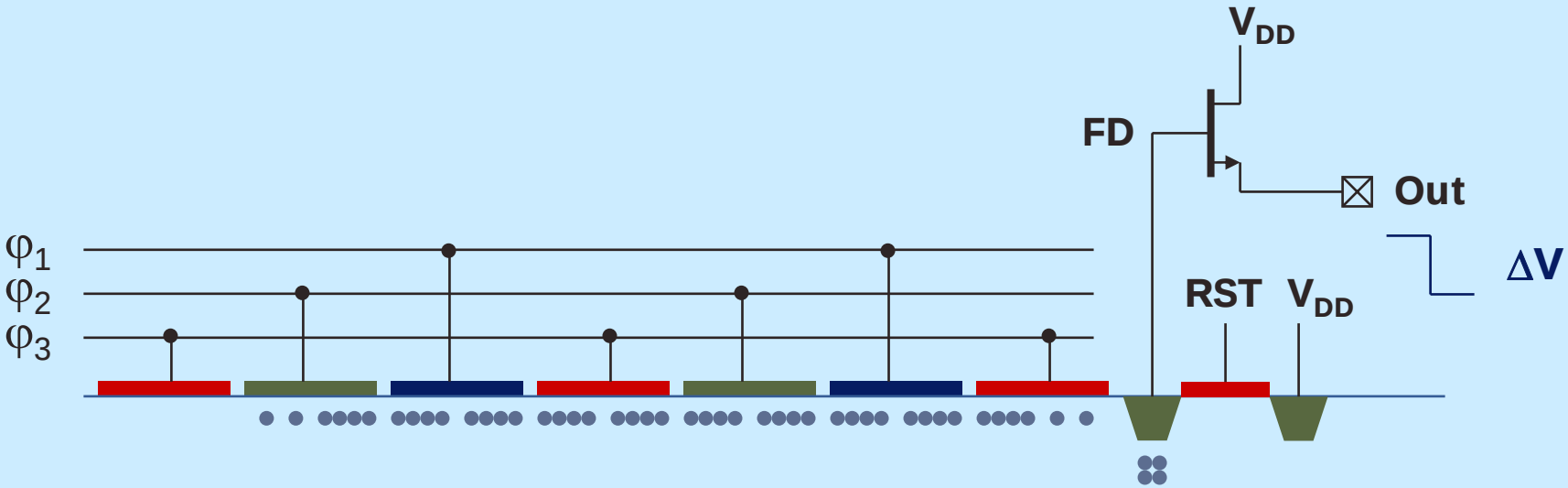


Scientific CCDs

Dumbbell nebula - LBNL CCD
Blue: H-α at 656 nm
Green: SIII at 955 nm
Red: 1.02 mm

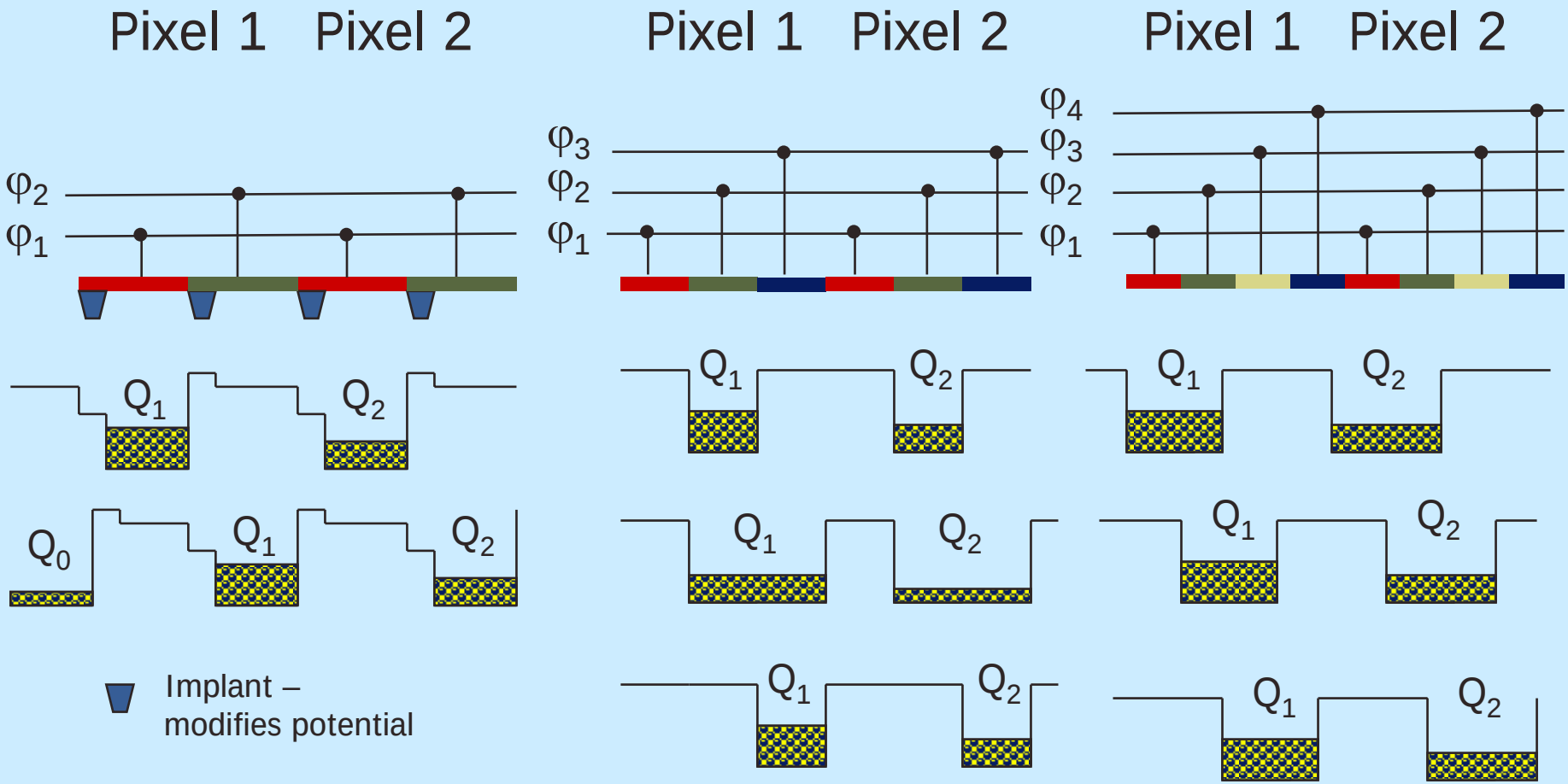
- CCD invented in 1969 by Boyle and Smith (Bell Labs) as alternative to magnetic bubble memory storage
- LST ("Large Space Telescope" – later Hubble) 1965 – how to image?
  - *Film was obvious choice, but - It would "cloud" due to radiation damage in space*
    Changing the film in the camera not so trivial
  - *1972 CCD proposed*

Conventional 3-Phase CCD

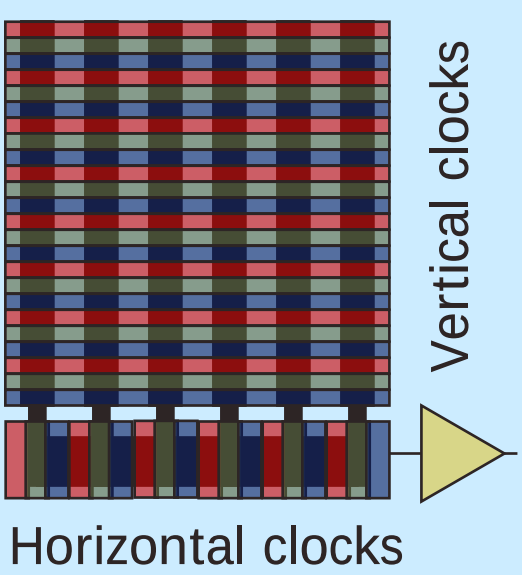


- Noiseless, ~lossless charge transfer
- High gain charge-to-voltage conversion $\Delta V = q/C_{FD}$
- Output amplifier (source follower, or ...) on-chip

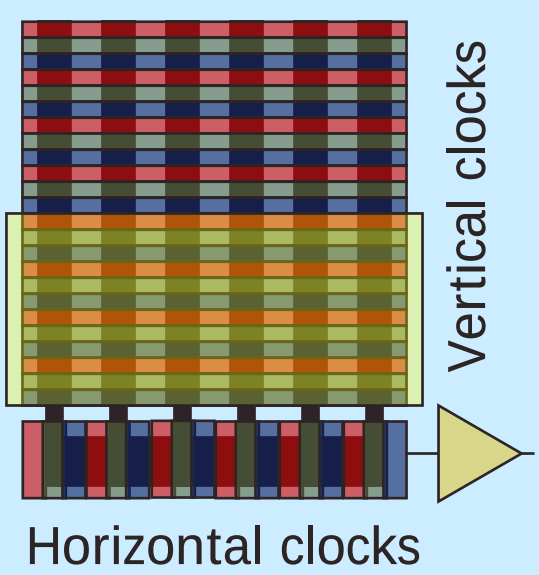
Many ways to do this



Several architectures



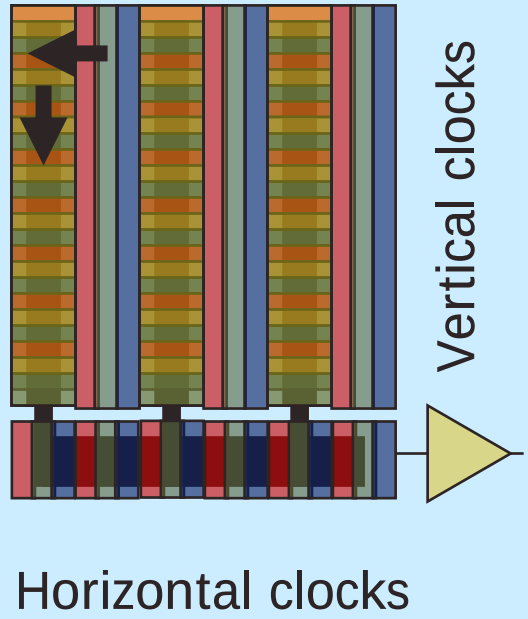
Full frame



Frame transfer

Rapid shift from image to storage

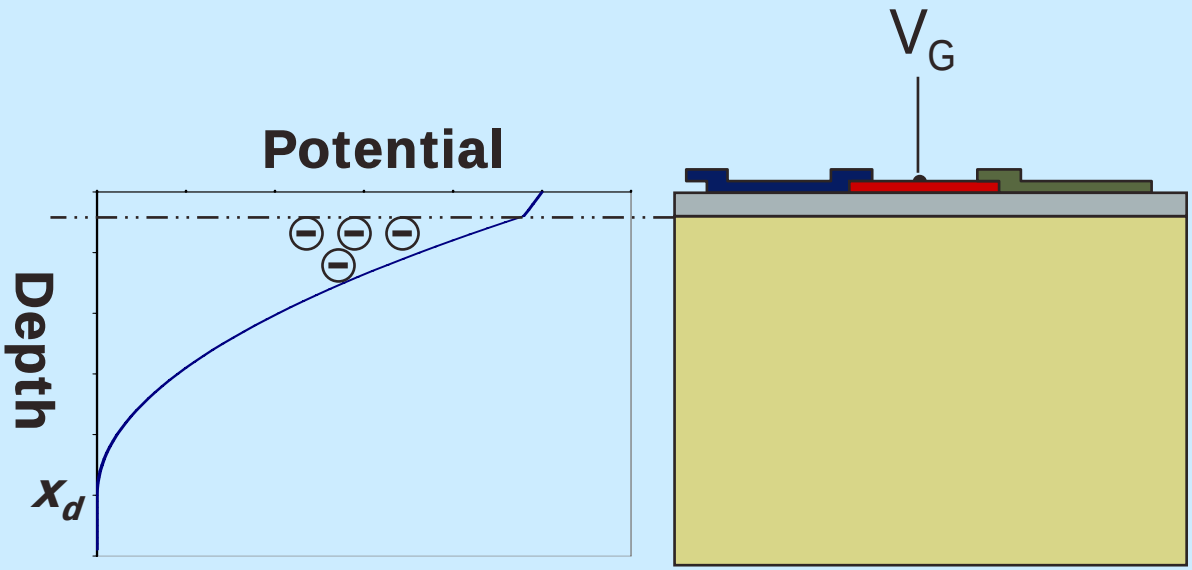
Slower readout of storage during integration

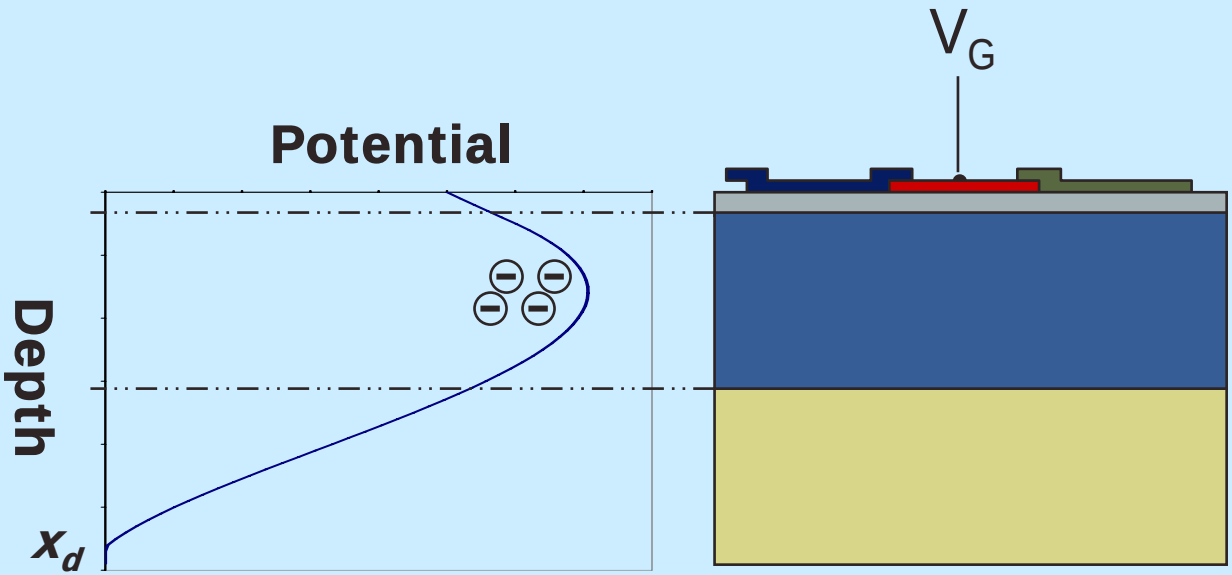


Interline

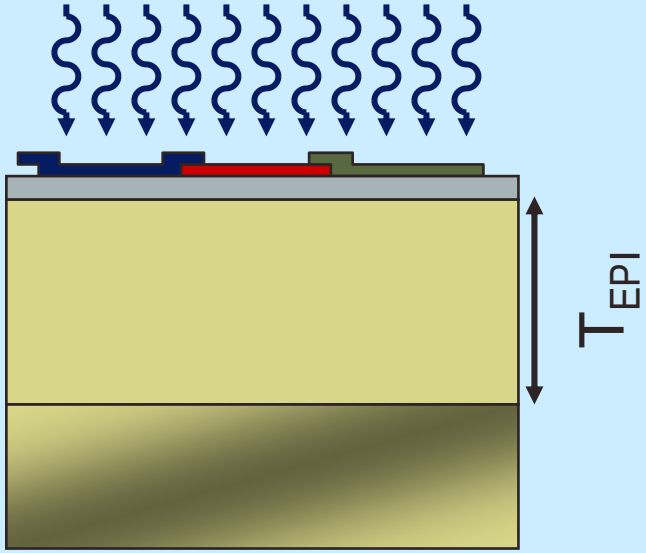
Surface vs buried channel CCD

- MOS capacitor
- Potential maximum at Si – SiO_2 interface
  - *CTE < 1 due to trapping at interface*
- Potential maximum not at Si – SiO_2 interface
  - *CTE typically > 99.9999%*



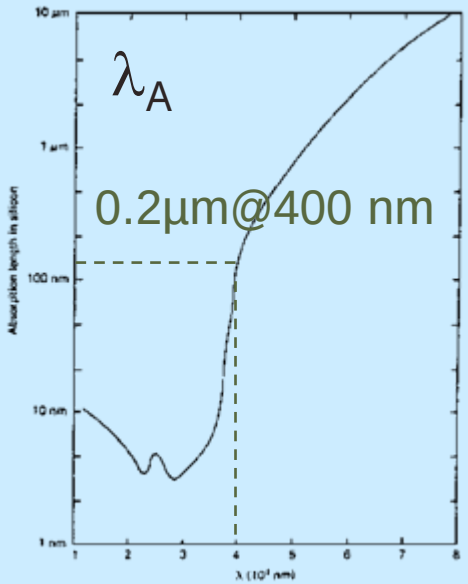


Frontside / Backside Illumination

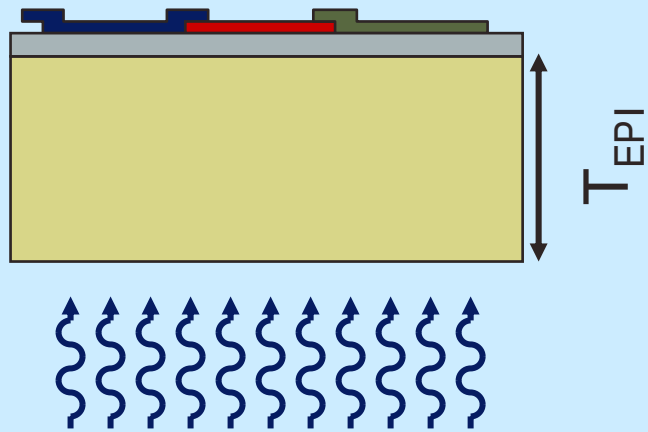


$$\varepsilon \propto e^{-T_{POLY}/\lambda_A}\left(1-e^{-T_{EPI}/\lambda_A}\right)$$

Fill factor < 1



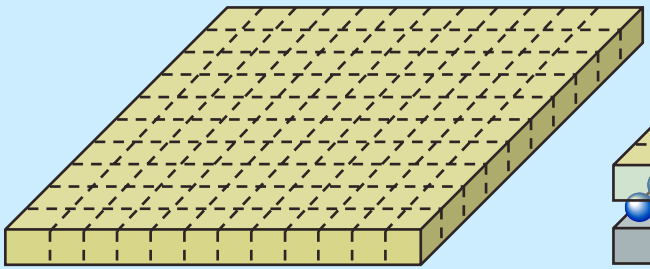
$$\varepsilon \propto \left(1-e^{-T_{EPI}/\lambda_A}\right)$$



Fill factor = 1

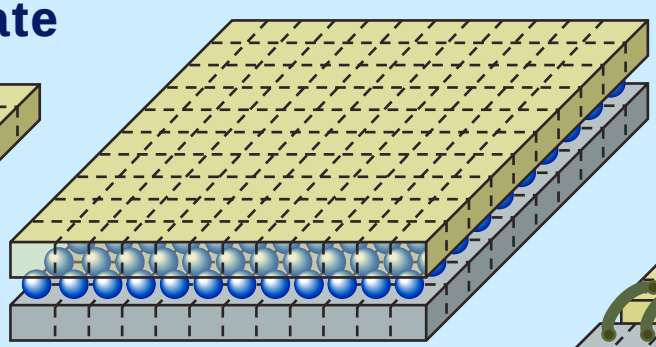
Imaging Detectors

Monolithic
sensor + readout on same substrate



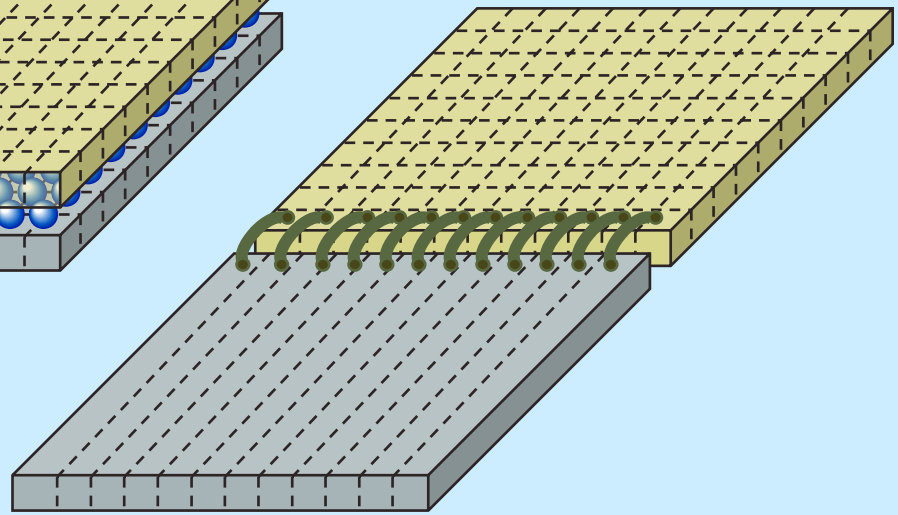
2D segmented Si

Hybrid



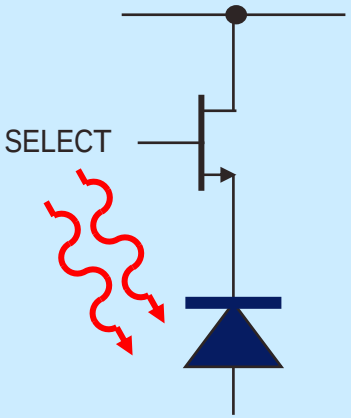
2D segmented Si attached to 2D segmented Si

Sensor + Readout

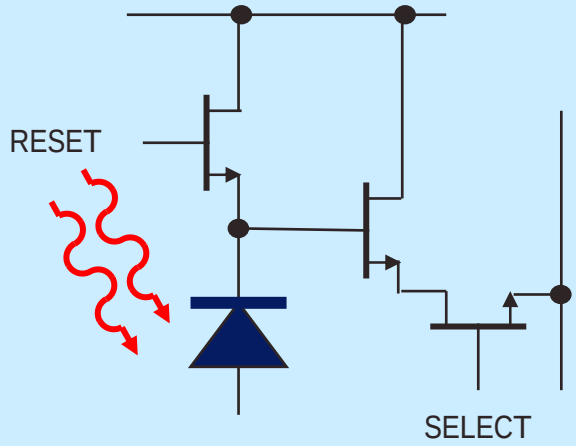


2D segmented Si attached to 1D segmented Si or other electronics

Monolithic Image Sensors



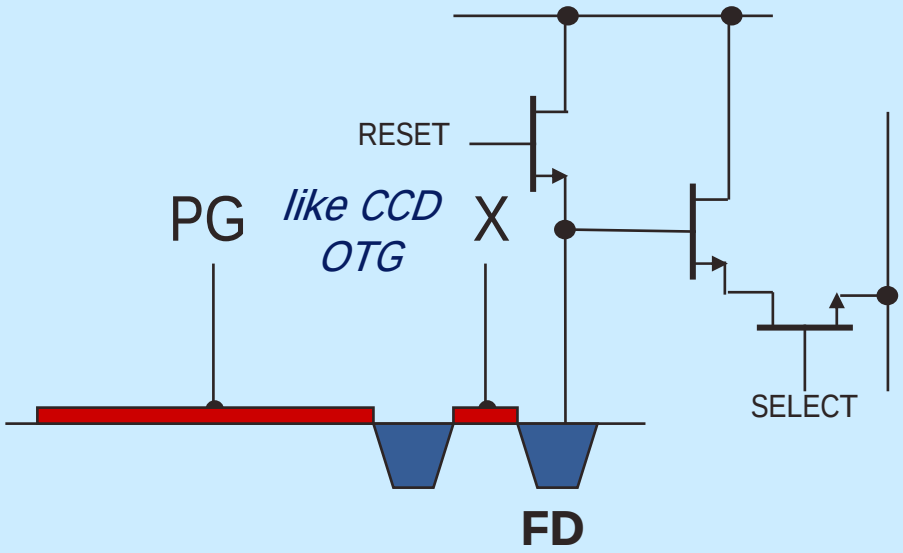
- Passive Pixel Sensor
- Proposed 1968
- No Reset, no in-pixel amplifier



- Active Pixel Sensor
- *Also* proposed 1968
- Many ways to make the photodiode

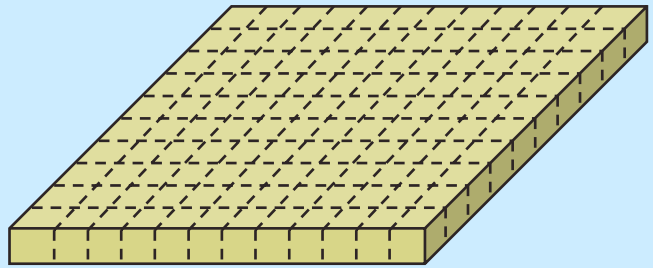
CCD vs APS

- APS – transfers a *voltage* down the column
- CCD – (noiselessly) transfers a *charge* down the column
- APS – can be more sensitive (source follower does not have to drive off-chip)
- APS – fill factor < 1 in general
- Photogate APS – like a matrix of individual CCDs
- Backside illumination – attempted for APS, work-in-progress



Glossary

Sensor with pixel pitch P



Sensor

- "Quantum efficiency"
  - *Probability of detection*
  - *Energy spread*
- Point spread function (PSF)
- Conversion gain (may be in readout) – Volts / ___ (electron, eV, ...)
- "Well depth" - Q_{MAX}
- Noise contribution, σ_{SENSOR}

Front-end readout

- Noise contribution, σ_{ELEC}

Readout

- Full-scale - V_{MAX}
- Speed – MPix/s (less ambiguous than fps)

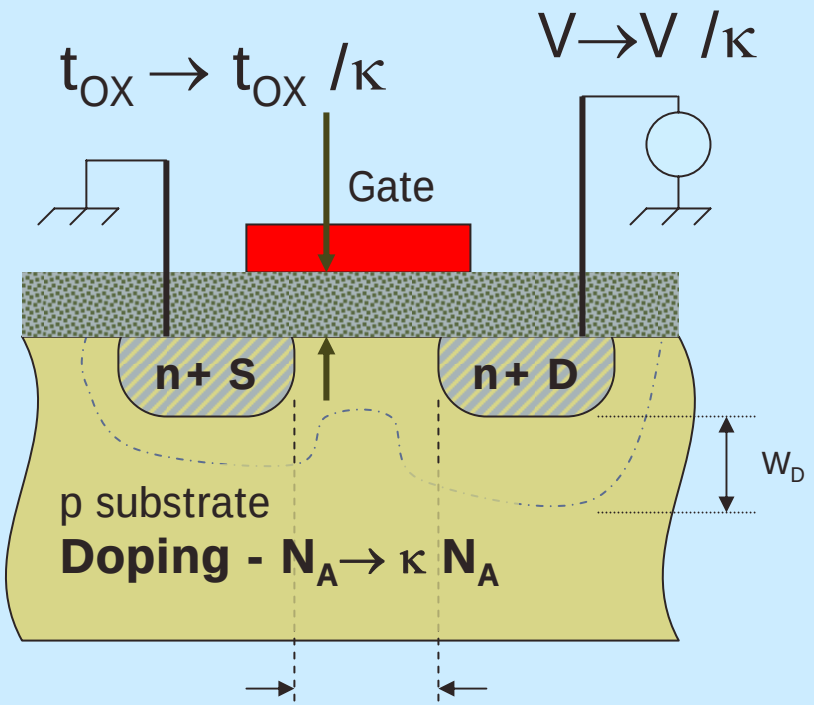
System

- Frequency-dependent DQE or equivalent
- $\Rightarrow$ Dynamic Range = $\min(Q_{MAX}, V_{MAX}) / \sigma_{SENSOR} \oplus \sigma_{ELEC}$

"dB" = $20 \log_{10}$ (DR)
"bits" = $\log_2$ (DR)

CMOS, CMOS "opto" and CCD processes

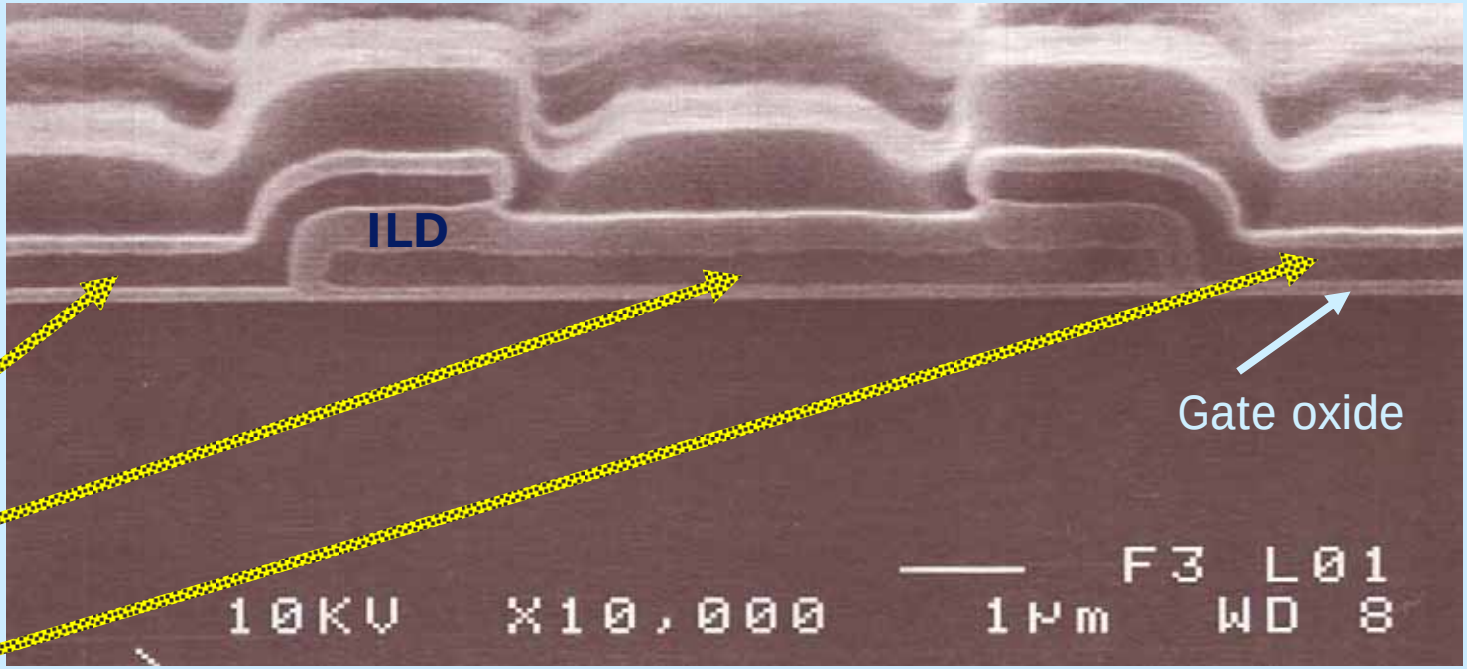
CMOS driven by
constant field scaling



Channel Length $L \rightarrow L/\kappa$

	CCD	CMOS
t_{ox} (Å)	500 - 1000	50
Well depth (μm)	2.5	0.5 deeper for RF
Implant (μm)	~1 channel stop	0.1 S/D implants
V	≥10	<3.3 <2.5 <1.x …
Poly layers	3 (2)	1 2 for analog
Subst. quality	Low leakage	Don't care Except opto

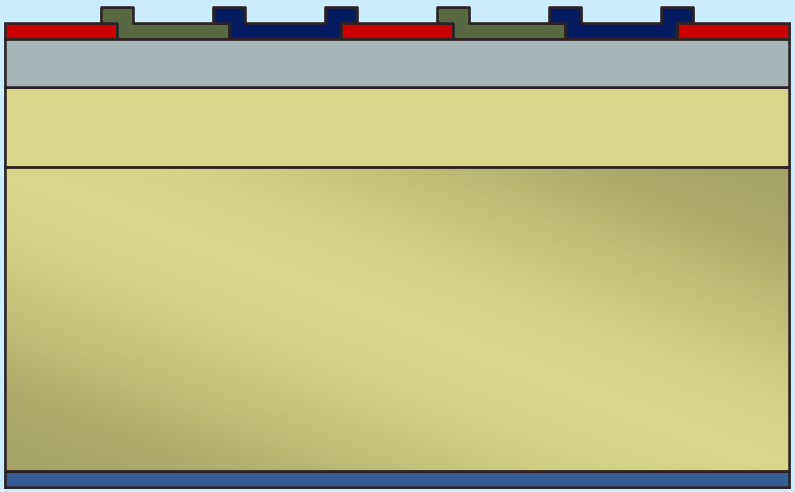
Triple Poly CCD Process



Poly 2

Poly 1

Poly 3

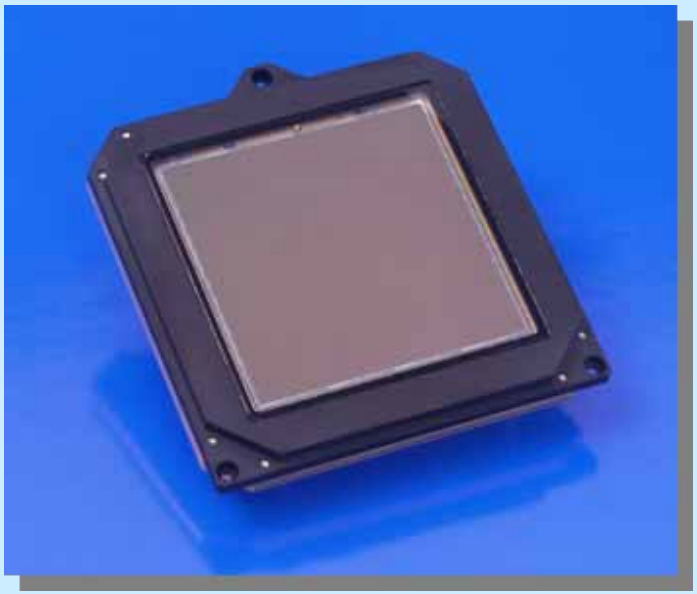


Why CCDs?

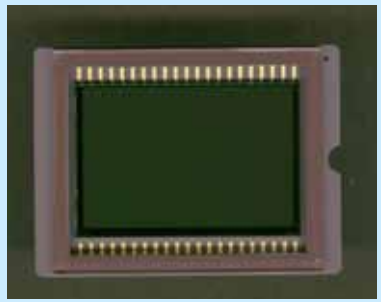
- Low noise (noiseless charge transfer, do everything to make C_{FD} small in order to get large conversion gain)
- Fill-factor = 1 (for backside illumination)
- Linear and easy to calibrate
- **Long history of scientific use**
- Large area devices easier (cheaper) to develop as CCDs than as state of the art CMOS devices
  - *Readily wafer scale*
- Commercially produced

Very Large Format CCDs (and CMOS imagers)

- Fairchild Wafer Scale Full Frame CCD
  - *9216 x 9216 x 8.75 µm pixel*
  - *80.64 x 80.64 mm^2 size CCD*
  - *Eight 3-stage output amplifiers*
  - *Readout noise < 30e- @ 2/fps*



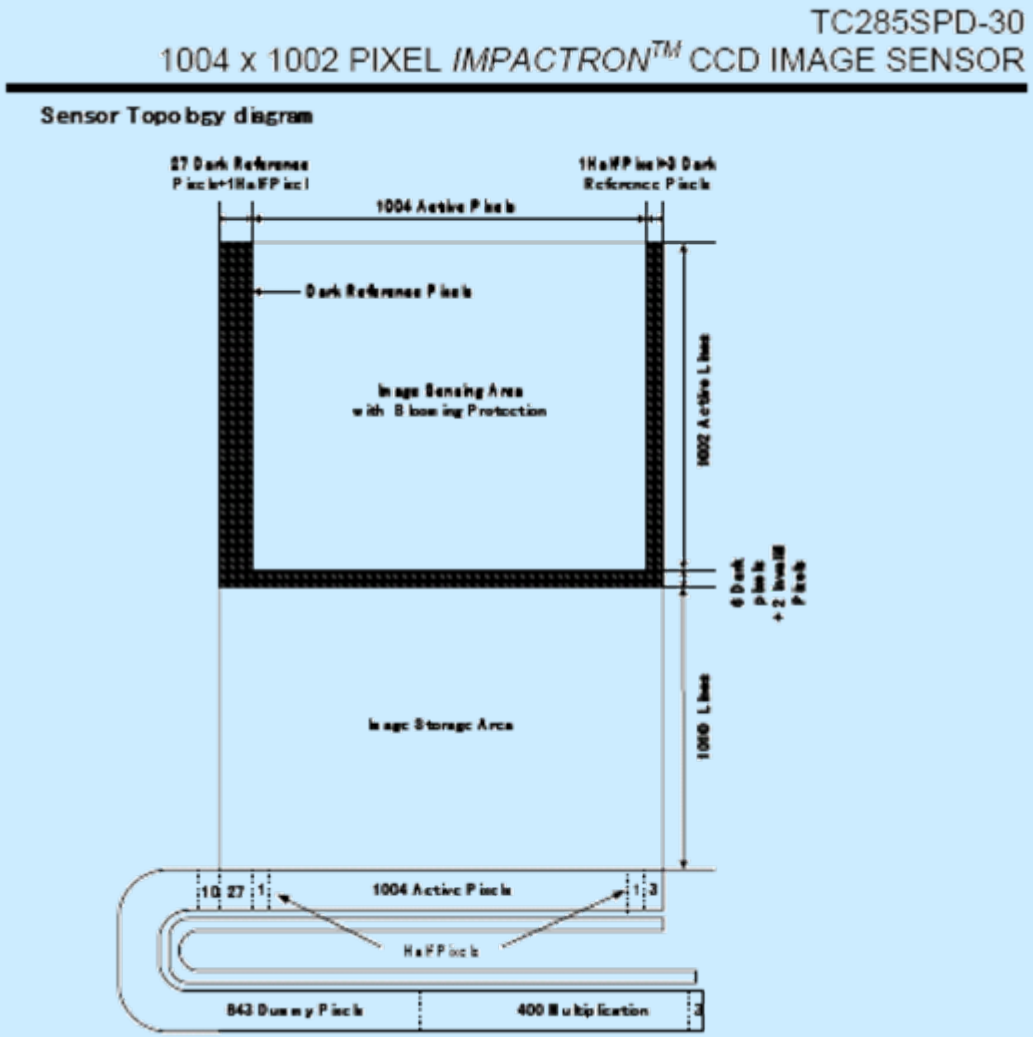
- Cypress CYIHDS9000
  - *3710 x 2434 x 6.4 µm pixel*
  - *23.3 x 15.5 mm^2 size APS*
  - *0.13 µm imaging CMOS process*



- Canon 16.7 MPix
  - *36 x 24 mm^2 4992 x 3328*
- Kodak 39 MPix
  - *36 x 48 mm^2*

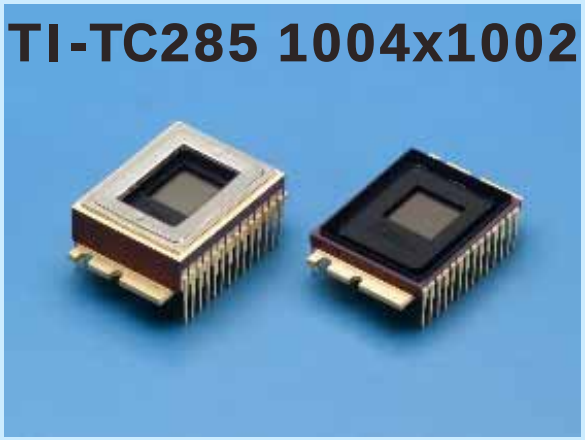
Electron-Multiplying CCDs

- Long serial register with avalanche multiplication pixels
- Gain $(1+\varepsilon)^N$ $\varepsilon \sim 1\%$
- Good for single-photon sensitivity
- Nonetheless, current devices have limited ($\leq$ 12 bit) dynamic range
- Excess noise factor, F



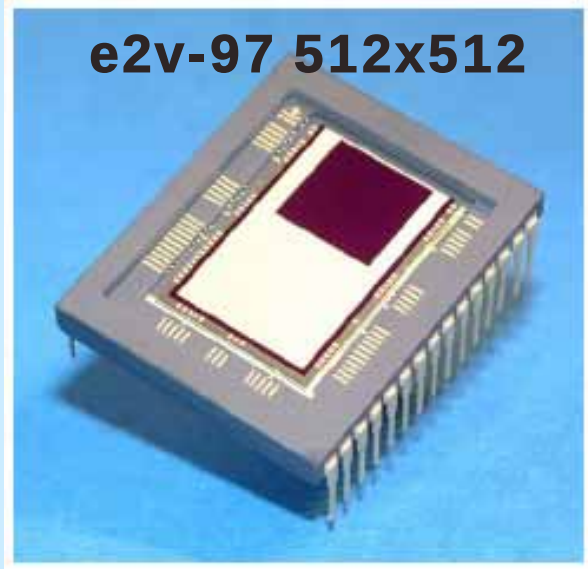
EM CCD

TI-TC285 1004x1002



PARAMETER	MIN	TYP**	MAX	UNIT
Charge multiplication gain**	1	200	2000	-
Excess noise factor for typical CCM gain (Note 2)	1	1.4		-
Dynamic range without CCM gain		66		dB
Dynamic range with typical CCM gain (Note 3)		72 ~12 bits		dB
Charge conversion gain without CCM gain (Note 4)		14		uV/e
τ Signal-response delay time (Note5)		16		ns
Output resistance (Note 6)		320		Ω
Amp. Noise-equivalent signal without CCM gain *		20		e
Amp. Noise-equivalent signal with typ. CCM gain *			1.0	e

e2v-97 512x512



PARAMETER	UNIT	MIN	TYPICAL	MAX
Output amplifier responsivity, HR amplifier (normal mode) (see note 1)	µV/e⁻	-	5.3	-
Output amplifier responsivity, LS amplifier (normal mode) (see note 1)	µV/e⁻	-	1.1	-
Multiplication register gain, LS amplifier (high gain mode) (see notes 2, 3 and 4)		1	-	1000
Peak signal - 2-phase IMO	e⁻/pixel	90k	130k	-
Charge handling capacity of multiplication register (see note 5)	e⁻/pixel	-	800k	-
Readout noise at 50 kHz with CDS, HR amplifier (normal mode) (see note 6)	e⁻ rms	-	2.2	-
Readout noise at 1 MHz with CDS, HR amplifier (normal mode) (see note 6)	e⁻ rms	-	5.4	-
Amplifier reset noise (without CDS), HR amplifier (normal mode) (see note 6)	e⁻ rms	-	50	-
Readout noise at 50 kHz with CDS, LS amplifier (normal mode) (see note 6)	e⁻ rms	-	6	-
Readout noise at 1 MHz with CDS, LS amplifier (normal mode) (see note 6)	e⁻ rms	-	14	-
Amplifier reset noise (without CDS), LS amplifier (normal mode) (see note 6)	e⁻ rms	-	120	-
Readout noise at 1 MHz (high gain mode) (see note 6)	e⁻ rms	-	<1	-
Maximum frequency (settling to 1%), HR amplifier (see notes 6 and 7)	MHz	-	-	3
Maximum frequency (settling to 5%), HR amplifier (see notes 6 and 7)	MHz	-	-	4.5
Maximum frequency (settling to 1%), LS amplifier (see notes 6 and 7)	MHz	-	-	9
Maximum frequency (settling to 5%), LS amplifier (see notes 6 and 7)	MHz	-	-	15
Maximum parallel transfer frequency (see note 1)	MHz	-	1.6	-
Dark signal at 293 K (see note 8)	e⁻/pixel/s	-	400	800
Dark signal non-uniformity (DSNU) at 293 K (see note 9)	e⁻/pixel/s	-	60	-
Excess noise factor (see note 10)		-	√2	-

Personal Prejudice

- CMOS has overtaken CCD in the consumer market
  - *short integration time – leakage is not* that *important*
  - *very high speed not required*
  - *Limited analog performance ok - <10 bits linear, ~16 bits logarithmic*
  - *Pixels! "The triumph of marketing over physics" – E. Fossum*
- CCDs will continue to dominate size x dynamic range
  - *size x dynamic range x speed are what is needed by the scientific community*

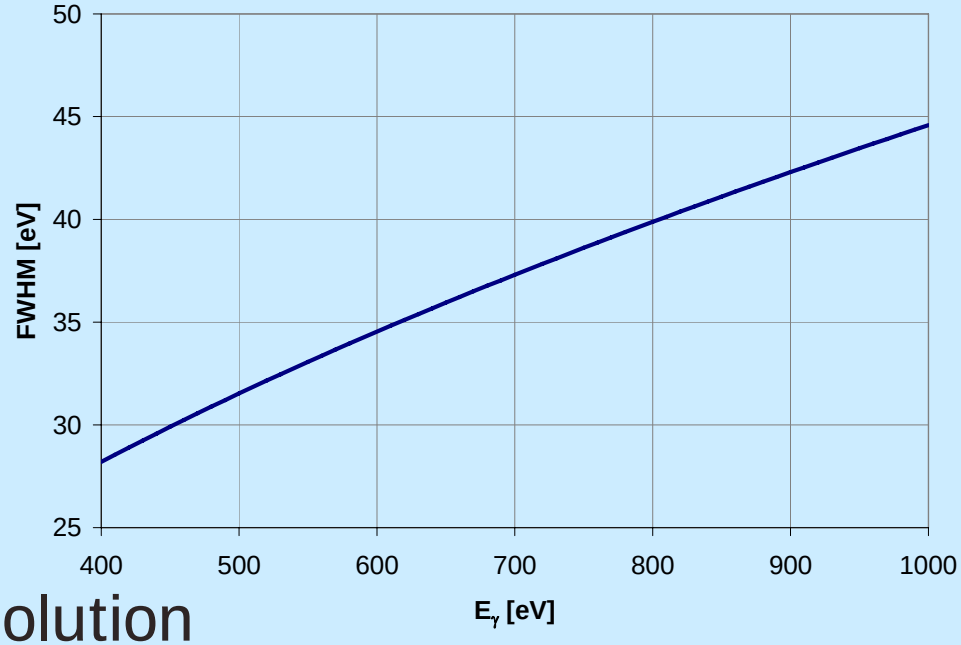
Direct x-ray detection

x-ray view of the galactic center

- Well established use of CCDs in x-ray astronomy
- Excellent spectroscopic resolution possible

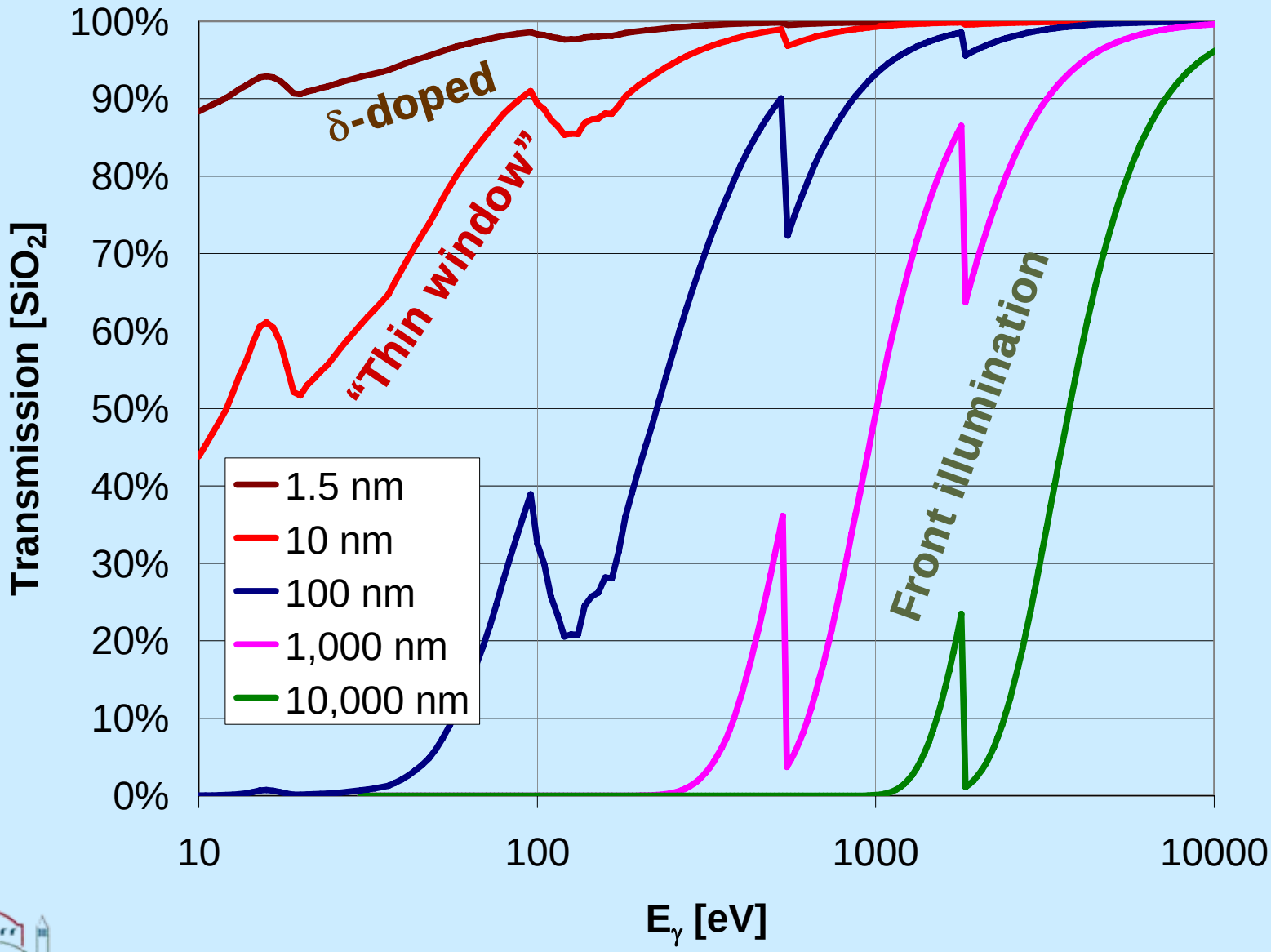
☺ and ☹

Intrinsic resolution in Si

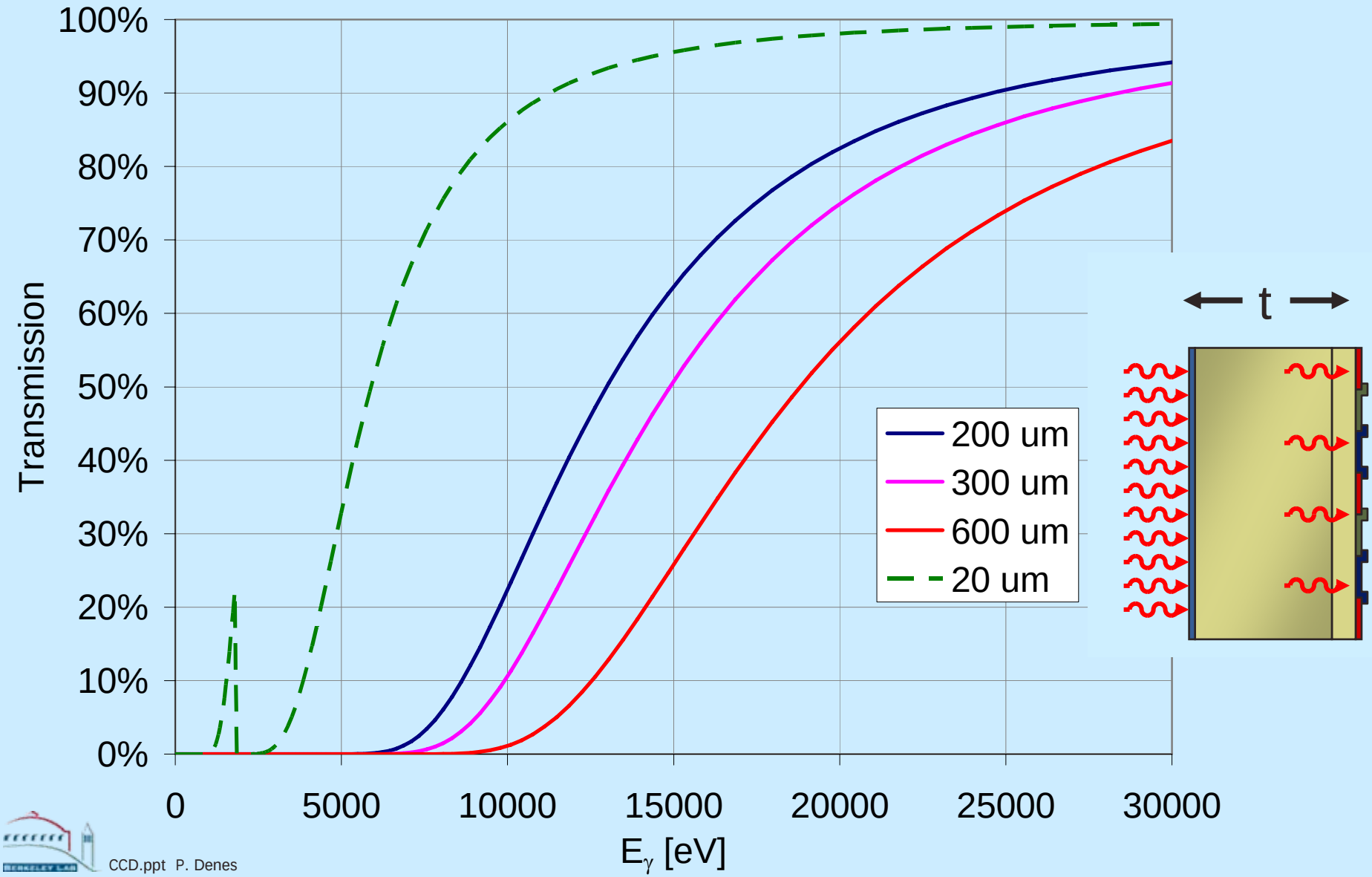


- Excellent spectroscopic resolution
- But only if not piled-up – low rate or fast readout
- $N_{\gamma,MAX}$ = Well Depth / (E_γ /3.6 eV)
  - *<1000*
  - *⇒ 9-10 bit ADC OK*
- Would really profit from high-speed readout as S/N is so high

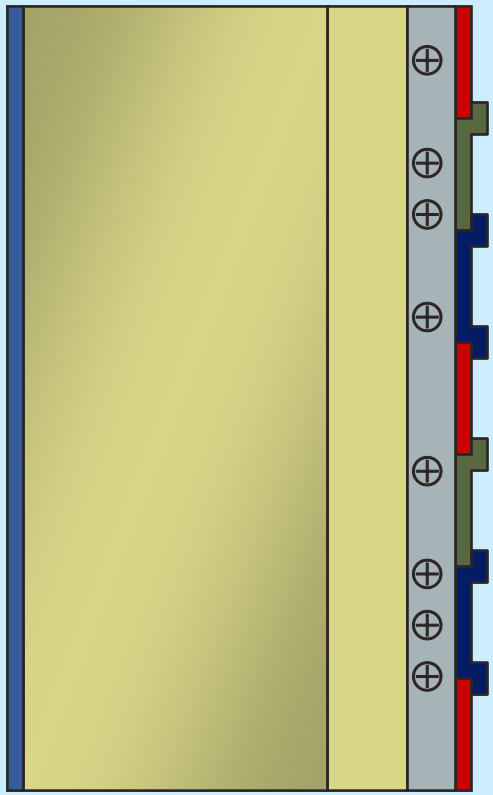
Back-illumination preferred



Thick Silicon

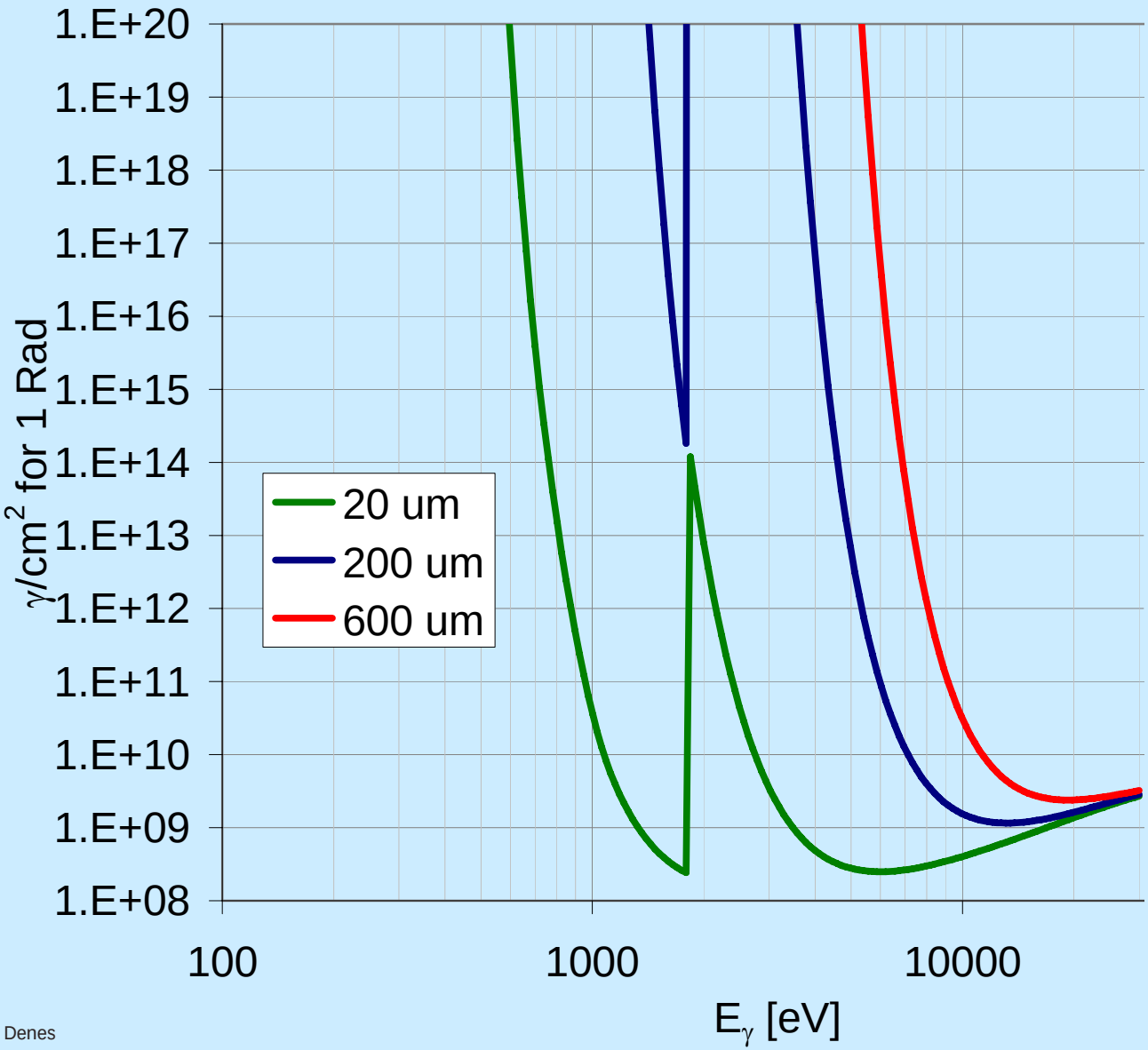


Radiation Damage

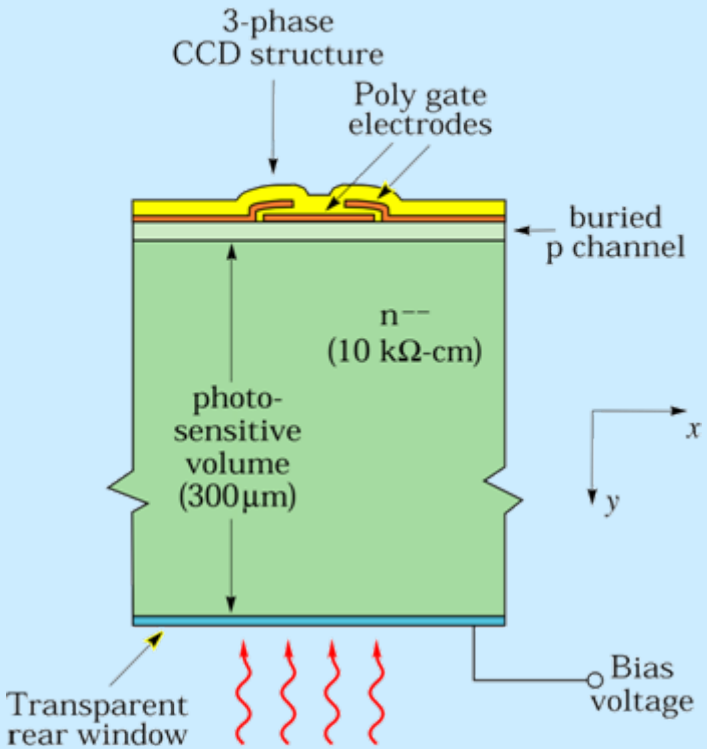


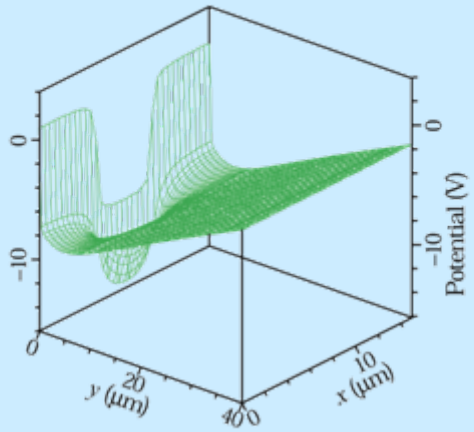
- Ionization damage
  - *Charge trapping in gate oxide*
    - *Threshold shift*
  - *Damage at the SiO_2 – Si interface*
    - *Surface dark current*
    - *Surface mobility loss*
  - *CCDs have thick oxides*

Flux for 1 Rad in gate oxide



LBNL CCD

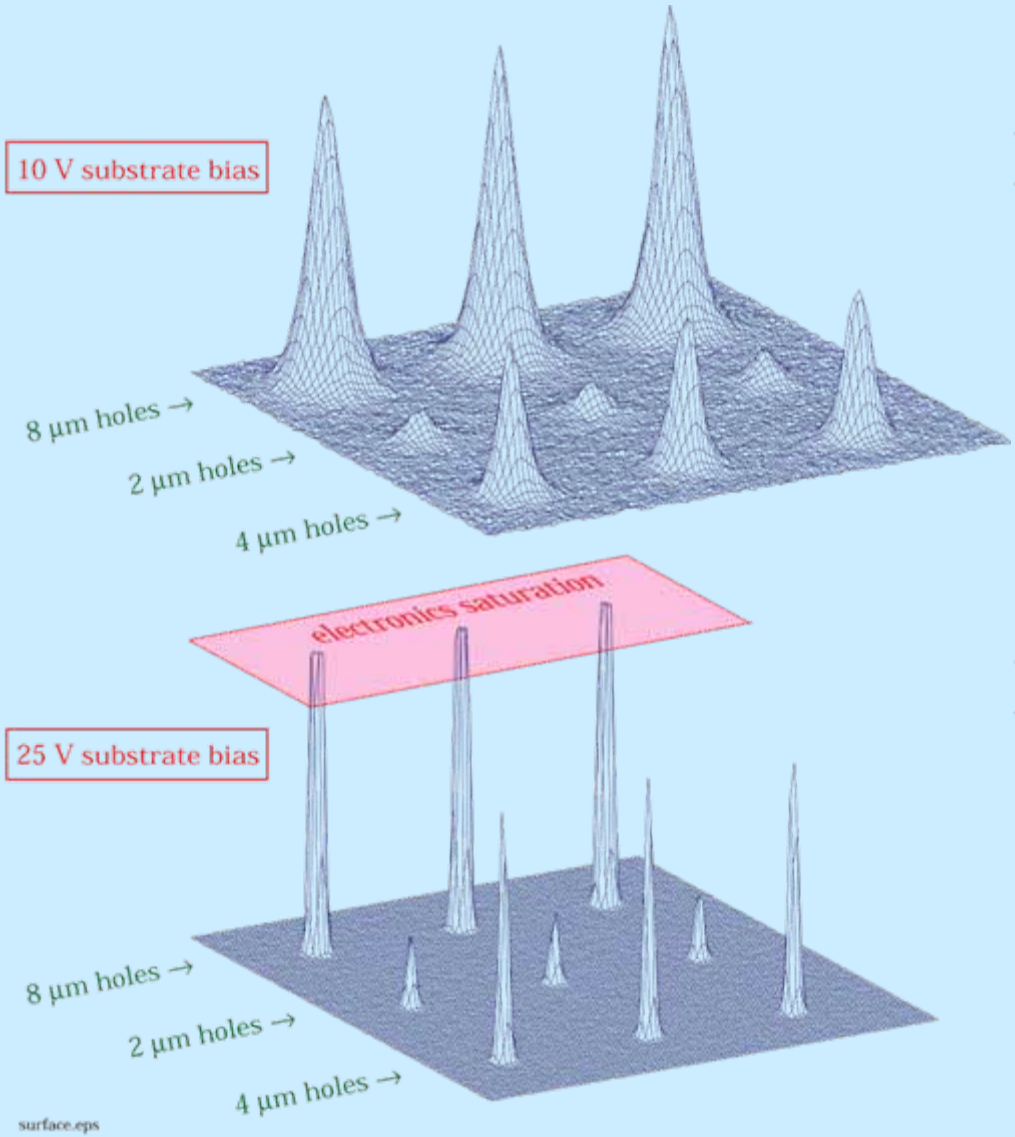


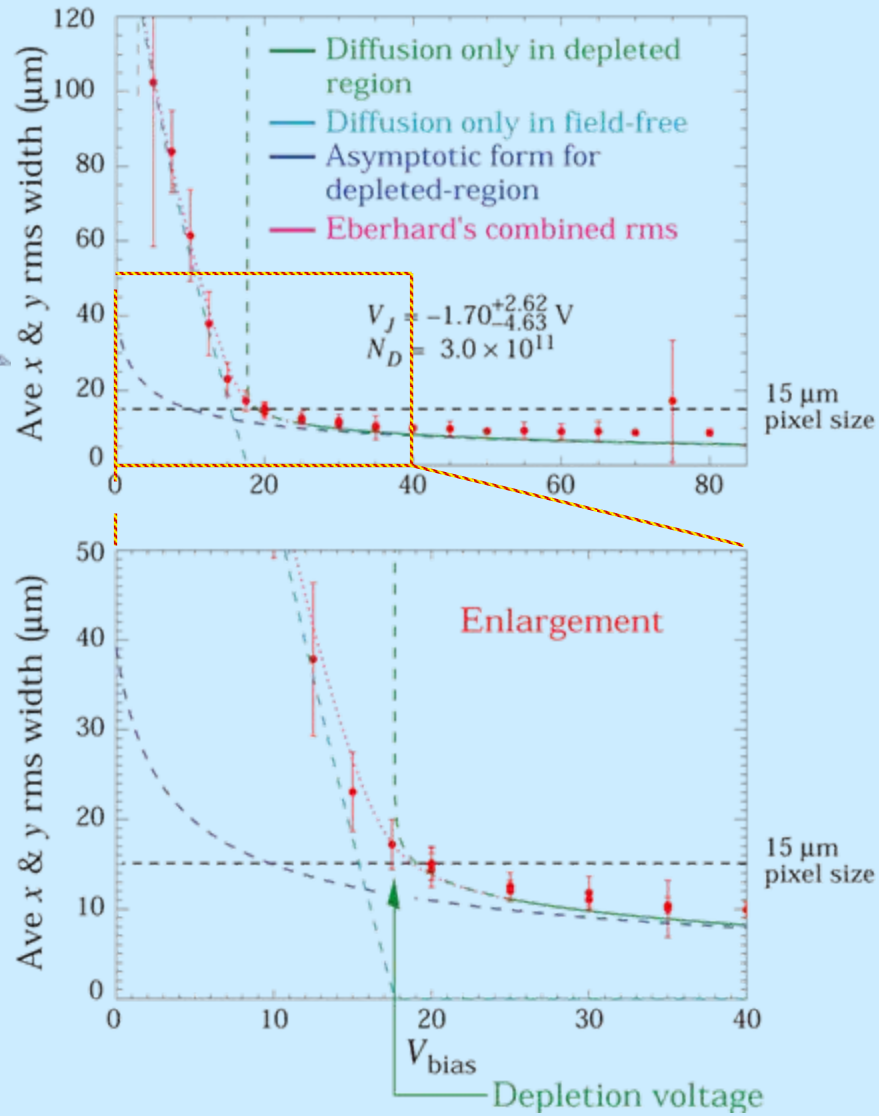


MEDICI 2-D simulation

- CCD on high-resistivity, fully depleted silicon
  - *No thinning needed*
  - *Good red (and blue) response*
  - *No field free regions for diffusion ⇒ good PSF*
- ***Bias*** depletes substrate independently of clock voltages

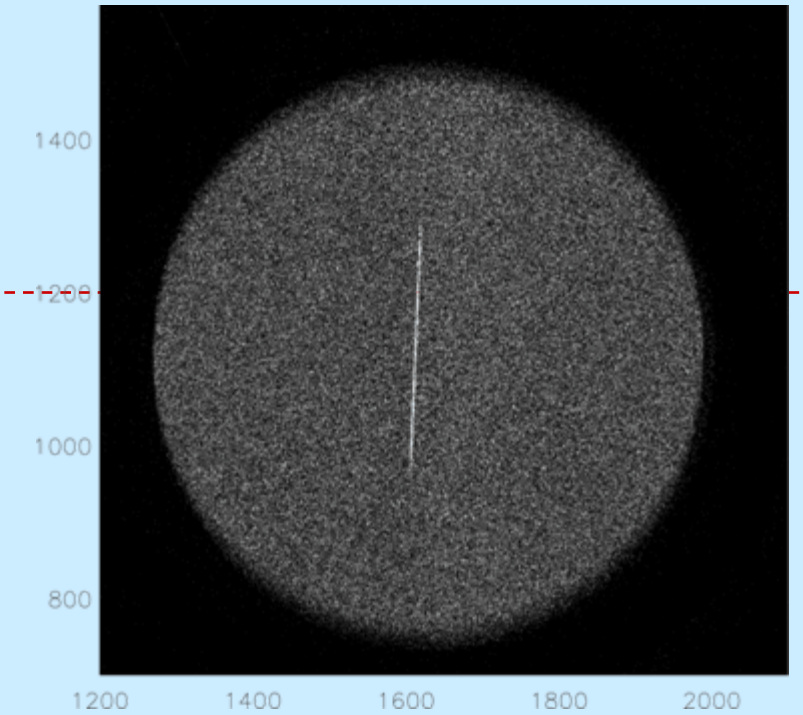
PSF – measured with pinholes at UCO Lick





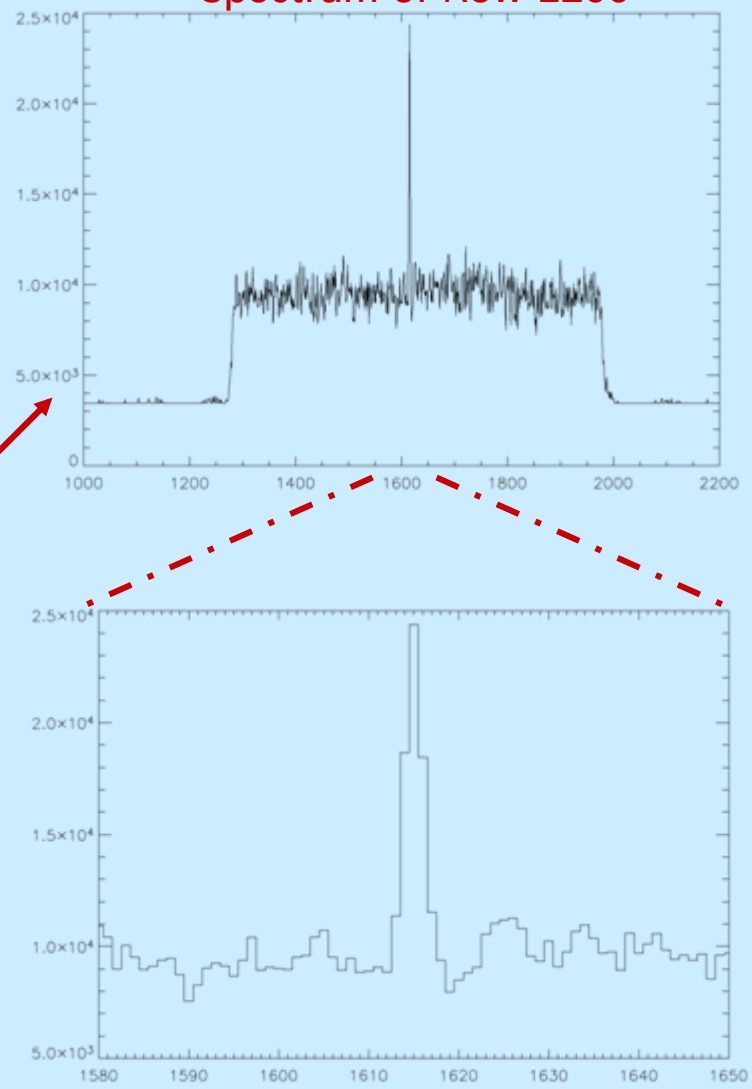
1st x-ray images in LBNL CCD

3,512 x 3,512 x 10.5μm pixel CCD
200 μm thick
Cu anode, 140K, 70 kHz



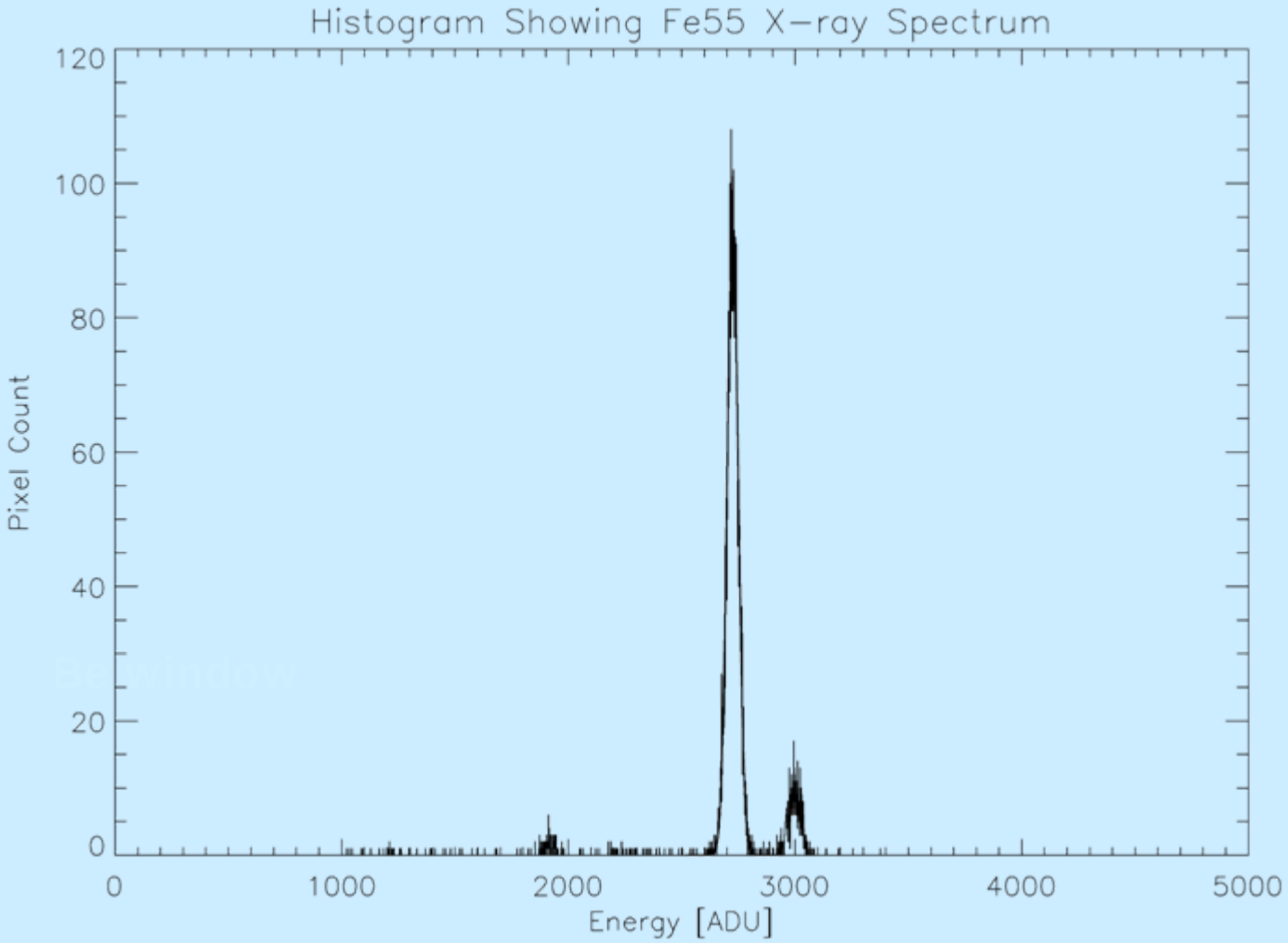
5 μm slit in semi-transparent stainless steel

Spectrum of Row 1200



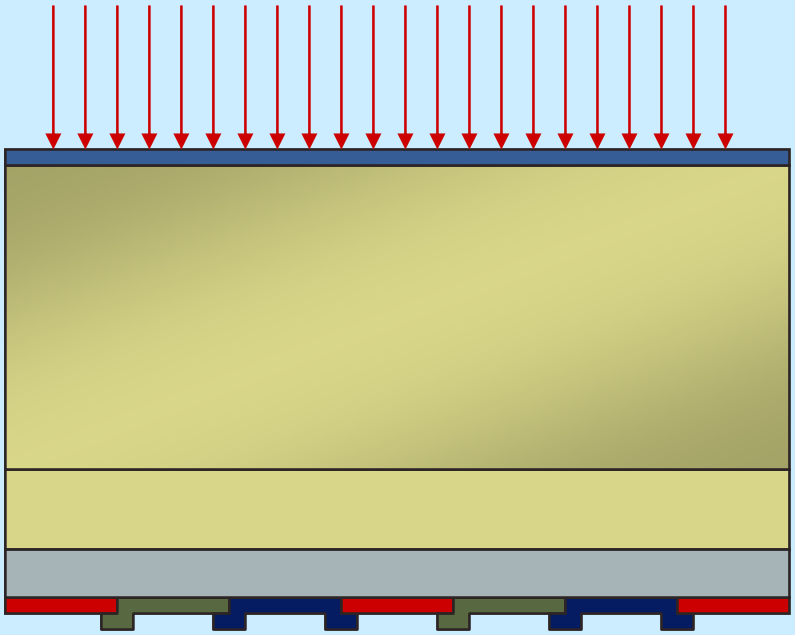
650 µm thick CCD

^{55}Fe K_α and K_β. Resolution ~ 126 eV at 5.6 keV

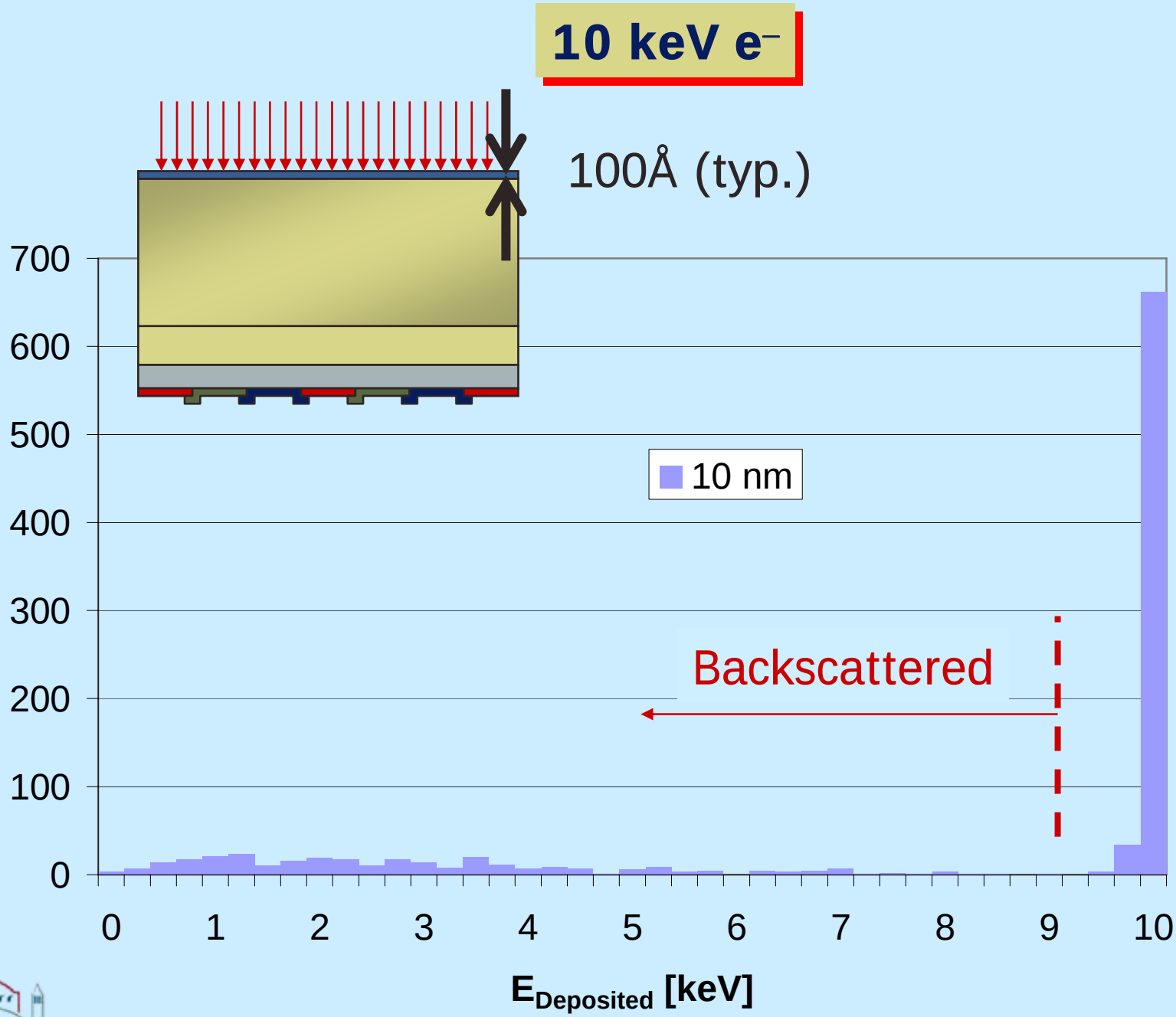


Back-illuminated CCDs for low-energy e^-

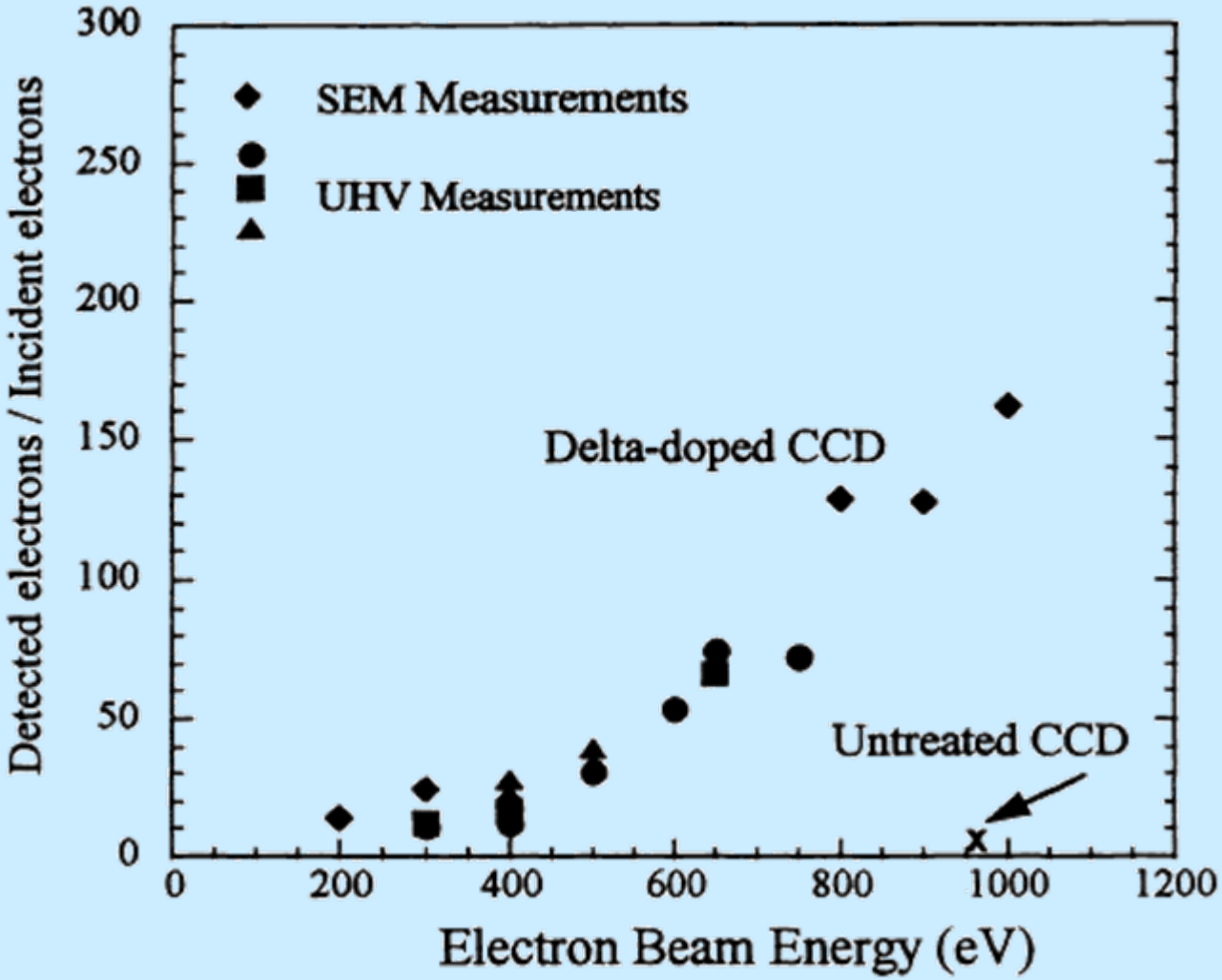
Thin entrance windows also good for electrons



- Window should be thin enough to allow electrons to penetrate
- Device should be thick enough to avoid radiation damage
- Excellent S/N (3.6 eV/e-h pair)
  - *Well depth*


10 keV e⁻
100Å (typ.)
700
600
500
400
300
200
100
0
10 nm
Backscattered
0
1
2
3
4
5
6
7
8
9
10
E Deposited [keV]

δ-doping ~15 Å



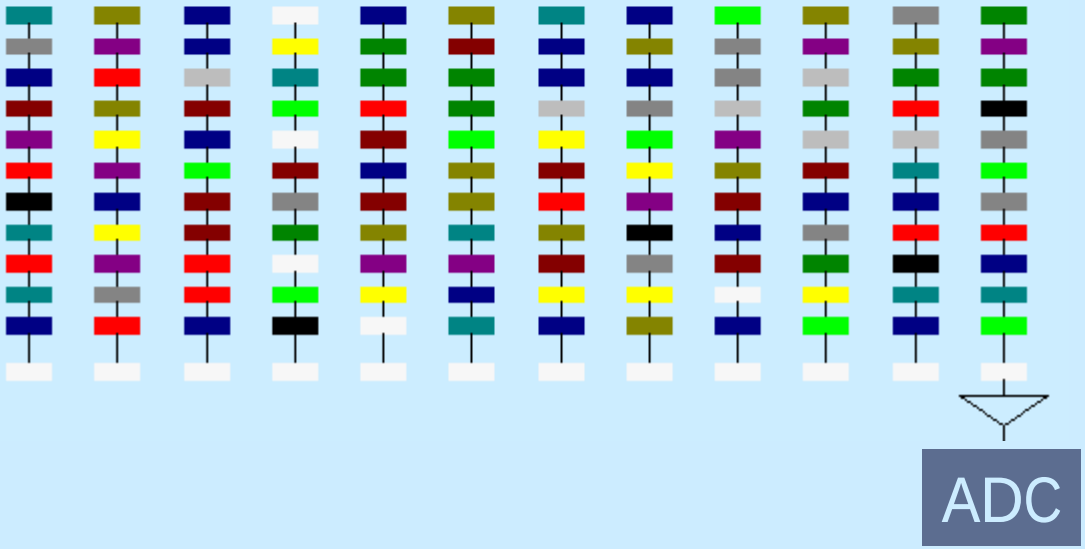
Nikzad et al SPIE 97

CCDs are wonderful

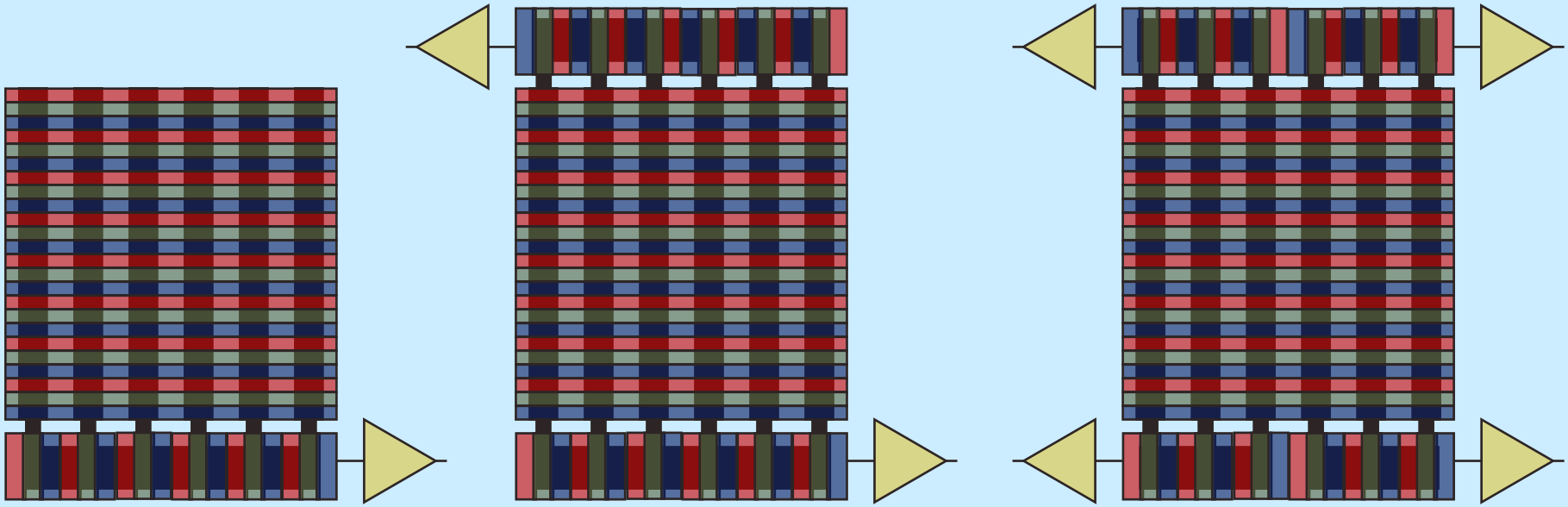
But they are slow

- Parallel exposure
- Serial readout

- Vertical clock
- Horizontal clock
- External, high resolution ADC



Easy



Now it gets more difficult

Increase ADC speed

$$T_f = \frac{N_V}{2}\left(T_V + \frac{1}{B_V}\left[B_H T_H + \frac{N_H}{B_H N_{port}} T_{CONV}\right]\right)$$

top+bottom readout

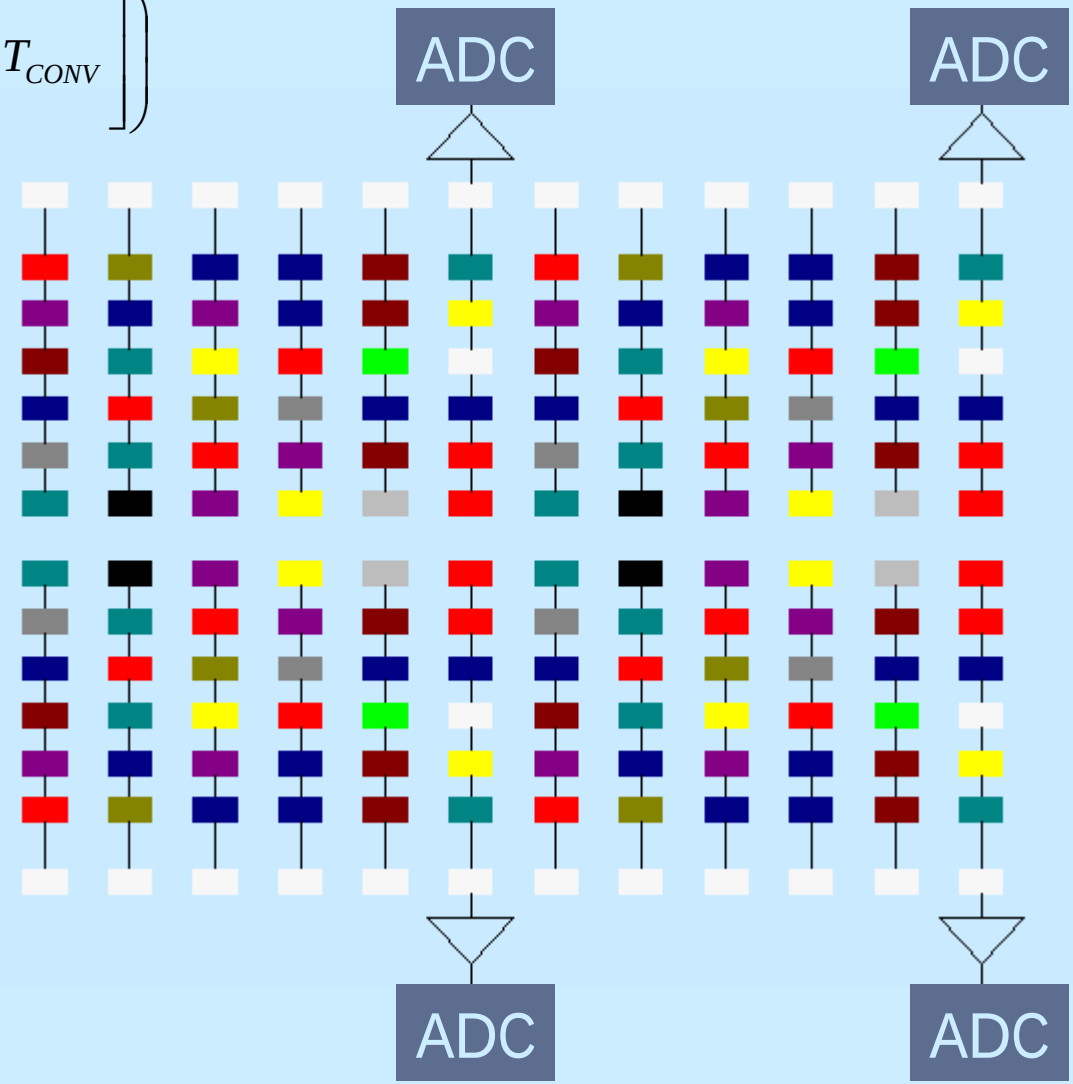
N_V, N_H = # H, V pixels

B_V, B_H = H, V binning

T_V, T_H = H, V shift time

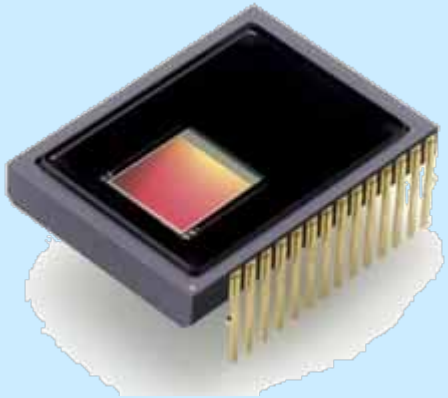
N_{port} = # ports

T_{CONV} = total conversion time including reset, summing well, ...



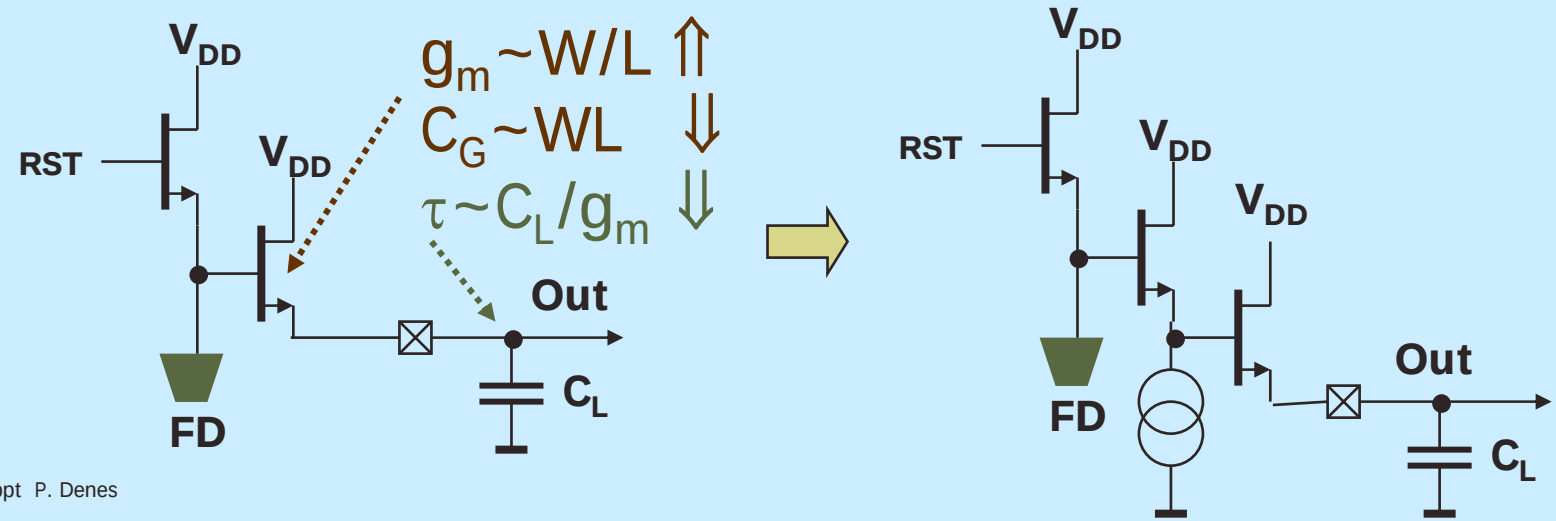
For example

Increase readout/ADC speed

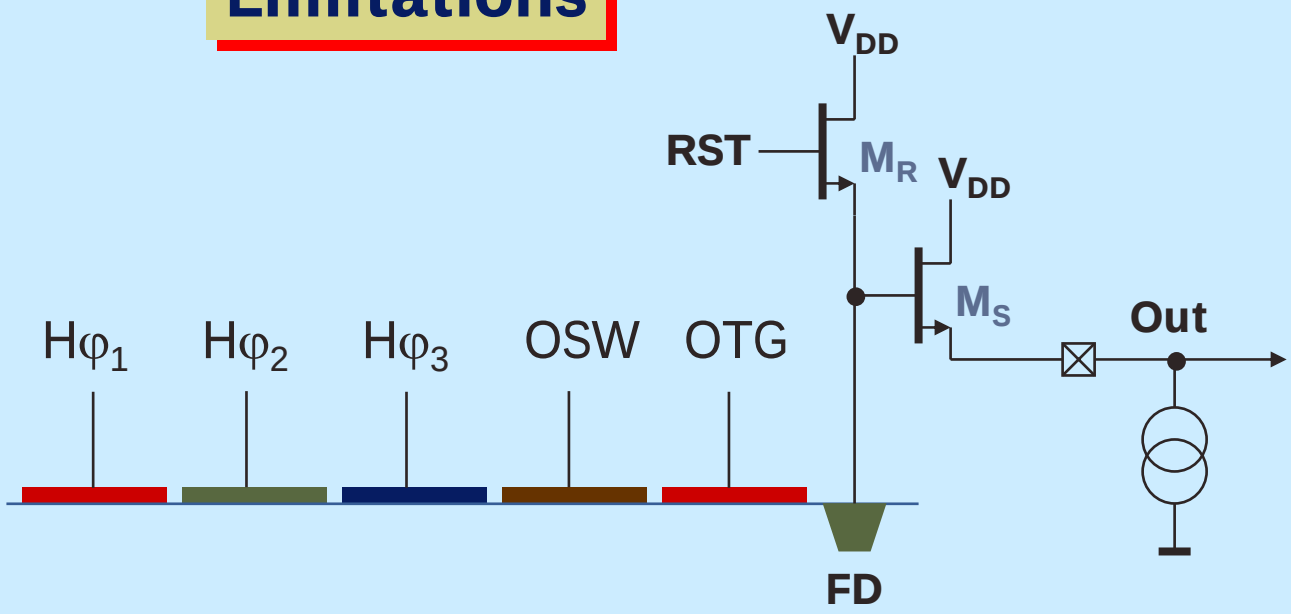


- Dalsa – FT50M
- 1024 x 1024 x 5.6 µm pixel
- Frame transfer / 2 ports
- 100 fps = 100 MPix/s
- 11.1 bits [67 dB] at 30/60 fps
- 10.1 bits [61 dB] at 50/100 fps

S/F Limitations



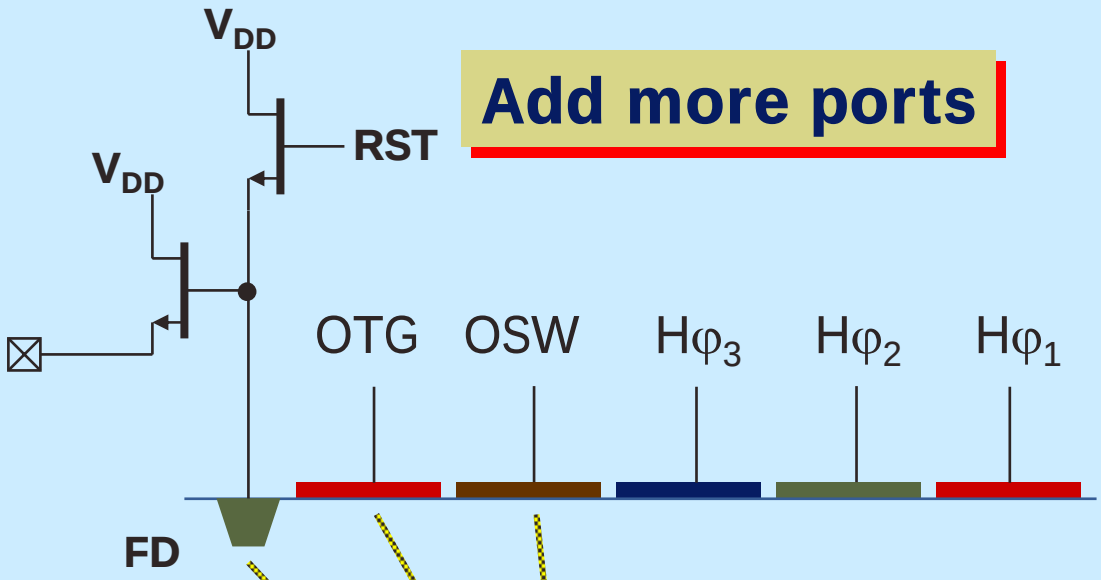
Limitations

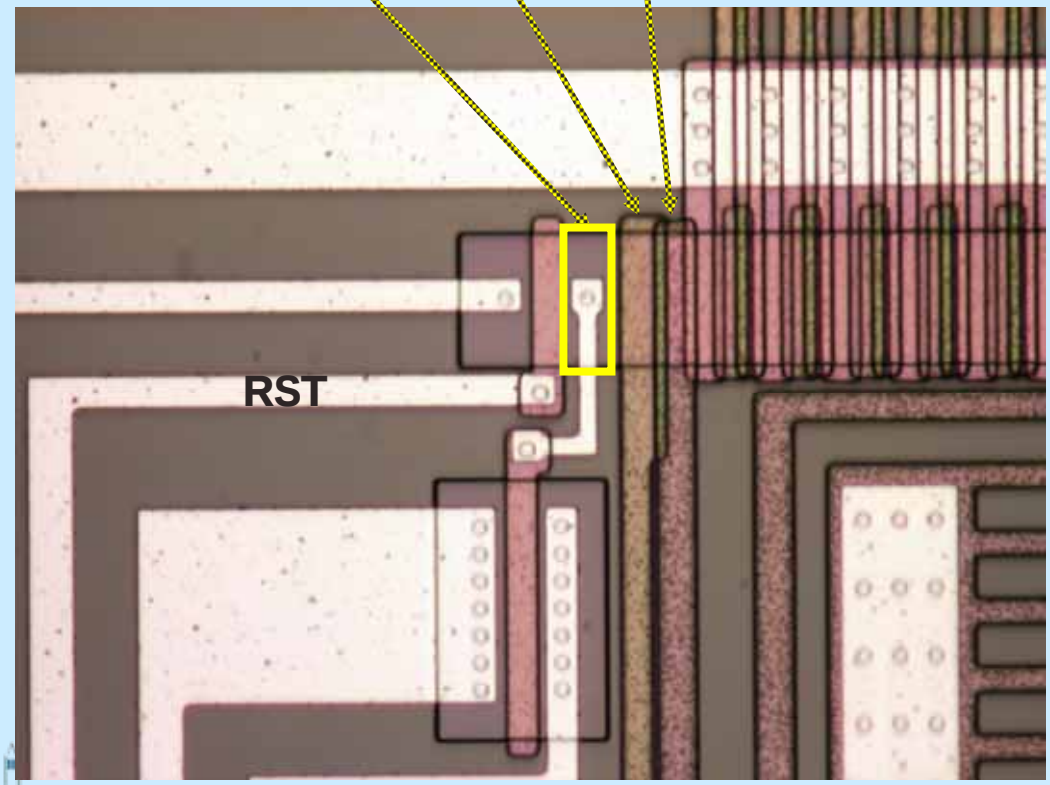


- $\sqrt{kTC}$ Noise contribution from M_R (reset switch) removed by CDS (correlated double sampling – measure V_R and $V_R + V_S$)
- Noise contributions from M_S (source follower)
  - *Thermal noise* $V_n^2 \sim 4kT\gamma g_m \int H^2(f)\, df$
  - *1/f noise* $V_n^2 \sim \frac{K}{C_{OX}WL} \int H^2(f) \frac{1}{f}\, df$
  - *Noise from current source*

↑ ~ √rate

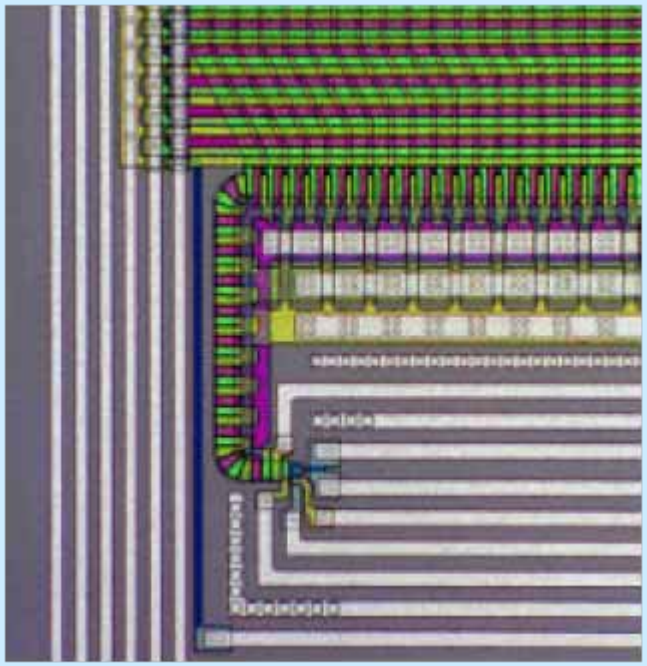
Add more ports





- Reset and output transistors need room
- Want to minimize C_{FD}
- Need space for the output stage!

One way to gain space



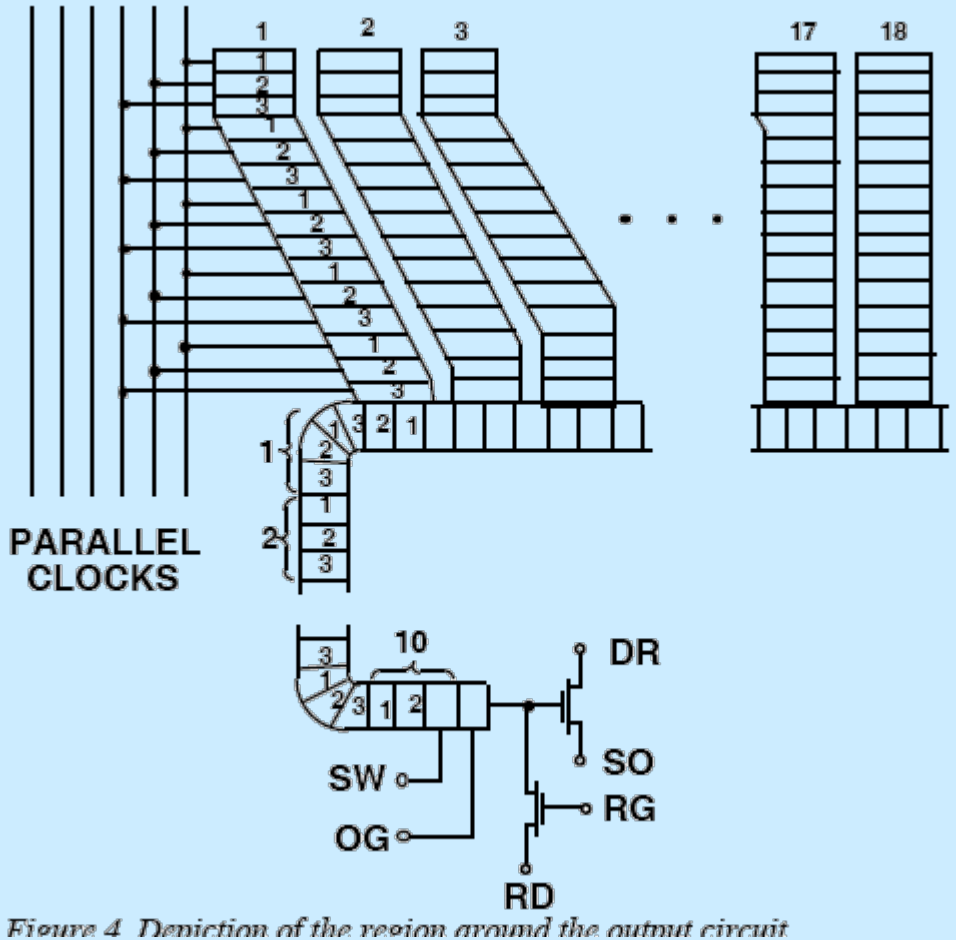
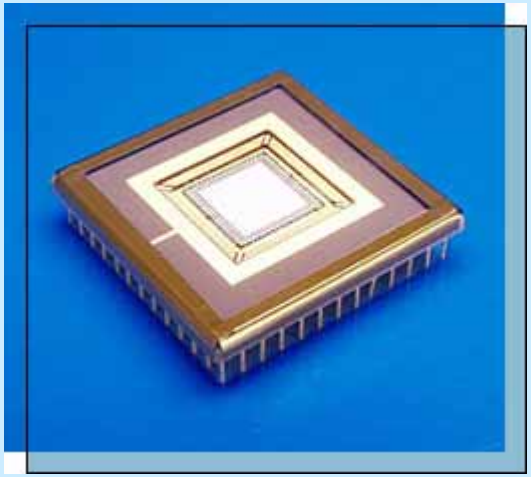


Figure 4. Depiction of the region around the output circuit

MIT Lincoln Labs multi-port CCD

For example

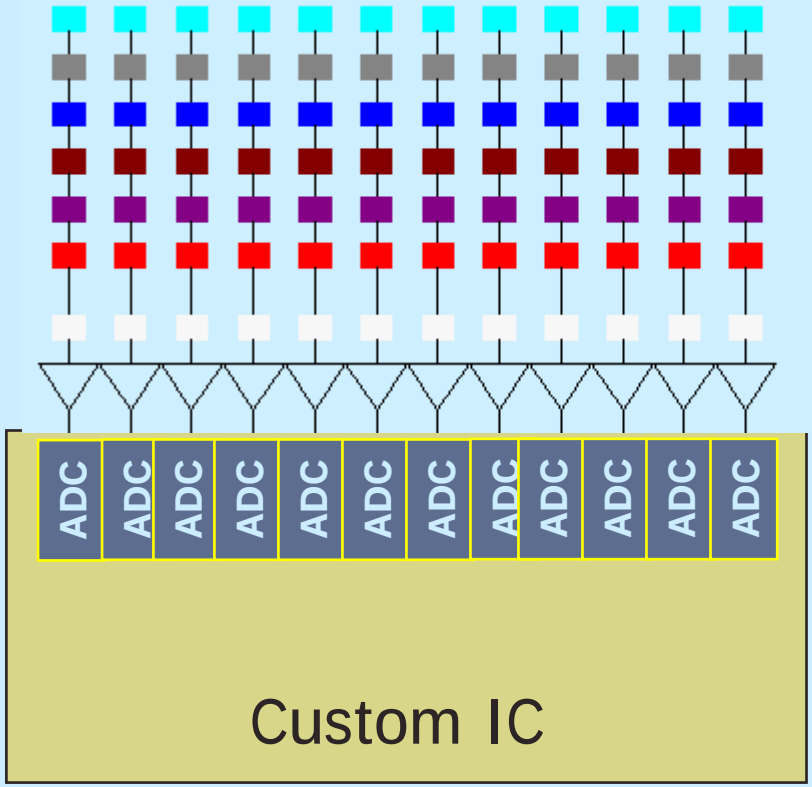


- Fairchild 456
- 512 x 512 x 8.7 µm pixel
- Interline transfer / 32 ports
- 1000 fps = 250 MPix/s

- On-chip current sources for 3-stage output ⇒ 2.5 Watts

At some point, adding more ADC ports becomes a connection nightmare → integrated circuit solution needed.

Fully column-parallel

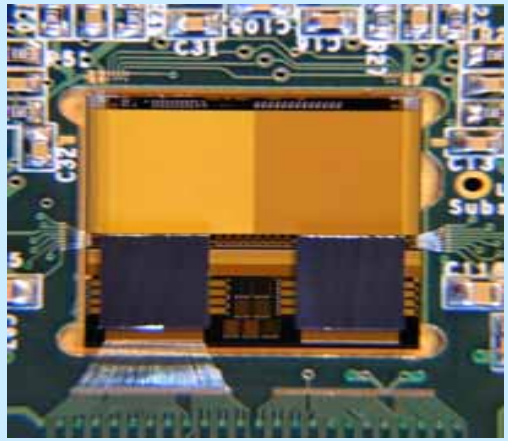


- 1 ADC/column
- Bump bonding required
- No source-follower

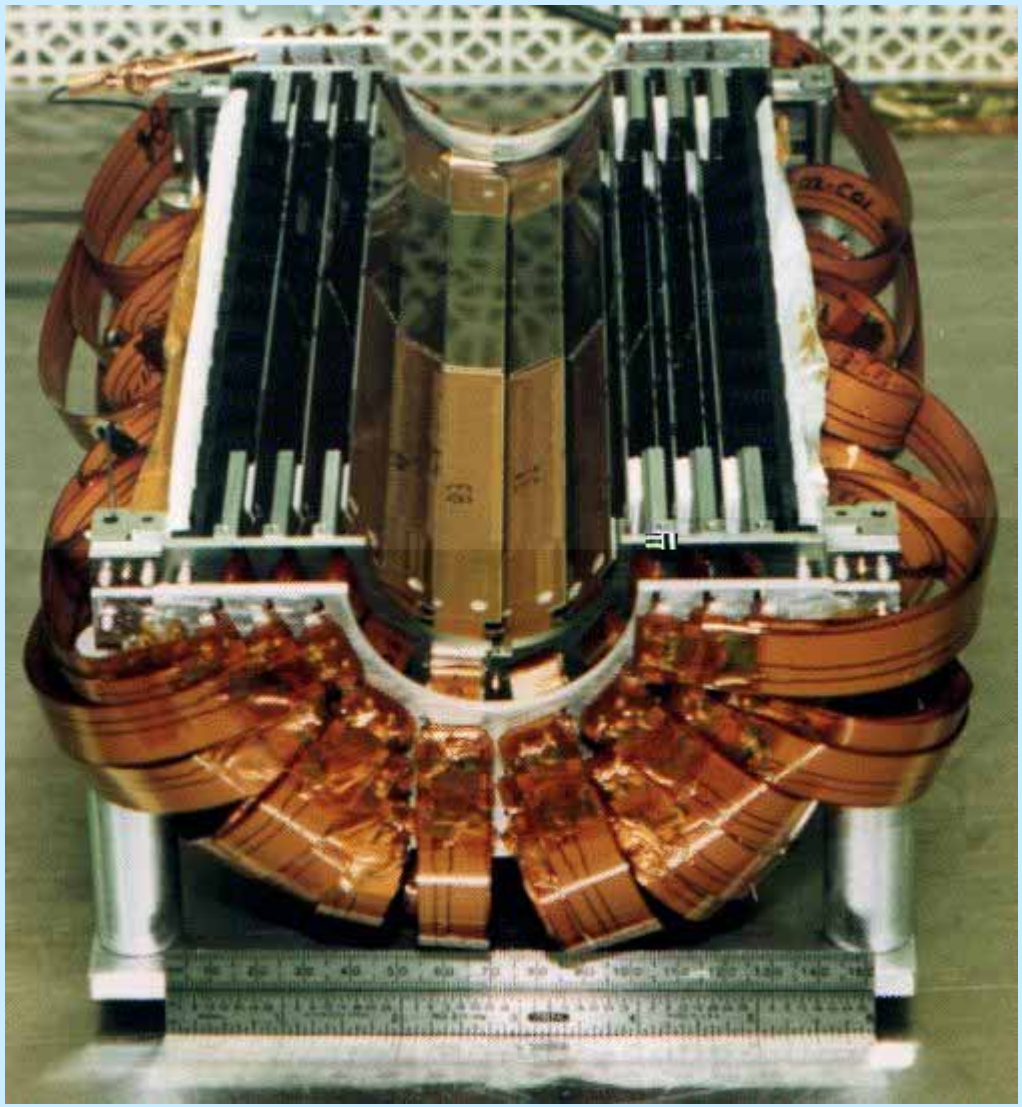
- Example – developments for ILC Vertex Detector
  - *50 MHz column readout*
  - *4-5 bits dynamic range*

LCFI

RAL et al.

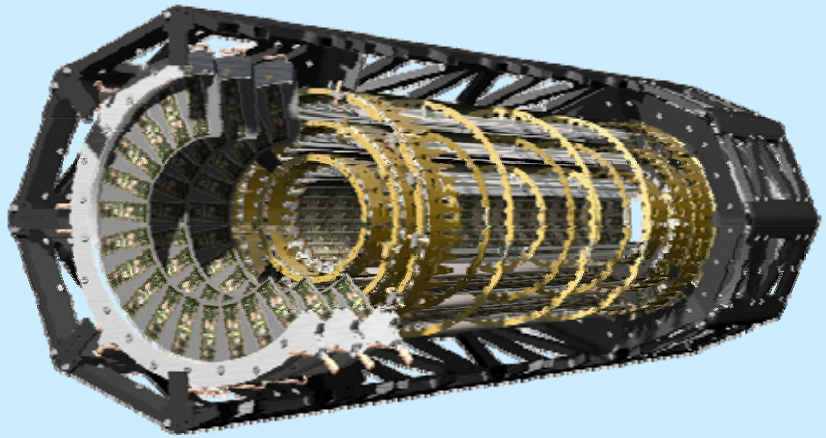


Precedent

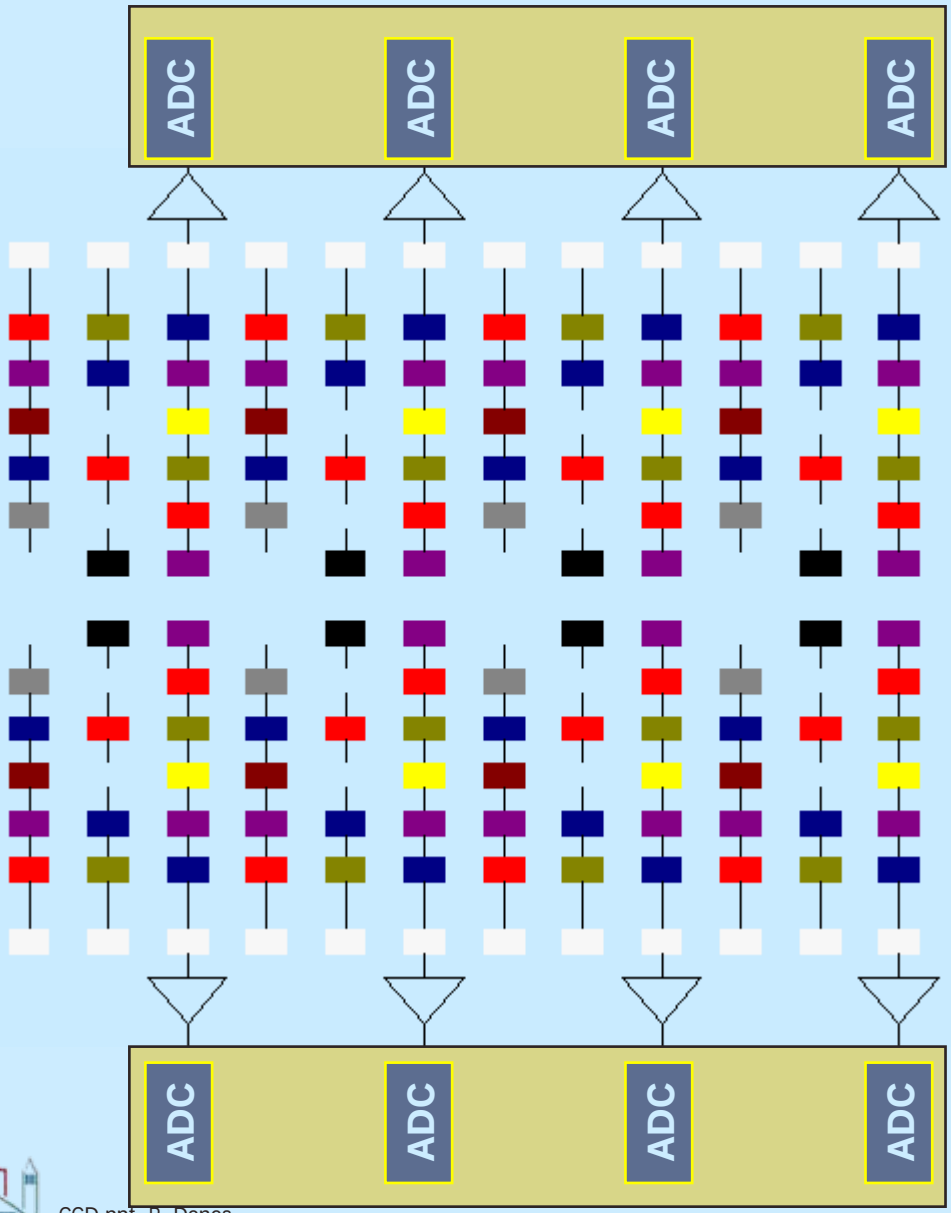


- 1996 - SLD Vertex Detector
- 3 x 10^8 pixels
- 96 x 3.2 MPix x 20 µm CCD

Tomorrow – ATLAS Pixel



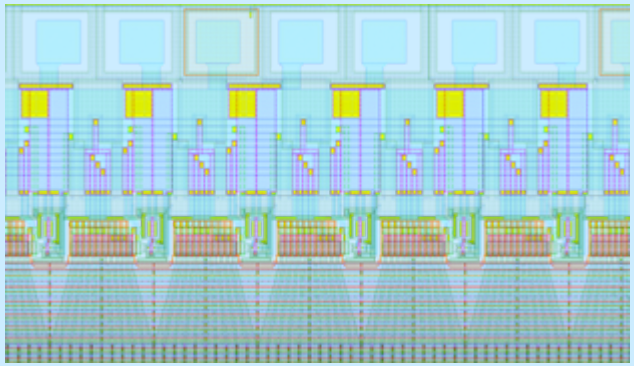
(Almost) Column Parallel CCDs

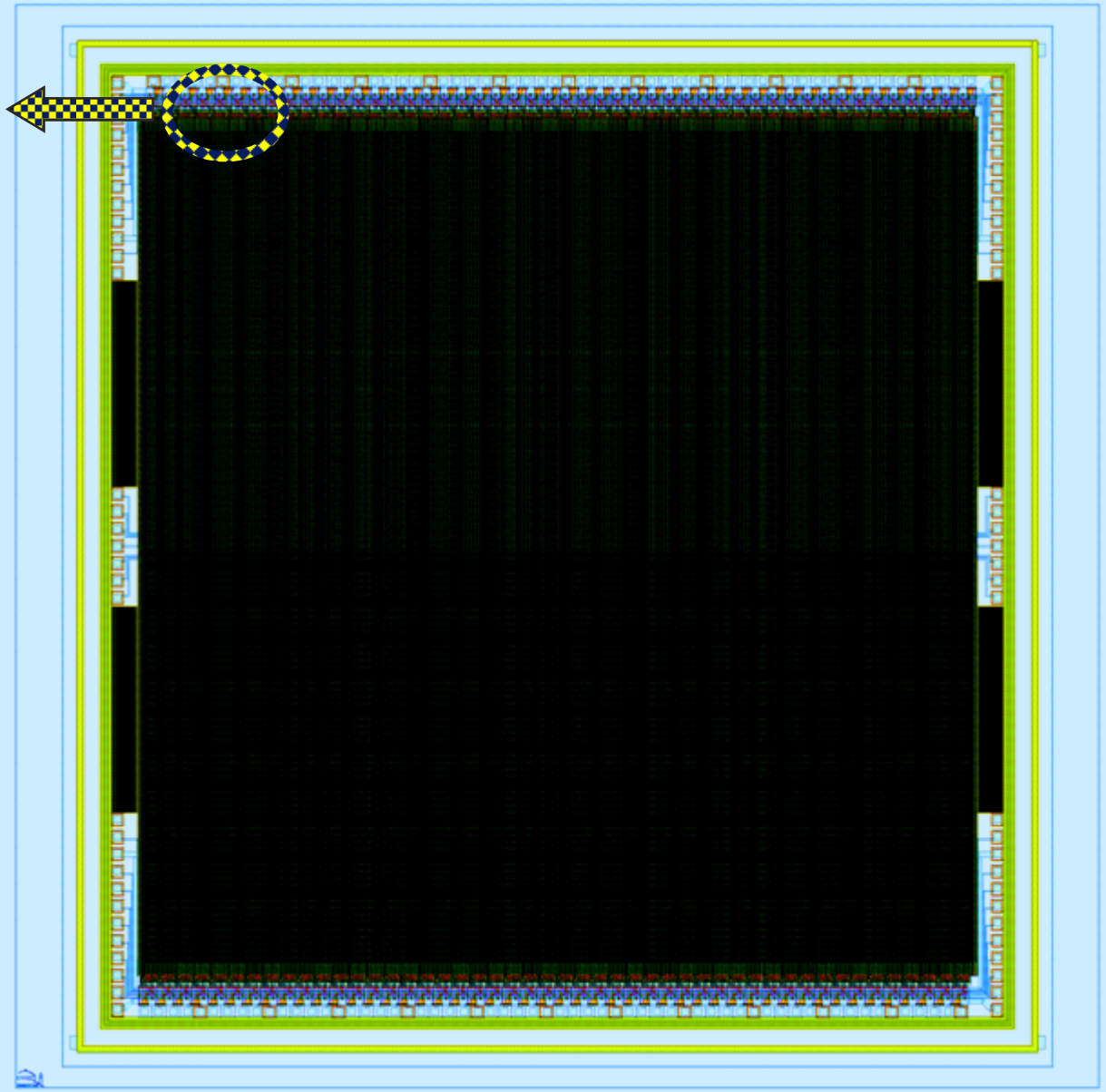


Solution chosen

- Speed increased by N_{PORTS}
- N_H *large* enough to minimize the number of ADCs needed
- N_H *small* enough to ensure fast readout
- Wire bonding still possible

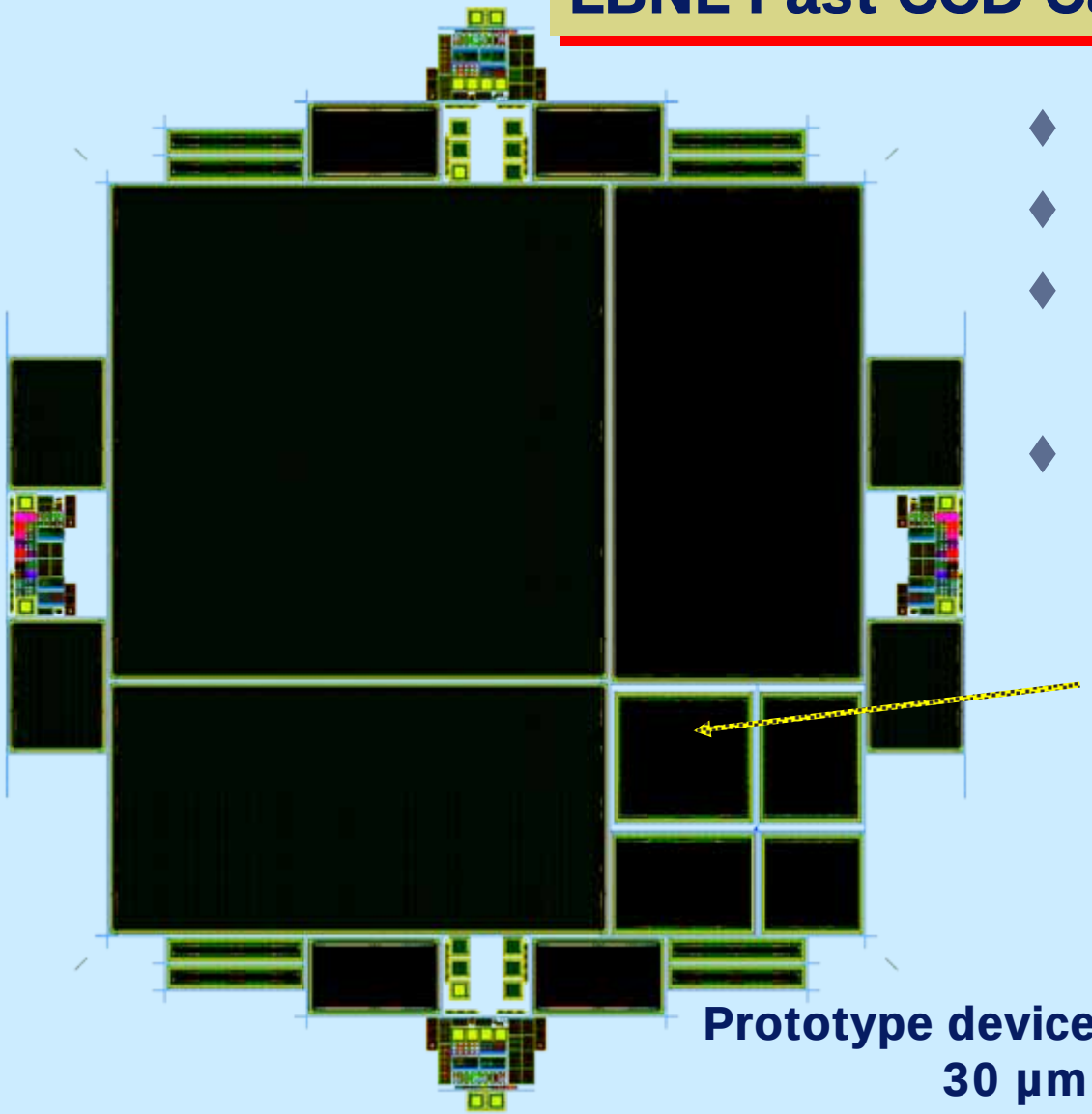
Prototype – 480 x 480 x 30 µm pixels





- Constant area taper
- 10 pixels/SR
  - *300 µm output pitch*

LBNL Fast CCD Camera

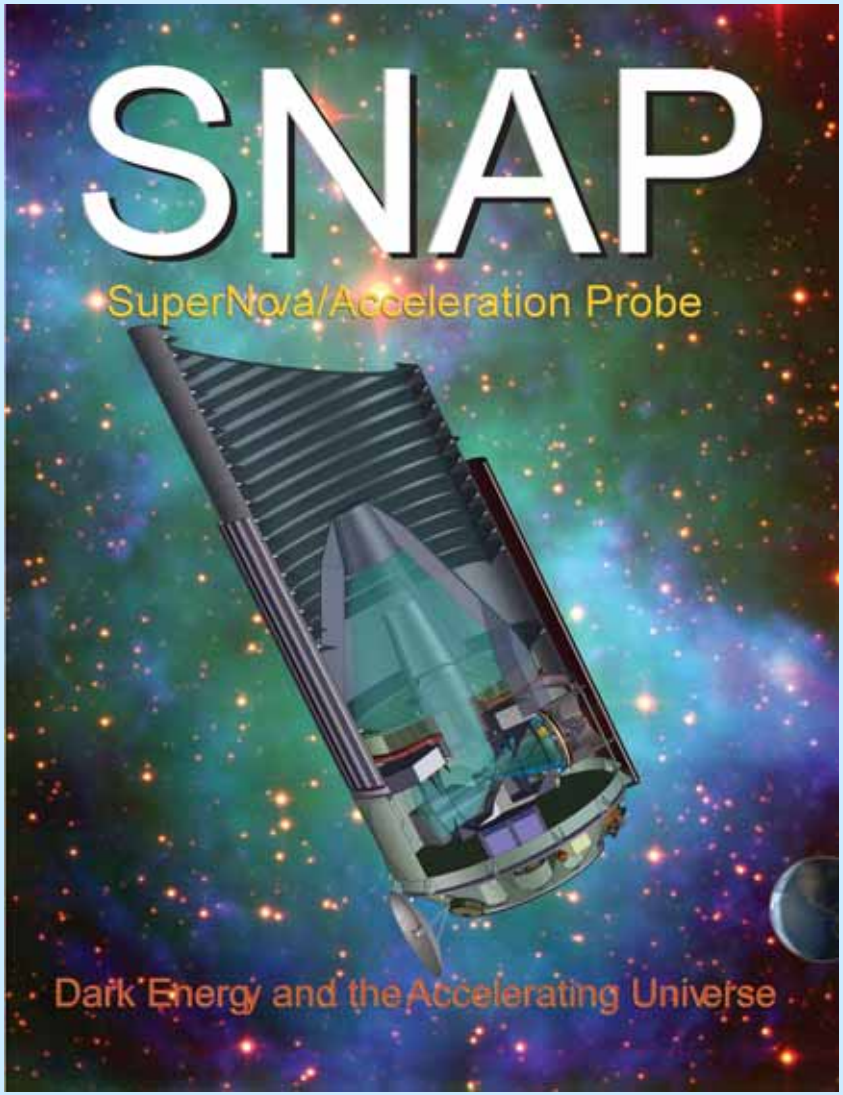


- Goals:
- 200 MPix / s
- ≥ 14 bits (84 dB)

- Proof-of-concept
  - *LDRD (internal lab R&D)*
  - *30 µm pixels*
  - *funding limited 480 x 480 device slipped onto 4k CCD run*
  - *custom readout IC*

Prototype devices with 30 µm pixels Metal strapped and not (a)CP and 4-port

CCD readout for the *SNAP* focal plane



SNAP requirements

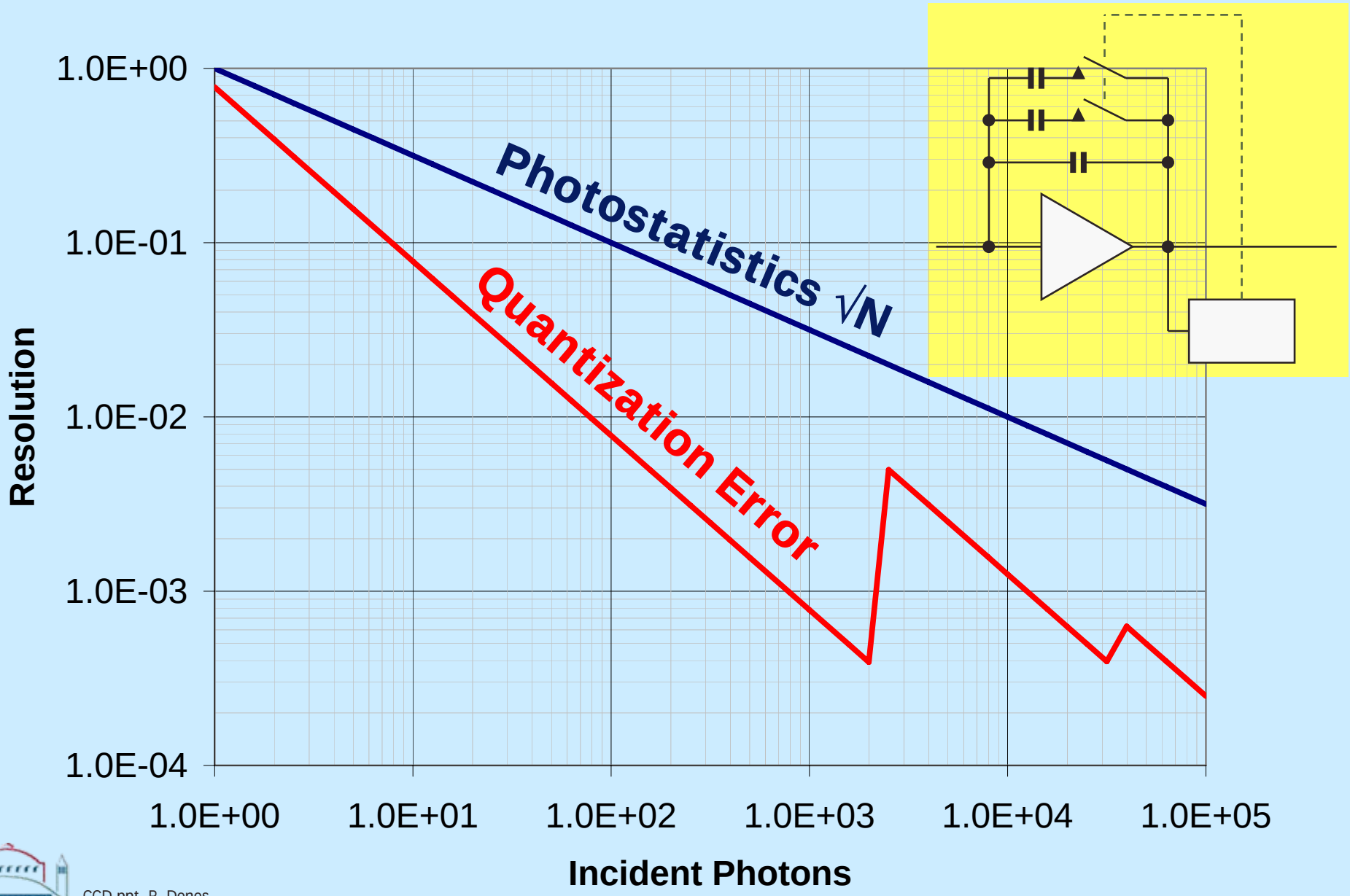
- *16 bit dynamic range at 100 kHz*
- *4 channels per chip*
- *low power*
- *space qualified*

Fast CCD (benefit from SNAP development)

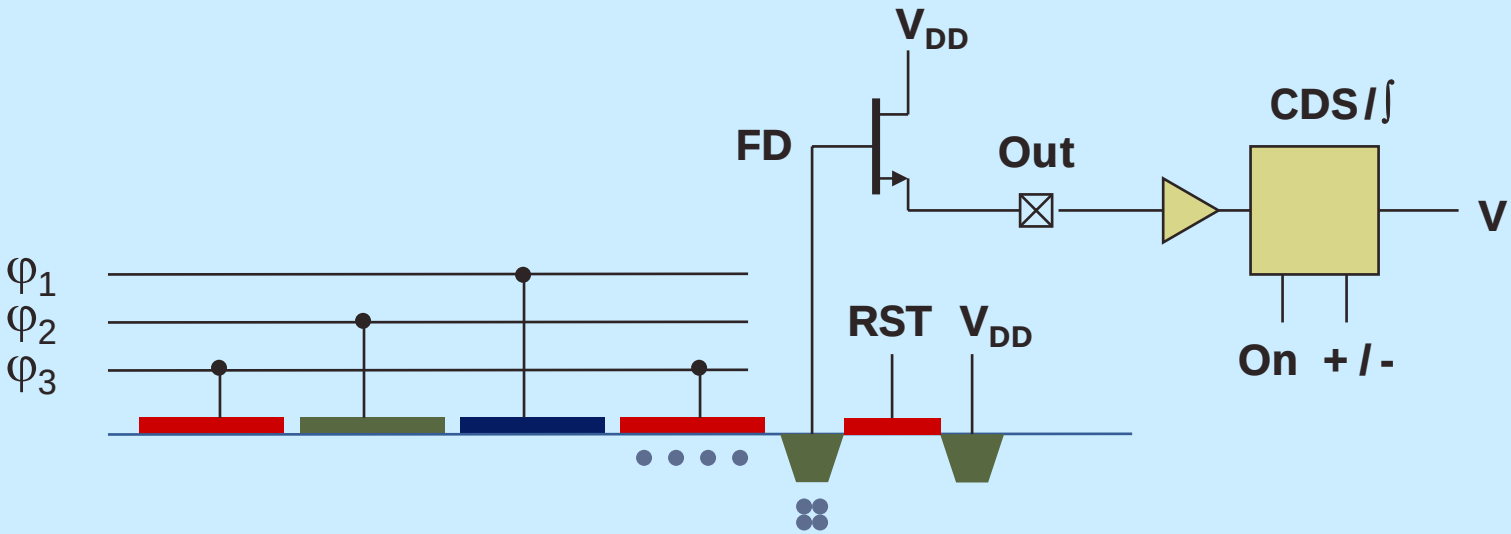
- *16 channels per chip*
- *ADC pitch < 300 µm (to match 300 µm output pitch) – actual: 235 µm*
- *10 x speed ⇒ DR = 16/√10 bits*

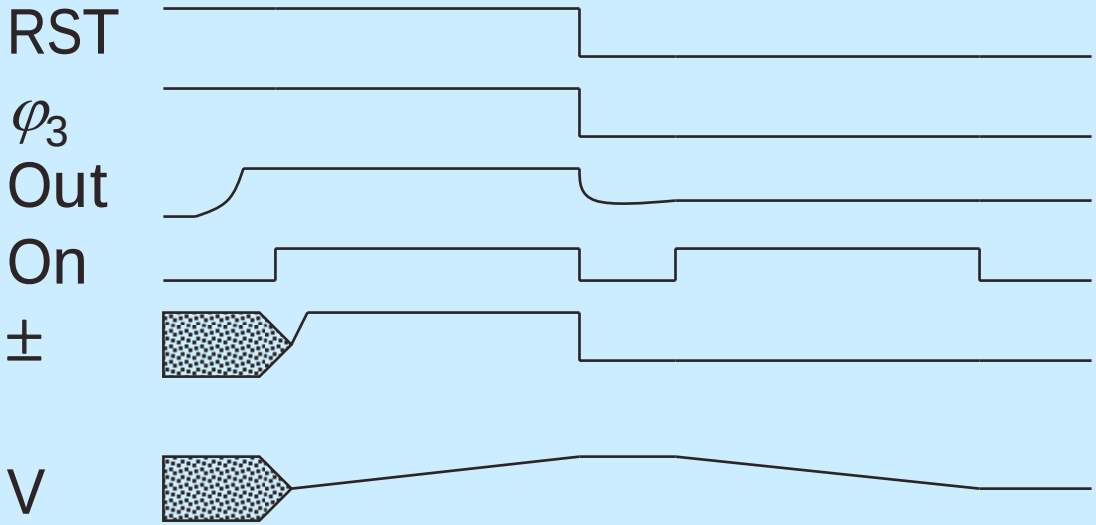
Structure of circuit lends itself to future designs

Floating Point Readout



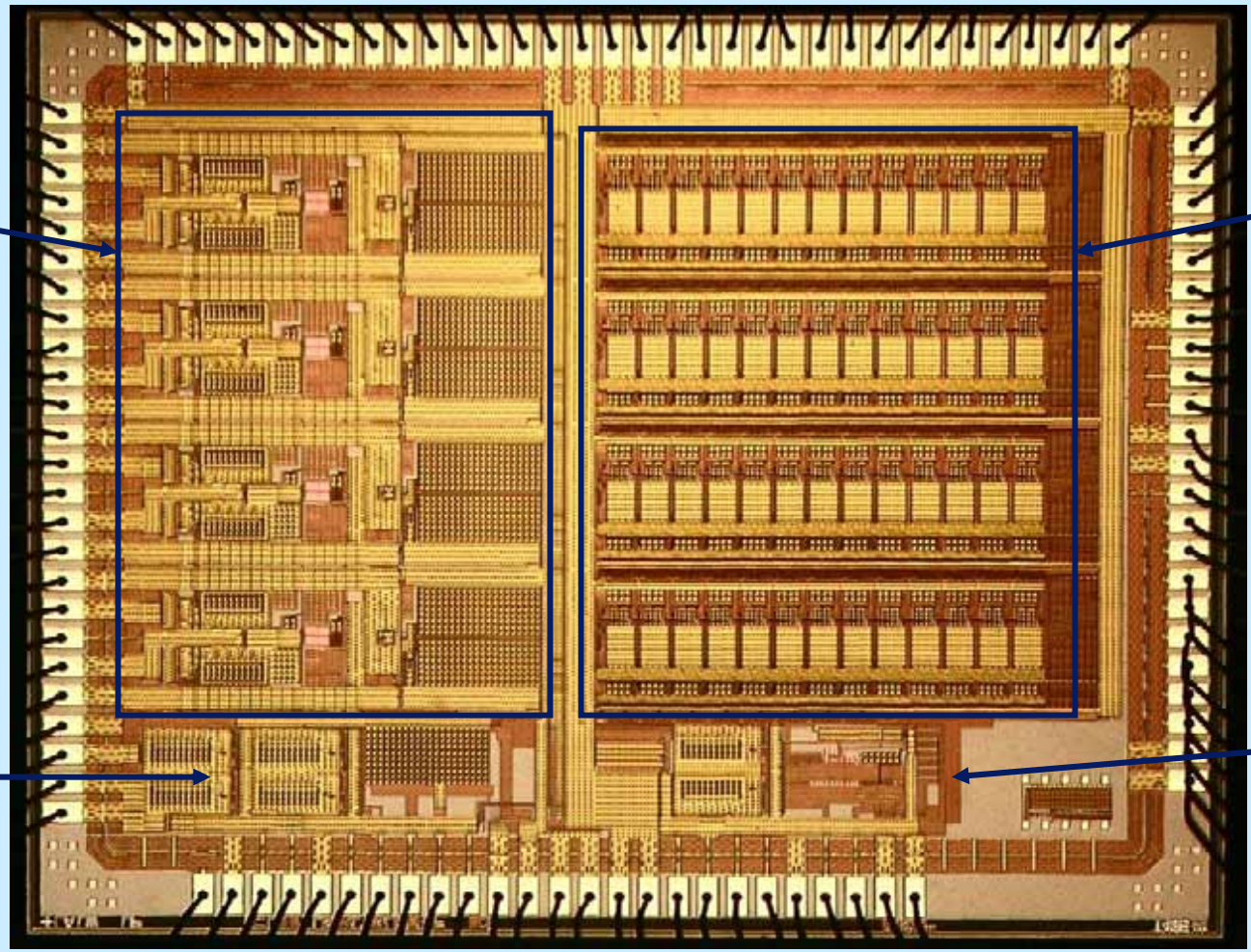
Digitize cycle



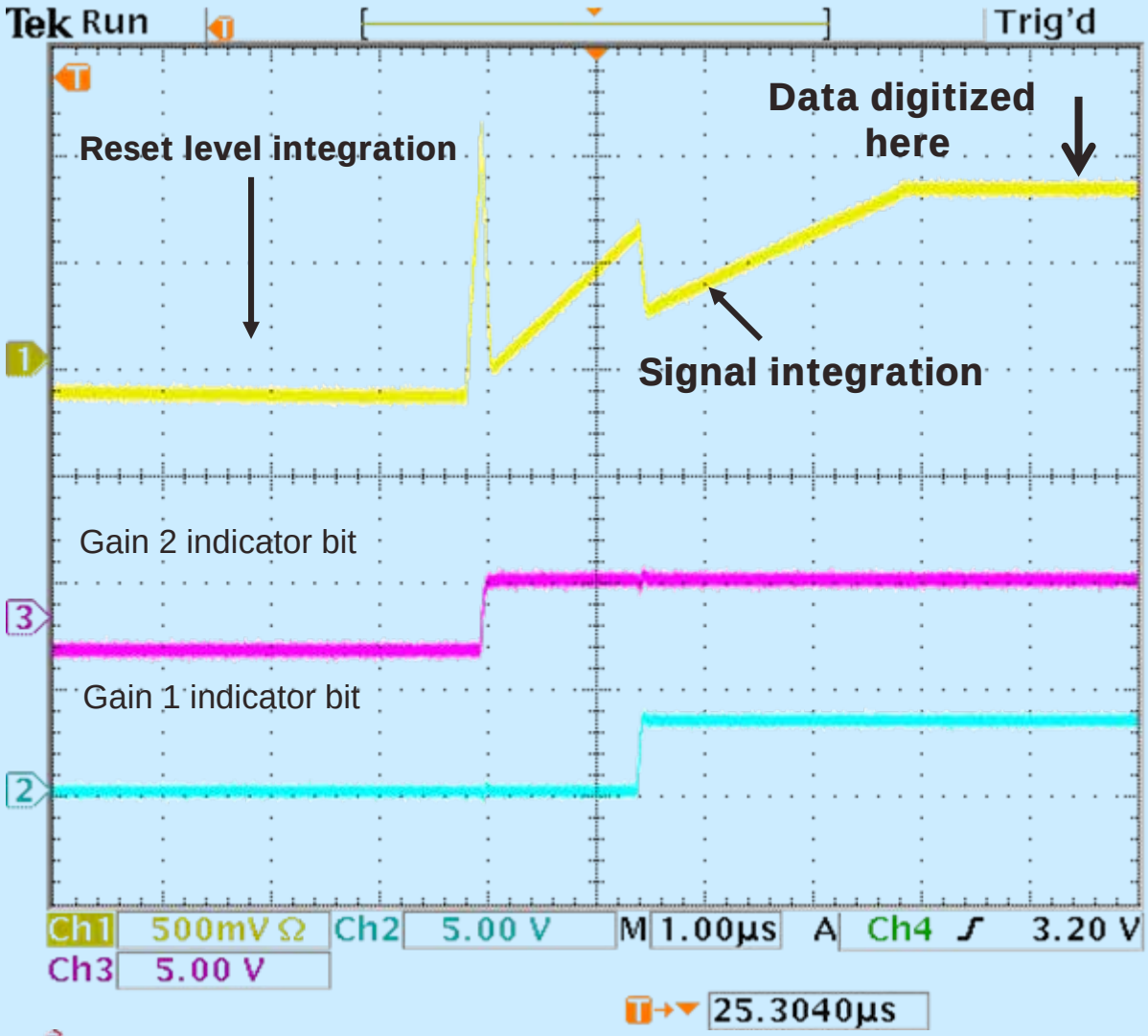


$\int V_R\, dt$ $\int (V_R - V_S) dt$

CCD Readout IC ("CRIC")



Full-scale signal in CRIC

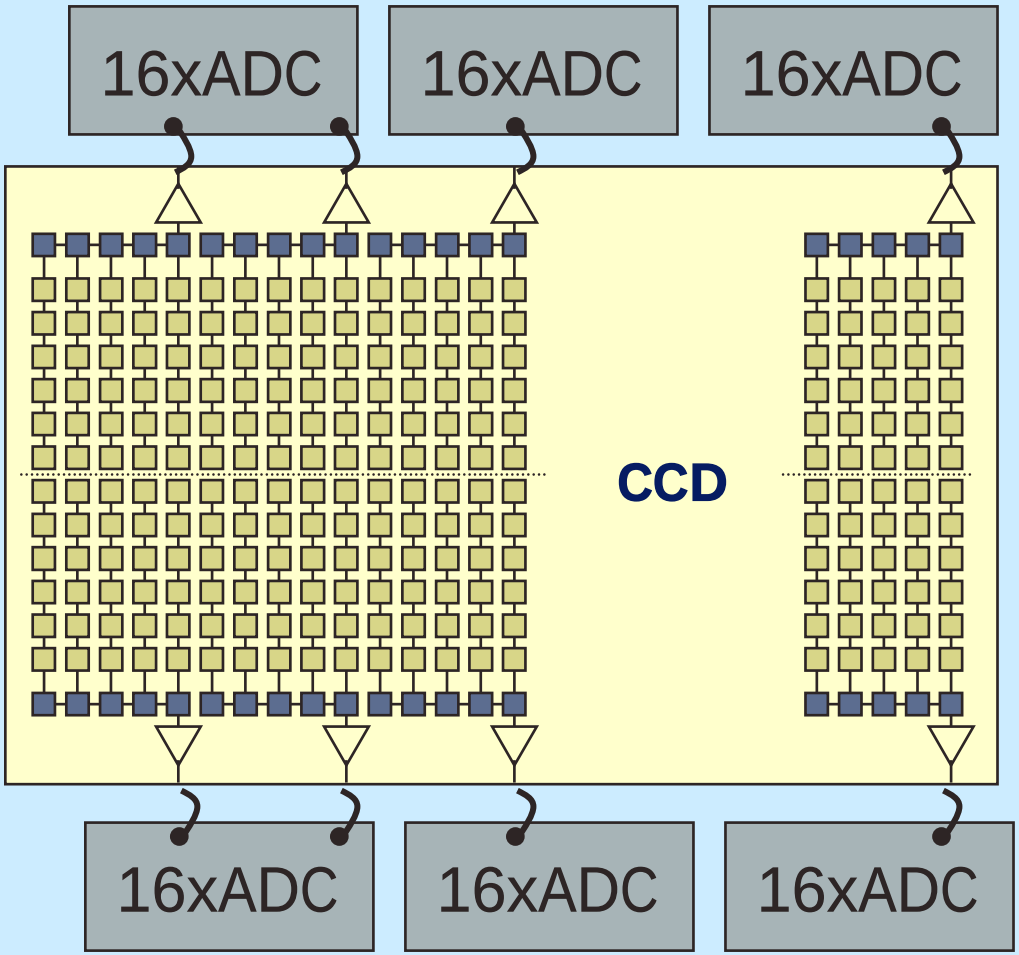


Measured Performance

- 3.6 µV/ADU ~ 1 e^-
- Noise ~2.2 e^- 300
- Noise ~1.9 e^- 140K
- INL <2 bits max
- DNL << 1 bit
- Crosstalk < 1 ADU
  (one channel at zero, adjacent full scale)
- 15 mW/channel

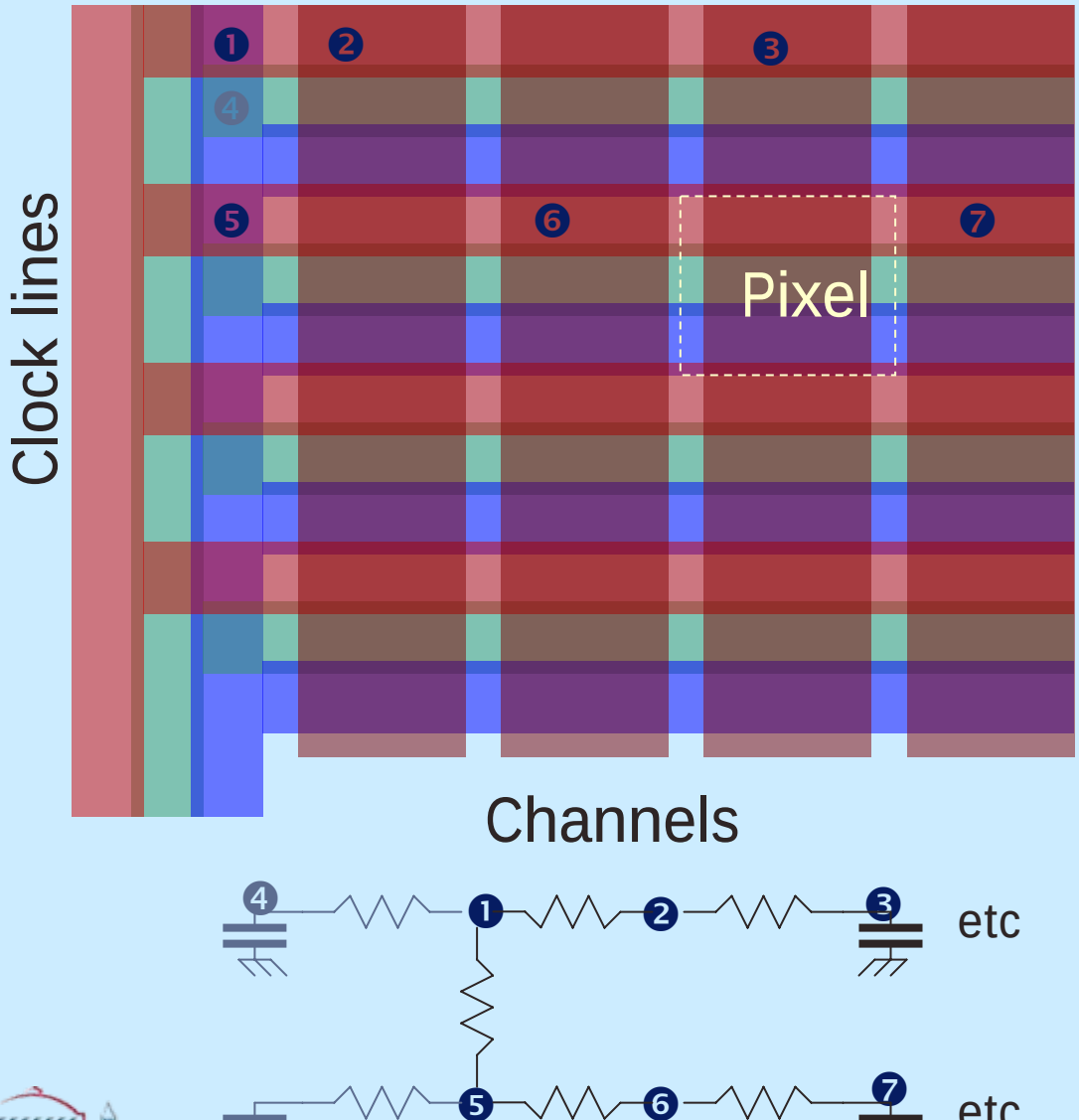
On spec

FCCD Plan



- Complete demonstrator camera
- LBNL thick CCD
  - *visible light + phosphor*
  - *x-rays*
  - *low energy electrons*
- Commercializeable
- Phosphor development

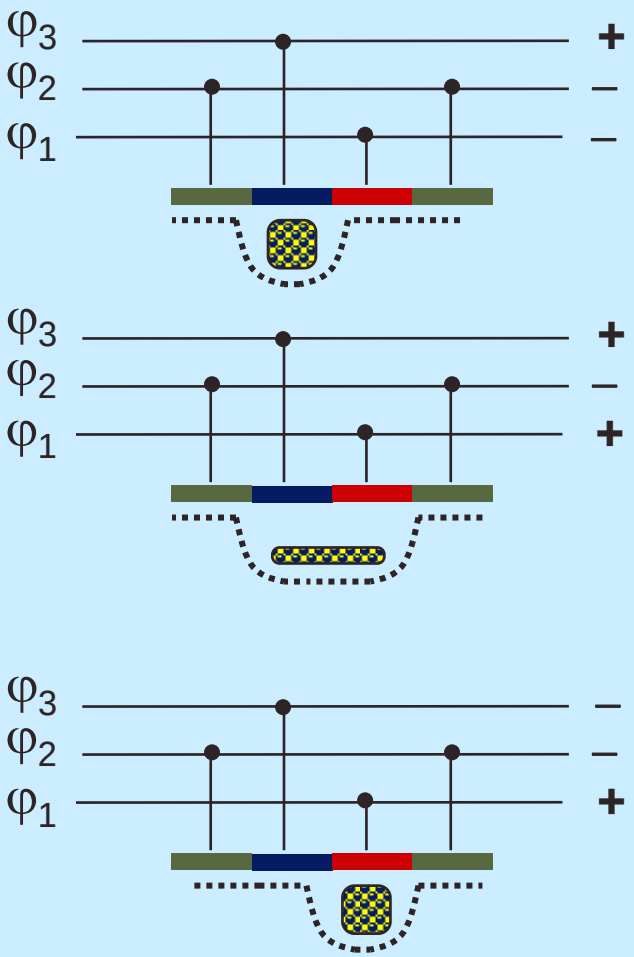
In general – what is needed to make CCDs fast?



- Poly gates are resistive (1000 x metal)
- To 1st order, distributed network of $R_{POLY}xC_{OVERALP}$ dominates speed of clock propagation
- Metal strapping needed for high speed
  - *opaque for front illumination*
  - *topological considerations*

Speed Limit

Ultimate limitation is CTI (1 – CTE) vs speed



Charge transfer:

$$\frac{\partial n}{\partial t} = \mu_{Si}\left(\frac{q}{C}\frac{\partial}{\partial x}\left[n\frac{\partial n}{\partial x}\right] - \frac{\partial}{\partial x}\left[n\frac{\partial V_c}{\partial x}\right] + \frac{kT}{q}\frac{\partial^2 n}{\partial x^2}\right)$$

Self-induced drift (concentration gradient of charge) — **Drift due to electrode fringe field** — **Thermal diffusion**

Time constants all $\propto L^2 C_{EFF}$

Typically ns or sub-ns, but

CTE	Time Constants
99.%	4.6
99.9%	6.9
99.99%	9.2
99.999%	11.5
99.9999%	13.8

Conclusions (1)

- Conflicting process requirements for CCD and CMOS imagers ⇒ *both* will fill important roles
  - *Could combine the two, but there is no commercial driver*
  - *Lab-foundry developments of CMOS on CCD, but …*
- CCDs will continue to be the best for max(area, pixels, dynamic range, speed)
  - *Our community can push that*
- Development area #1 – speed (combination of micro-electronics and CCD optimization)
- Development area #2 – why just silicon?
  - *Ge CCD – spectroscopy, x-rays*

- Improving CCDs and the ubiquitous detector maximizes dBang/d$
  - *Provided it is done in such a way as to benefit the whole community*

Conclusions (2)

(not just for CCDs – more general)

- A straightforward sophisticated detector (a 'simple' custom sensor with a 'simple' custom readout chip) ~ 8-10 FTEyr and needs 2-3 years to complete
- Specific detector developments should be run as a project
- R&D base support is needed at a relatively modest level

- Projects need to address community access
  - *Commercialize if possible – often difficult*
  - *If labs build and support instruments then*
    - *Need a way to support that ($)*
    - *Other labs need to sign up early – 10 at once ≠ one 10 times*