# Formats of LL1 Data from FEMs

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**Section 1.** Discussion of L1 data on fiber - format of the table describes the input/outputs of the mux/demux of the 20-bit data word. (Text of November 18, 1997, revision by FW)

**Section 2.** Additional Information for FEM to LL1 data connections - specifications for the G-link transmitter circuit. (Text of December 16, 1998, provided by HS)

## Section 1.

At the Online Meeting at BNL in September, 1996, formats for the data transfer from FEMs to LL1s were presented and discussed. I was asked to repeat this at the January, 1997, Online meeting at BNL, thus I produced a report that included some other L1 data flow information. This second report, dated January 6, 1997, called "Data Formats from FEMs to Level-1" was placed on the PHENIX L1 web site. The current revision deals only with the formats (with the Muon ID no longer a "tbd") and the so-called "Al" bit. In January, 1997, the new name "Al" was chosen to replace the short-lived idea associated with the bit called "Sy" in the September 30, 1996, writeup. More than its name changed, since the whole concept of how we plan to do alignment has changed since September 30, 1996, which calls for an updated explanation of the "Al" bit.

Describing the "Al" bit is the prime reason for the current rewrite. A second reason is that L1 just learned that the anticipated mux 4 for the Muon ID needs to be replaced by a mux 6 in order to transmit 96 bits on each of 80 fiber-optic cables (40 per endcap) from Muon ID FEMs to LL1. Therefore the appended table has been updated again. [Since the table aimed to be a (readable) one-page transparency, extreme brevity was necessary. The few additional paragraphs of text below expand on a few topics (especially "Al").

The various LL1 subsystems all receive data from the FEMs at each beam crossing, thus at the basic pipeline rate of 9.4 MHz. In order to accomplish this, it is necessary to mux the data. We need to do a mux x6 for the EMCal, since there are 117 (3x36+8+1) data bits plus one “Al” (for Alignment) bit, which we propose to do as 6 20-bit words. We also want to use the same word size of 20 bits for all FEM-to-LL1 data transfers, thus for most of the rest of the subsystems, we will use a mux x4 of 20-bit words. However, the Muon ID also needs mux 6 for its 96 bits per link and the “Al” bit. The 96 bits will be sent as 6 20-bit words. As shown in the updated table, for each 20 bits, the first (least significant) 16 bits will be data bits, followed by 4 empty bits (except for the sixth word, which will have 3 empty bits and the “Al” bit as the last bit - bit number 119).

Details of what constitutes the LL1 data from each subsystem can be found in the L1 writeups on the PHENIX L1 web site. Most have not changed since CDR and uCDR days, but two are new and are described here. A “Cosmic Muon Trigger” bit is produced when 5 2x2 sums each register an energy in excess of a Cosmic Muon Threshold of about 40 MeV. (Since there are 36 such 2x2 sums to an EMCal FEM, this requires that any 5 of the 36 are above this threshold.) The EMCal LL1 algorithm can use these sums to determine whether to issue a one-bit EMCal Cosmic Hit trigger. The EMCal LL1 logic will incorporate a LUT (Look-up-Table) with a one-bit Sector Cosmic Hit input from each of the 8 sectors. The LUT can be programmed to form an exclusive OR (so that the EMCal Cosmic Hit will be true if one and only one EMCal sector received such a hit) or it can be programmed for other choices. Also input into this LUT are the 4 bits (one per granule) of “FEM Unreliable” in order to disable an EMCal Cosmic Hit when any of the 4 granules have its FEMs in a unreliable state (such as when integrators are being reset). This is one example of a general feature of all LL1 systems - the “FEM Unreliable” bit will be used to zero any sum produced by the algorithm to avoid having an unreliable sum being input into GL1 and thus leading to a false trigger accept due to the value of an unreliable sum.

The “Al” bit is included as the last bit (bit number 79 for mux x4 and bit number 119 for mux x6) of all FEM-to-LL1 data formats. This “Al” bit is an input bit that will be used on each LL1 board to check time alignment of the data coming from the FEMs to each LL1 board. Usually the “Al” bit is in its “off” state (which will probably be low or “0”). For a single beam crossing, such as a fiducial marker for RHIC, selected by Timing and Control, the Timing Module for each granule can turn the “Al” bit “on” (probably high or “1”) and deliver it to all FEMs in that granule. Although “Al” is thus granule specific, to be effective for PHENIX as a whole, each granule needs to receive the same “Al” bit an any beam crossing. If every FEM gets the “Al” bit at the same beam crossing, then this bit can be used by L1 to verify beam-crossing alignment of the data sent to each LL1 system by the associated “participant” FEMs (i.e., those who provide data for a LL1 algorithm). (There are 12 LL1 participant granules, leaving 20 non-LL1 or “spectator” granules of the 32-granule GL1 design.)

Since each LL1 system also gets an “Al” bit directly from the Timing Module for each granule in that LL1 system, L1 can use these bits in two ways. First, on the LL1 Brd-1s (the LL1 9U board connected to the L1 fiber receiver transition board) to perform a logical AND of all the fiber links on that Brd-1. This logical AND is passed along to the Brd-2 of that LL1 system to do the next steps of a logical AND tree that tells if all granules have their FEMs aligned to the same beam crossing. This happens for 6 LL1 subsystems that together get input from the 12 participant granules. Then the second way is that these

ANDed "Al" bits are used in GL1 to check if all of the 6 LL1 subsystems (thus all 12 granules) are aligned with each other and with GL1, who gets its "Al" bit directly from the L1 Timing Module. (Note that GL1 is a special granule: it is a spectator since it gives no input to any of the LL1 algorithms, but, unlike any other granule, it does not belong to any partition because it gets an accept when any partition gets an accept, making its accept the equivalent of a logical OR of the 31 granule accepts of the other 31 granules.) If all is aligned, the end of the 12-granule-plus-GL1 AND tree will have its "Al" bit high. If not, the final "Al" bit will be low. and then diagnostics are in order. This final "Al" bit is a status bit in a status word in the accepted-event data stream that L1 sends to the L1DD (L1 Data Distributor). For diagnostic purposes at LL1, the individual "Al" bits will be stored in VME-accessible registers so that the VME link can be used to find out which FEM (or FEMs) were out Table of Formats of 20-bit data words from FEMs to LL1s of alignment. Discussion of the VME diagnostics is beyond the scope of the current writeup.

## Section 2.

The FEM to LL1 data link operates fully synchronously at either 4 times beam crossing rate, or 6 times beam crossing rate. Incorporated into the mux/demux logic for this link is a correlation circuit whose function is to maintain frame lock, thus insuring that for each group of 4 or 6 frames, all members of the group belong to a single beam crossing, rather than two adjacent beam crossings. In order for this circuit to operate properly, the following connections must be made to the G-link transmitter circuit:

1. CAV*, pin 69 should be de-asserted (tied high).

2. DIV1 and DIV0, pins 20 and 19 respectively, should be tied low to invoke the 700 to 1800 megabit/sec bandwidth.

3. DAV*, pin 70, and ED, pin 67, should both be asserted (DAV* held low and ED held high) begining with the first data to be transmitted. Even then, the frame correlation circuit mentioned above will require 4 full frames to lock, so the data sent during these frames will be lost. However, once lock is achieved, the circuit should remain locked for the duration of the data run.

4. The following signals should all be tied low: EHCLKSEL, pin 78, HCLKON, pin 10, LOOPEN, pin 16, MDFSEL, pin 74.

5. M20SEL, pin 30, must be tied high to invoke the 20-bit data mode.

6. FF (Fill Frame select), pin 68 should be asserted (tied high) to invoke FF1a or FF1b (depending on line balance).

7. FLAGSEL, pin 71, must be tied high to enable the FLAG bit.

8. FLAG, pin 60: This pin is the input bit for the framing information. It should be driven high when the data for the first frame of the 4 or 6 frame group, then dropped low for the remaing frames. If you are using the MUX circuits designed at Ames Lab, this function is already implemented in the FPGAs.

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Table of Formats of 20-bit data words from FEMs to LL1s       updated 1-12-98

Legend: "mt" means empty for the bit showing mt
        "Al" is a "Aligned" bit - the last (most significant) bit for any mux
        "1/2 FADC" means lower 4 bits of EMCal's 8-bit FADC on each FEM
        "2/2 FADC" means upper 4 bits of EMCal's 8-bit FADC on each FEM
        "Co" means the "Cosmic Muon Trigger" bit for and EMCal FEM
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        Gran-           FEM Tx     Format of 20-bit data words from FEM to LL1
        ules   FEMs    to LL1s      0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
                                     0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9
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  BBC    1       1     16 @ mux 4   <-------01------><-------05------>mtmtmtmt
                        (8 8-bit    <-------02------><-------06------>mtmtmtmt
                       words, 1 Al  <-------03------><-------07------>mtmtmtmt
                       bit & 15 mt  <-------04 -----><-------08------>mtmtmtAl
                      bits per FEM)

  MVD    2     136     12 @ mux 4   <----- 01 -----><----- 02 ----->mtmtmtmt
                        (8 8-bit    <----- 03 -----><----- 04 ----->mtmtmtmt
                       words, 1 Al  <----- 05 -----><----- 06 ----->mtmtmtmt
                       bit & 15 mt  <----- 07 -----><----- 08 ----->mtmtmtAl
                      bits per FEM)

 PbSc    3     108     108 @ mux 6  <------------------ Photon-1 36 bits ----
                        (3 36-bit   -------------------------------->1/2 FADC
                        words + 2   <------------------ Photon-2 36 bits ----
                       4-bit words, -------------------------------->2/2 FADC
                       1 Co bit, 1  <------------------ Electron 36 bits ----
                      Al bit & 2 mt -------------------------------->ComtmtAl
                      bits per FEM)

 PbGl    1      64      64 @ mux 6  <------------------ Photon-1 36 bits ----
                        (3 36-bit   -------------------------------->1/2 FADC
                        words + 2   <------------------ Photon-2 36 bits ----
                       4-bit words, -------------------------------->2/2 FADC
                       1 Co bit, 1  <------------------ Electron 36 bits ----
                      Al bit & 2 mt -------------------------------->ComtmtAl
                      bits per FEM)

 RICH    2      32     32 @ mux 4   <----- 01 -----><----- 02 ----->mtmtmtmt
                        (8 8-bit    <----- 03 -----><----- 04 ----->mtmtmtmt
                       words, 1 Al  <----- 05 -----><----- 06 ----->mtmtmtmt
                       bit & 15 mt  <----- 07 -----><----- 08------>mtmtmtAl
                      bits per FEM)

  TOF    1      32     16 @ mux 4   <--------------- 01 ------------->mtmtmtmt
                       (4 16-bit    <--------------- 02 ------------->mtmtmtmt
                       words, 1 Al  <--------------- 03 ------------->mtmtmtmt
                       bit & 15 mt  <--------------- 04 ------------->mtmtmtAl
                      bits per FEM)

 MuID    2      80     80 @ mux 6   <--------------- 01 ------------->mtmtmtmt
                       (6 16-bit    <--------------- 02 ------------->mtmtmtmt
                       words, 1 Al  <--------------- 03 ------------->mtmtmtmt
                       bit & 23 mt  <--------------- 04 ------------->mtmtmtmt
                      bits per FEM) <--------------- 05 ------------->mtmtmtmt
                                    <--------------- 06 ------------->mtmtmtAl
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Example: Data format for TOF has bits 0-79 alocated as described above, with
64 hit pattern bits, in 4 groups of 16, as Data(0)-Data(15), Data(20)-Data(35),
Data(40)-Data(55), and Data(60)-Data(75). The "mt" bits are Data(16)-Data(19),
Data(36)-Data(39), Data(56)-Data(59), Data(76)-Data(78). "Al" bit is Data(79).
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