D0 Upgrade Electronics

D0Note 3551

CTT TDR

Technical Design Report

for the

Upgrade L1/L2 Tracking Trigger

Including

Central Fiber Tracker,
Central Preshower Detector,
Forward Preshower Detector,
Forward Proton Detector

Version 5

by CTT Group*

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1. Introduction

1.1 About the Document

1.1.1 Scope of the Document

This document is the technical design report for the front end electronics and trigger for four of the upgrade detectors, the Central Fiber Tracker, CFT, the Central Preshower, CPS, the Forward Preshower, FPS, and the Forward Proton Detector, FPD. Three of these detectors share the same Front End, FE, location the VLPC cassettes and all share the same hardware. The electronics for the four detectors are grouped into four systems that are not arranged along detector boundaries.

The FE and trigger systems included in this document are:

CFT/CPS Trigger	The detector inputs for this system are the Central Fiber Tracker, CFT, Axial fibers and the Central Preshower, CPS, Axial strips. This system forms the L1 Fiber Tracker Trigger and supports the L2 Central Fiber Tracker preprocessor, CFTpp, the proposed Silicon Tracking Trigger preprocessor, STTpp, and the proposed Preshower preprocessor, PSpp.
CFT Stereo	The detector inputs for this system are the Central Fiber Tracker Stereo fibers. This is a FE system only and does not support any trigger.
PS Trigger	The detector inputs for this system are all of the Forward Preshower detector strips and the Central Preshower Stereo strips. The FPS strips are used to form the proposed L1 Forward Preshower Trigger. The FPS and CPS stereo strips are used for the proposed L2 Preshower Trigger preprocessor, PSpp.
FPD Trigger	The detector inputs for this system are the proposed Forward Proton Detector. These inputs would be used to form the proposed L1 Forward Proton Detector Trigger and supports the proposed L2 Forward Proton Detector preprocessor, FPDpp.

The first of these systems, the CFT/CPS Trigger, is the largest system and has the most mature design. This document will describe that system first and in detail. For the other systems this document will point out the shared features and describe in detail only the unique features of each system.

Note that, for some of the systems, parts of the design presented in this document are not approved projects. For the purposes of this document they are treated as if approved and the complete system designs are presented. It is expected that those parts not approved can later be omitted with minimal impact on the overall operation of the as-built system.

1.1.2 Structure of the Document

This document has three mayor roles to fulfill:

1) It supplies a functional description of each of the five systems and its interaction with other elements of the upgrade detector.
2) It supplies a complete as possible description of the hardware and/or firmware already designed.
3) It supplies a complete as possible design criteria to follow in the design of elements not yet fully designed

This document is divided into five sections. The first addresses the environment and features shared by all the systems and the next sections each describe one of the above four systems. Each system is at the '0.' level of the document headings. Within each system one or more sub-systems are described, which are at the '0.0' level of the headings. For each of these subsystems a brief functional description and detailed system architecture description are given, which is at the '0.0.0' level of the headings. The functional description is intended to give the major functionality of each part with a general audience in mind. The system architecture description is intended to detail the system at the expert level. This part of the document is aimed at those designing and building the not yet finished parts of the system. And by those who install and maintain the systems as a basic reference document.

This document also points which part of the described systems are, at the time of the writing, either built, designed, or simply specified. The document is followed by several appendixes, which give design details on specific aspects of the systems.

1.1.3 Glossary of Abbreviations

Most of the abbreviations used in this note and their meanings are listed here.

CFT	Central Fiber Tracker
CTT	Central Tracking Trigger
DAQ	Data Acquisition System
FPS	Forward PreShower Detector
CPS	Central PreShower Detector
FE	Front End board
CN	Concentrator System
GS	Geographical Sector

SCL Serial Command Link
TCL Tracker Command Link
L1(2,3) Level 1(2,3) Trigger

1.2 CTT System Overview

The FE and Trigger electronics for the four systems share four basic sub-systems. The sub-systems and the board types in each are:

CTT_FE	Analog FE System	
CTT_FE		Analog FE board
CTT_DG	Digital FE System	
CTT_DG		Digital FE board
CTT_DCC		Digital-Crate Controller board
CTT_CN	Concentrator System	
CTT_RC		Receiver board
CTT_CN		Concentrator board
CTT_TM	Trigger Manager System (from the L1 Muon system)	
CTT_TM		Trigger Manager board
CTT_…		The many other boards from the L1 Muon system

The functionality of each sub-system is:

CTT_FE

Discriminate the analog signals from the VLPC with the SIFT chip
Sort, buffer and transmit the discriminated signals to the CTT_DG
Digitize the analog signals with the SVX2e, an eight bit ADC
Supply an L3 readout for the digitized signals
Supply an L3 readout for the ADC signals
Supply the Bias voltage for the VLPC chips in each cassette and monitor the current drawn
Supply temperature monitoring for the VLPC cassette and control local heaters to trim the VLPC temperatures within the cassette

CTT_DG

Use the discriminated signals to form tracks/clusters
Count the number of tracks/clusters in several categories and send that count to the CTT_TM via the CTT_CN for an L1 trigger decision
Pipeline the tracks/clusters for output to L2pp
Transmit via the CTT_CN a list of tracks/clusters to various L2pp

CTT_CN

Receive the L1 sums from several CTT_DG boards
Form those L1 sums into sums by Octant
Transmit the octant sums to the CTT_TM
Transmit copies of the input and output data to the L3 readout
Receive the L2 track/cluster lists from several CTT_DG boards

Concatenate the lists from several CTT_DG boards
Transmit the resulting track/cluster lists to various L2pp matching the phi segmentation for that L2pp

CTT_TM

Receive the L1 sums from several CTT_CN boards
Make a L1 trigger decision based upon its inputs and send the results via the AND/OR network to the trigger framework

The major sub-systems of the CTT are shown in figure 1.1. The different detector sub-systems are arrayed vertically and the different hardware types are arrayed horizontally. The FE hardware is represented by the boxes in the left hand column. The CFT Axial and CPS Axial integrated into the same set of FE hardware and form the CFT/CPS Trigger System. The FPS and CPS Stereo share FE hardware design but are in different crates. The CFT Stereo and the proposed FPD are in the same hardware sub-system but in different crates as well.

The second column from the left represents the CN hardware type. There are three of these, one for each of the detector sub-systems. The third column, which is made up of the staggered row of smaller boxes, represents the L1 trigger and L2pp hardware. The same hardware is used within each of the L1 boxes and is the L1 hardware developed for the L1 MUON trigger. While this hardware is supplied by our MUON colleges, developing the firmware and defining the system installation is part of this project. The other boxes in the third column labeled L2 represent the L2pp. The L2pp are outside the scope of this project. However, the data interface needs to be defined by this note and others. The right hand column represents the L3 readout system geographical sector, GS, crates. Those GS connected to the FE and CN hardware are composed of the same hardware as the silicon detector system FE. Those GS connceted to the L1 boxes are supplied by the Muon group. In both cases the L3 hardware is supplied to this project and the system definition and installation is part of this project.

1.2.1 CTT_FE, Analog FE System and Board

The FE analog boards support the VLPC cassettes on which they are mounted, process the analog signals from the VLPC channels, and supply that data for readout to the L1, L2 and L3 systems.

Visible Light Photon Counters, VLPC, are used to convert the light produced in both scintillating fibers as for the CFT and scintillating strips as for the CPS and FPS into electronic signals. Each VLPC chip surface has a two by four array of 1mm-diameter photosensitive areas. This light sensitive device operates at from 6 to 14 degrees Kelvin with a bias voltage of -6.5 volts. The cryogenic operating temperatures allow a very high quantum efficiency, in the range of 80%, but present several challenges. The VLPC chips are mounted in groups of eight into modules each of which has 64 channels. Eight modules are mounted in a single cassette. Two FE boards service each cassette. Each 1024 channel cassettes is inserted from the top into a special cryostat and the tops of the cassette assemblies when in place cryostat form an electronics crate. This crate contains special back planes and holds the FE electronics boards, CTT_FE. For space reasons, 1/2 of the FE boards (every other board) has its components mounted on the left-hand side of the board, when viewed from the front of the crate. The other half have their components mounted on the right hand side. Therefore, each type of FE board has two 'handedness' versions.

The VLPD bias is generated and monitored separately for each of the eight modules. Each VLPC module has a common bias supply and each chip has a single bias-supply line but each of its eight pixels has its own bias-return line. Please see figure 1.2 for a circuit schematic showing four representative VLPC channels. This single bias return line doubles as the signal line from the VLPC. The bias supply is -6.5V and the return is at 0V. A dominant failure mode of a VLPC pixel is for the output to latch up and draw a large current. This excess current can warm the entire chip and cause that entire chip to fail. To guard against this a current restricting resister is placed in series with the bias return on the FE board. After this resister, all the bias returns are tied together.

The monitoring of the cassette temperature and the power for heaters for each group of 64 channels is also located on the FE boards. These services are only routed on the right hand boards.

1.2.1.1 MCM

The expected mean signal level from the VLPC can vary from as low as 30,000 electrons per photoelectron to as high as 50,000. The longest charge collection time is about 70ns. The number of photoelectrons varies widely from roughly 10 at the center of the fiber tracker to 1500 for the preshower detectors. The signal needs to be both digitized and discriminated. The fiber tracker needs only a few bit ADC while the pre shower detectors need 11 bits because of their larger dynamic range and the discriminator threshold needs to be programmable over a factor of 10 range. Because of radiation damage expected during the running and downward fluctuations of the signals, the minimum discriminator threshold is 4 fC (24,000 electrons) for the fiber tracker while the maximum is around 50 fC for the preshower. The signal processor must also provide for up to a 32 crossing latency for forming the L1 trigger. Also 512 channels are needed per circuit board. All of these criteria are met by combining the preexisting SVX2e chip with a special ASIC designed for this project (the SIFT chip) in an MCM.

Each MCM has 72 input channels that are divided into two groups of 36. Figure 1.3 shows a block diagram for an MCM. Each MCM is a single leaded package of 2" by 3.5". Each half of the MCM has a separately settable gain range for the discriminator and charge transfer to the SVX. Each half also has a separate analog-voltage input, which sets the discriminator threshold. All the SVX I/O pads, (except the inputs) are routed directly to I/O pins on the MCM.

Each SIFT chip has 18 useable channels. Four SIFT chips and one SVX IIe are packaged together in a multichip module (MCM) where only 72 of the 128 channels in the SVX IIe are used. There are 8 MCMs on each board and all the SVX chips on each board are connected together into one readout string (the equivalent of one high density interconnect in the silicon system) and read out with a D0 sequencer module.

1.2.1.1.1 The SIFT Chip and Analog Input Circuits

The VLPC output signal is superimposed on the bias return. Therefore, the input into the MCMs must be AC coupled to the bias return and this capacitor is inserted in series on the input to the MCM. Figure 1.2 shows a the basic circuit for four representative channels. On the FE board each group of 64 channels is connected electrically as shown. That is each group of 64 channels, 8 VLPC chips, shares a common bias source located on the FE board. This common bias source is routed down to the VLPC chips over a special cable called the Flex Cable. This cable must deliver the bias current and transmit the VLPC signal with a minimum of loss. At the same time it must minimize the heat loss within the cassette. Too much heat loss on this cable, which goes from room temperature at the FE board to 5 to 10 degrees Kelvin at the chip end has two undesired effects. First, a larger heat load would require extra refrigeration for the liquid Helium, LH, cryogenic system, which is shared with the super-conducting solenoid. Second, excessive heat load over the cable would cause the LH to boil at the VLPC end. A phenomena which would lead to uncontrollable temperature fluctuations at the cold end.

The Flex cable is a two layer circuit laid out on Kapton with very small cross section copper traces on the top and bottom. The top layer carries the 64 traces that are the combined signal and bias return. A combination ground, bias supply, trace is located between each signal trace pair. The bottom has a mesh ground plane, which consists of bias supply / signal return traces along the length of the cable and directly under each signal trace, and a ladder of periodic intersecting transverse traces. Also at some of the junctions of the longitudinal and transverse traces vias are located, which connect the bottom side ground to the guard traces on the upper surface. The combination of small traces and small vias all on a Kapton substrate pushes the state of the art.

Once on the FE board the combination signal traces, bias returns, are routed to the MCM inputs and the bias return tap. The signal is extracted from the bias return with a series capacitor that AC couples the MCM input. The DC bias return is then routed through a large resistor coupled to the other return currents and returned to the bias supply. For the preshower FE circuits a larger dynamic range on the ADC and a second discriminator are required. For those FE boards the single capacitor in series is replaced with a capacitive divider. This divider has three capacitors in parallel. Two of them couple part of the signal to two independent MCM channels and the third shunts most of the input signal to analog ground. A simple schematic of the capacitive divider is shown in figure 1.4.

The input signals to the MCM are routed directly to four SIFT chips. The SIFT chips serve two functions. First they supply a fast discriminated signal for use in the L1 trigger. Second, they have a higher bandwidth than the SVX chips and therefore allow for a shorter integration time than the SVX chips. As a consequence the SIFT and SVX combination located in an MCM is used for the CFT Stereo channels as well where no L1 trigger is planned.

The SIFT chip is a custom ASIC designed for this application. This design was coordinated by some of us from the University of California at Davis. The design was done by an independent design firm, Adapt Designs. Most of the early prototype testing was done at UC Davis. Most of the later testing including all of the testing in combination with the SVX chip was conducted at Fermilab. The chip is to be fabricated in 0.8 micron three metal process by Hewlet Packard in the first two months of 1999. HP through the MOSIS chip service will fabricate 30 wafers that will be tested and then diced into some 15,500 chips for placement into 2200 MCM's.

Each SIFT chip has twenty channels laid out with a 100 micron pitch. The channels at either end, channels 1 and 20 are not used and have both their input and outputs grounded. The eighteen channels each have an input and two output. One output is the discriminator output and is a +5V logic level. This level is raised during a cycle when the input signal passes the level of the discriminator threshold and is held in a flip flop until reset at the end of the cycle. The extension of the output is necessary to facilitate the latching of the outputs into the first stage of the trigger logic. Figure 1.5 shows a simple schematic of a SIFT chip.

The ADC is the SVX IIe chip, which was developed for the silicon detector. It has an 8 bit ADC with programmable gain so that the full scale charge ranges from 25 fC to 150 fC. The fastest rise time is 90ns (42ns charge collection time for 132ns crossing intervals). This does not meet all the requirements mentioned above. To meet these demands, another custom chip (called SIFT) which fits in front of the SVX IIe was designed. It has a selectable gain of 0.25 or 0.5 and a discriminator with a variable threshold of either 3 to 50 fC. Both the discriminator range and gain are selectable on the chip. The SIFT charge acquisition time is 70ns.

1.2.1.1.2 The SVX Chip and L3 Readout Support

The 11 bit ADC requirement is met by using 2 SIFT-SVX channels for each of the preshower channels. A 3 way capacitor charge divider (figure n) is used so that one channel will get one tenth of the charge of the other giving slightly more than 11 bits of range. The third capacitor shunts the excess charge to ground so that the large amplitude signals are within the range of the SIFT and SVX IIe. For example, by shunting 90% of the charge, the 5000 fC preshower signal will is reduced to 500 fC at the SIFT input. If the SIFT has a gain of 1/4, 125 fC is sent to the SVX IIe which is well within its range. The 300 fC discriminator threshold is on the input charge so this signal is above the highest discriminator setting. At the other end of the scale, a few fC signal is reduced by only a factor of 2 which is also well within the range of the SVX IIe.

1.2.1.1.3 Charge Pileup

The preamplifier in the SVX chip is not reset every crossing since it needs a large fraction of a microsecond to settle. Therefore it is only reset during a time when beam crossings are not seen by the detector. Initially there will be three super-bunches in the Tevatron and eventually there may be only one. Between preamplifier resets it sees all of the charge from all particles traversing a given scintillation fiber. The average amount of charge into the SVX per turn can be calculated. This value is important because the digitized output of the SVX is the difference of the integrated charge after a pipeline stage minus the integrated charge before that stage. The SVX preamplifier saturates at about 450 fC and once it has reached saturation all subsequent pipeline stages will digitize to zero, the pedestal value. Also as the preamplifier approaches saturation a single hit may push the preamplifier into saturation resulting in a truncated digitized value.

Luninosity	20	E+31		
Bunches	36		108	
Ave. # of Int	5.13		1.71	
Occupancy per interaction	8%		8%	*100tracks/80/16*
pe per hit	15		15	
Charge from VLPC	96	38 fC	96	13 fC
SIFT Gain	0.4	15 fC	0.4	5 fC
Crossings	36	554 fC	108	554 fC
	12	185 fC	36	185 fC

In the above table the average amount of charge into an SVX in the innermost layer is calculated. The table assumes that there are 100 tracks per interaction, each track deposits 15 photo electrons in the fiber, and that the VLPC gain is 40K. Then each track sends 96 fC of charge from the VLPC to the MCM and SVX. From the table it is clear that at the highest luminosity the SVX will need to be reset three times per turn. Only at 8 E+31, the luminosity at the end of run I, could the SVX be reset only once per crossing.

1.2.1.2 Exporting Data for Triggers

1.2.1.2.1 Data PLD Chips

1.2.1.2.2 LVDS Circuits

1.2.1.3 VLPC Bias Supply and Monitoring

1.2.1.4 VLPC Temperature Monitoring and Control

1.2.2 CTT_DG, Digital FE System

The digital FE system consists of Digital FE boards, DG, in a VME type crate along with a crate controller board. Each DG receives the discriminated signals from the FE board over a special lvds link. Each DG uses this input for form tracks for the CFT-DG or clusters for the FPS-DG. The number of tracks (clusters) is counted and sent to the L1, the tracks (clusters) are pipelined and sent to the L2. The outputs are not sent directly to the L1 nor L2 but are first sent to the Concentrator System, which is described below, and forwarded from there. In the case of the CFT-DG there is an additional link directly from the boards to the Muon L1. Each DG contains several large FPLD's which must be re-programmed after each power interruption. The interface to the HOST for this re_programming is made through the crate controller board. The crate controller board is a commercial VME board with a processor and a fast network link.

1.2.2.1 CTT_DG, Digital FE board

As listed in section 1.2 the Digtal FE board must:

Use the discriminated signals to form tracks/clusters,
Count the number of tracks/clusters in several categories and send that count to the CTT_TM via the CTT_CN for an L1 trigger decision,
Pipeline the tracks/clusters for output to L2pp, and
Transmit via the CTT_CN a list of tracks/clusters to various L2pp.

As the signals, called HITS, arrive on the DG board they are put onto several wide busses called the HIT busses. The HIT busses are routed to several large FPLD's, called TRACKING FPLD's; each of which is connected to all the lines of the busses. The HIT signals are time multiplexed on this bus in seven clock cycles per crossing, or 53MHz. In the TRACKING FPLD chips the HITS are formed into tracks for the CFT and clusters for the FPS and CPS. Each of the TRACKING FPLD's output a track or cluster LIST which is put onto a LIST bus dedicated to that FPLD. The several LIST busses are routed to a formatting FPLD which ….

1.2.2.2 CTT_DCC, Digital-Crate Controller board

1.2.3 CTT_CN, Concentrator System

1.2.3.1 CTT_RC, Receiver board

1.2.3.2 CTT_CN, Concentrator board

1.2.4 CTT_TM, Trigger Manager System

1.2.4.1 CTT_TM, Trigger Manager board

1.2.4.2 CTT_…, The many other boards from the L1 Muon system

1.3 Tracker Command Link, TCL

The D0 detector uses a set of Serial Command Links, SCL, to maintain coordination and synchronization between the various detector parts. Each SCL servers a single Geographical Sector, GS, of the detector. The CFT/CPS Trigger FE, is one GS. The CFT Stereo FE is another and the Preshower, which includes the Forward and Central Stereo, is a third. The command information and timing must be translated from the SCL to the FE hardware and the status information returned. The Silicon Detector readout constitutes several GS and also uses the same command system. This section describes the system command links for the tracking system called the Tracker Command Link, TCL.

1.3.1 System Overview

The major features of the TCL from the SCL to the FE and back are:

A single SCL is sent to the Sequencer Crate on the platform. This is a slave of a duplicate link sent to the corresponding VRB crate.

The SCL is landed in the Sequencer Controller Board. This is a dual board, it lands two SCL links and serves two GS.

The Controller board actively fans out selected SCL signals over the Sequencer crate back plane. Which of 20 slots receives each output is remotely selectable. Trace lengths on the controller board and back plane fix the phase delays between the 20 slots.

Each Sequencer board receives the signals from the controller and translates them into signals to control the SVX chip strings, the SIFT chips associated with each string, and the operations on the FE analog boards containing the strings.

Relevant SCL information is transferred from the analog FE board to the Digital board over the same LVDS links as the digital data.

Each FE board, analog and digital, may generate status information, which is sent back to the SCL. The information from each FE board is put onto a crate wide bus.

The information from each crate is returned to the Controller board which OR's the result to a single set of information.

The information from the Sequencer Controller board is returned to the VRB Controller board.

The VRB Controller board records for host computer retrieval whether the status information it received came from the link to the Sequencer or from within its own crate. It then sends the combined information back over the SCL. The passing of information back from the Sequencer at the VRB controller can be remotely disabled with a command from the host.

The TCL not only tells the system what to do but also when to do it. The 'absolute' timing of some commands relative to the beam crossing is critical, as is the relative timing within several groups of signals. The origin of the SCL is expected to be timed relative to beam crossing to fewer than 5ns and to maintain that accuracy over the course of the run period. This system is designed to control the timings at the FE boards at 2.5ns.

The overall timing of the GS is controlled remotely by delaying the SCL at its source. Controlling the relative path lengths to each FE board closely controls the timing within each GS. At each of the FE boards the start and duration of each of the many local clocks are controlled independently.

1.3.2 Sequencer Controller Board

The Sequencer Controller Board is a singlewide 9U VME style board mounted in the first slot of a Sequencer Crate. This board has two SCL receivers, 20 channels of timing and control output to the sequencer boards, 16 channels of status input from the FE crates, and 2 channels of status output for the VRB Controller.

Each board serves two GS by interfacing with two SCL links. These links are realized in optical fiber and the receivers are located on plug in daughter boards. After the daughter board has landed the SCL signals, several are routed to the mother board where they are translated to the NRZ protocol described below and transmitted over each of the 20 output channels. Each of these 20 channels is independent and can receive SCL commands from either of the two SCL inputs. Which of the 20 channels is linked to each of the two SCL is set and sensed remotely. At the back plane interface of the board are 20 sets of 4 traces. Each set of four traces is routed over the crate back plane to a single sequencer board slot.

For each channel, the 53 Mhz signal is converted into a signal pair, clock and clockbar, and sent over two of the four back plane lines. Other command signals are extracted from the SCL and coded into two separate protocols using a non-return-to-zero format. Each of these signals is sent over the back plane on the remaining two lines. The phase delay for all channels is controlled to be equal to better then 1ns from controller board to sequencer board with controlled path lengths on the controller board.

The 16 channels of status return are each 3 signals plus ground. Eight channels are wire OR'ed together and sent over each of the two status output channels. The grouping of the 16 channels down to 2 is built into the board.

1.3.3 Signals on the NRZ Back Plane Links

Four traces from the controller card to each pair of sequencer boards carry the differential 53 Mhz clock on two lines and a separate NRZ protocol bit sequence on each of the other two lines. Each of the NRZ protocol signals consists of a bit string of 7 bits. The first bit, the framing bit, must always be present, equal to 1, and is used to keep the decoding hardware in synchronization with the encoder. The next 5 bits carry information and the 7th and final bit encodes the parity of the preceding 6 bits. The signals on both lines use a non-return-to-zero protocol, NRZ. That is if two or more successive bits are all high, the signal stays high. The definitions of these 7 bits are listed in table 1. <u>The details of this may be modified during the sequencer board design</u>. The bits carried in each line are extracted in coincidence with the 53 MHz clock, stored, and executed at the start of the next framing bit.

Line 1 encodes the information for the SVX chip strings and is necessary for the silicon system readout as well. Line 1, bit 2 is the crossing bit and marks this crossing as having beam. In 132ns mode this bit is always present. During 396 running this bit is present only for every 3rd Framing bit and marks a crossing with beam. Line 1, bits 3 through 6 are used to encode 16 possible commands. This packing of commands into 4 bits maximizes the amount of information that can be sent. But only one of those commands can be sent each crossing. The bit coding for these 16 commands are defined elsewhere. Line 1 is sufficient for controlling the SVX chip strings.

Line 2 encodes the signals for the SIFT chips and the trigger and is necessary only for this system. It is not transmitted across the back plane for those systems where it is not needed. Line 2, bit 2 is a spare bit and Line 2, bit 3 marks a GS reset. Line 2, bit 4 marks the one gap each turn that is used as the synchronization gap. Crossing number 1 occurs within this gap. Line 2, bit 5 marks the first crossing of a turn. Line 2, bit 6 marks that a L1 accept has occurred.

1.3.4 Sequencer Card

Each sequencer board receives the NRZ signals and decodes them. It translates the information coded on line 1 into the command format expected by the SVX chip strings and the information coded on line 2 into the command format expected by the FE boards. If the line 2 signals are not present the sequencer board does not generate the signals in block type.

Each sequencer board has 4 output 50-conductor cables. Each of these cables is used to read out two strings of SVX chips.

1.3.5 Signals on 50-conductor Cables

The signals carried on the 50-conductor cable are shown in table xx. The FE uses the signals shown in block print exclusively. The SVX chip strings use the signals shown in italic print. Twenty-one signals connect to SVX chip string A and twenty-one to string B. The FE board uses the other 8.

1.3.6 FE Boards

Each 50-conductor cable is connected to the FE back plane and the signal routed to two FE boards. Therefore each FE crate has 8 cables which come from two adjacent sequencer boards. The 21 signals for SVX chip string A are routed to the LH board and those for string B to the RH board for each cassette. The 8 shared signals are bussed to the same pair of FE boards.

Listed below are the eight timing and command lines to each FE and concentrator board, along with a short explanation of their use and meaning.

Signals received by the FE boards

CROSS is the crossing signal, which is 53/7 MHz in 132ns mode and is 53/21 in 396ns mode.

/CROSS is the inverse of the CROSS signal.

SYNC_GAP is the Synchronization Gap marker. This signal goes high at the start of the synchronization gap and goes low at its end and is used to maintain synchronization of the fast serial links off the FE boards. In coincidence with the start of the SYNC_GP and the local 53 MHz clock, the fast links start sending control sequences. In coincidence with the end of the sync-gap and the clock they resume sending data.

1ST_CROSS is the first crossing of a turn marker. Each FE board keeps a count of the present crossing, 8 bits, and turn, 16 bits. The crossing count is reset with each 1^{ST}_CROSS and the turn count is incremented. The turn number is reset after a reset flag and if not reset within about 1.38 sec wraps around.

L1_ACCEPT is the L1 accept indicator. When this signal is received the FE switches from L1 process mode to L2 readout mode.

RESET is the Global Sector reset signal and is used to reset all parts of a GS at the same time. When it goes high each FE resets, when it returns to low each FE waits for the next 1st_cross marker and then resumes.

1.3.6.1 FE board Clocks

At each FE board the control signals are received and translated into local clocks. One set of clocks called the analog clocks are used by the SIFT chips and are time locked to the SVX clocks which come directly from the Sequencer. The other set of clocks called the digital clocks are used to control the flow of digital information on each FE board and the flow of information off each Fe board.

Each of the FE boards has 8 multiple-chip-modules, MCM, each of which contains one SVX chip and four SIFT chips. The clock and the control signals for the SVX chips are all generated in the sequencer board and transmitted to the FE board. Hardware on the FE board must generate the start time and duration of each of the SIFT clocks. This hardware generates two sets of analog clocks at the middle of the FE board. One set is routed to the rear of the board and the other to the front. This arrangement minimizes the on board trace length for any of these clock signals.

The SIFT can cycle at 132ns or 396ns depending on the beam crossing frequency. Which cycle time is used is set at each FE board by the clock generation hardware. At either of these cycle lengths it operates in three possible modes.

RESET	a special cycle(s) with longer preamp and discriminator reset times,
CLAMP	a special cycle executed in coincidence with an SVX preamp reset, which is used to match the SIFT output level with the SVX input level,
ACQR	the normal or acquire mode used for data taking.

The five SIFT clocks are;

PRST	reset the SIFT preamp,
DRST	reset the discriminator,
S/H	switch the analog signal onto the output capacitor,
READ	switch the output capacitor onto the output line for the SVX to sample, and
PCLMP	clamp the baseline of the analog output to the input level of the SVX channel.
LATCH	Latch V-Out within the SIFTs

Each SIFT cycle starts with the CROSS signal. If the RESET signal is high a SIFT RESET cycle is executed. If the CLAMP signal is high a SIFT CLAMP cycle is executed. For all other cases an ACQR cycle is executed with each Crossing signal.

The nine digital clocks are;

D_READ	Latch the V-Outs from the SIFTs into the PLD's
SEND(4)	Send data across the BP and out of home PLD's

STORE(4) Store data from across BP and other sources into PLD's

These nine digital clocks are in phase between the FE crates as well as within each crate.

1.3.7 Return Signals

The signals returned from the FE are;

BUSY indicates that the FE is busy and unable to generate the information for a L1 Trigger.

ERROR indicates that an error condition exists that keeps the FE from generating the information for a L1 Trigger.

INIT_ACK indicates that the FE has received a RESET but has not yet finished resetting itself.

The three returned signals are the L1 busy status, the L1 error flag and the initialize acknowledge flag. Each FE board generates its own L1 busy bit if it is unable to process L1 events, and a L1 error if some error has occurred on the board. Each FE board raises the INIT_ACC when it receives the reset signal and lowers it when it is finished with its reset and is ready to resume processing.

The signals returned from each FE board are connected to a bus in the back plane shared by all 16 FE boards in a crate. Therefore only at the FE is it possible to determine which FE is busy or has an error. This information is latched at significant event times and stored in each FE board for access via the host computer, a process that is detailed elsewhere in this document.

1.4 Cassette Ownership

Three of the systems in this document have their FE boards mounted on VLPC cassettes located in the center row of the center platform. Several of the systems have a L1 trigger and several of the systems support a read out for input into a L2 preprocessor. But most importantly for this document, since they share so many common attributes, they are designed to share most the same hardware.

The different detectors are arranged in the VLPC cassettes and FE crates as shown in figure 1.6. The VLPC cassettes are numbered from east to west with numbers 1 through 51 for both the east and west cryostats. The CFT/CPS Axial fibers are in the 40 cassettes numbered from 12E through 51E. These cassettes are arranged into groups of 8 that share the same back planes and form a single FE crate. Each cassette holds two FE boards and therefore each crate holds 16. There is no room in any crate for any boards other than FE boards. Therefore other boards which might normally be located in a FE crate have to be located in a remote Utility crate. These five crates belong to the CFT/CPS Trigger System.

The CFT stereo fibers are in 38 cassettes numbered 1W through 38W and populate most of 5 crates. The FPS South (North) is in 8(8) cassettes numbered 1E(44W) through 8E(51W), which are at either ends of the row of cassettes and occupies one crate at each end. The CPS stereo is divided with part in the east cryostat and part in the west. The CPS stereo south and some of north are in cassettes 9E through 11E and the remainder of CPS north is in cassettes 42W and 43W. Cassettes 40W and 41W are spares. All of the crates are 16 FE boards or 8 cassettes wide except the two holding the CPS stereo. These are short crates, each of which is 6 FE boards or 3 cassettes wide. These short crates are in the center of the cassette string so that all the spare cassettes are grouped together.

The location of the FPD FE boards is has not yet been determined but for strong reasons will probably be located on the West platform

1.5 L3 Readout

The L3 readout hardware for the FE and CN boards is the silicon readout system, which as the name implies is shared with the silicon detector. In the tracker readout, the signals are digitized in the SVX2e chip. Several SVX chips are connected together into a string, and share a common download and data readout path. This string is an HDI, high density interconnect, each of which can contain from 1 to 10 SVX2e chips daisy chained together. The programming for N SVX chips is downloaded per HDI as a single string of N x 190 bits. In addition, the readout for each HDI is a serial readout of all the channels for all the chips. In non-zero suppressed mode the readout is N x (2 + 2 x 128) bytes long. In zero suppressed mode only those channels above threshold are read out. Therefore in zero suppressed mode the occupancy times N, the length of the string, determines the readout time and the L1 dead time.

Eight HDI strings are connected via a parallel copper cable to eight channels of a Sequencer board, SEQ. Figure 1.7 shows a sketch of the readout system. The SEQ boards are located in special crates on the center platform. The SEQ board is used to control and download the SVX chips on each HDI and is used to translate the signals from the HDI into a fast serial optical fiber link for transmission to the MCH. The eight SEQ channels are sent over four links to eight corresponding channels on a VME Readout Buffer board, VRB. The SEQ board is designed to match the VRB board one-to-one and channel-to-channel so that the SEQ board ID is redundant with respect to the VRB ID. Therefore, the following rule has been adopted.

<u>Each Sequencer board is always connected to one and only one VRB board, and in the proper manner so that the Sequencer ID is identical to the VRB ID</u>.

Several VRB boards are in a VRB crate, each of which has a VBD for DAQ readout and receives a Serial Command Link, SCL, from the Trigger Framework. Each VRB crate forms one Geographical Sector, GS.

An HDI can also contain a Virtual SVX chip, VSVX. A VSVX chip is a PLD plus buffer memory, which appears to the sequencer exactly as another SVX, chip in the HDI. The data it contains, however, is arbitrary. That data can be inserted during each crossing for that crossing and pipelined until readout, or inserted just before the HDI is read out. In general a VSVX contains both types of data. The utility of a VSVX chip is that it can be used to transfer non-SVX chip FE information to the L3 and offline systems on an event by event basis without modification of the readout hardware or software.

The data from a GS has the following structure.

GS

```
VRB   (14 word header )
Sequencer ID (byte)          Sequencer Status (byte)
    HDI ID (byte)                HDI status (byte)
        Chip ID (byte)               00 (byte)
            Channel Number (byte)        Data (byte)
            Channel Number (byte)        Data (byte)
                                ....     .....
        Chip ID (byte)               00 (byte)
            Channel Number (byte)        Data (byte)
            Channel Number (byte)        Data (byte)
                                ....     .....
        C0                           C0  (EOR)
    HDI ID (byte)                HDI status (byte)
        Chip ID (byte)               00 (byte)
            Channel Number (byte)        Data (byte)
            Channel Number (byte)        Data (byte)
                                ....     .....
        C0                           C0  (EOR)
VRB   (14 word header )
Sequencer ID (byte)          Sequencer Status (byte)
    HDI ID (byte)                HDI status (byte)
        Chip ID (byte)               00 (byte)
            Channel Number (byte)        Data (byte)
            Channel Number (byte)        Data (byte)
                                ....     .....
        C0                           C0  (EOR)
```

Each GS is one VRB crate, which contains up to 11 VRB boards.
Each VRB has 4 optical fiber inputs from one sequencer board.
Each sequencer reads out 8 HDI, SVX strings.
Each HDI contains 8 SVX chips plus 1 or more VSVX chips at the end of each string.
NOTE - The SVX Channel Number is from 0 to 127, therefore the msb is ALWAYS 0, Thus the msb set to 1 in the EOR is used to signal then end of data.

The L3 readouts for the four detectors are divided into 3 GS each in one VRB crate. A summary of the GS for the systems is shown in Table B1, appendix B table 1. The CFT system is divided into 2 GS, with the axial fibers in one and the stereo fibers in the second. The FPS is completely included in the third. The CPS is split into two GS, the axial strips are combined with the CFT axial in the first and the stereo strips are combined with the FPS in the third. The FPD has space reserved in the second, which it shares with the CFT stereo. The L1 hardware, which is located in Muon Trigger Manager crates, comprises two additional GS. One GS is for the L1 CFT and another for the L1 FPS.

The locations for each of the detector's FE boards within the VLPC cassette cryostat is shown in figure 1.6. The cryostat row is located in the center row of the central detector platform. The Sequencer boards are located in crates in the north and south rows of the center platform. The VRB crates are located in crates in the second floor of the Moving Counting House, MCH-2.

A block diagram of the CTT systems is shown in figure 1.1. The six different FE board types are shown along the left-hand column. The second column shows the concentrator systems and the third column the L1 and L2 systems. The fourth column shows the different GS. The data from the FE boards and the CN system are sent to a common GS via the SVX readout system. The data from the L1 is sent to a different GS via the Muon readout system. And the data from the L2pp is sent to a third GS vial a VBD located in the L2pp crates. The L2pp and their readout is not a subject of this note and they are mentioned only for completeness.

Appendix A contains four figures which show the connection from each of the eight cassette modules per FE board to the MCM and SVX chips on each FE board. Appendix B contains tables listing the location of the FE boards for each of the systems and the VRB/HDI/SVX ID for each of the channels. The first set of tables list the FE boards sorted by cassette location. The second set gives the locations of the VSVX channels in the CN systems. The third set gives the information for both previously mentioned groups but now sorted by VRB/HDI/SVX ID.

The following sections will give details unique to each system.

1.5.1 Structure of the CFT Axial and CPS Axial

Send to section x.x

The CFT Axial and the CPS Axial are intermixed on the FE boards, and in the L3 data at the SVX chip level. Each FE board contains one HDI. The chips on each FE board / HDI are numbered from 0 to 15, using 4 bits. The contents of each chip are shown in Appendix A, figures 1, 2 and 3. Figure A.1 shows the distribution of fiber and strip signals from the VLPC cassette modules to the MCM and SVX. Figure A.2 lists the contents of all the chips in the HDI including the VSVX's and figure A.3 list in some detail the contents of the VSVX chips.

Chips 0 though 6 are SVX2e chips and contain the digitized analog signal values for each of the 480 fibers on a FE board. Chip 7 is a SVX2e chip, which contains the 64 digitized values for the 32 CPS strips. Chips 8 and 9 are Virtual SVX chips.

There are two FE boards for each VLPC cassette and while the fiber content into each of the 40 cassettes is identical, the two FE boards are asymmetric. Figure A.2 shows the division of the fibers from a single cassette into the two FE boards. This asymmetry is a result of requiring that the fibers be plugged into the top of each cassette in groups of 16. In figure A1 the left-hand board, LHB, is shown of the left-hand side of the figure and the RHB is shown on the right. On each side there are three columns of boxes. The center columns, which are open boxes, represent the fibers from each doublet layer on the CFT. The boxes on the left represent the cassette modules. The boxes on the right represent the MCM's. Since each MCM contains only one SVX they also represent the SVX chips. Looking at the figure we see, for example, that the A-layer fibers for the LHB are routed into MCM #1 in 32 of the 68 used channels. Note that each MCM has 72 channels. And we see that MCM #1 on the LHB has 32 inputs from the A-layer, 32 from the B-layer and 4 from the C-layer, while MCM #1 on the RHB has 32 inputs from the A-layer and 36 from the B-layer. The 32 channels from the CPS axial are always input as 64 channels into MCM #8.

The CFT/CPS VSVX chips contain several types of data, which are listed in figure A.3.

The CFT and CPS axial are in GS #80 and are located in the East cryostat. Appendix B contains a series of tables listing the locations of the FE boards in the Cassettes and the routing of the readout. The two charts labeled 'East Cryostat' and 'West Cryostat' list the FE boards sorted by cassette location and the three charts labeled 'Geographical Sector 1' through 3' list the FE boards sorted by Sector/VRB and HDI numbers.

1.5.2 Structure of the CFT Stereo

Send to section x.x

The CFT Stereo consists of 75 FE boards, each of which contains 512 CFT Stereo fiber channels. Each FE board contains one HDI. The chips on each FE board / HDI are numbered from 0 to 15, using 4 bits. The contents of each chip are shown in figures A.4 and A.5.

Chips 0 though 7 are SVX2e chips and contain the digitized analog signal values for each of the 512 fibers on a FE board. The fiber tracker has 16 stereo doublet layers alternating between u and v layers laid down in ribbons 256 fibers wide. Each FE board receives the input from two ribbons.

The contents of each SVX chip in the CFT FE stereo board is shown in figure A5. There are two FE boards for each VLPC cassette. The analog aspects of the FE boards for the CFT Stereo are identical to those for the CFT axial.

The CFT stereo is in GS #81 and is located in the West cryostat in crates 1 through 5. Since there are only 75 FE boards, 37.5 cassettes are occupied and 2.5 in crate 5 are open or spares. The L3 readout from these FE boards constitutes the bulk of a single GS.

1.5.3 Structure of the FPS

Send to section x.x

The FPS is on 32 FE boards in two crates. Each of the crates is at either end of the cryostat row in the platform. Each FE board contains two HDI's and the chips on each HDI are numbered from 0 to 15, using 4 bits. The contents of each chip are Shown in figures A.7 through A.9.

Chips 0 though 3 on HDI 0 are SVX2e chips and contain the digitized analog signal values from the 101 forward strips in each of the u and v layers. Chips 4 though 7 on HDI 0 are SVX2e chips and contain the digitized analog signal values from the 135 back strips in each of the u and v layers for the high gain arm of the charge division. Chips 0 though 3 on HDI 1 are SVX2e chips and contain the digitized analog signal values from the 135 back strips in each of the u and v layers for the low gain arm of the charge division. Chip 4 on HDI 1 is a Virtual SVX chip.

The FPS VSVX chips contain several types of data, which are shown in figure A.9.

1.5.4 Structure of the CPS Stereo

Send to section x.x

The CPS Stereo is on 10 FE boards in two 'small' crates. Each of the crates is at either end of the cryostat row in the platform just inboard of the FPS crates. The CPS Stereo is made up of two layers, u and v, at two ends, n and s, of the detector cylinder. The cylinder is broken up in phi into 5 groups of 256 strips. Two of these groups of 256 contiguous strips from overlapping u and v layer from a single end are routed to each FE board. Each FE board contains two HDI's and the chips on each HDI are numbered from 0 to 15, using 4 bits. The contents of each chip are shown in figures A10 through A12.

The CPS Stereo VSVX chips contain several types of data, which are shown in figure A12.

1.6 Triggers

The CTT supplies information for both L1 and L2 triggers. The systems take in the discriminated signals from fibers or strips and use them to find tracks or clusters. A new set of information is input each crossing or 132ns. The information from each crossing is processed over several crossings. This is done by pipelining the data in the trigger logic. When the information has finished processing, the time from start to finish is the latency, it is formatted for multiple clients. These clients include other detector L1 triggers. The one instance of this is the CFT trigger supplies track information to the L1 Muon. These clients also include the decector's own L1 trigger and several L2pp.

1.6.1 L1

L1 Triggers are available from the CFT Axial fibers, the CPS axial strips, the FPS strips and the FPD spectrometers. No information is available at the L1 from the CFT Stereo fibers or the CPS Stereo strips.

1.6.1.1 CFT L1

Each CFT Trigger FE board provides the number of found tracks in each of 4 Pt-Th, Pt threshold bins, the number of those tracks in each of 4 Pt-Th bins which have a matching cluster in the CPS Axial, and whether there is an isolated track or isolated matched track. A track with a matching cluster is called a electron. The Pt-Th bins are nominally:

Pt-Th-1	11	-	1000 GeV
Pt-Th-2	5	-	11 GeV
Pt-Th-3	3	-	5 GeV
Pt-Th-4	1.5	-	3 GeV

Also each FE reports out the number of fibers hit within its sector. This number can range from 0 to 255, with 255 reported out whenever the number exceeds this amount. The number of found tracks is less than or equal to 6 as is the number of matched tracks. Note that the set of matched tracks is a subset of the found tracks. If 5 tracks are found the number of tracks is 5, if 3 of them are matched to clusters the number of matched tracks is 3. The number of isolated tracks is always 0 or 1, but there can be 1 isolated track and 1 isolated matched track, which is one and the same track. The number of unmatched clusters, called photons, is also reported out. Since a cluster can be 1 or more strips wide this number ranges from 0 to 8. A total of 12 numbers is reported out of each FE.

The information from the FE's is combined into octants in phi before it is sent to the L1 TM, Trigger Manager. The octant boundaries match 2 to 1 with the quadrant boundaries of the L1 Calorimeter Trigger. To form the octants the information from 10 FE boards is combined. Ten sets of 12 numbers are combined into a single set of 12 numbers and sent to the L1 TM. For 11 of the numbers the combination is a simple sum, for the 'number of fibers hit' a threshold is applied to each FE and the number of FE's above that threshold is reported to the L1 TM.

The information at the CFT L1 TM is then;

# of ALL tracks	by Pt-Th (4bins)	by Phi (8bins)	0-60
# of 'electrons'	by Pt-Th (4bins)	by Phi (8bins)	0-60
# of isolated trks	(1bin)	by Phi (8bins)	0-5
# of iso-electrons	(1bin)	by Phi (8bins)	0-5
# of 'hit' FE's	(1bins)	by Phi (8bins)	0-10
# of 'photons'	(1bins)	by Phi (8bins)	0-80

The information for each Phi is over a separate cable, for a total of 8 cables into the TM. Which results in a total of 65 bits per octant (cable) and 520 bits total. More details of the CFT FE trigger can be found in sections 2.1, 2.2 and 2.3.

1.6.1.2 CPS L1

The CPS L1 is included in the CFT L1. See the above section. CPS specific details can be found in section 3.

1.6.1.3 FPS L1

In the FPS detector clusters are found in separately in the backward u and v layers and each of these clusters is matched with hits in the forward layer to tag them as either electron or photon type. Each FE board of the FPS contains 1/16th of the north(south) detector, which is one physical detector module. Each of the FE boards reports out the number of electron and photon type clusters found in each of the u and v layers. This process is duplicated for two sets of thresholds in the backward layers. The result is 8 numbers per FE board. The 8 numbers from each pair of FE boards is combined into a quadrant sum, which is sent to the FPS L1 TM.

The information at the FPS L1 TM is then;

# of 'electrons'	north	by u/v	(2bins)	by Phi (4bins)	0
# of 'photons'	north	by u/v	(2bins)	by Phi (4bins)	0
# of 'electrons'	south	by u/v	(2bins)	by Phi (4bins)	0
# of 'photons'	south	by u/v	(2bins)	by Phi (4bins)	0

This information is sent over 4 links, which results in a total of 64 bits per cable and 256 bits total. More details of the FPS can be found in section 4. Details of the L1 transfer can be found in section 4.1.2.4.2

1.6.1.4 FPD L1

The FPD has nine spectrometers, each of which consists of two separated detectors. Track segments are found in each detector and matched to find tracks in each of the spectrometers. The number of tracks in each spectrometer is sent to the FPD TM which is located in the same Geographic Sector, GS, and crates as the CFT TM.

These 9 numbers, each of which can be up to 8 bits, are sent to the TM.

1.6.2 L2

1.7 Schedule and Budget

The CTT project is within two WBS sub-projects. The FE, including the analog and digital boards and their support is in WBS 1.1.5.3, the Fiber/Preshower Readout System, as part of the Tracking electronics budget. The Concentrator system is in WBS 1.4.3.3, the Central Fiber Tracker L1

Trigger, as part of the Trigger budget. The cost in WBS 1.1.5.3 with contingency is some $1.88M and in WBS with contingency is some $0.23M.

1.7.1 Fiber/Preshower Readout System - WBS 1.1.5.3

The schedule calls for the design, layout and fabrication of a single analog FE board. This board is stuffed differently for use in the CFT/CPS Trigger, CFT Stereo, and FPS uses. The estimated duration for the design, testing and production of this board is 70 weeks from 1-Jan-1999. The production of this board is dependent upon the production of the SIFT chip and subsequent production of the MCM. It is also dependent upon a definitive specification for the sizing of the capacitors within the analog circuits on the boards. The preshower and fiber groups have specified their needs. What remains is the final measurement of the VLPC gains and tests of the capacitance of the board, connector, FLEX circuit combinations. If it proves impractical to fabricate one basic board and a second board design is required the schedule would stretch on the order of 6 months.

The schedule calls for the design, test and fabrication of two digital FE boards. While the DG board for the CFT/CPS Trigger and the FPS Trigger are substantially the same, it seems more cost effective to tailor the board to either use. Since they are so similar, the design for both will proceed in tandem. Only the CFT version will go into pre-production and both will enter production together. Therefor the duration for the one board is longer but both will reach completion at the same time.

Our best information on the scheduling indicates that all the boards can be ready by June of 2000. It also seems given the board designs and personnel available that all the board types can and should be developed in parallel and completed at about the same time.

The final major cost drivers for this project are the large FPLD chips used in the tracker or cluster logic and in combining tracks with clusters. The cost curve for these is dropping dramatically and our design lends itself to, waiting until well into the production, for the purchase of these chips. In fact, some of the chips could be added after production. In this were done the lower cost and/or increased performance could offset the added cost of a second round of component placement.

1.7.2 Concentrator System - WBS 1.4.3.3

As of this writing the design of the Concentrator system is in its final phase. In this phase the board schematics are drawn and the components identified. The design with the exception of defining the interface between the DG boards and the RC boards is de-coupled from the FE board design. The design is also being conducted by different personnel in each case. The estimate for the completion of the design is 3 months from 1-Jan-1999. Following the completion of the design, the layout and pre-production take about 6 months and the production another 6 months.

1.8 Figures

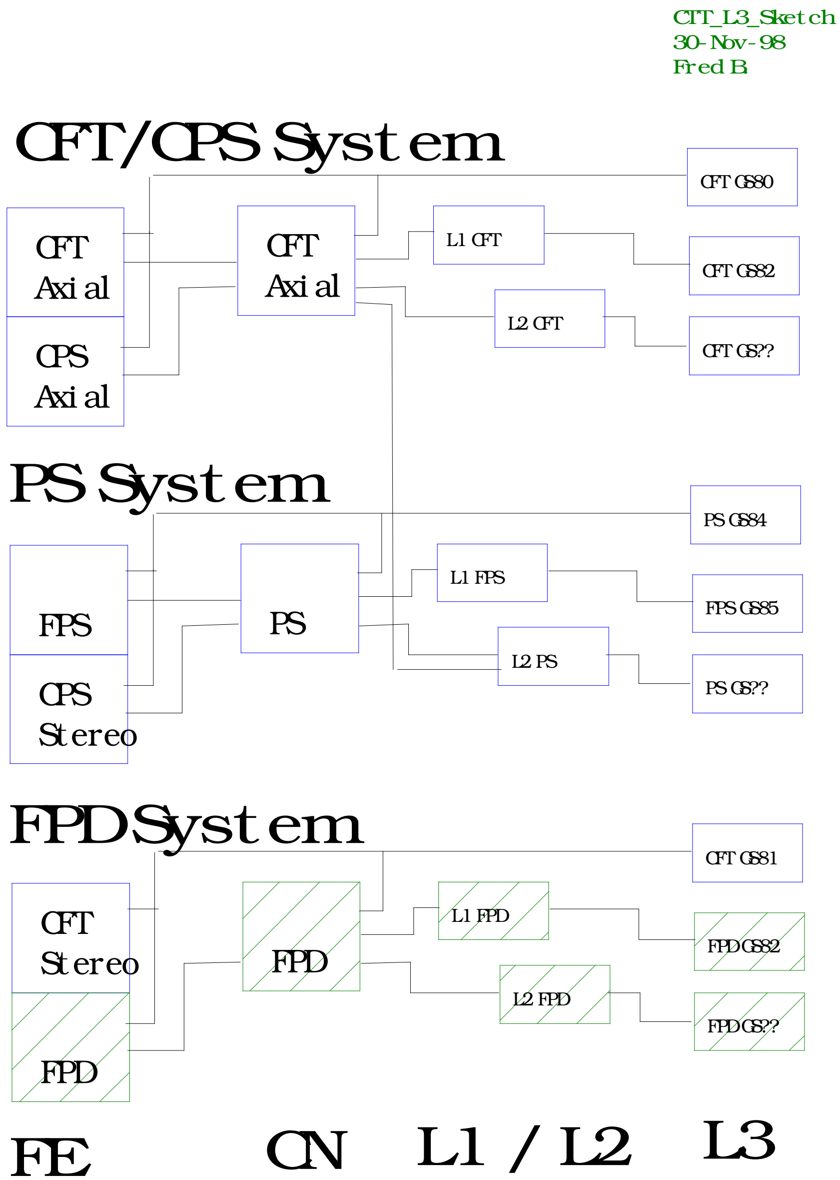


Figure 1.1 - Block diagram of all the systems. The six types of FE boards are listed in the left-hand column, the next column lists the CN systems, the third column the L1/L2 systems and the fourth or right-hand column lists the GS. The FE and CN boards are in GS which are read out using the VRB's. The L1 boards are read out using the muon L3 system.

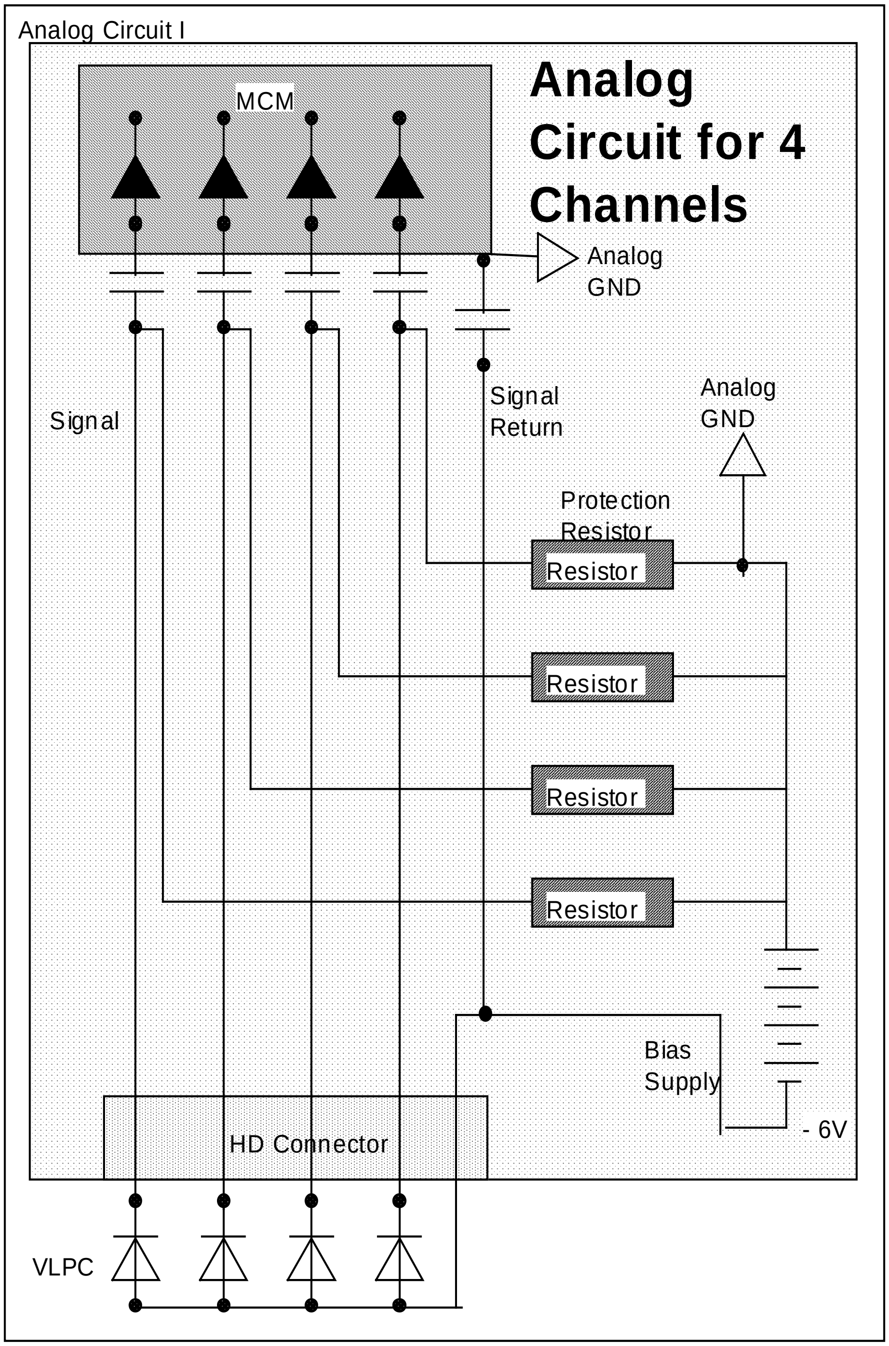


Figure 1.2 - Circuit schematic for an analog FE board. This illustration shows four circuits connected, on the FE board the VLPC circuits are connected into groups of 64 signal channels. Each group has a common BIAS supply on the board and a shared trace into the cassette. The common bias supply circuit is also the common signal return. The 64 individual signal return lines are also bias return lines. For those detectors with charge splitting the single capacitor shown coupling the signal into the MCM is replaced with a charge division network.

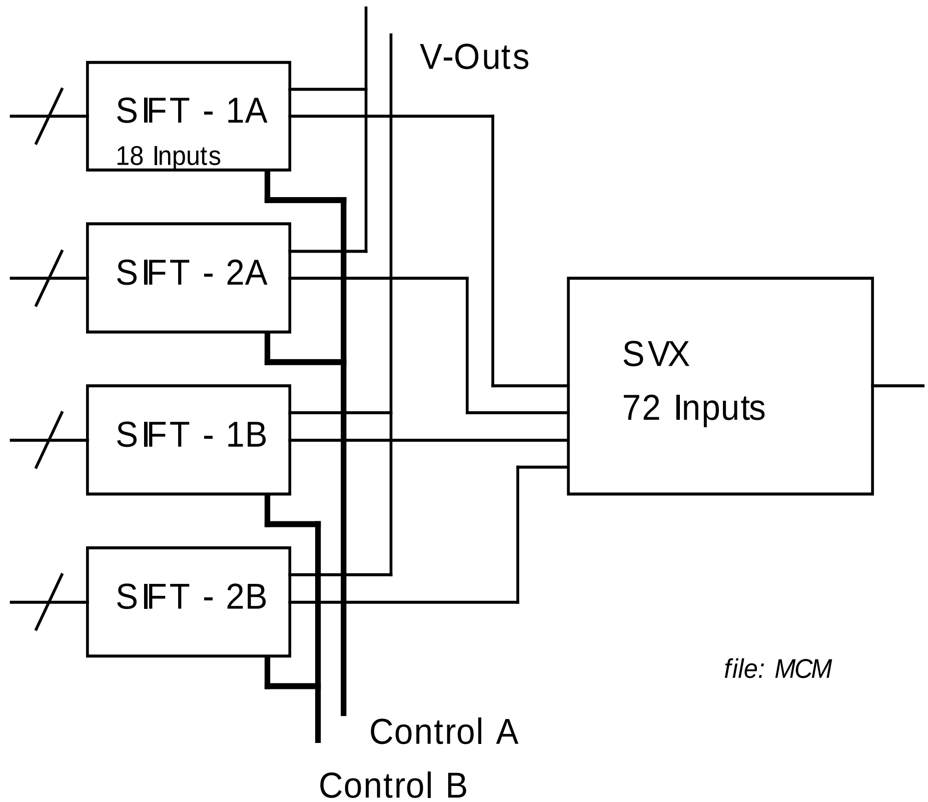


Figure 1.3 - Block diagram of the interior of the MultiChip Module, MCM. Each MCM contains 4 SIFT chips and one SVX chip. The SIFT chips share common controls as two pairs. The control consists of the discriminator gain range setting and threshold voltage, and the analog output gain range setting. SIFT channels 2 through 19 are used. The outer two channels are grounded and serve as guard channels. The SVX2e chip has 72 of 128 channels bonded. The bonded channels are for the most part every other channel.

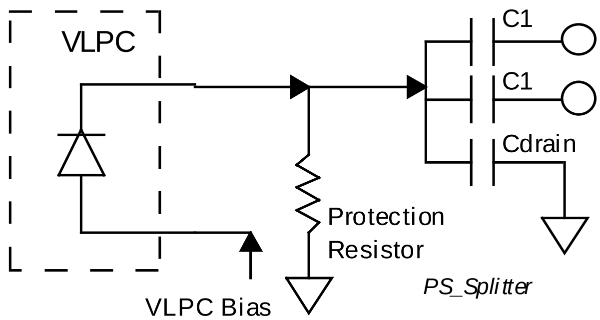


Figure 1.4 Simplifiied schematic of the charge splitting on the FE board for the PS channels. The charge from the VLPC is split 3 ways with most of the charge dumped through the drain capacitor. Since C1 and C2 are much smaller the charge division is proportional to C1(2) / SUM.

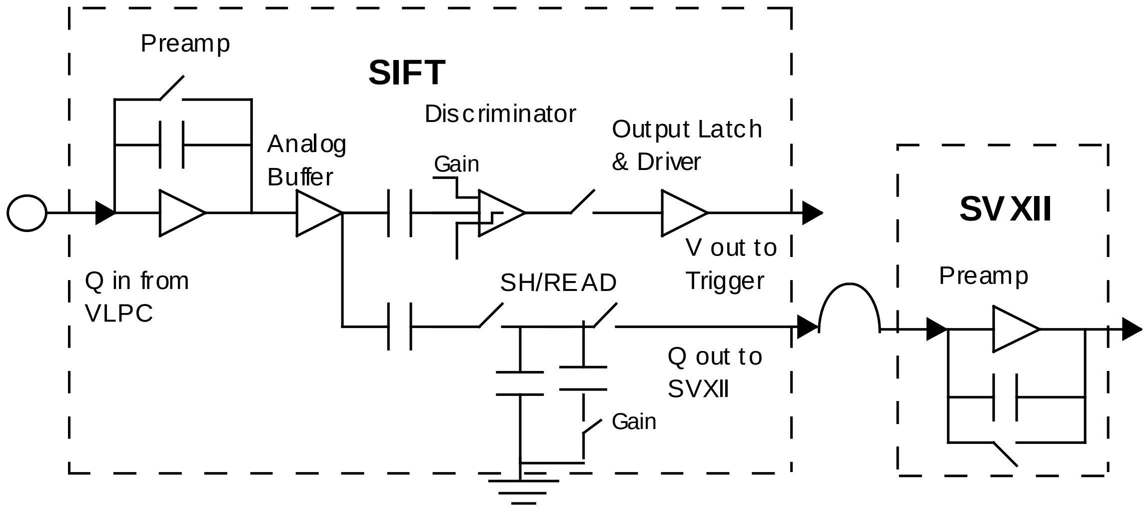


Figure 1.5 - Simplified schematic of a single channel of the MCM. Each analog input is routed to a SIFT channel where it is discriminated for a Voltage output and integrated and passed onto an SVX2e chip input channel. The output of the SVX2e is a digitized amplitude.

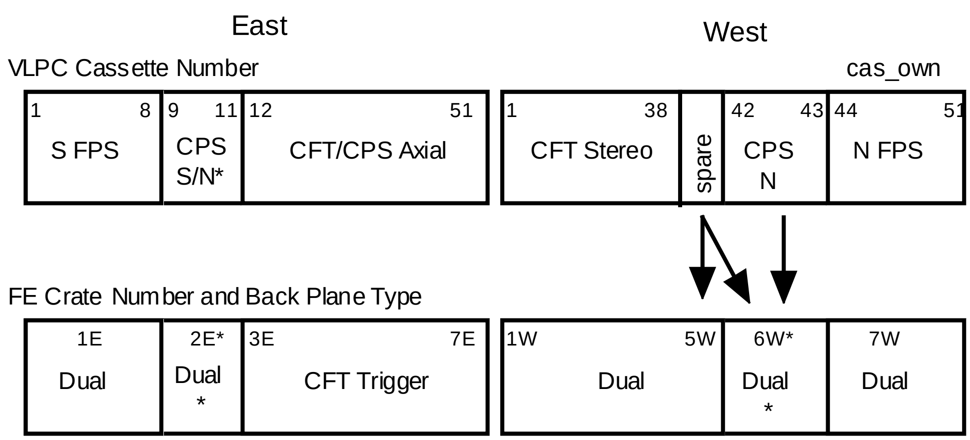


Figure 1.6 - The layout of cassettes for the VLPC based FE electronics. The top half of the figure lists the cassette numbers, from 1 to 51 in each cryostat. The detector types in each cassette are also given. The bottom half shows how the cassettes are divided into FE crates. The crate types are also given.

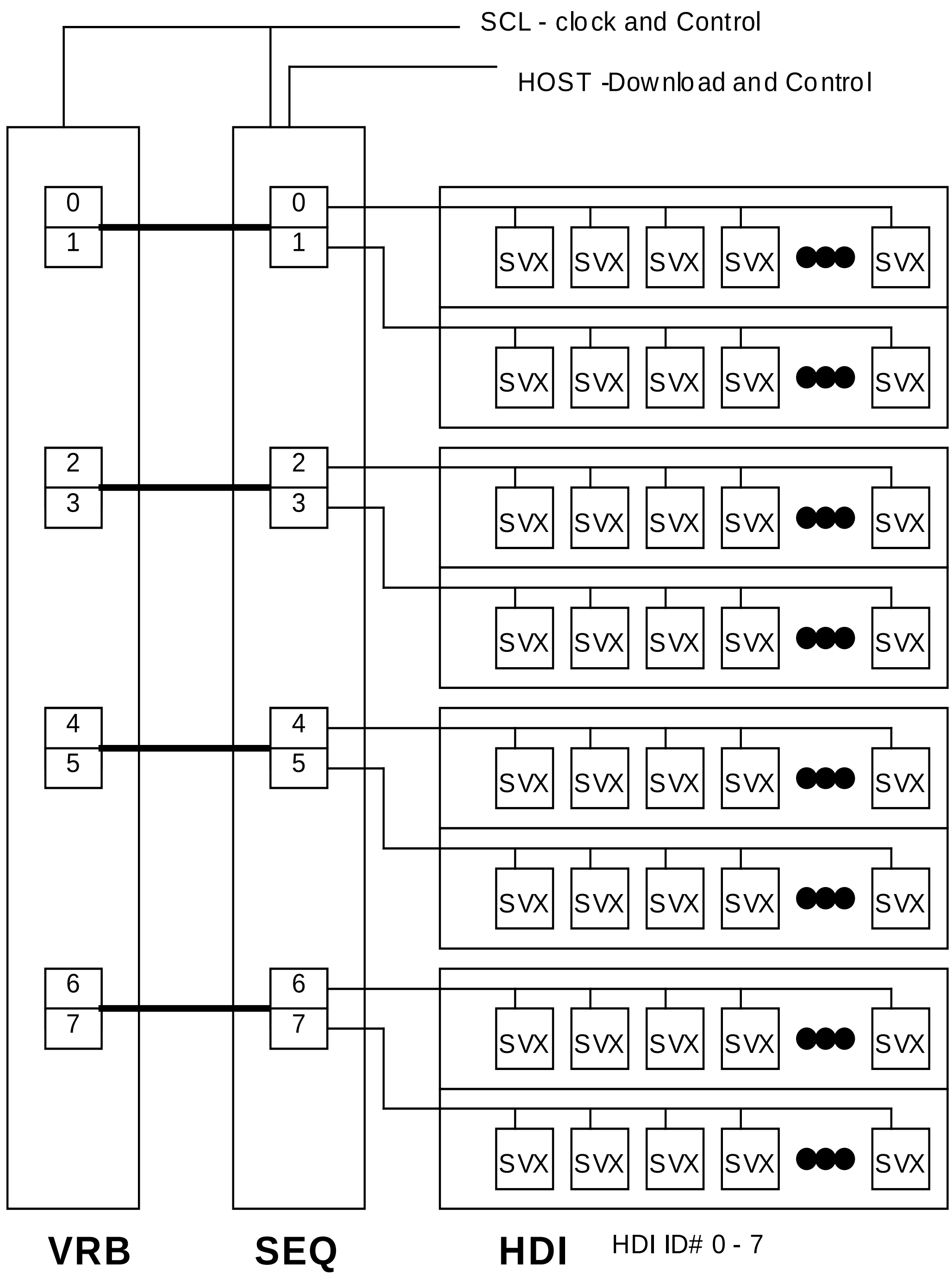


Figure 1.7 - Schematic of the tracker L3 Readout system. Each HDI contains several SVX chips (or VSVX) daisy chained together. Eight HDI's are connected to eight channels within a single SEQUENCER board located on the platform. The eight SEQ channels are connected to eight channels within a single VRB board which is located in the MCH. The SEQ channel to VRB channel connections are always made as shown so that SEQ channel ID # is idedentical to VRB channel ID #.

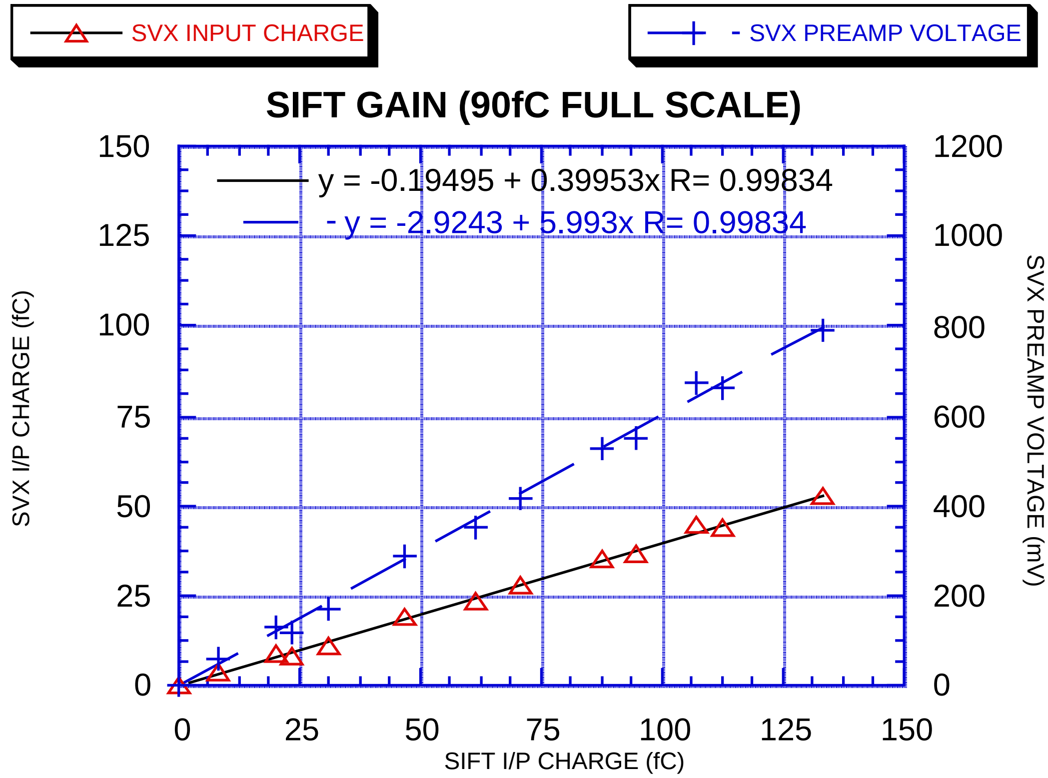
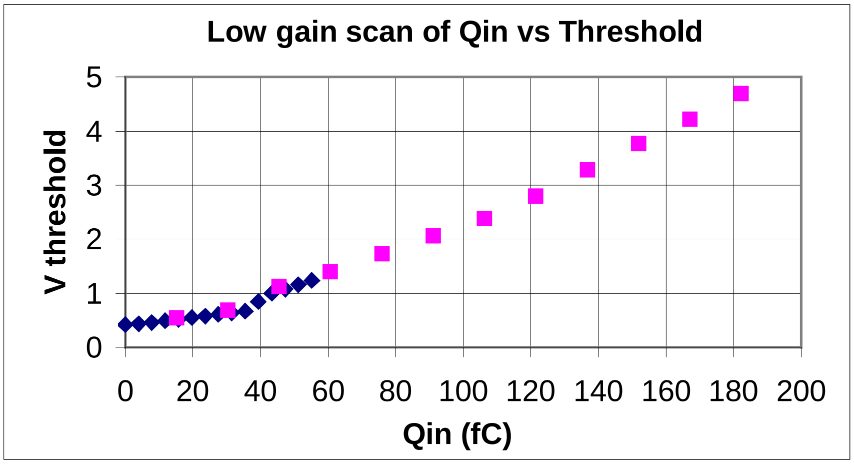


Figure 1.8 The SIFT analog gain into the SVX chip. The high gain is just under 0.4 and the low gain is 1/2 of that or about 0.2.



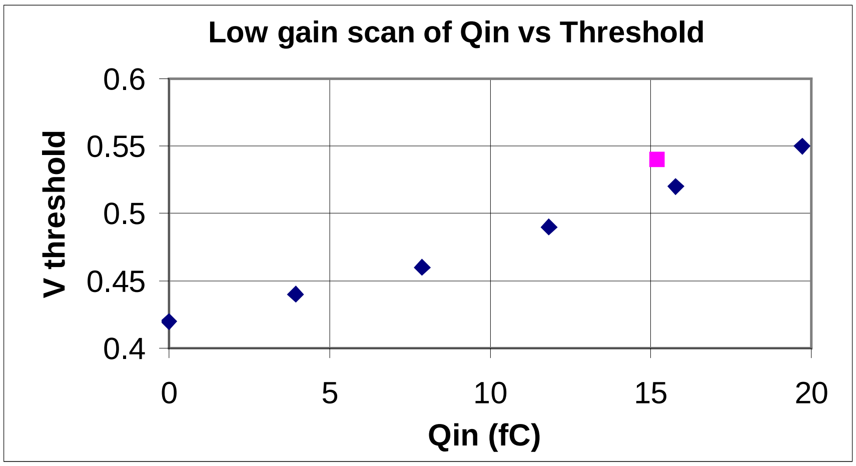


Figure 1.9 Threshold setting versus change input into the SIFT chip for the low gain setting. The bottom plot shows the lower end of the spectrum in more detail. The high gain setting requires 2 times the input change for the same threshold.

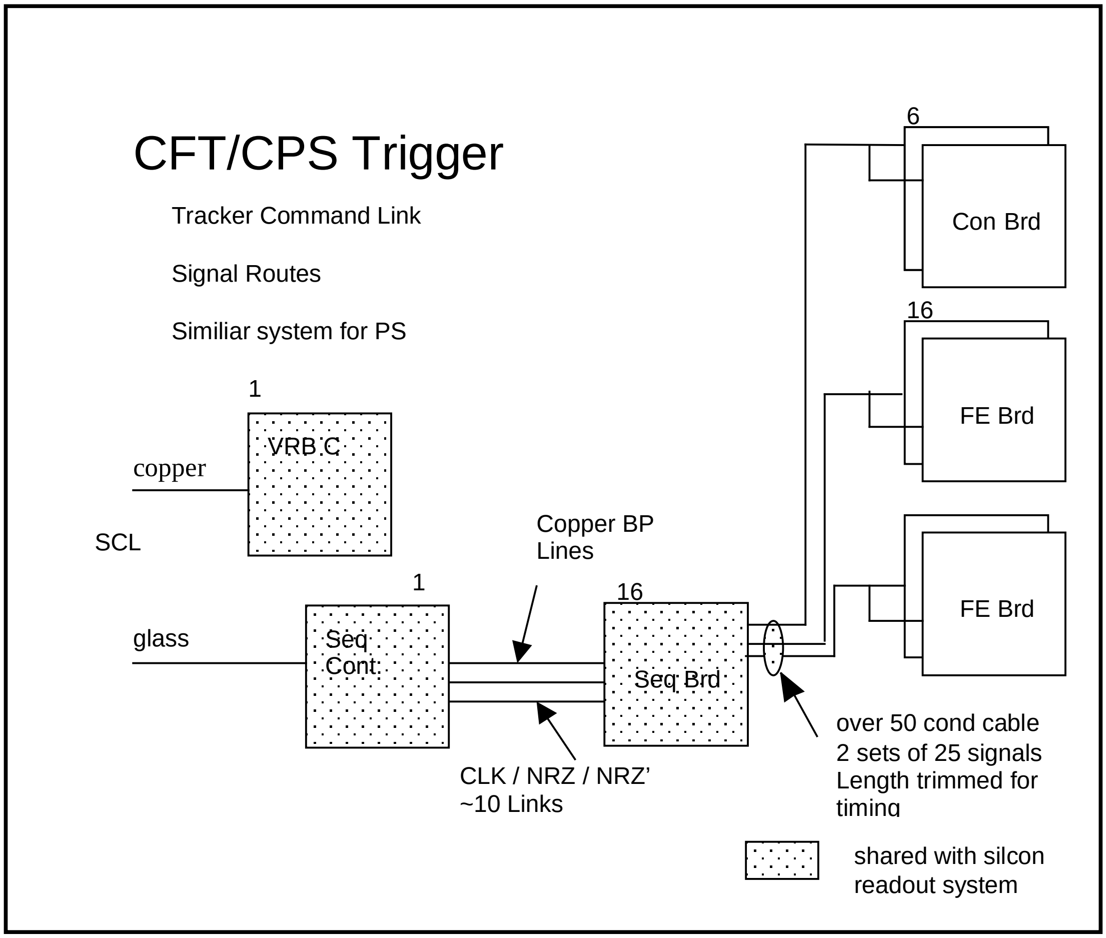


Figure 1.10. Tracker command link system. This is an overall view of the entire system.

Line	Bit Number	Name	Description
1	1	Framing Bit	Start of 7.6 MHz Crossing Cycle
1	2	Crossing	This is a beam crossing*
1	3	D1	Data
1	4	D2	Data
1	5	D3	Data
1	6	D4	Data
1	7	Parity bit	Parity of preceeding 6 bits
2	1	Framing Bit	Start of 7.6 MHz Crossing Cycle
2	2	Spare	
2	3	Reset	Start/Continue RESET
2	4	Sync. Gap.	Start/Continue SYNC_GP
2	5	1st Crossing	Start/Continue 1ST_CRS
2	6	L1 Accept	Start/Continue L1_ACC
2	7	Parity bit	Parity of preceeding 6 bits

Table 1.x Definition of the NRZ protocol bits. The first line carries information used by the SVX chips exclusively. The second line carries additional information used by the FE boards.

Net no.	Net Name	Connector no.		Description
1	CROSS	1	38	53/7 (53/21) always present
2	/CROSS	26	14	53/7 (53/21)
3	GND	2	39	Connect pin to GND Shield
4	*CLK_A*	*27*	*15*	*SVX clock -*
5	*/CLK_A*	*3*	*40*	*frequency varies*
6	SYNC_GAP	28	16	Synchronization Gap
7	1ST_CROSS	4	41	First crossing of turn indicator
8	*PRIORITY_IN_A*	*29*	*17*	*Top Neighbor*
9	*CHANGE_MODE_A*	*5*	*42*	*Mode control*
10	*MODE1_A*	*30*	*18*	*Mode control*
11	*MODE0_A*	*6*	*43*	*Mode control*
12	*D7_A*	*31*	*19*	*Data Buss*
13	*D6_A*	*7*	*44*	*Data Buss*
14	*D5_A*	*32*	*20*	*Data Buss*
15	*D4_A*	*8*	*45*	*Data Buss*
16	*D3_A*	*33*	*21*	*Data Buss*
17	*D2_A*	*9*	*46*	*Data Buss*
18	*GND*	*34*	*22*	*Connect pin to Gnd Shield*
19	*D1_A*	*10*	*47*	*Data Buss*
20	*D0_A*	*35*	*23*	*Data Buss*
21	*HDI_ENABLE_A*	*11*	*48*	*Enable String*
22	*DVALID_A*	*36*	*24*	*Data Strobe*
23	*PRIORITY_OUT_A*	*12*	*49*	*Bottom Neighbor*
24	*DIR_A*	*37*	*25*	*Transceiver direction*
25	*VCAL_A*	*13*	*50*	*Cal Voltage - DC level*
26	L1_ACCEPT			L1 Accept indicator
27	CLAMP			Clamp the SIFT to SVX
28	GND			Connect pin to GND Shield
29	*CLK_B*			*SVX clock -*
30	*/CLK_B*			*frequency varies*
31	RESET			Reset the FE board systems
32	Spare			

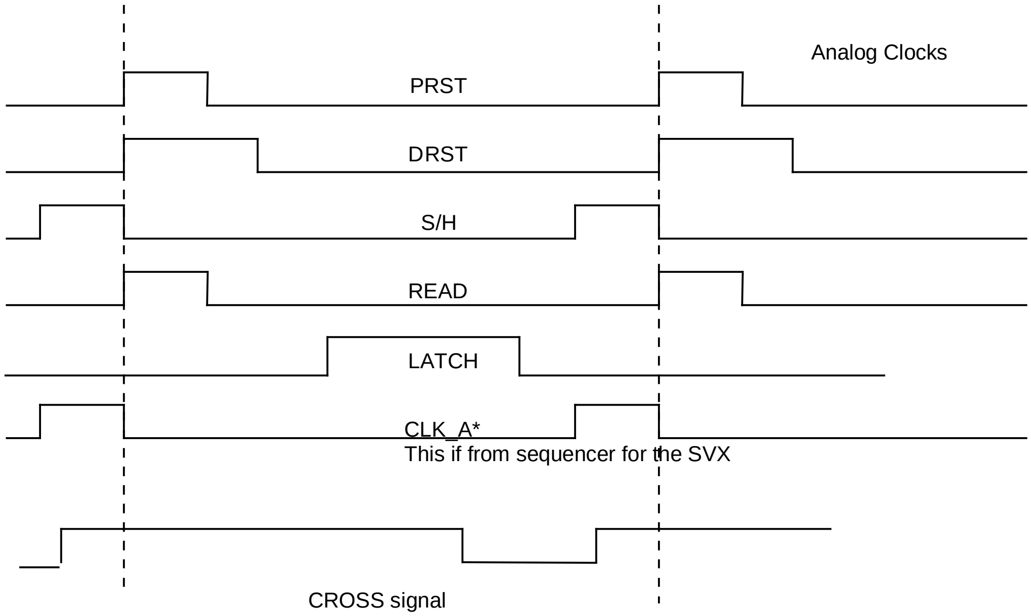
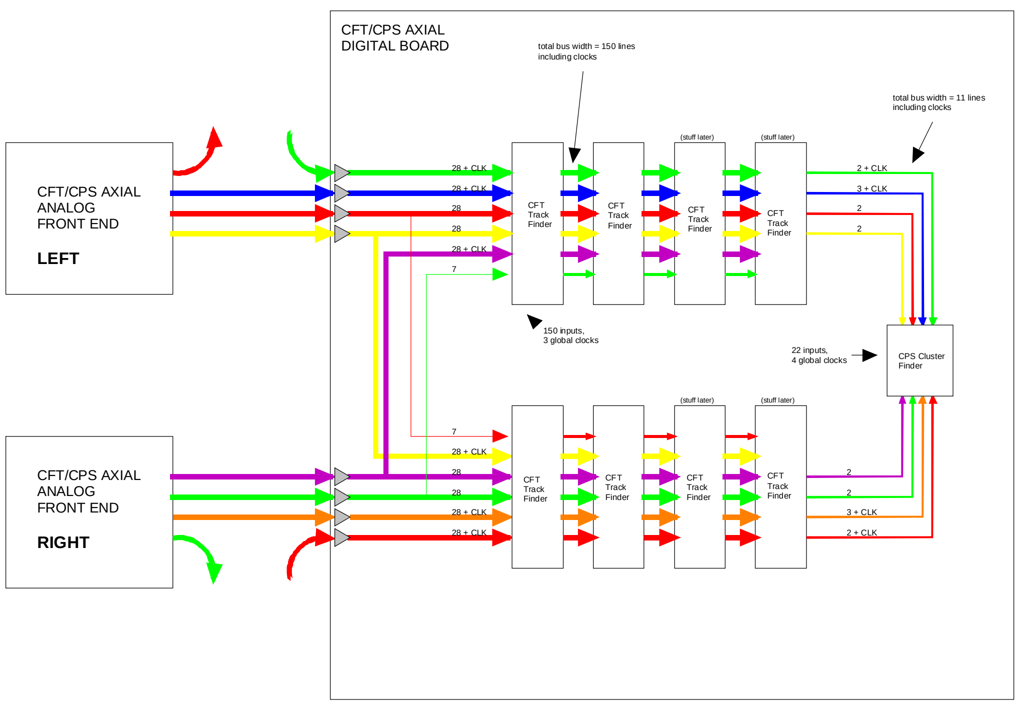


Figure 1.11. Relative clock timings for the SIFT and SVX chips during acquire, ACQR, mode. CLK_A is the SVX clock. LATCH is the clock for latching the SIFT V_OUT signals.



Analog / Digital Front End Boards:
CFT / CPS AXIAL

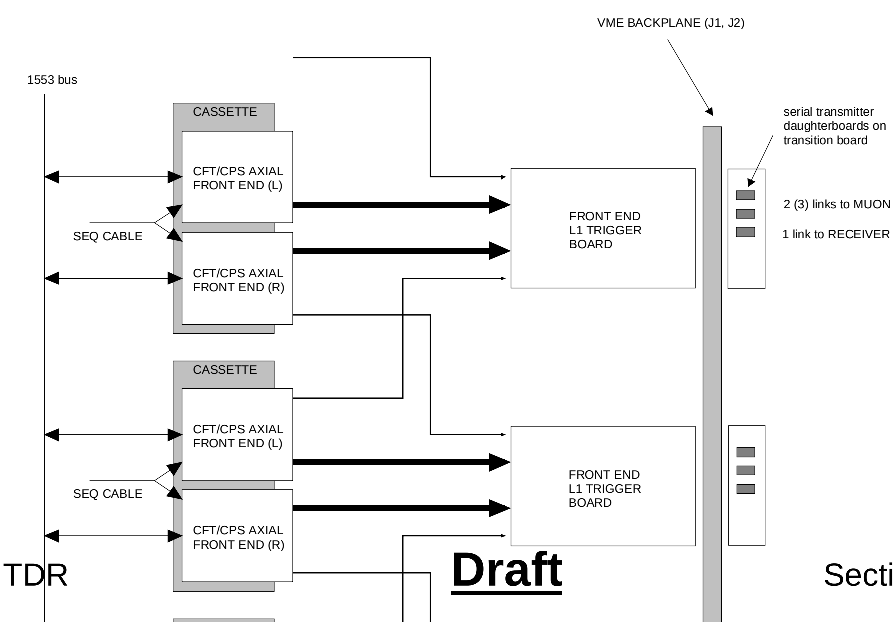


Figure 1.12. Dig ….

Analog / Digital Front End Boards: FPS

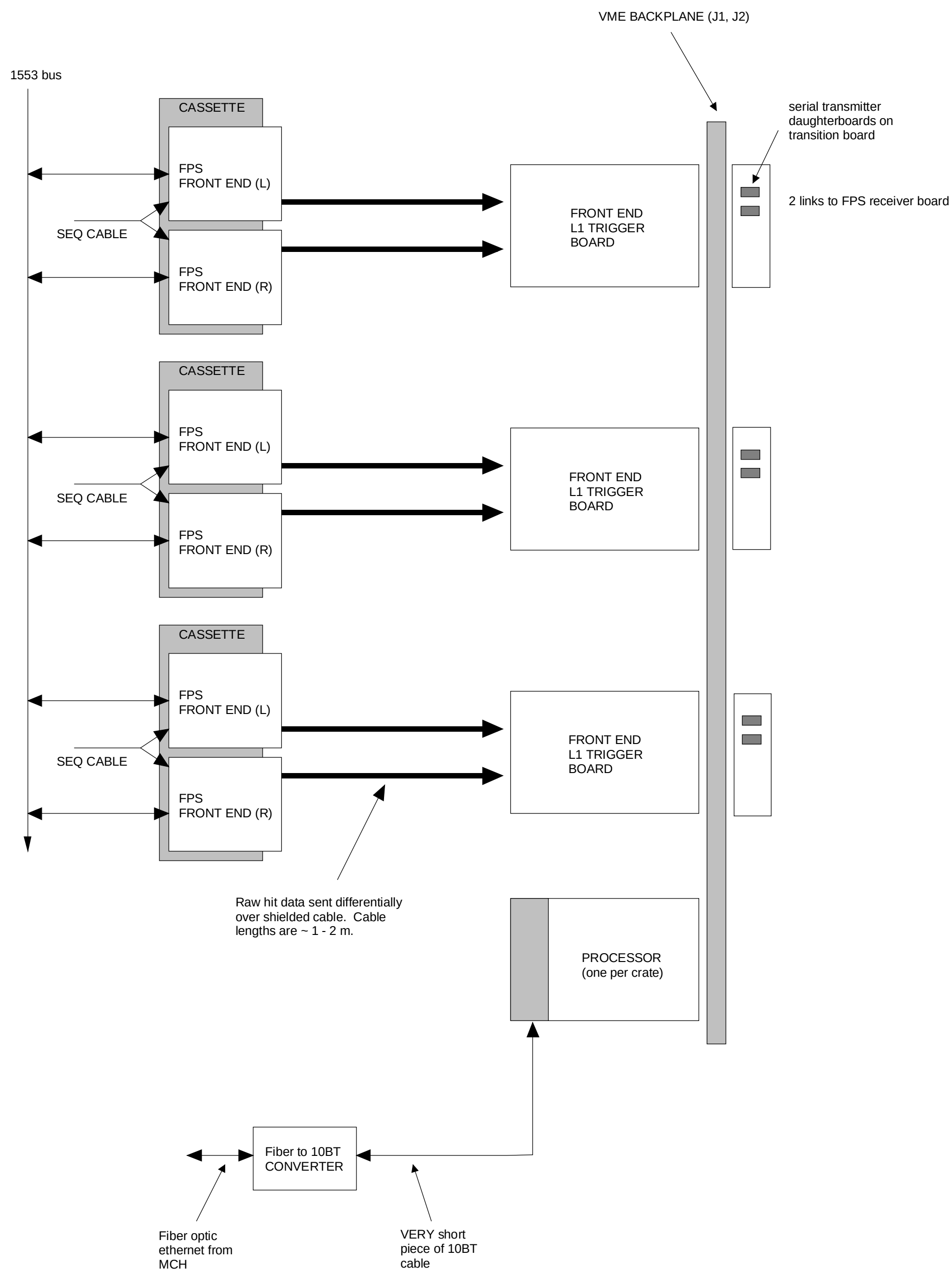


Figure 1.13. Dig ….

Analog / Digital Front End Boards: CPS Stereo

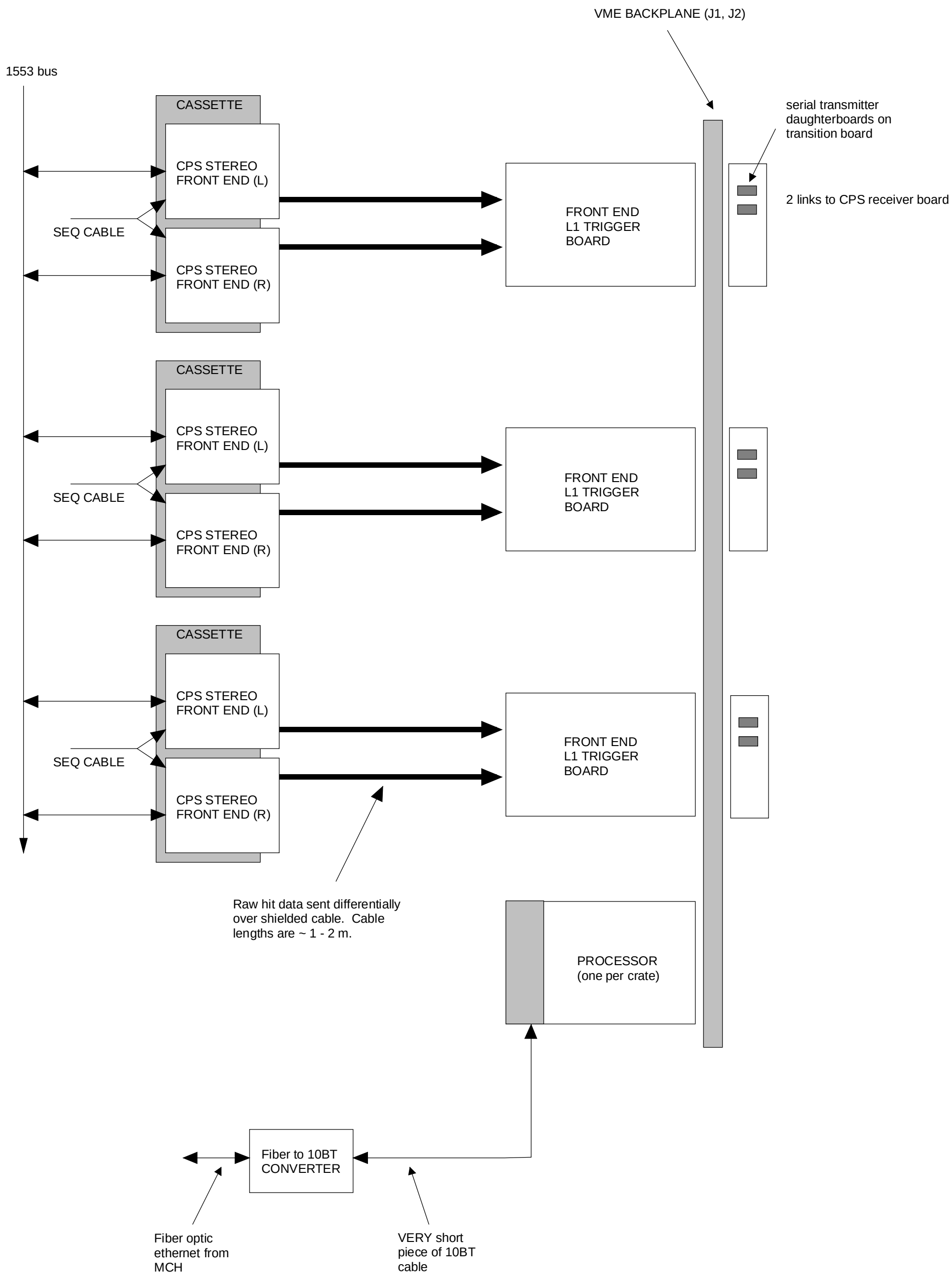


Figure 1.14. Dig ….

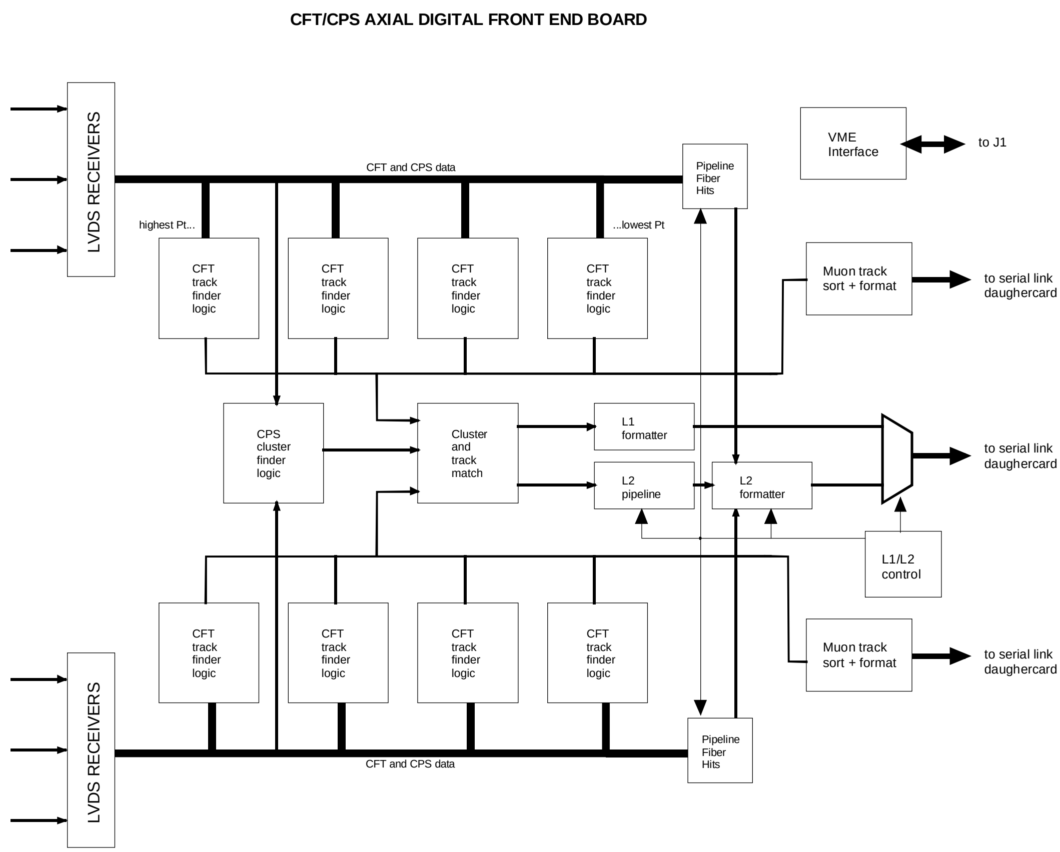


Figure 1.15. Dig ….

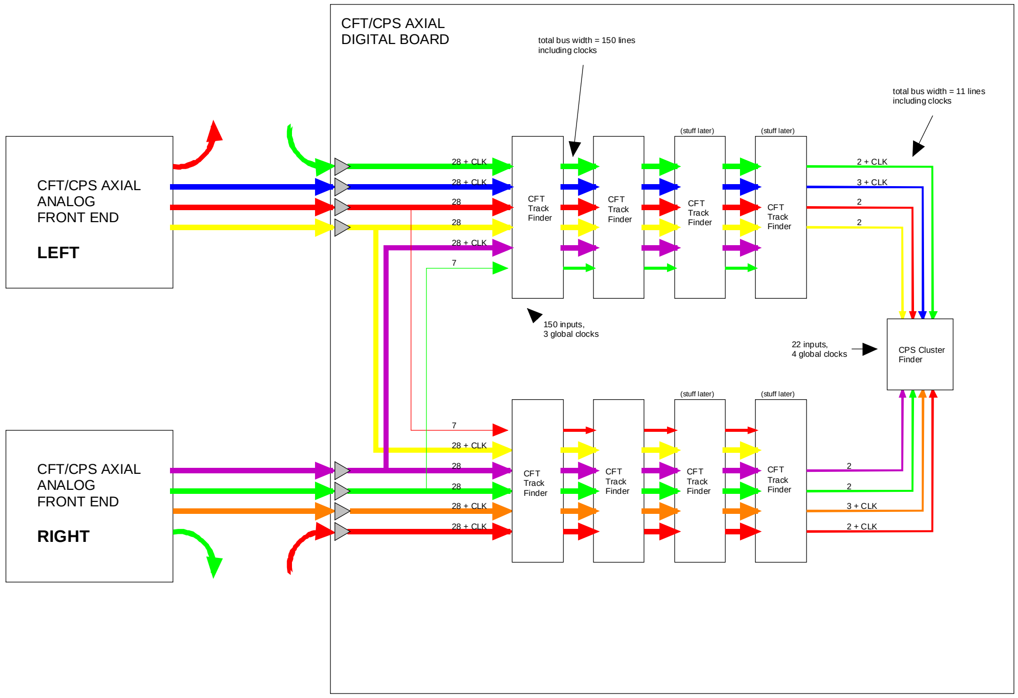


Figure 1.16. Dig ….