CDF Run II Silicon Tracking Projects

8th INTERNATIONAL WORKSHOP ON VERTEX DETECTORS

Texel, Netherlands

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Presented by

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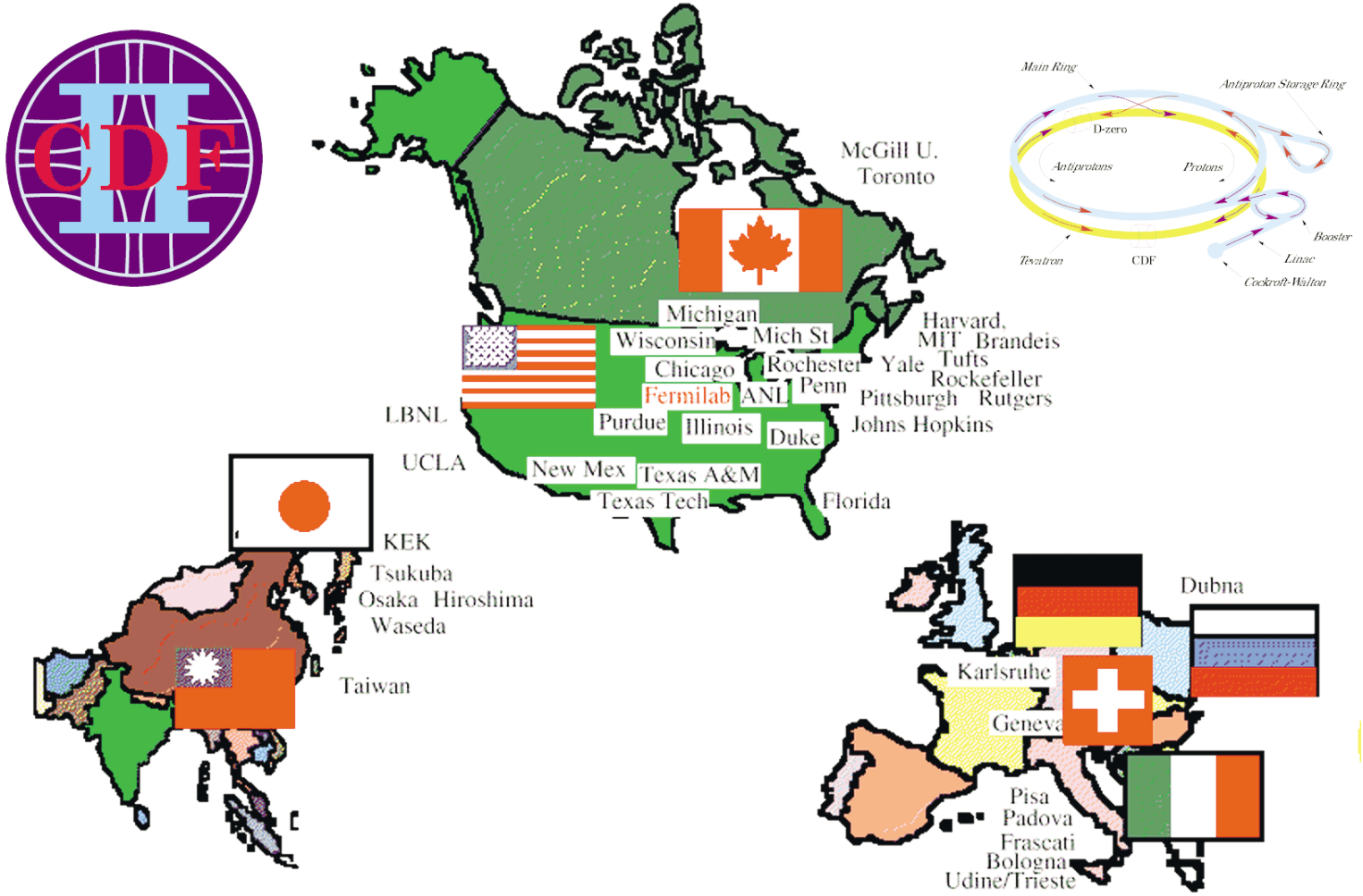
The CDF Collaboration for Run II



490 physicists from 41 institutions representing 8 countries

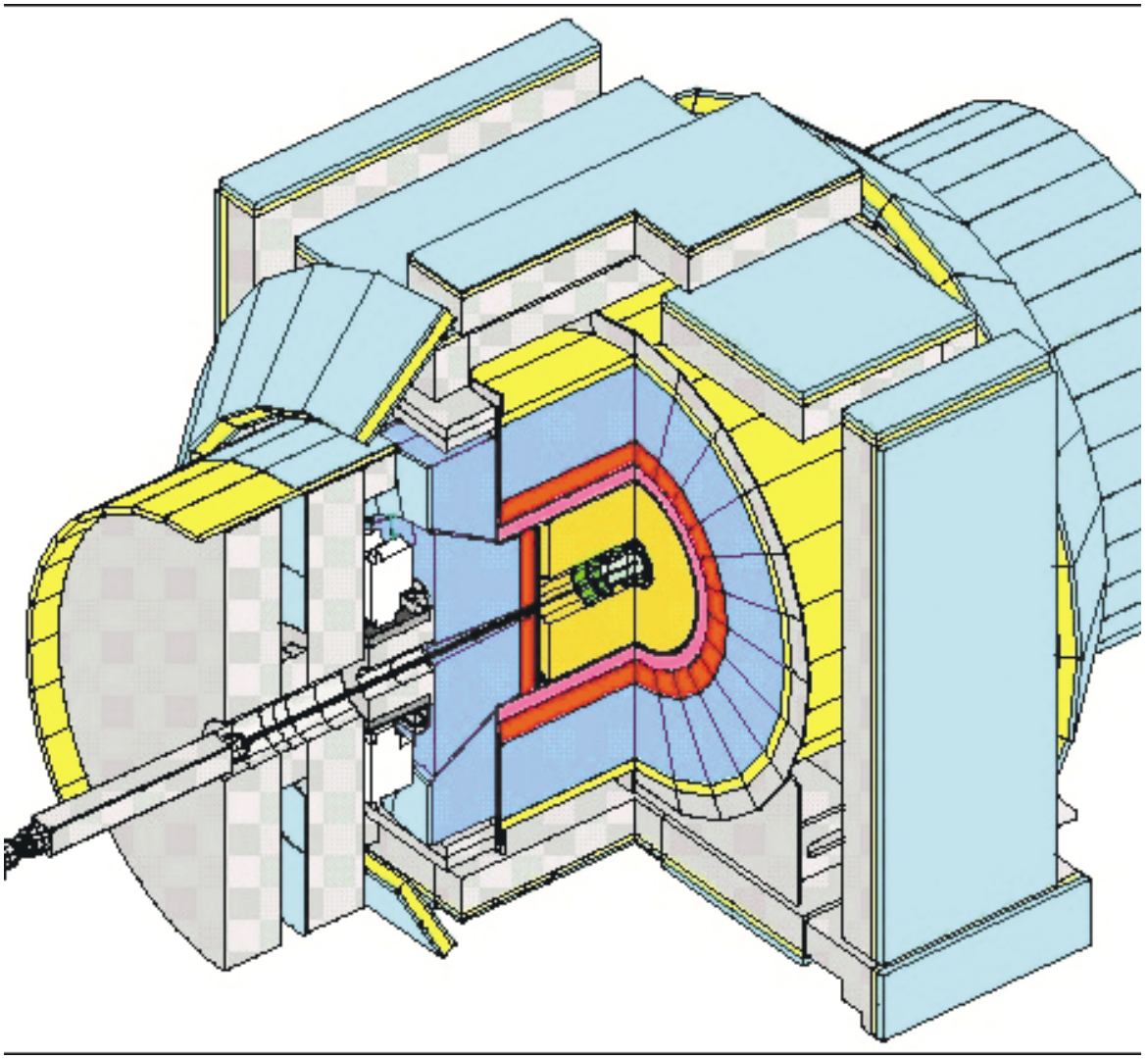
Goals for CDF Run II Silicon

- Increase acceptance and coverage of luminous region along beam
  - **Previous CDF vertex detectors covered interactions within $|z| < 0.27$ m, New silicon detectors designed to cover $|z| < 0.43$ m**
  - **Interaction region expected to be more concentrated in z in Run II**
  - **Increase silicon angular acceptance to cover approximately $\eta \leq 2$.**
  - **Overall effect should be approximately a factor of 2 increase in acceptance for particles with good tracking and vertexing**
- Improve top tagging for high-p_T physics:

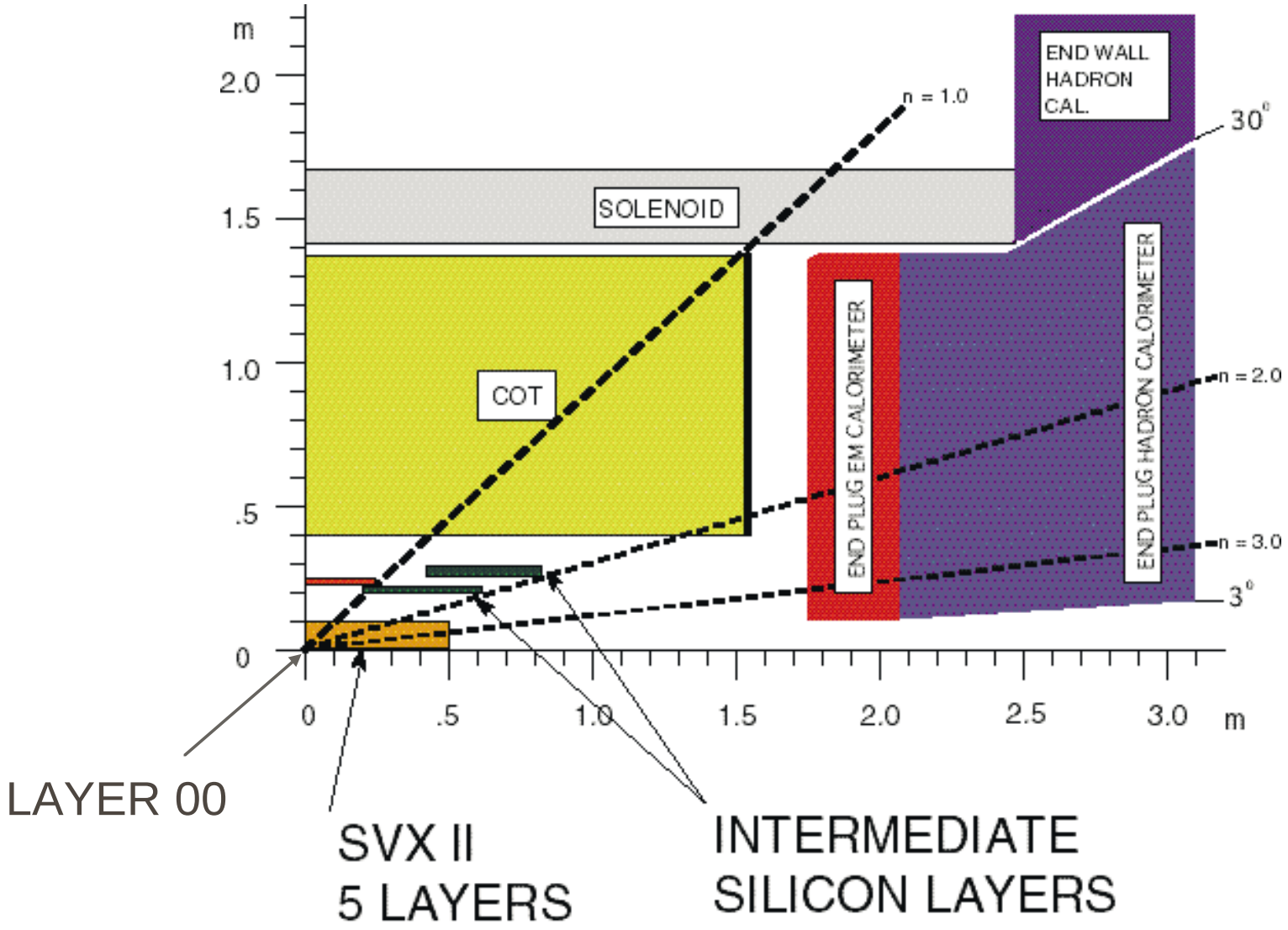
	Single tag eff. (%)	***Double tag eff.(%)***
SVX + CTC (Run 1)	37.6 ± 1.0	6.9 ± 0.5
SVXII + COT	46.7 ± 1.1	8.7 ± 0.6
SVXII + ISL + COT	60.1 ± 1.0	15.1 ± 0.8

- Improve B physics capability of the experiment

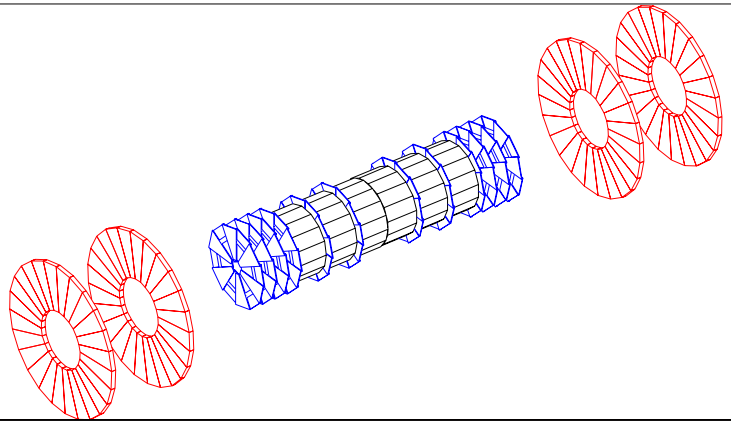
CDF II Detector - Run II Configuration



Quadrant of CDF II Tracker

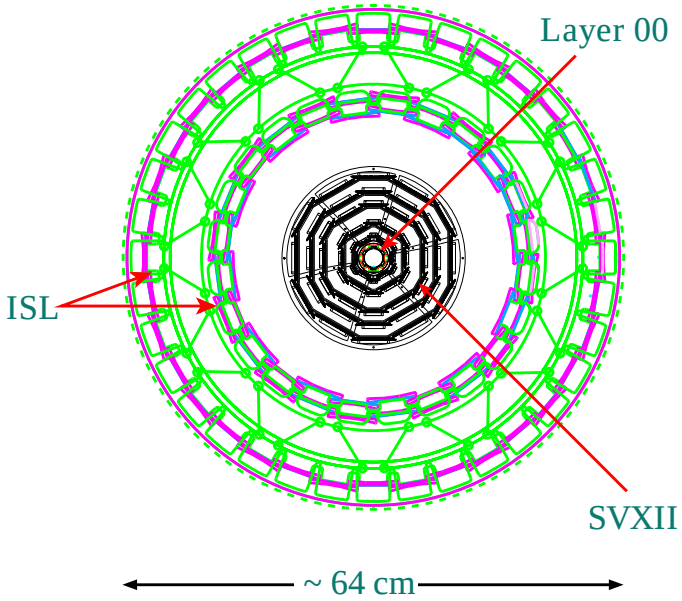


Fermilab Run II Silicon

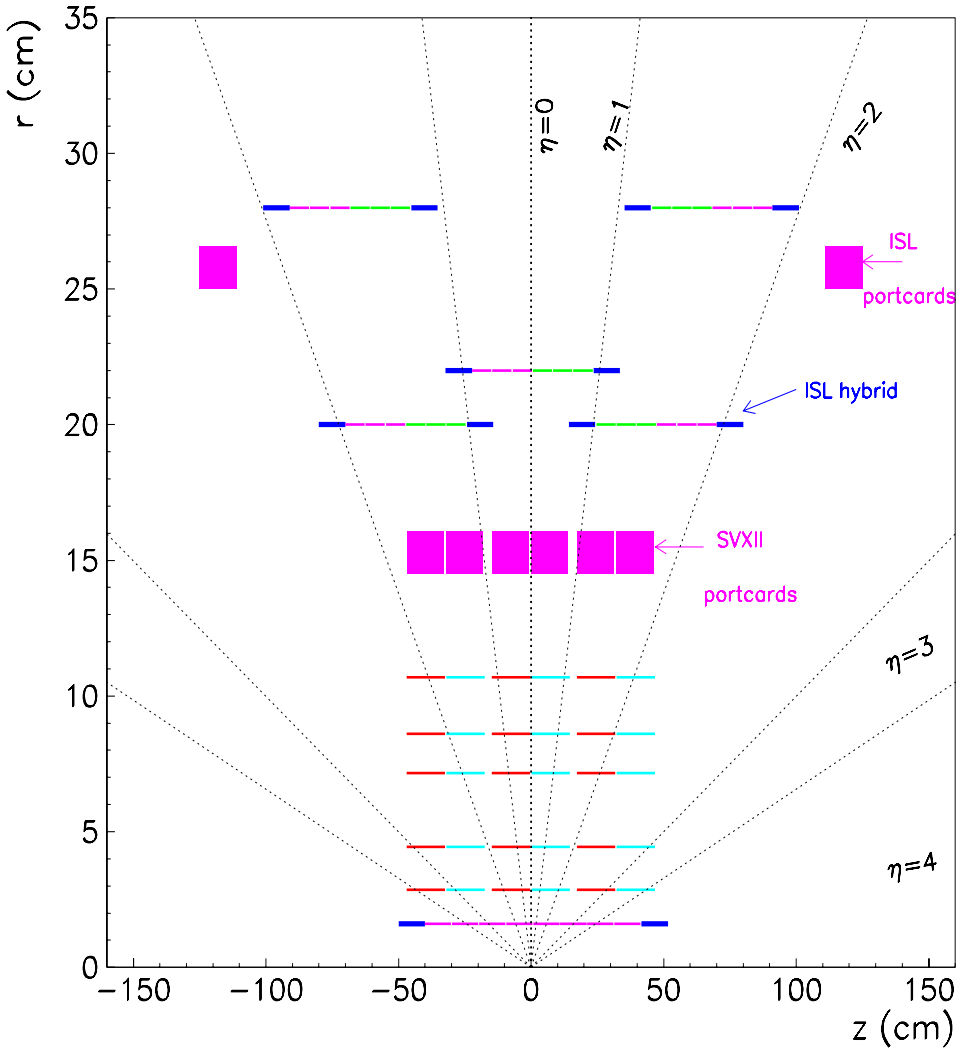


DØ	6 Barrels	F Disks	H Disks	Totals
Layers/planes	4	12	4	
Δ_z	77 cm	48 cm	10 cm	
Channels	387120	258000	147456	792576
Modules	432	144	192	768
Readout Length	12 cm	7.5 cm	14.9 cm	
Inner Radius	2.7 cm	2.6 cm	9.5 cm	2.6 cm
Outer Radius	9.4 cm	10.5 cm	26 cm	26 cm

CDF	Layer 00	SVX II	ISL	Totals
Layers	1	5	2	8
Length	0.9 m	0.9 m	1.9 m	
Channels	13824	405504	303104	722432
Modules	48 SS	360 DS	296 DS	704
Readout Length	14.8 cm	14.5 cm	21.5 cm	
Inner Radius	1.35 cm	2.5 cm	20 cm	1.35 cm
Outer Radius	1.65 cm	10.6 cm	28 cm	28 cm
Power	~100 W	1.4 kW	1.0 kW	1.5 kW



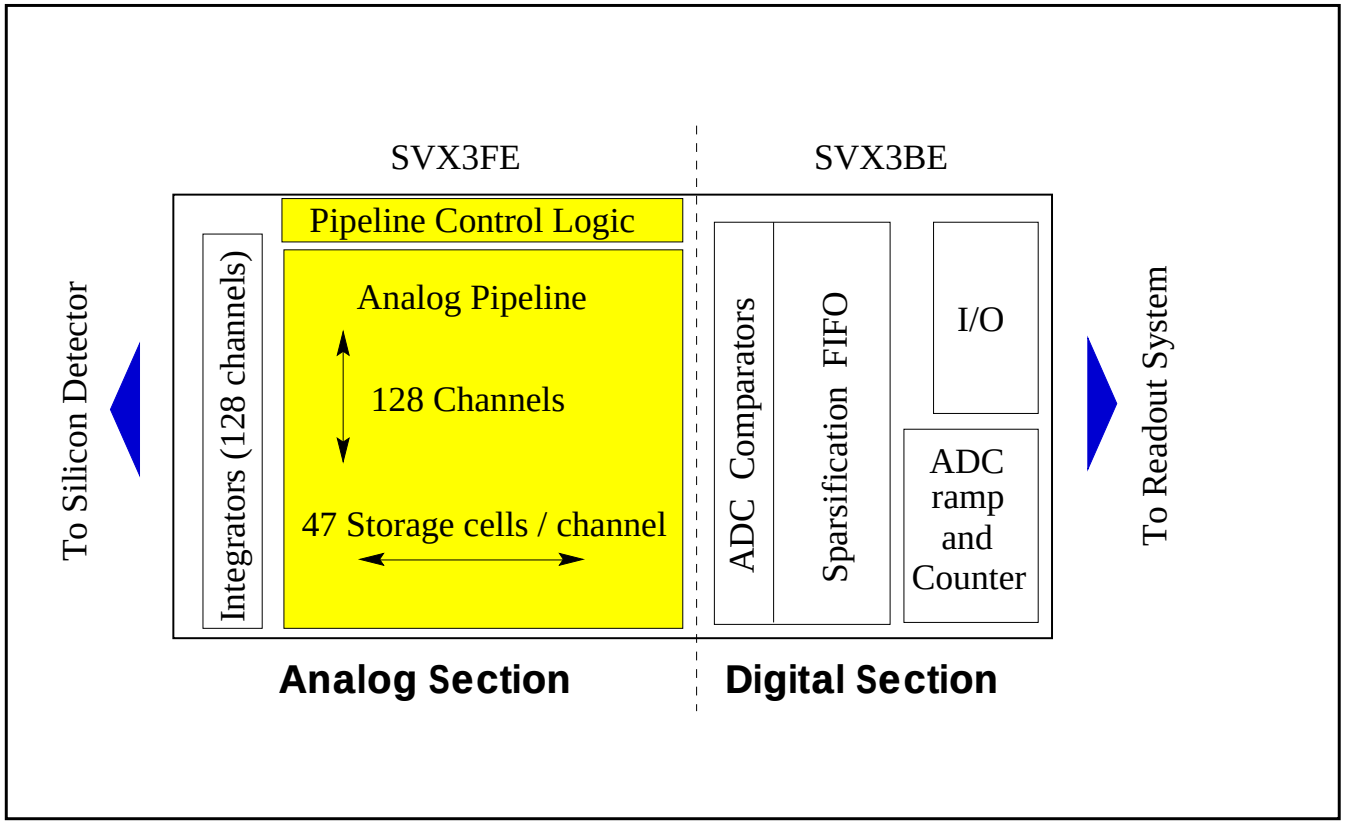
CDFII Silicon Tracker: Layer 00 + SVXII + ISL



Goals and Features:

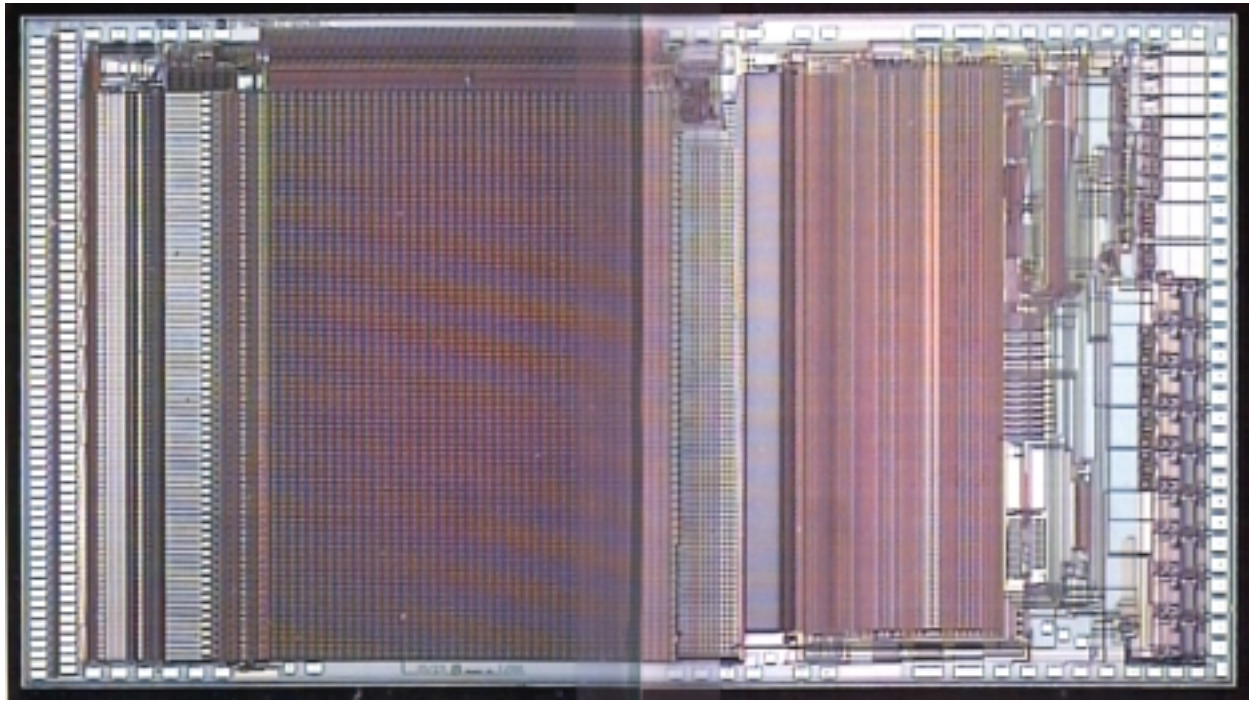
- Precise 3D track impact parameters
  - **B tagging: top, SUSY, Higgs**
  - **B Physics**
- Improved forward coverage
  - **$0 \leq |\eta| \leq 2$**
- Level II displaced-track trigger (SVT)
  - **Hadronic B decays**
  - **Calibration triggers**
- Improved p_T resolution
- High tracking efficiency with good purity

SVX3D R/O Chip



- Rad-hard 0.8 um Honeywell CMOS
- Tested to ~ 4 MRad
- Deadtimeless
- Dynamic pedestal subtraction
- Common to all Run II CDF silicon projects

SVX3D R/O Chip



Readout Chip Specifications

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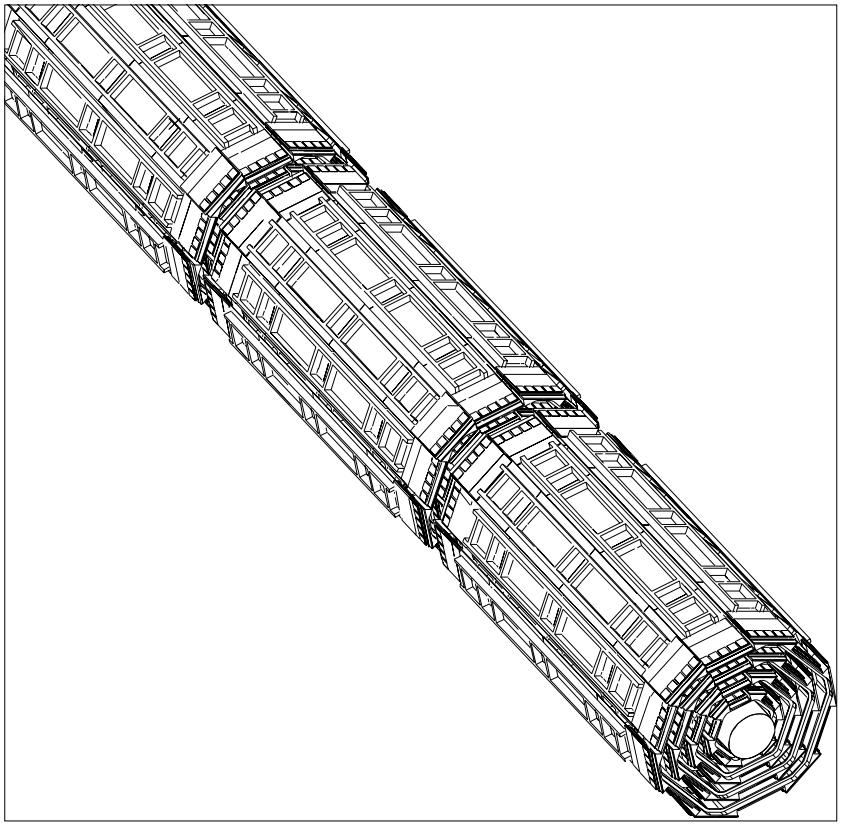
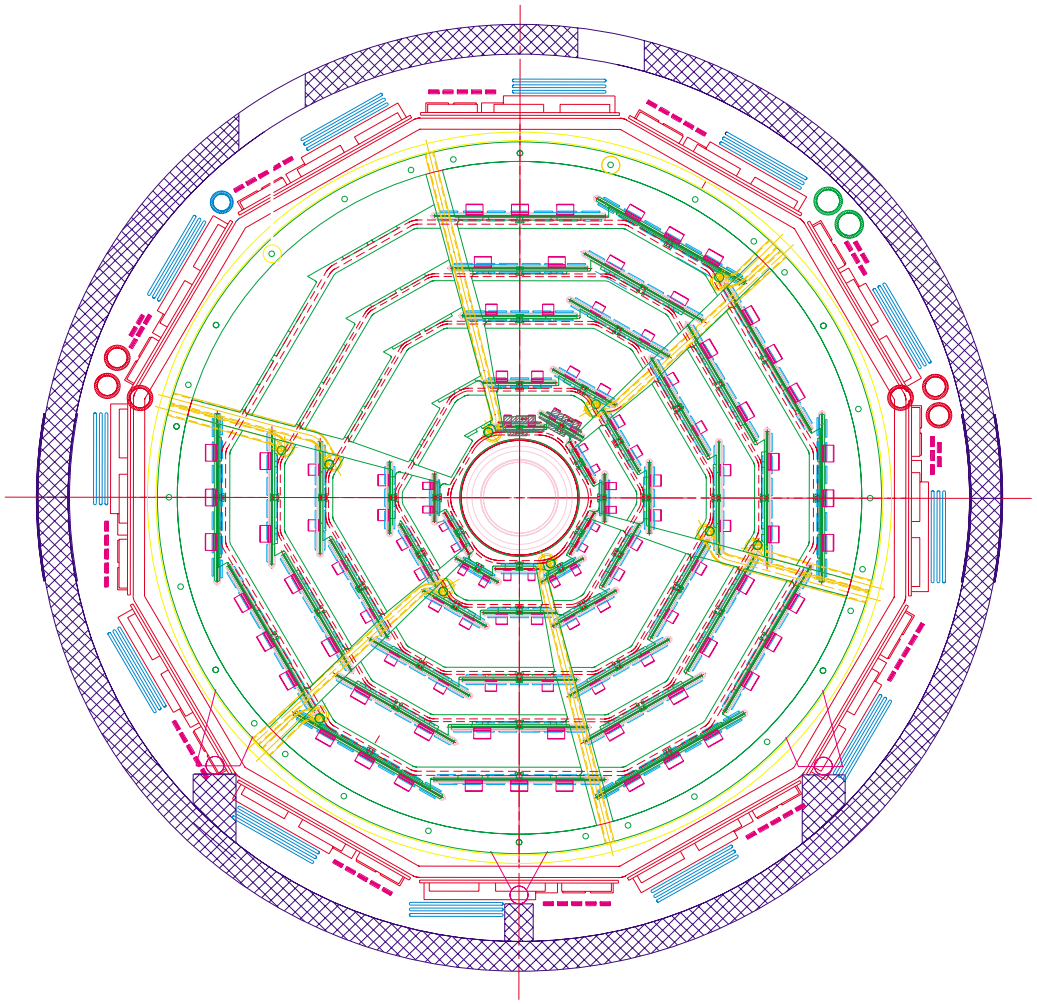
Specification	Description	Value or Range
GENERAL		
Power	Power dissipation depends on L1 rate	350 mW-450 mW
Noise	ENC versus cap. at min and max BW	500 e + 21 e/pF -- 750 e + 53 e/pF
Radiation hardness	Meet operating specs after dose	1.5 MRad
PREAMPLIFIER		
Input channels	Charge to voltage amplifier	128 parallel channels
Polarity	Polarity of the input signal	Selectable at initialization
Gain	Preamplifier gain	5.0 mV/fC
Gain variation	Channel to channel gain variation	< 0.5 mV/fC
Dynamic range	Linear range of preamplifier	≥ 450 fC
Rise time	10-90% rise time @ 22 pF	10ns-62ns
Maximum rise time	Maximum rise time versus capacitance	≤ 2.8 ns/pF
Reset time	Preamplifier reset time	≤ 1.6 μs
PIPELINE		
Length	Analog dual ported pipeline length	42 cells-length selectable at initialization
Buffer	Number of cells for L1 accept	4 cells
Speed	Variable depending on clock speed	100ns-400ns
Gain	Pipeline read/write amplifier gain	3.0 V/V
Gain variation	Variation in pipeline gain	≤ 1 mV
Reset time	Time to clear old and setup for new	25 ns
ADC		
Principle feature	Digitization of 128 channels in parallel	NA
Bits	Number of bits utilized	7 bits
Gain	Selectable with external resistor	300-4000 e/count
Pedestal	Selectable with external resistor	0-63 counts
Threshold	Selectable	0-127 counts
Threshold variation	Channel to channel threshold variation	≤ 1000 e
Time	Time to digitize 7 bits	≤ 1.2 μs
Sparse	Sparsification of data an option	Yes with nearest neighbor option
Speed	Readout of digitized data	≥ 53 Mbytes/s
INPUT/OUTPUT		
Differential	Protocol for differential signals	LCDS 2.5 V ± 0.1 V swing
Single ended	Protocol for single ended signals	0-5 V CMOS

SVX II Collaboration

Academia Sinica, Taiwan
Fermilab
Harvard University
Hiroshima University
The Johns Hopkins University
Lawrence Berkeley National Laboratory
University of New Mexico
University of Padua
University of Pittsburgh
Purdue University
University of Rochester
Rutgers University
Texas A&M University
Texas Tech University
Toronto University
Yale University

SVX II: 3 Barrels, 5 Layers





SVX II vs. Previous Detector

	SVX'	*SVX II*
Readout Coor	r-ϕ	r-ϕ, z
# of Barrels	2	3
# of layers / barrel	4	5
# of wedges / barrel	12	12
Ladder length	25.5 cm	29.0 cm
Barrel length	51 cm	87 cm
Layer geometry	3^{o} tilt	staggered radii
Radius inner layer	3.0 cm	2.44 cm
Radius outer layer	7.8 cm	10.6 cm
r-ϕ readout pitch	60;60;60;55 μm	60;62;60;60;65 μm
r-z readout pitch	absent	141;125.5;60;141;65 μm
Length readout channel (r-ϕ)	25.5 cm	14.5 cm
r–ϕ chips / ladder	2;3;4;6	4;6;10;12;14
r-z chips /ladder	absent	4;6;10;8;14
r–ϕ channels	46,080	211,968
r-z channels	absent	193,536
Total channels	46,080	405,504
Total chips	360	3168
Total detectors	288	720
Total Ladders	96	180

SVXII Parameters

SVX II Parameters	
Number of Barrels	3
Active length per barrel	29 cm
Number of layers	5
Readout coordinates per layer	Φ+z / Φ+Φ'
Radius of inner and outer layers	2.45 cm, 10.6 cm
Ladders per barrel-layer = Φ sectors	12
Each 1/2 ladder is one electrical unit of length	14.5 cm
Total number of electrical Φ sector wedges	72
Readout channels: Φ	211,968
Readout channels: z	193,536
Total	405,504

parameters per layer	Φ readout (inner to outer radius)					z readout (inner to outer radius)				
z, Φ' angle (deg)	0	0	0	0	0	90	90	1.2	90	-1.2
readout pitch pitch (μm)	60	62	60	60	65	141	126	60	141	65
Readout chips (128 channel) per 1/2 ladder	2	3	5	6	7	2	3	5	4	7

Silicon Specifications

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SVX II silicon sensor specifications for Hamamatsu (90° layers 0,1, 3) and Micron (1.2° layers 2, 4)

Table 1: Electrical specifications of the sensors

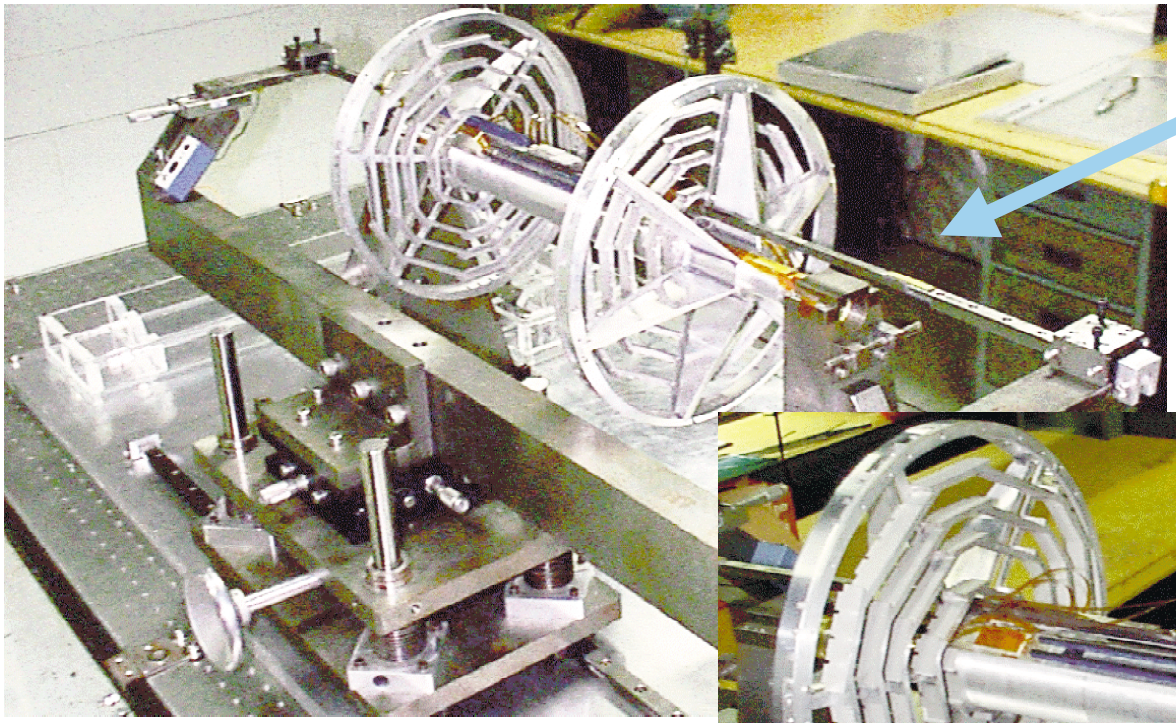
Specifications:	Description:	Hamamatsu:	Micron:
$I_{leakage}$	current from bulk, surface, and edge	<50nA/cm^2 100V, 20 C	<100nA/cm^2 at 80 V, 20 C
$dI_{leakage/dV}$	change in leakage current	<0.12nA/V/cm^2?	--
$V_{depletion}$	depletion voltage	45V<V_{dep}<80V	--
rho	bulk resistivity	--	Approx.=3KOhmcm
$V_{junction\_break}$	junction breakdown with open readout	>200V	>150V
$V_{micro\_discharge}$	onset voltage of micro-discharge (balanced bias, readout grounded, n & p side)	>150V	>150V
V_{break}	breakdown of voltage of coupling capacitor	>100V	>120V
$R_{interstrip}$	interstrip resistance	>2 GOhm	>2 GOhm
R_{bias}	polysilicon resistor value, variation p-side n-side	2.5±1.0 MOhm 3.5±1.0 MOhm	2.5±0.5 MOhm 2.5±0.5 MOhm
$R_{implant}$	resistivity of implant strip	<100 KOhm/cm	--
R_{Al}	resistivity of Al layers	<25 Ohm/cm	<30 Ohm/cm
C_C	capacitance of coupling capacitor	>10 pF/cm	>12 pF/cm
C_{total}	total capacitance (full length at bias voltage of 1.2 x Vdepletion) p-side n-side	<(10,10,10) pF <(13,14,15) pF	<10 pF <10 pF
Bad Strips	number of bad strips	<3% on all, <2% average	<3% on all, <2% on at least half

Table 2: Mechanical properties and specifications of the sensors.

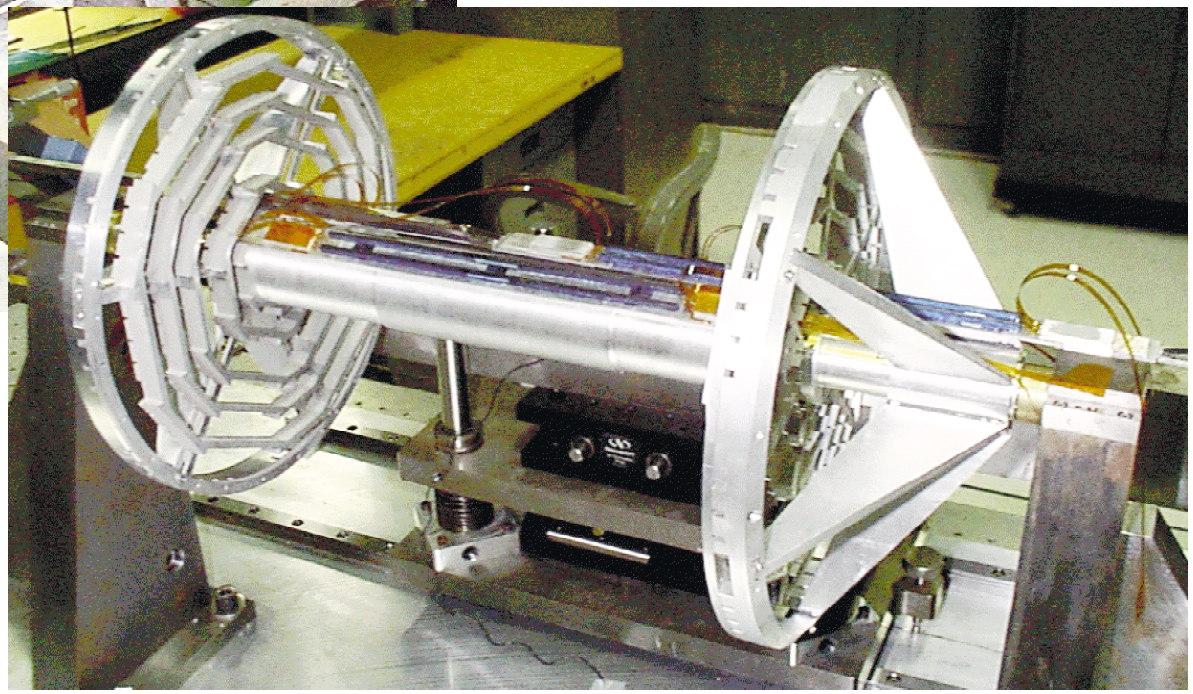
Property:	Layer 0:	Layer 1:	Layer 2:	Layer 3:	Layer 4:
stereo angle, n-strips (deg.)	90	90	-1.2	90	+1.2
number of production sensors+	144	144	144	144	144
total width (mm)	17.14	25.60	40.300	47.80	60.170
total length (mm)	74.3	74.3	74.3	74.3	74.3
active width (mm)	15.4	23.8	38.340	46.10	58.175
active length (mm)	72.43	72.43	72.38	72.43	72.38
thickness (um)	300±15	300±15	300±25	300±15	300±25
flatness#	<100	<100	<100	<100	<100
Phi strips	256*	384*	640*	768	896*
Z strips	512*	576*	640	512	896
Phi chips	2	3	5	6	7
Z chips	2	3	5	4	7
Phi strip pitch (um)	60	62	60	60	65
Z strip pitch (um)	141	125.5	60	141	65
2nd Al layer pitch (um)	58	60	--	60	--
bond pads (um)	60x200	60x200	60x150	60x200	60x150
Phi implant width (um)	14	14	15	14	15
Z implant width (um)	20	20	15	20	15
Al width, n and p (um)	8	8	10	8	8
p-stop width, common (um)	21	21	28	21	30
p-stop width, individual (um)	15	15	--	15	--
implant to p-stop (um)	10	10	9	10	10
implant depth (um)	1.5±0.3	1.5±0.3	>0.75	1.5±0.3	>0.75
p-stop implant (boron/cm^2)	≥1x10^{14}	≥1x10^{14}	>5x10^{13}	≥1x10^{14}	>5x10^{13}
SiO_2 passivation, p-side (um)	3.0	3.0	1.0	3.0	1.0
SiO_2 passivation, n-side (um)	0.5-0.8	0.5-0.8	1.0	0.5-0.8	1.0
$C_{coupling}$ dielectric (um)	0.22SiO_2 +0.1Si_3N_4	0.22SiO_2 +0.1Si_3N_4	--	0.22SiO_2 +0.1Si_3N_4	--
double metal SiO_2 (um)	5	5	--	5	--

+Number of sensors does not include spares or rejects.
*Indicates 2 "dummy" strips are also present.
#Each sensor of thickness T must fit between plates seperated by T+100 um.

SVXII Barrel Fabrication



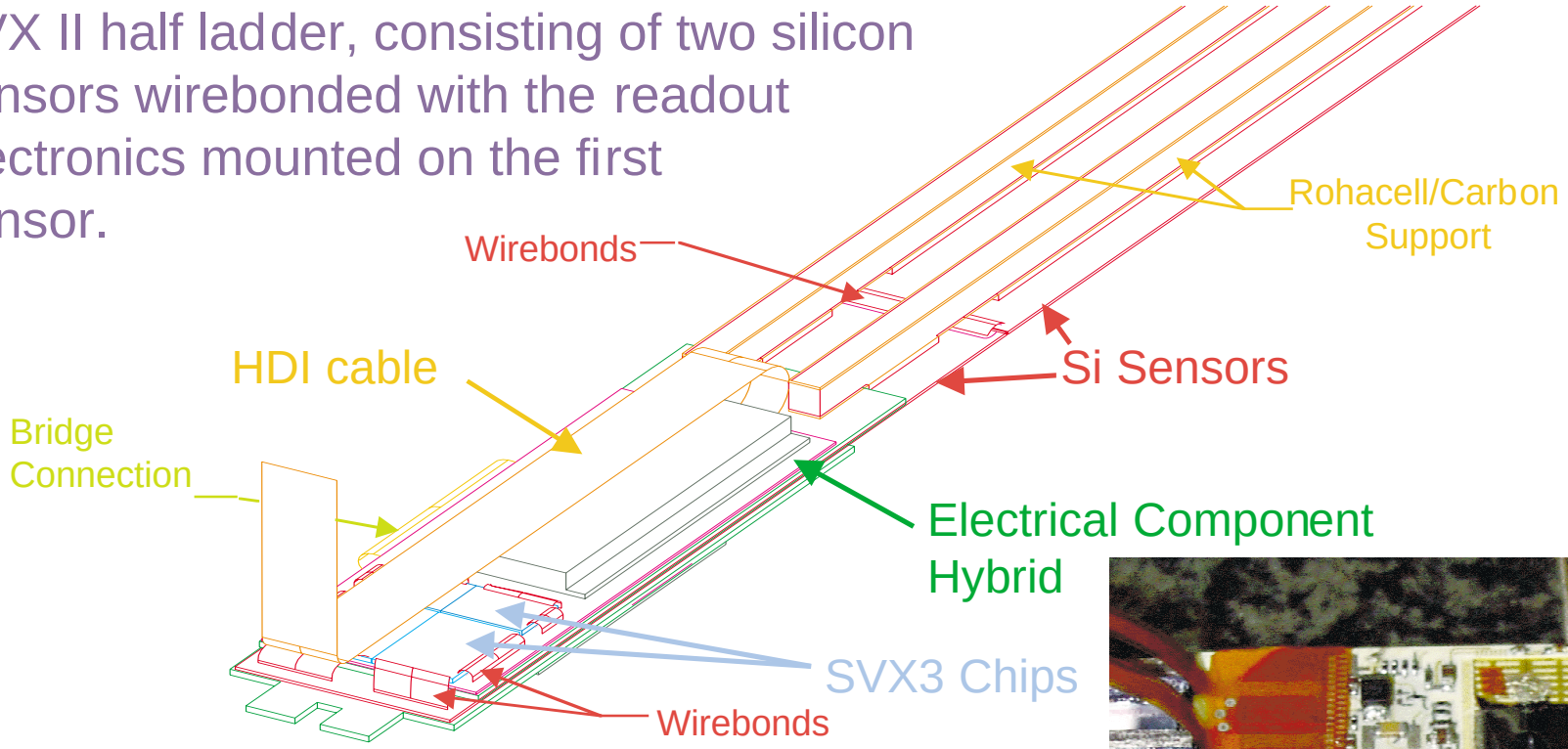
Fixture for installing SVX II ladders into barrel (precision aligned bulkhead pair)

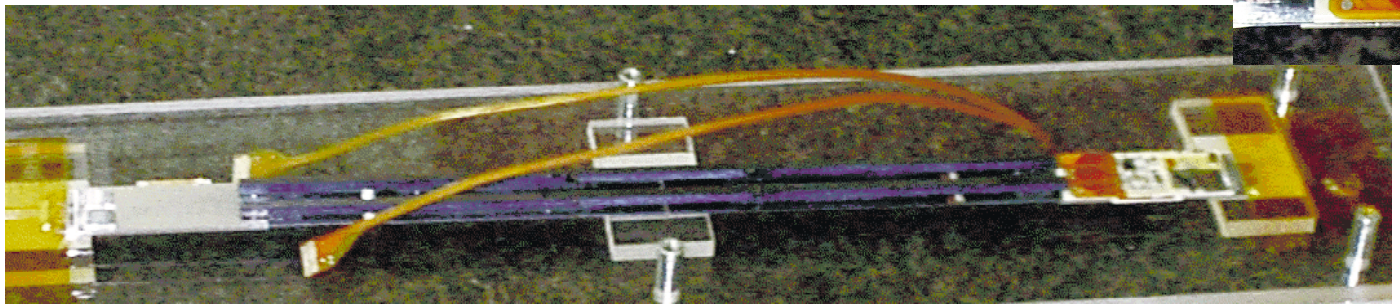


Test assembly with mock aluminum bulkheads and mechanically accurate ladders

SVX II Ladders

SVX II half ladder, consisting of two silicon sensors wirebonded with the readout electronics mounted on the first sensor.





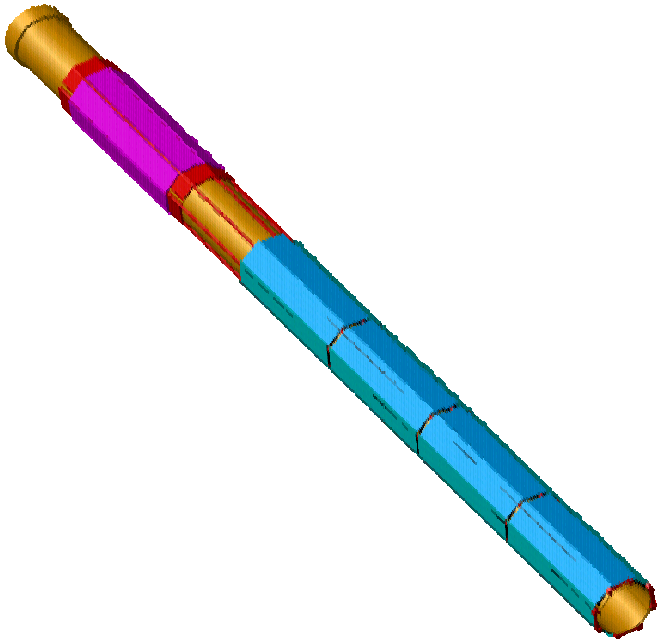
Layer 00 Collaboration

FNAL, INFN-Pisa, INFN-Padova,

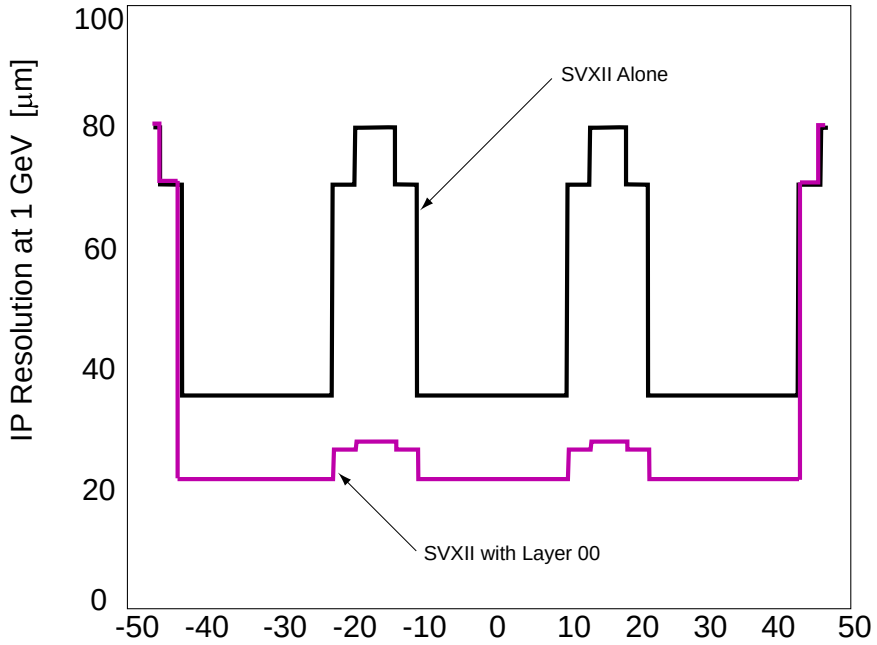
LBNL, Purdue,U.California-Davis,

U. Florida, U. Glasgow, U. Liverpool

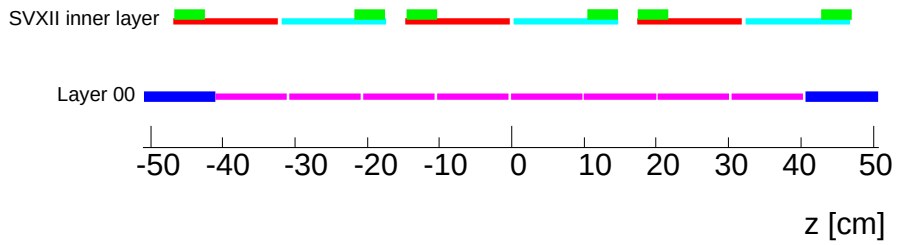
Layer 00



Resolution improvements:



- Beam pipe layer of 1-Sided Silicon
  - **Improve IP resolution**
    - Better B tagging for higgs, SUSY
  - **Extend useful lifetime**
  - **Long-term operational experience with LHC rad-hard silicon**



Layer 00 Design Values

Layer 00 Mechanical Specifications

General

Property	Value	Tolerance	Status	Notes
# channels	13,824	n/a	final	*
# phi segments	6 wide + 6 narrow	n/a	final	60 degree symmetry
R_{narrow}	1.35 mm	*	+/- 0.5mm	*
R_{wide}	1.62 mm	*	+/- 0.5mm	*
phi overlap	~30 strips	n/a	*	*
# z segments	6	n/a	final	2 sensors/z-segment
gap at z=0	10mm	*	+/-5 mm	*
operating temperature	5C	*	+/- 5C	*

Silicon Sensor Units

Property	Value	Tolerance	Status	Notes
# sensors / sensor unit	2	n/a	final	wirebonded together
sensor unit length	157.0 mm	*	+/- 1mm	2 X 78.4 + 0.2
# wide units	36	n/a	final	*
channels / wide unit	256	n/a	final	*
# narrow units	36	n/a	final	*
channels / narrow unit	128	n/a	final	*

Cabling

Property	Value	Tolerance	Status	Notes
# cables (total)	120	n/a	final	*
# cables / wide segment / end	6	n/a	final	3X(2/sensor unit)
# cables / narrow segment / end	4	n/a	final	2X(1/sensor unit) + 1X(2/sensor unit)

Hybrids

Property	Value	Tolerance	Status	Notes
# hybrids (total)	48	n/a	final	12 triplets + 36 doublets
# hybrids / wide segment / end	3	n/a	final	doublets (2 chips)
# hybrids / narrow segment / end	1	n/a	final	triplets (3 chips)

SVXII Inner Screen

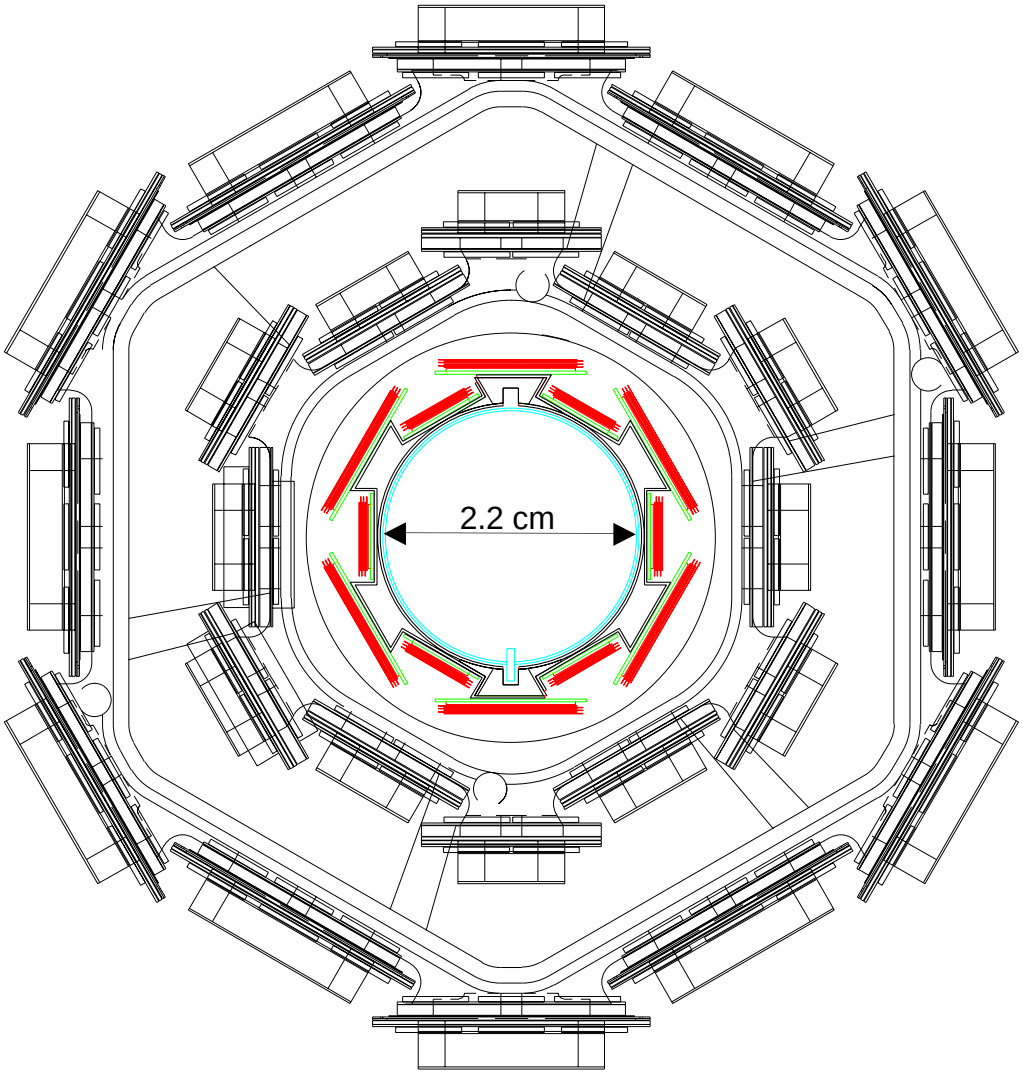
Property	Value	Tolerance	Status	Notes
composition	3-ply pre-preg carbon fiber	n/a	final	0-60-120 layup
length	960 mm	*	final	centered on z=0
outer radius	20.50 mm	*	final	*
inner radius	20.25 mm	*	+/- 0.05 mm	*

Cooling

Property	Value	Tolerance	Status	Notes
# cooling tubes	4	n/a	?	*
coolant	water/glycol	n/a	?	*
coolant temp	0C	*	?	*
tube R_{outer}	0.75mm	*	?	*

*Information not yet available
? = current best guess

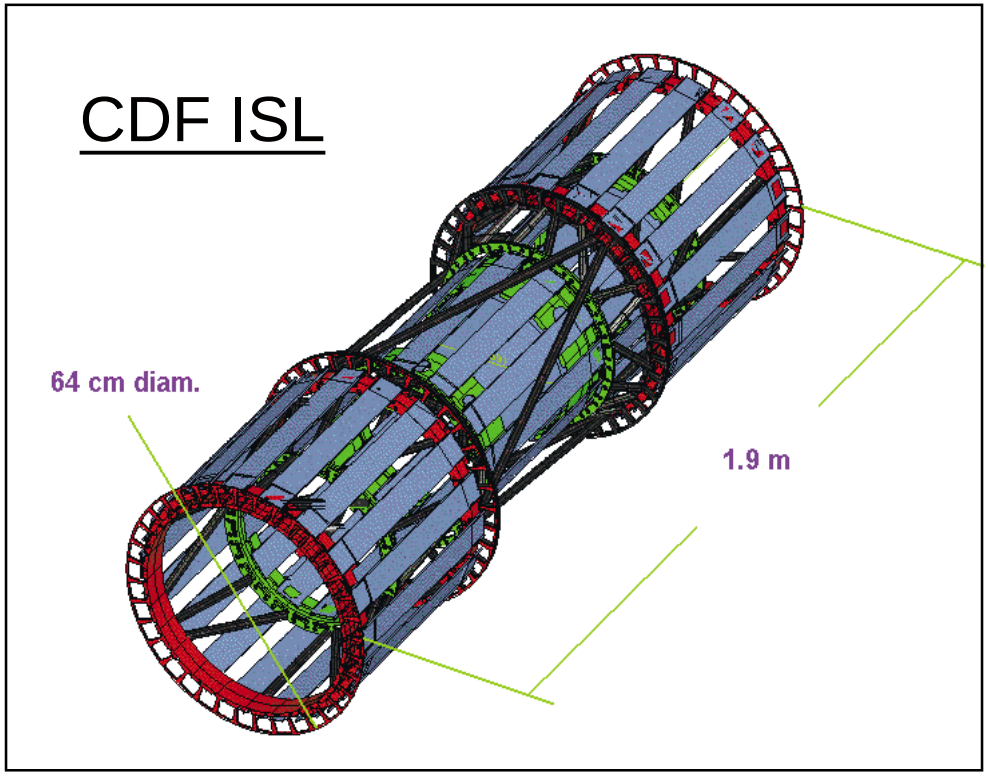
Layer 00 in SVX II



ISL Collaboration

FNAL, INFN-Pisa, INFN-Padova,
INFN-Bologna, LBNL,Texas A&M,
U.California-Davis, U.California-Los Angeles,
U. Cassino, U. Florida, U. Karlsruhe,
U. Rochester,U. Tsukuba, Osaka City University

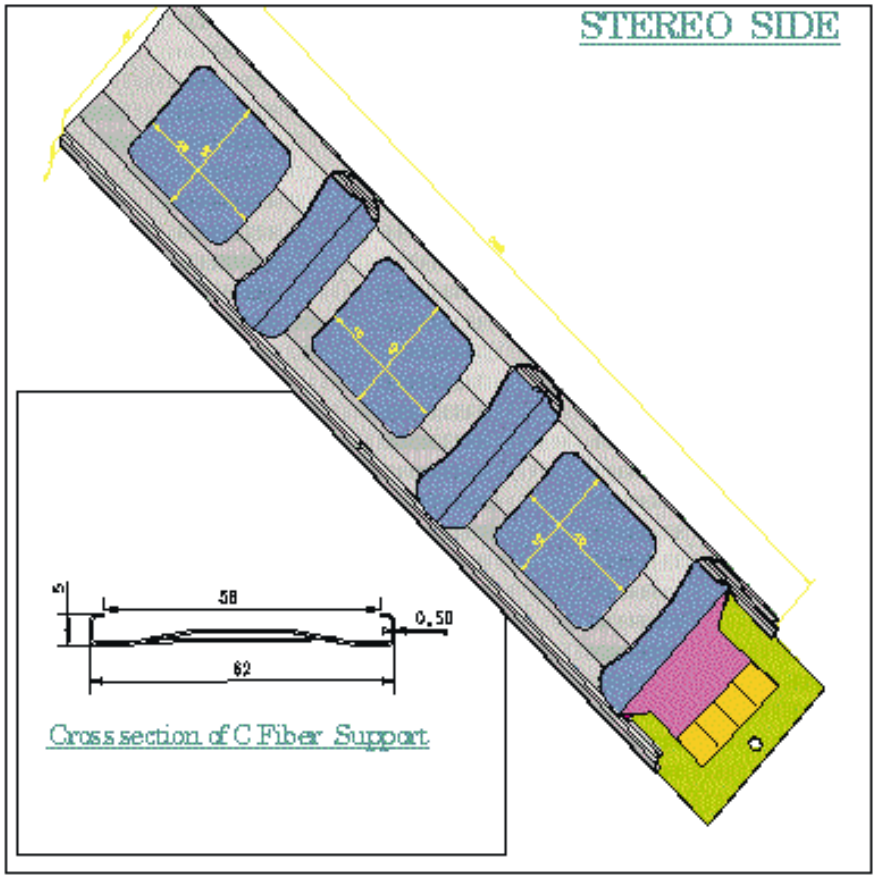
Intermediate Si Layers



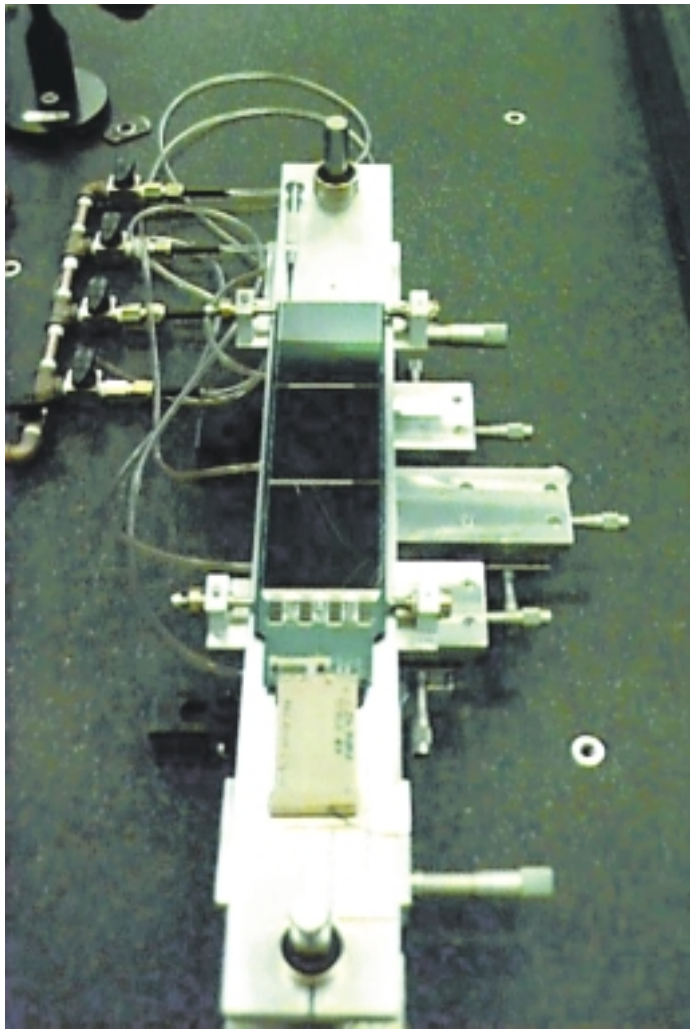
- CDF ISL: Proposal and Conceptual Design (FNAL). Final Design (Pisa).
  - **Emphasis on simplicity and low cost.**
- Space frame manufactured in Italy; INFN Pisa & FNAL are the main production sites (roughly half each).

ISL Modules

- Overview of Design
  - **C Fiber substrate**
    - All bond pads are accessible from both sides
  - **3 Sensors**
    - 112 μm pitch (both sides)
    - Double Sided 1.2º Stereo Angle
  - **Hybrid mounted off Silicon**
    - 8 readout chips per hybrid
- Module Production
  - **Mechanical Fabrication:**
    - less than 2 hours
  - **Wirebonding:**
    - 20 minutes per side (roughly 1 hour total w/setup)
  - **Testing & Repair**
    - Under study

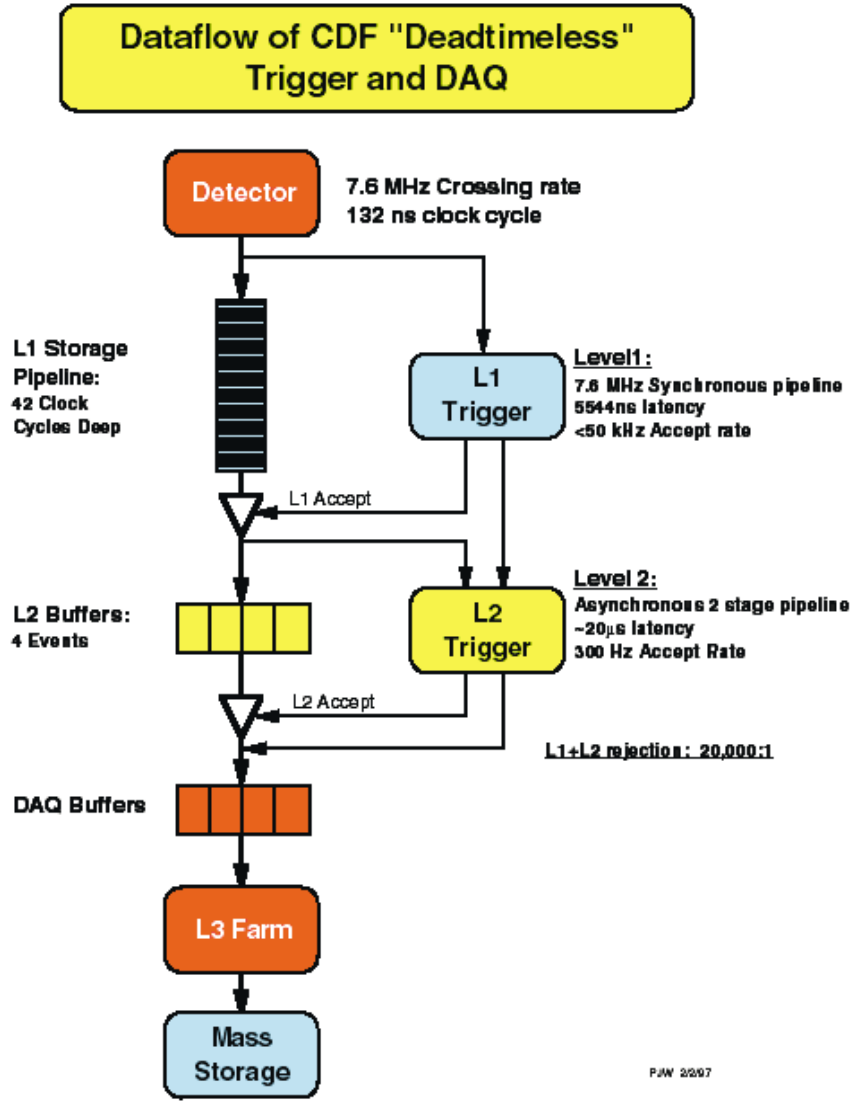


ISL Ladder Assembly



- Pilot production ladders
  - **Karslruhe fixtures refined w/use**
- Hybrids
  - **Expect all substrates end of summer**
  - **Prototypes operate as expected**
  - **Final assembly limited by SVX3D availability**

CDF Run II DAQ



- Fully pipelined DAQ+Trigger architecture (396 -->132 ns)
- Operates “deadtimeless”
- One of our largest subprojects
- Total board count >15,000.
- ~100 different custom boards
  - **~ 35 High volume boards (qty >100)**
- For SVX3D, everything up to L1 accept is on the chip
- SVT (not covered here) provides L2 displaced-track trigger

Silicon DAQ

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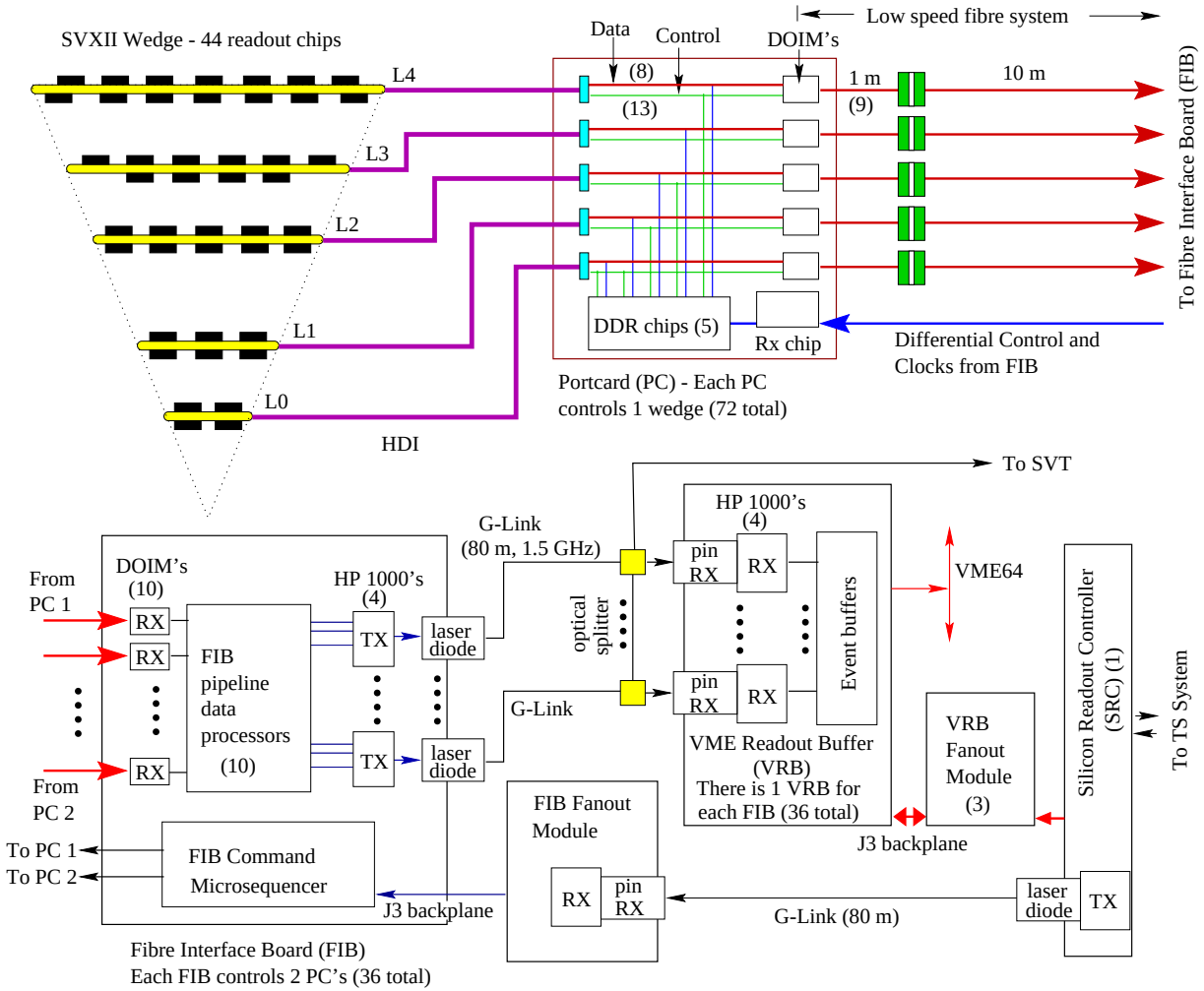
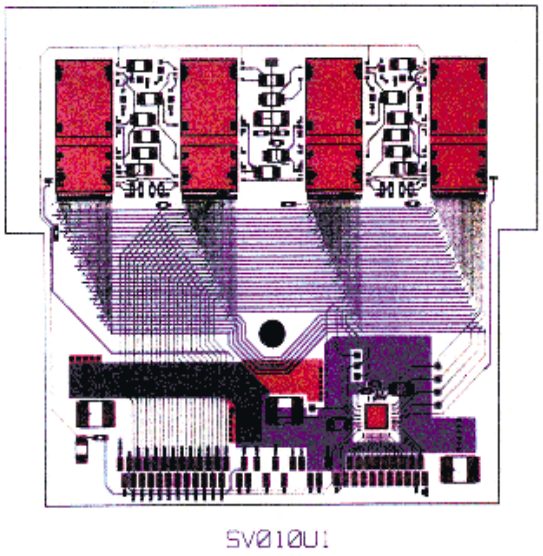
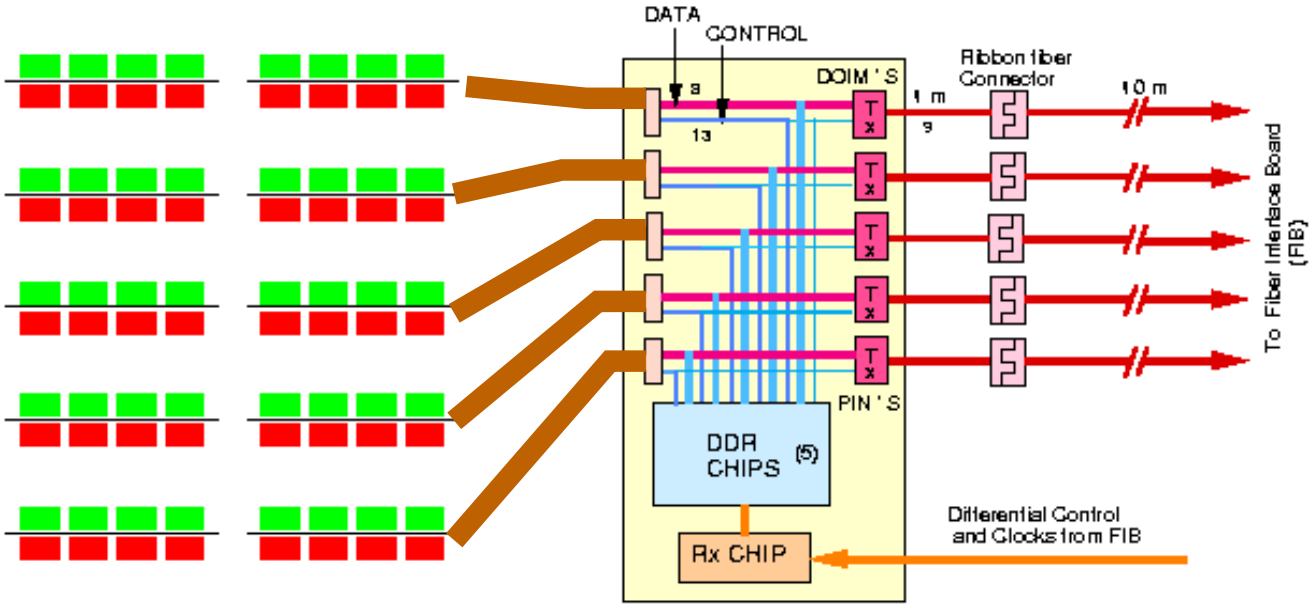
Component	Description
Hybrid	BeO ceramic circuit glued to silicon sensor surface (both sides). Local bus, bypassing etc for SVX3 chips.
HDI	Flex cable ladder to portcard: control & data signals, & power
Portcard	Multiplex controls and power to hybrids, transfer data from HDI (Cu) to DOIM (fiber).
DOIM	Dense Optical Interface Module: parallel fiber ribbon for data, 53 MHz, with laser diode array driver and pin diode array receiver. 5 DOIM links per portcard.
Control Link	Cu control signals and clock, and power to the portcard.
FTM	Fib Transition Module: DOIM receiver daughter board for the FIB.
FIB	Fiber Interface Board: send control sequences to chips, multiplex data10 DOIMs into 4 GLinks (22.5:1).
FFO	Fib Fan Out: fan out SRC command signals to FIBs, error handling.
GLink	Commercial 1.5 GHz fiber link: Controls (SRC to FFO) and data (FIB to VRB [and SVT]).
Fiber Splitter	Commercial optical splitter: FIB GLink to both VRB and SVT.
VTM	VRB Transition Module: GLink receiver daughter board for the VRB
VRB	VME Readout Buffer: data buffer for Level2 readout, data checking
VFO	VRB Fanout: Distribute commands to VRBs
SRC	Silicon Readout Controler: Master controller, trigger interface, synchronizes buffers with the rest of CDF, handles errors and recovery.
Power Supplies	Commercial power supplies for sensor bias and chip power, one per portcard.

SVXII DAQ


SVXII Wedge - 44 readout chips
L4
L3
L2
L1
L0
HDI
Data
Control
DOIM's
Low speed fibre system
(8)
(13)
1 m
(9)
10 m
To Fibre Interface Board (FIB)
DDR chips (5)
Rx chip
Differential Control and
Clocks from FIB
Portcard (PC) - Each PC
controls 1 wedge (72 total)
To SVT
G-Link
(80 m, 1.5 GHz)
HP 1000's
(4)
From
PC 1
DOIM's
(10)
HP 1000's
(4)
RX
TX
laser
diode
FIB
pipeline
data
processors
(10)
optical
splitter
pin
RX
Event buffers
VME64
G-Link
From
PC 2
VME Readout Buffer
(VRB)
There is 1 VRB for
each FIB (36 total)
VRB
Fanout
Module
(3)
Silicon Readout Controller
(SRC) (1)
To TS System
To PC 1
To PC 2
FIB Command
Microsequencer
J3 backplane
FIB Fanout
Module
J3 backplane
G-Link (80 m)
Fibre Interface Board (FIB)
Each FIB controls 2 PC's (36 total)

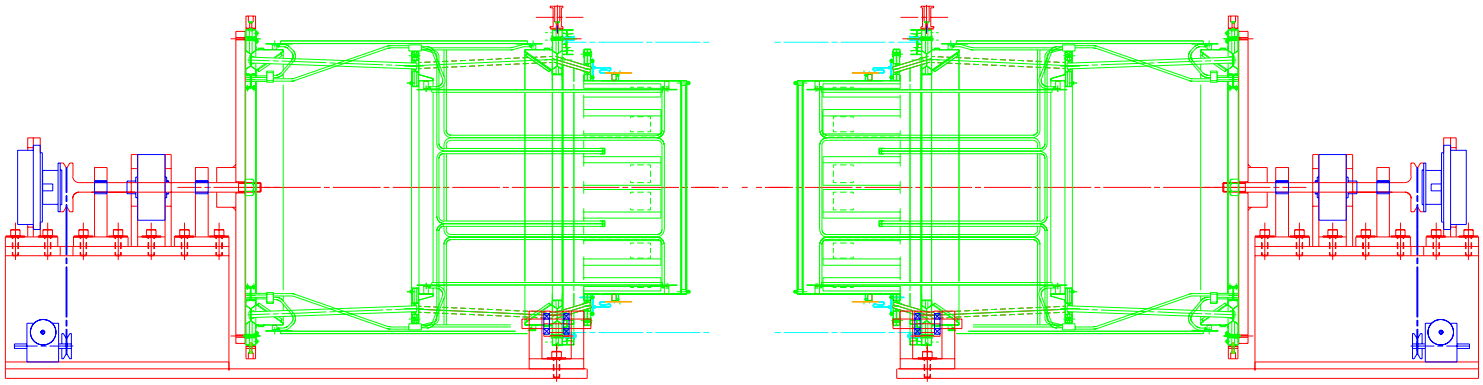
ISL DAQ

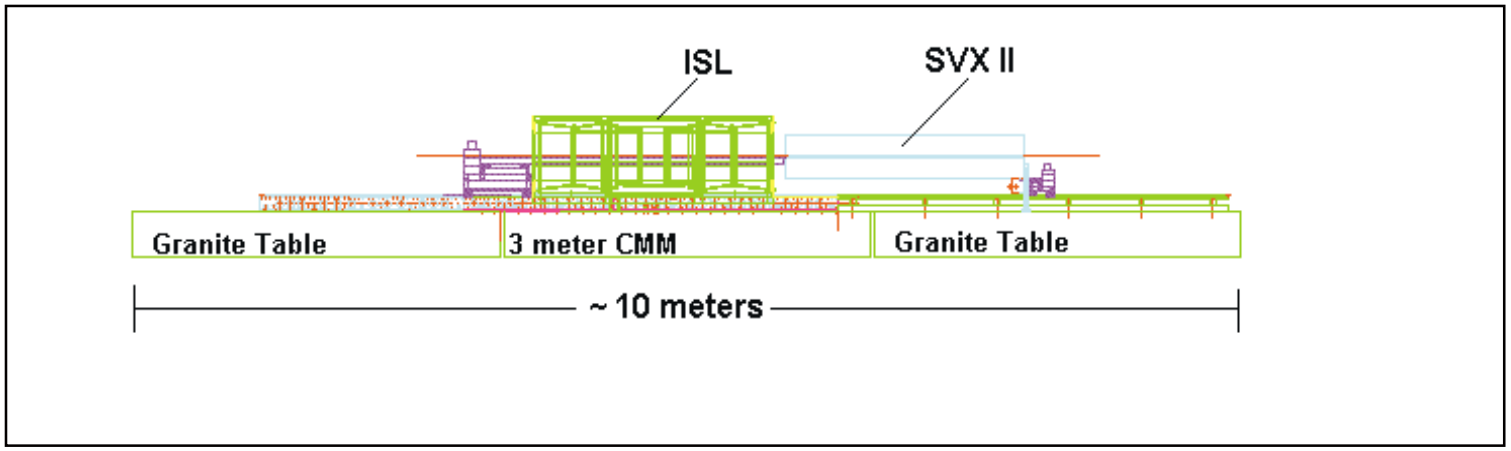




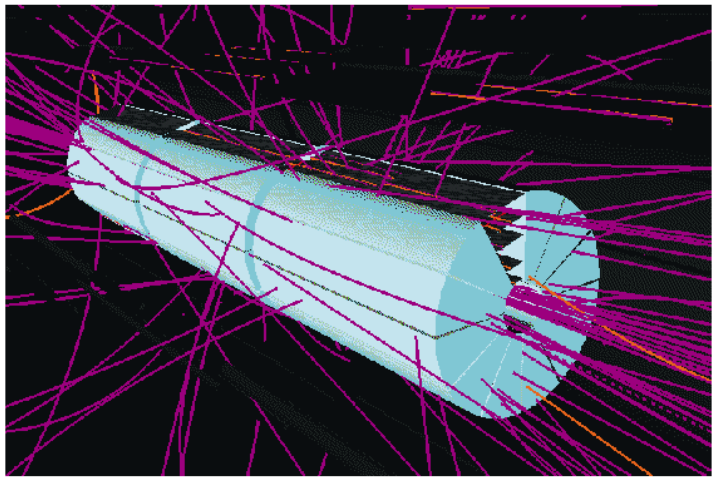
each HDI (and DOIM) has 16 chips
— 4 per side on each of two ladder ends

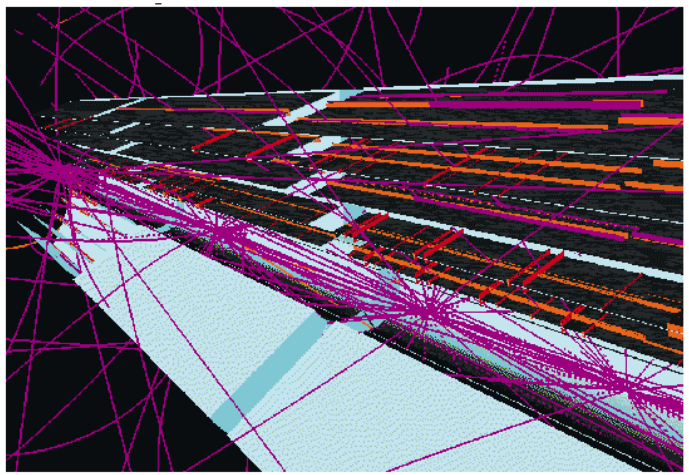
Final Assembly / Installation

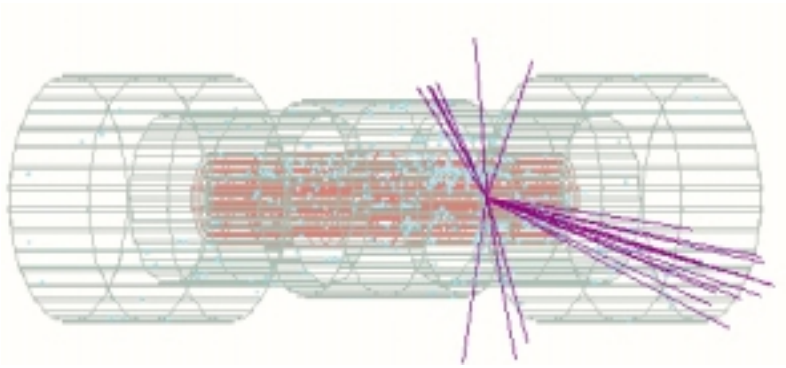


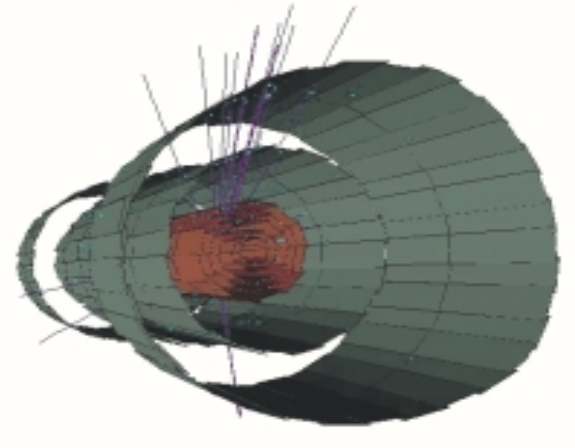


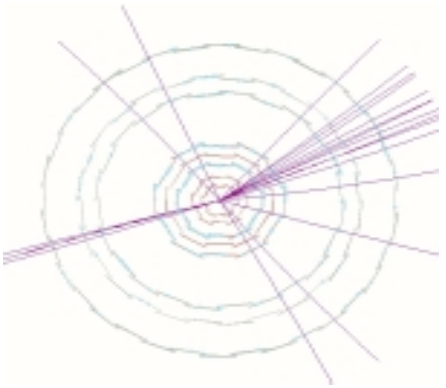
Simulation: Run II CDF Si









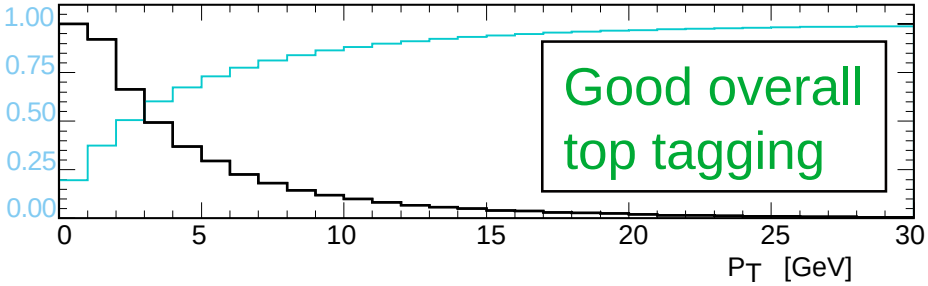


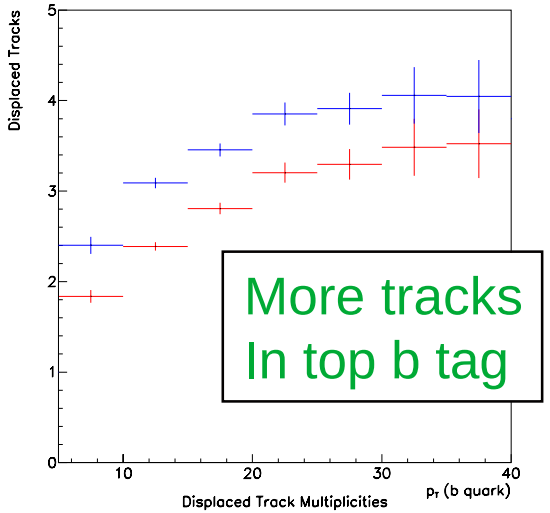
Open Inventor based

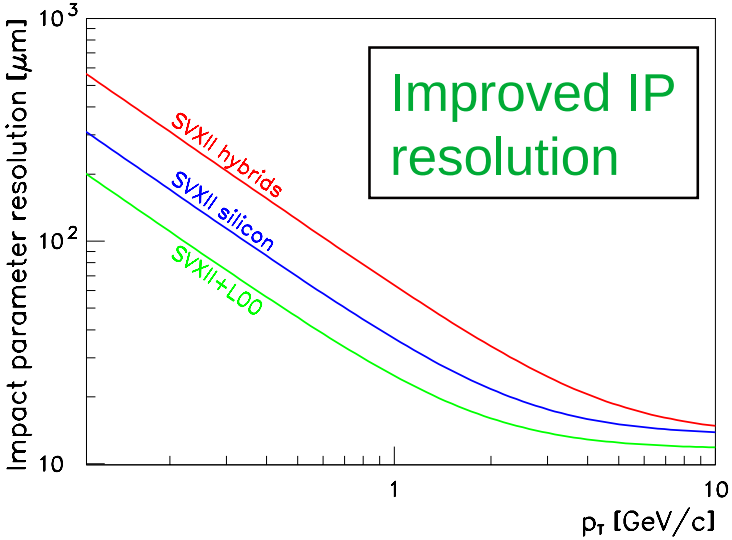
ROOT based

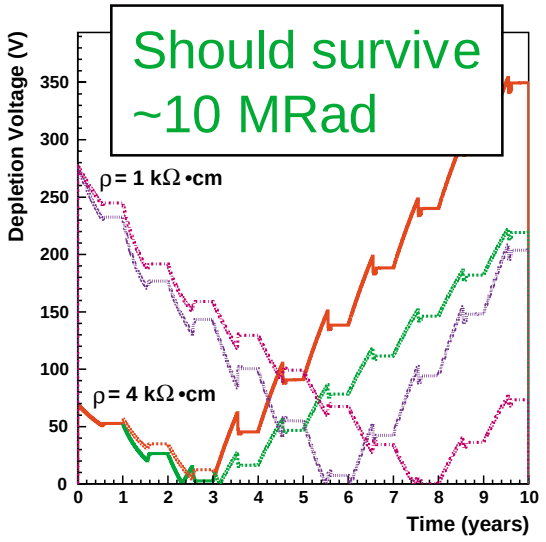
Expected Performance

- Reported previously for SVX II, ISL
- Improvements with L00:









Conclusions

- SVXII + ISL + L00 design provides complete silicon tracker that should give robust performance throughout Run II
- Silicon on track for complete delivery by early to mid 2000
- Hybrid substrates complete (SVXII) or will be soon (ISL, L00); population in progress
- SVX3D chip provides rad-hard deadtimeless operation

- PROBLEMS:
  - **Slow delivery of some silicon has delayed sensor production**
  - **Yield problems and other difficulties with Honeywell SVX3D**
  - **Infancy failures of some chips**
- SUCCESSES:
  - **Overall the projects are on track**
  - **Many problems solved**
  - **Installation sometime in 2000 should be possible**