

The D0 Silicon Microstrip Tracker



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Vertex 2004





Overview

- Design of the D0 Silicon Microstrip Tracker
- Detector status
- Performance tracking / vertexing
- Radiation
- Layer 0



DØ

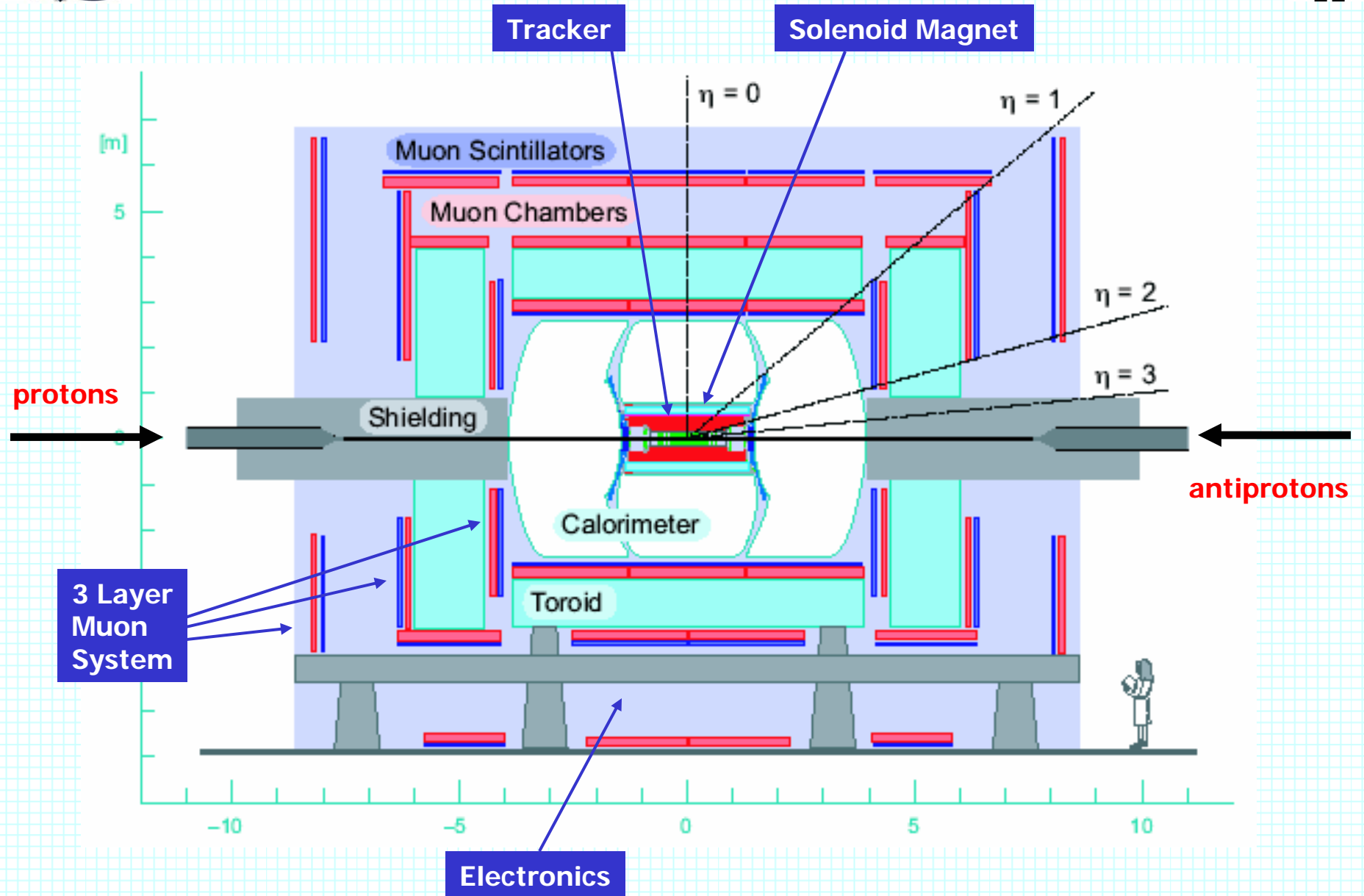
The DØ Collaboration

 AZ U. of Arizona CA U. of California, Berkeley U. of California, Riverside Cal. State U., Fresno Lawrence Berkeley Nat. Lab. FL Florida State U. IL Fermilab U. of Illinois, Chicago Northern Illinois U. Northwestern U. IN Indiana U. IA U. of Notre Dame Iowa State U. KS U. of Kansas Kansas State U. LA Louisiana Tech U. MD U. of Maryland MA Boston U. Northwestern U. MI U. of Michigan Michigan State U. NE U. of Nebraska NJ Princeton U. NY Columbia U. U. of Rochester SUNY, Stony Brook Brookhaven Nat. Lab. OK Langston U. U. of Oklahoma RI Brown U. TX U. of Texas at Arlington Texas A&M U. Rice U. VA U. of Virginia WA U. of Washington	 U. de Buenos Aires	 LAFEX, CBPF, Rio de Janeiro State U. do Rio de Janeiro State U. Paulista, São Paulo	 U. of Alberta Simon Fraser U.	 IHEP, Beijing
 Charles U., Prague Czech Tech. U., Prague Academy of Sciences, Prague	 LPC, Clermont-Ferrand ISN, IN2P3, Grenoble CPPM, IN2P3, Marseille LAL, IN2P3, Orsay LPNHE, IN2P3, Paris DAPNIA/SPP, CEA, Saclay IRIS, Strasbourg IPN, IN2P3, Villeurbanne	 U. San Francisco de Quito	 U. of Aachen Bonn U. U. of Freiburg U. of Mainz Ludwig-Maximilians U., Munich U. of Wuppertal	 Panjab U. Chandigarh Delhi U., Delhi Tata Institute, Mumbai
 FOM-NIKHEF, Amsterdam U. of Amsterdam / NIKHEF U. of Nijmegen / NIKHEF	 University College, Dublin	 KDI, Korea U., Seoul	 CINVESTAV, Mexico City	 JINR, Dubna ITEP, Moscow Moscow State U. IHEP, Prokino PNP, St. Petersburg
 Lund U. RIT, Stockholm Stockholm U. Uppsala U.	 Lund U. RIT, Stockholm Stockholm U. Uppsala U.	 Lancaster U. Imperial College, London U. of Manchester	 HCIP, Hochiminh City	

Amr Hassan, UC Riverside

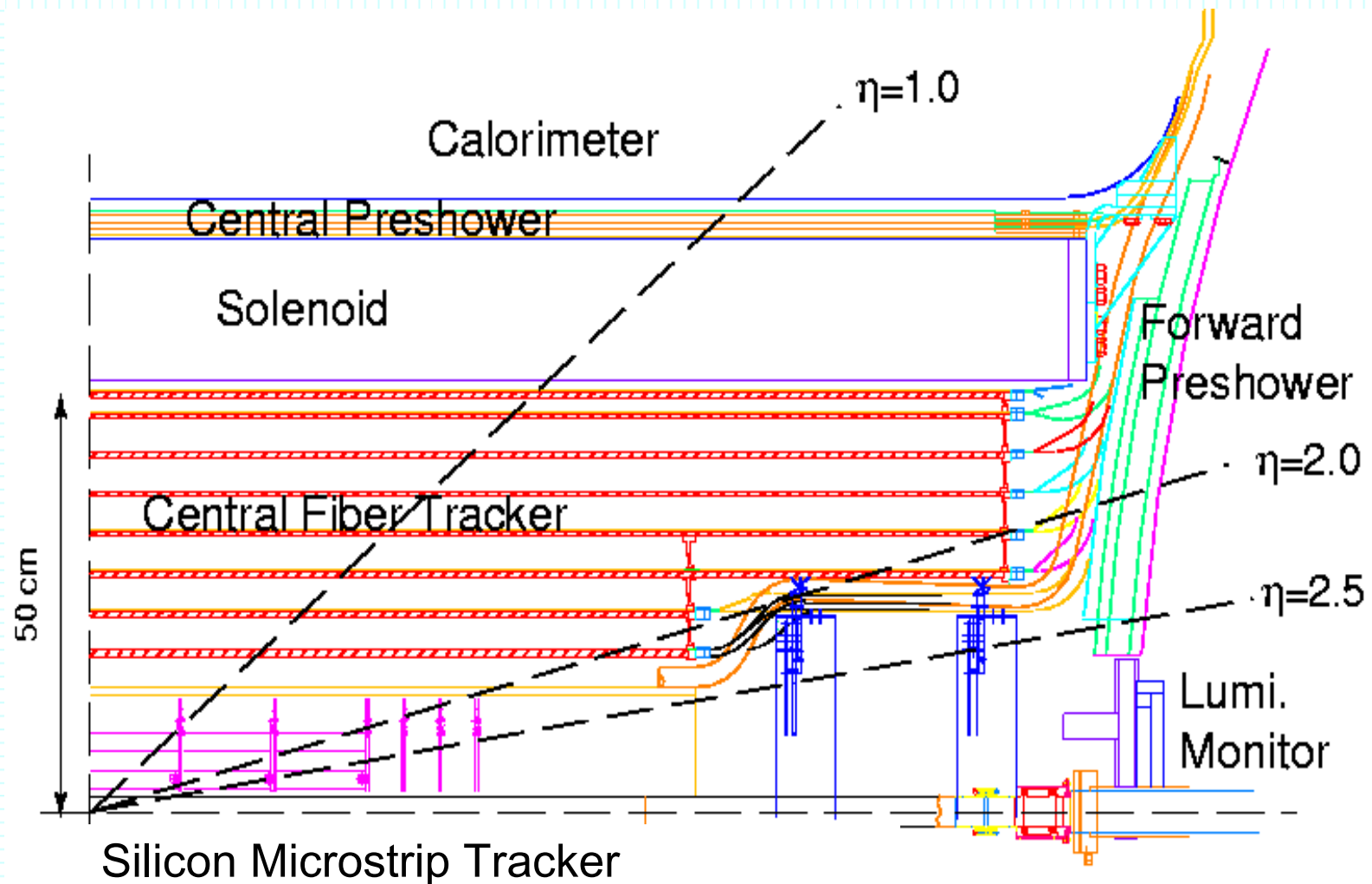


19 Countries
77 Institutions
~ 650 Collaborators
 ~ 100 postdocs
 ~ 140 grad. students





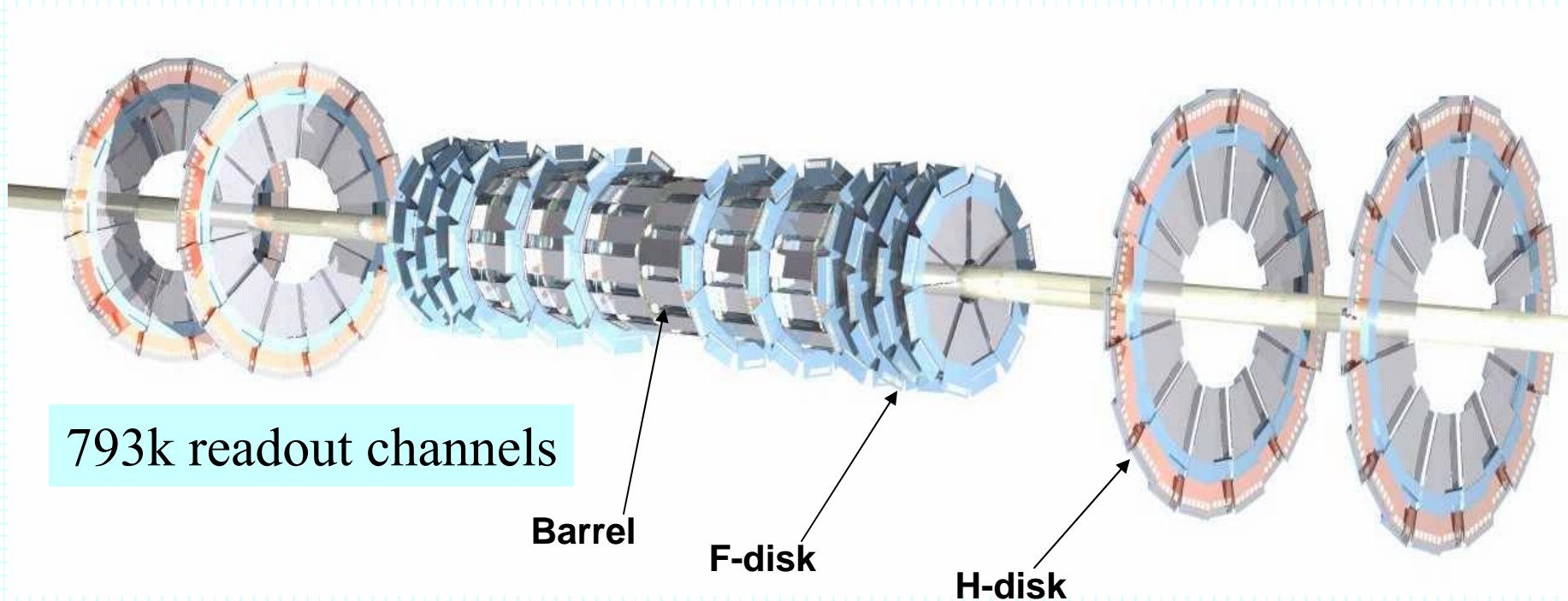
Inner tracker





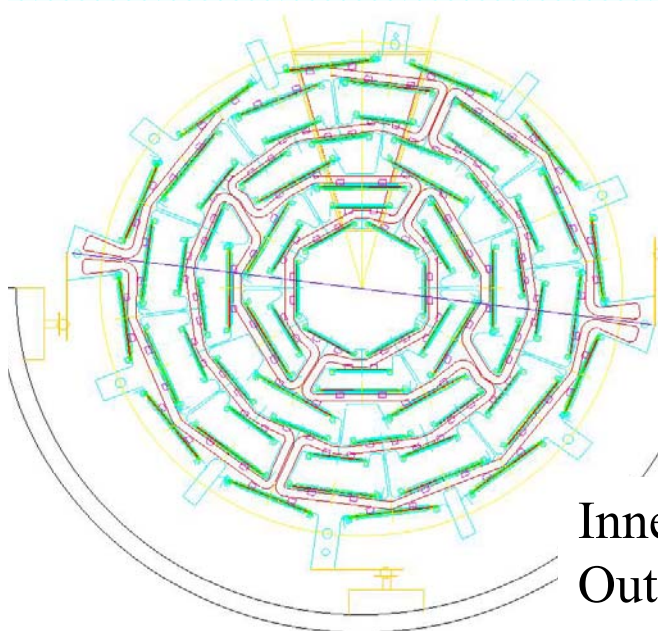
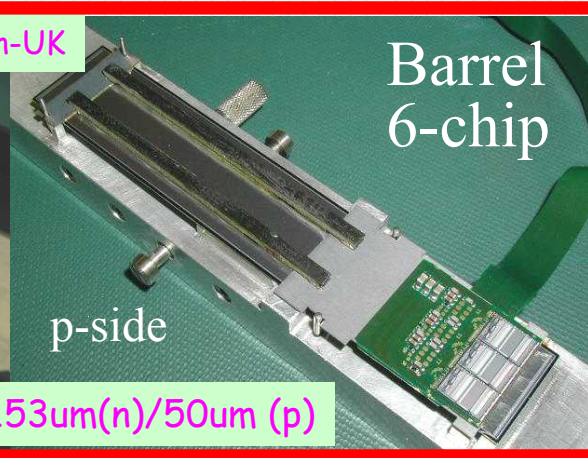
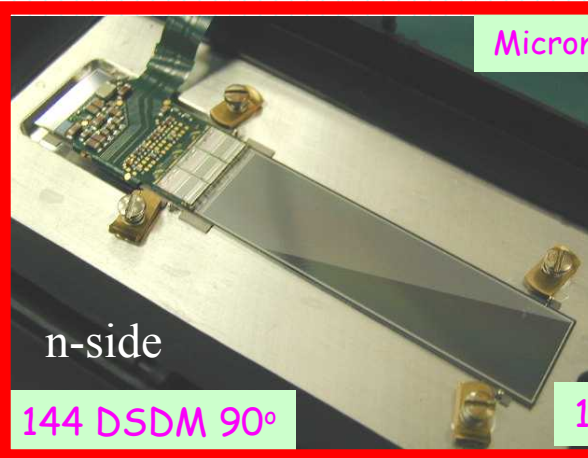
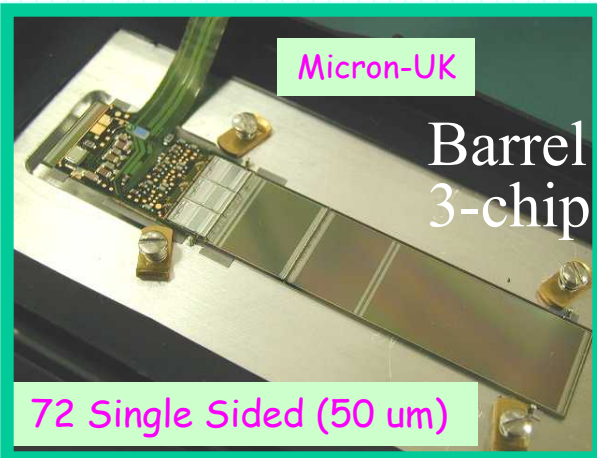
Silicon Tracker Design

- six 12cm long barrels (four detector layers) with interspersed disks (F-disks) for forward tracking
- External large area disks (H-disks) for forward tracking ($2 < |\eta| < 3$),
- 3D track reconstruction capabilities
- Good acceptance for high p_T tracks

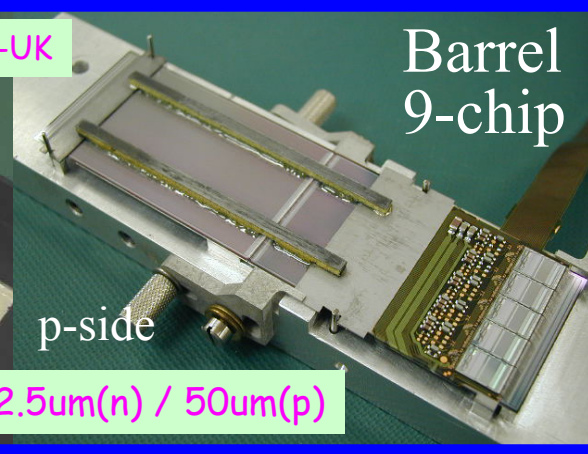
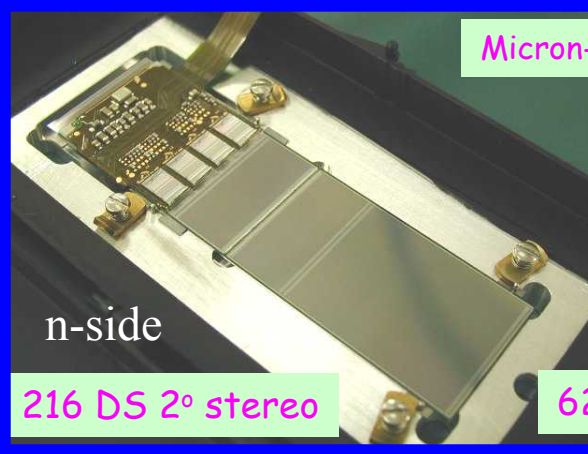




6 Barrels



Inner radius: 2.7cm
Outer radius: 9.4 cm

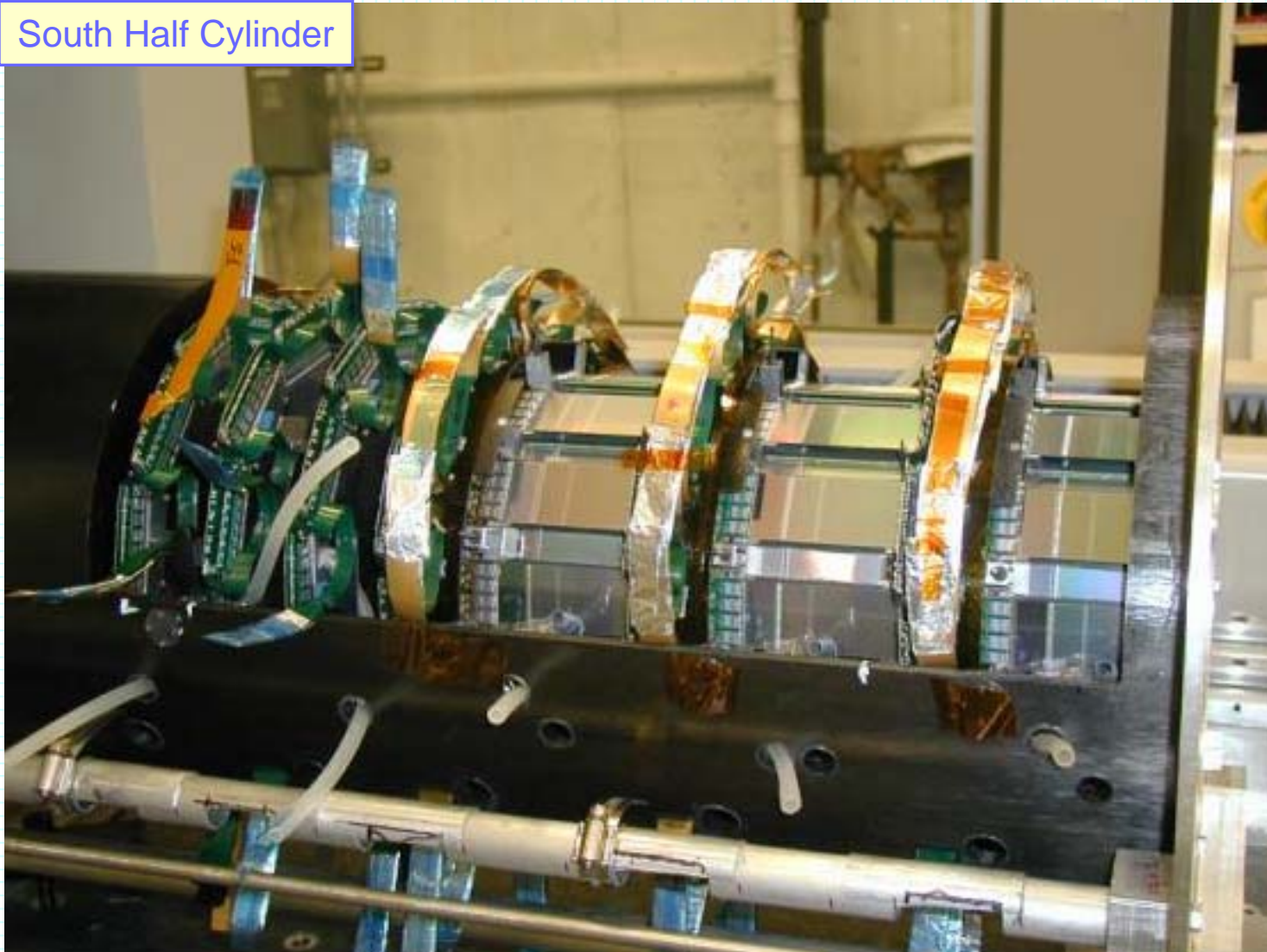


Layer 4						
Layer 3						
Layer 2						
Layer 1						
BEAM						



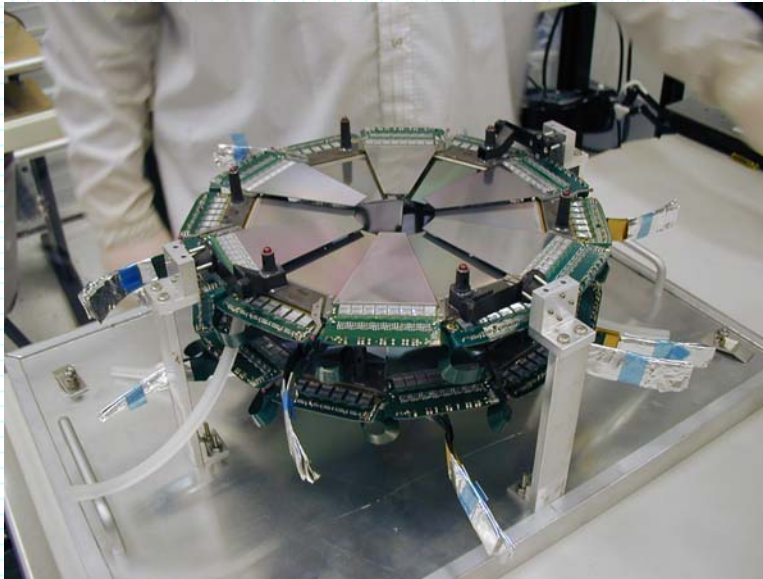
Assembly: 1/2-cylinder

South Half Cylinder

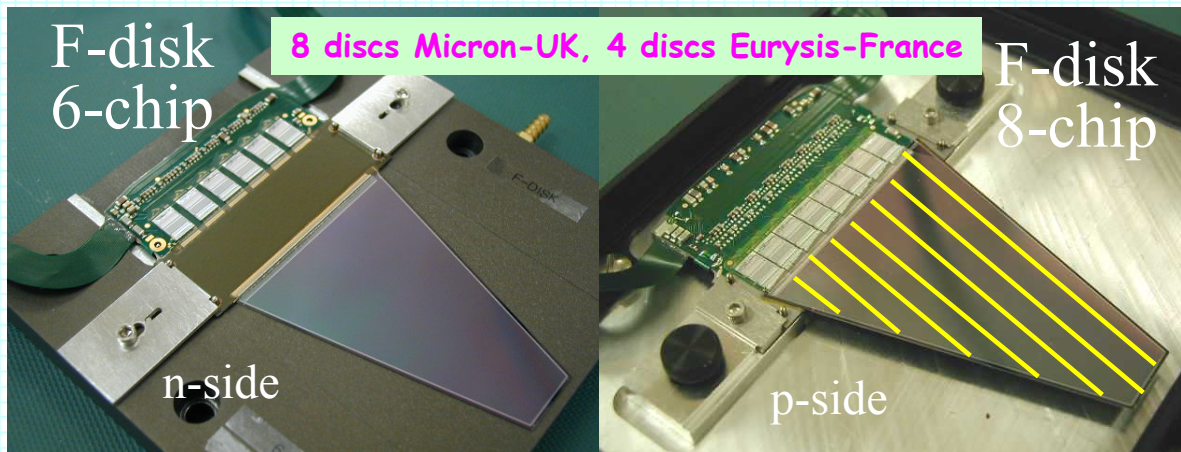




12 F-Discs



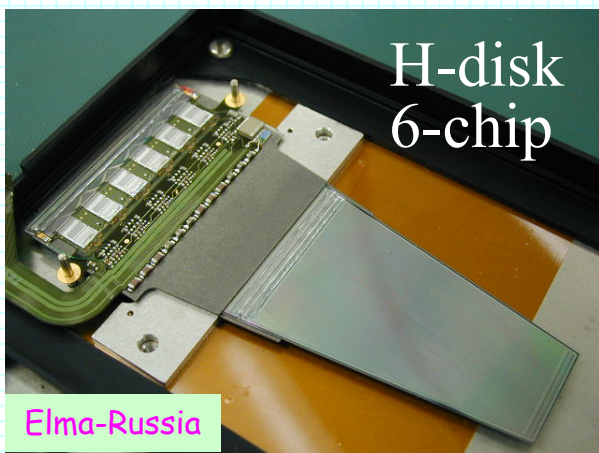
- 144 wedges
- $2.6 \text{ cm} < r < 10 \text{ cm}$
- $50 \mu\text{m}$ (p-side)
 $62.5 \mu\text{m}$ (n-side) pitch
- Double sided wedges
with $\pm 15^\circ$ (30° effective stereo)
- Variable strip length





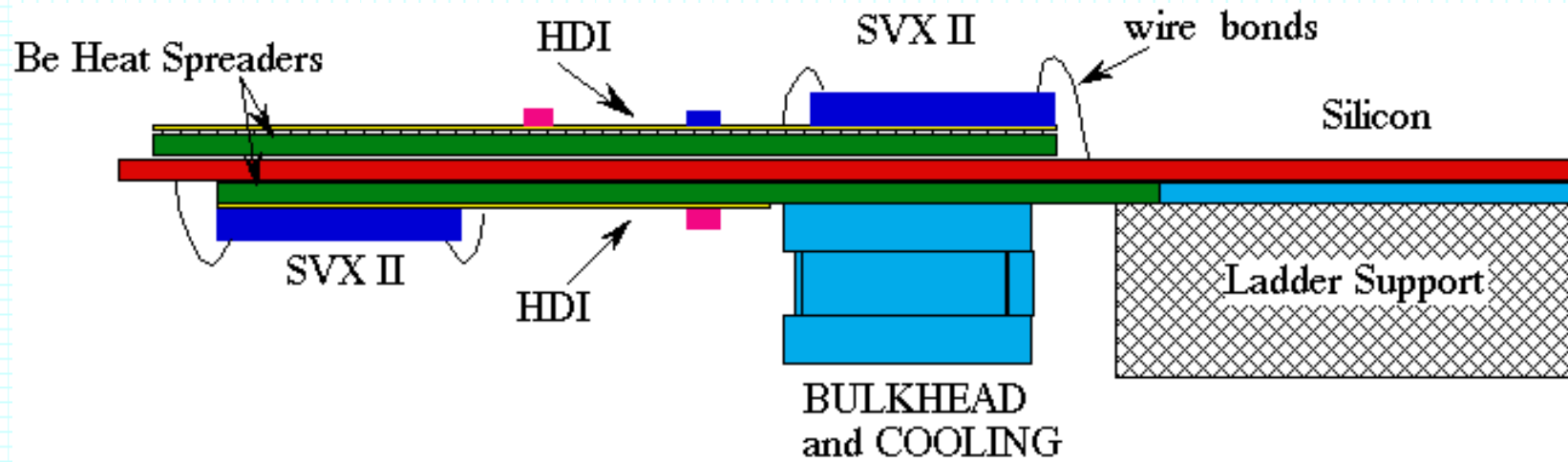
4 H-Discs

- $9.6 \text{ cm} < r < 23.6 \text{ cm}$
- 192 Wedges
- Single sided, glued back-to-back with $\pm 7.5^\circ$ (15° effective stereo)
- $40 \mu\text{m}$ (p-side) strip pitch
 $80 \mu\text{m}$ readout pitch
- Variable strip length

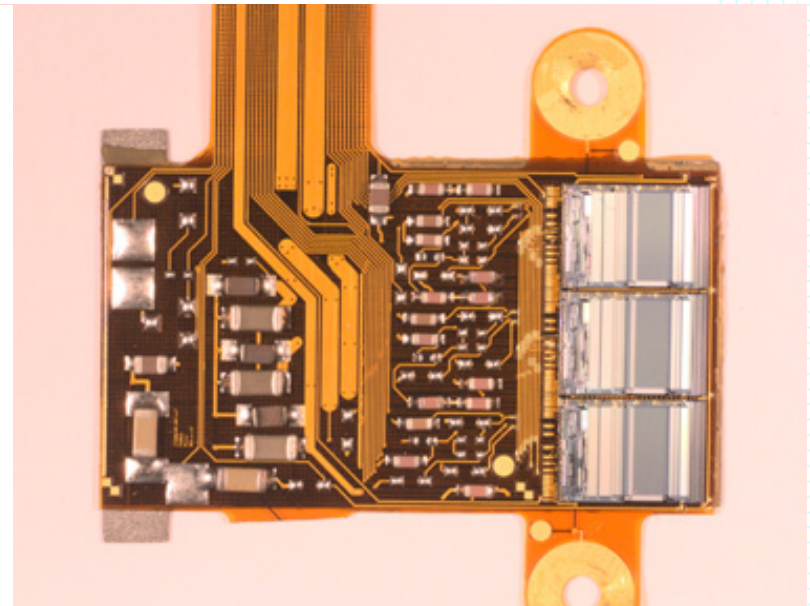


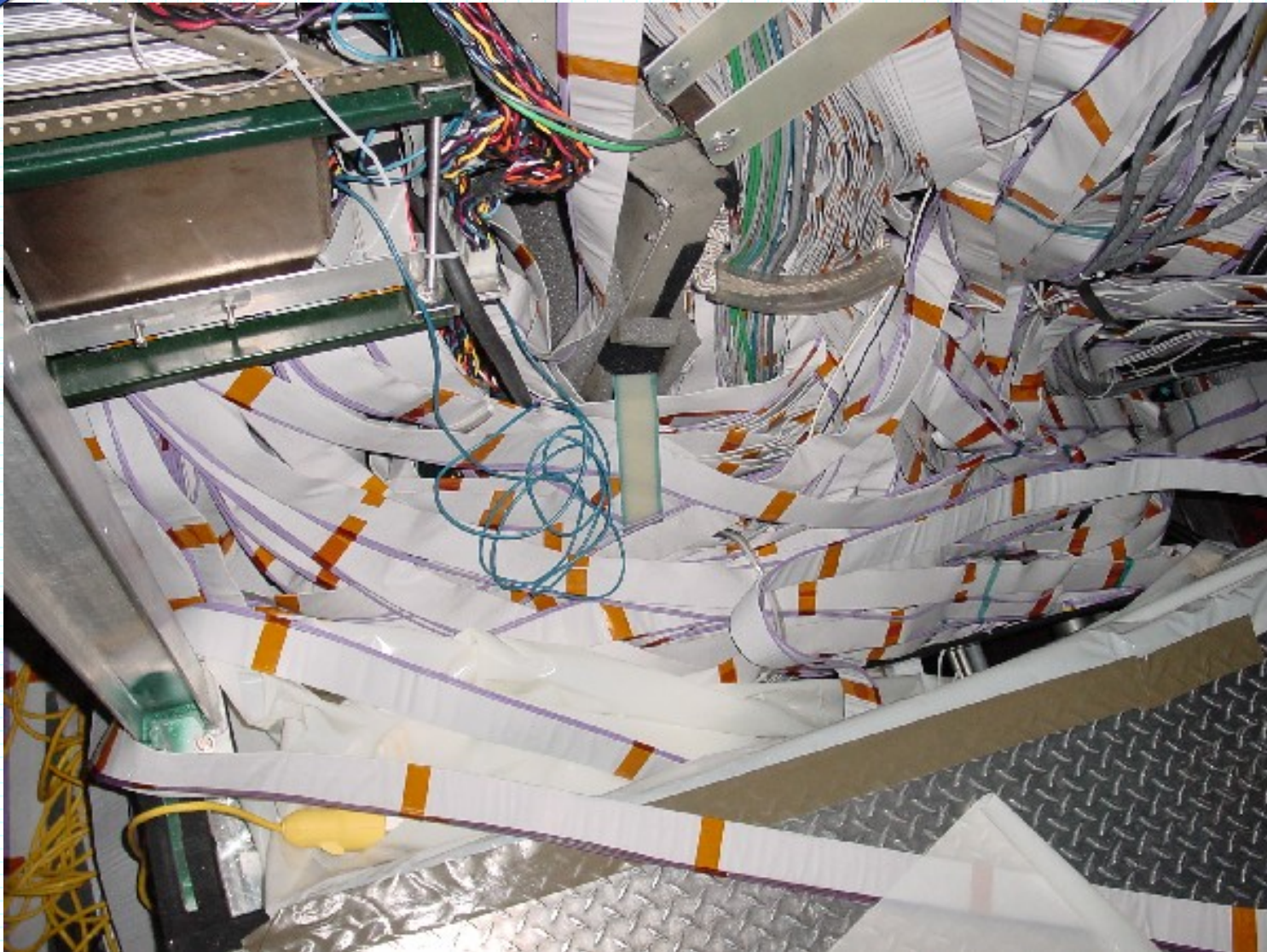


High Density Interconnect (HDI)



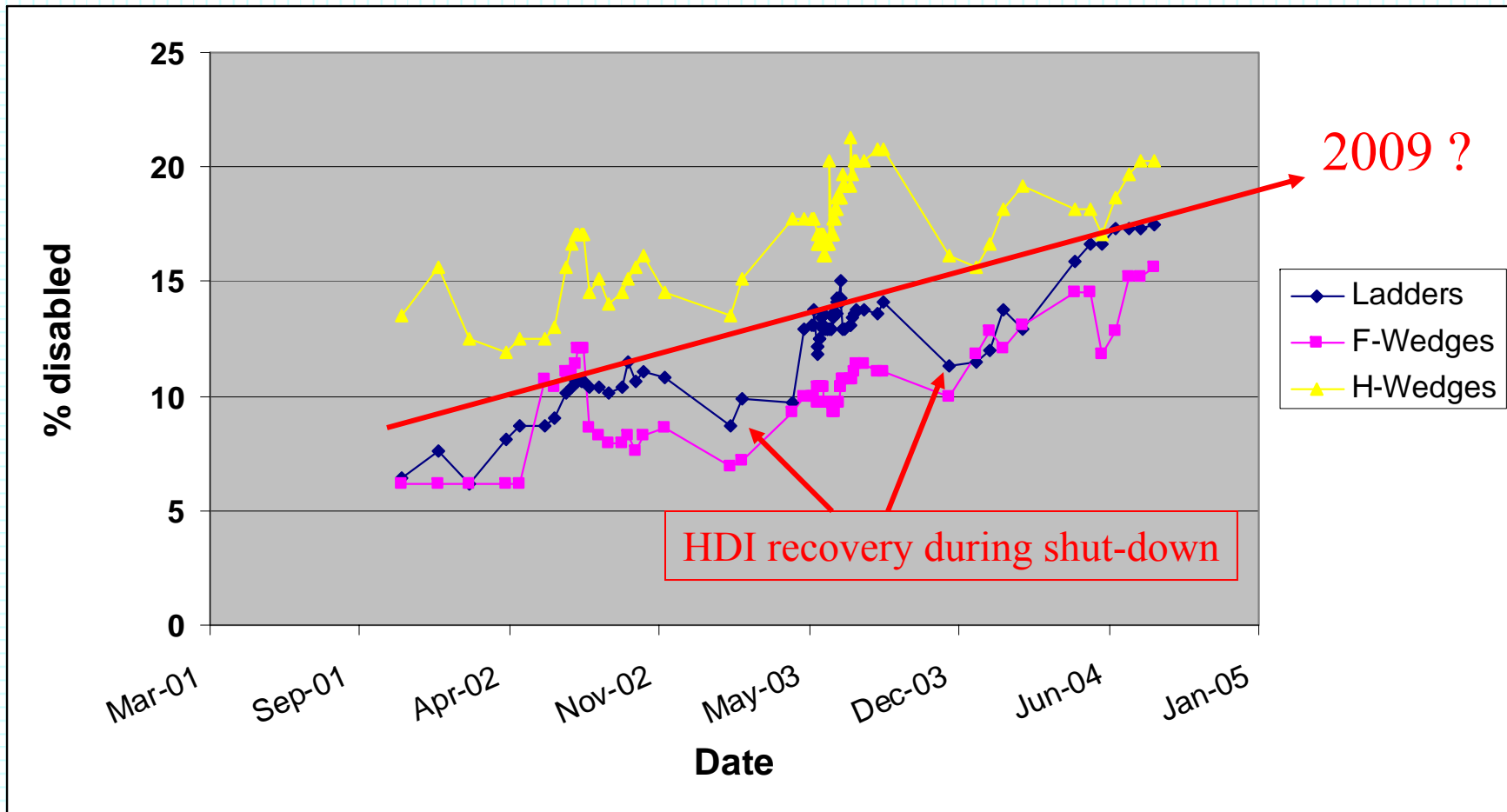
- Kapton based flex circuit with SVX IIe
- Laminated to beryllium substrate, and glued on silicon sensor
- Connected to low mass cable which carries signal out to the interaction region







% Disabled HDIs



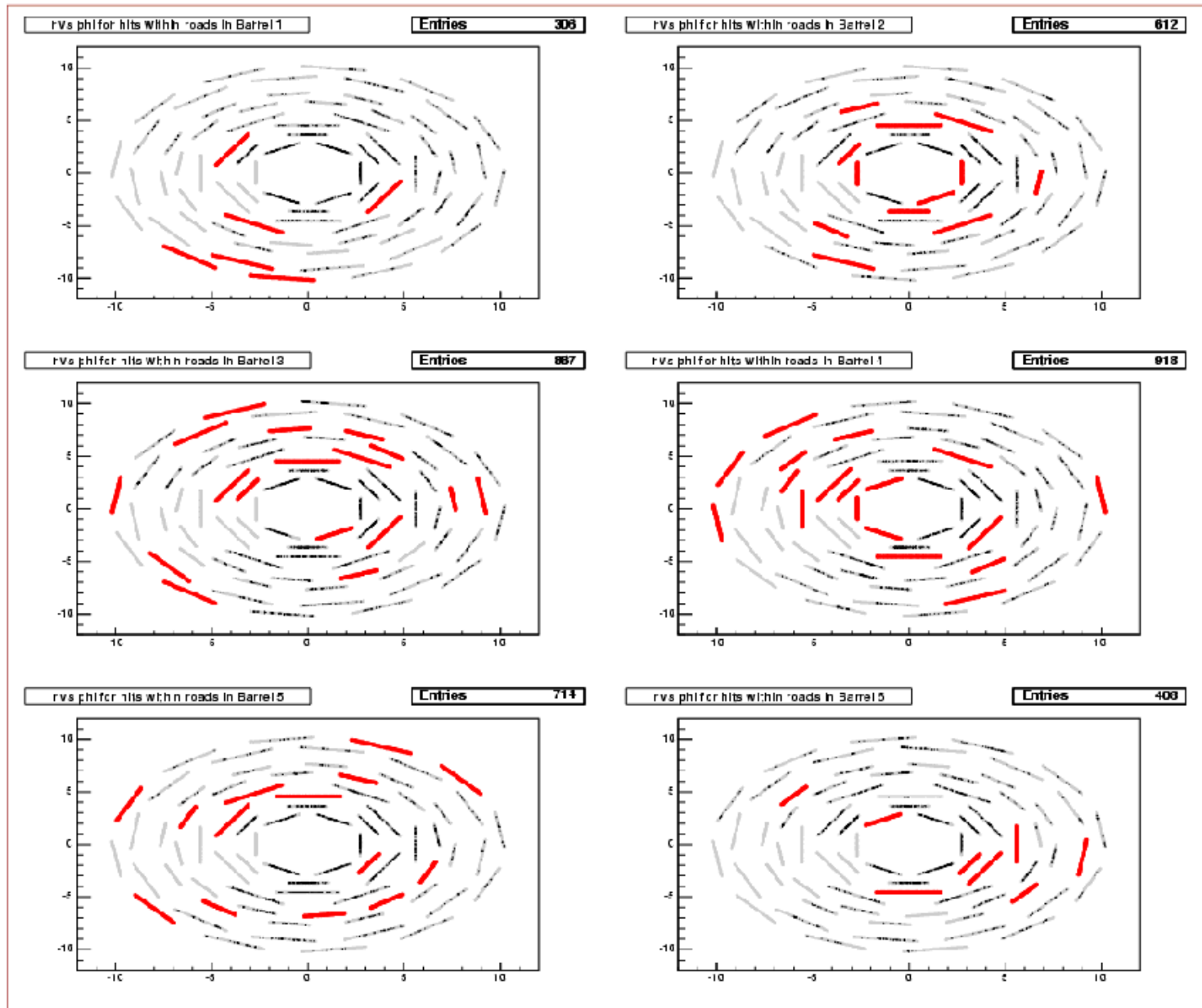


Status

Total 912 HDIs

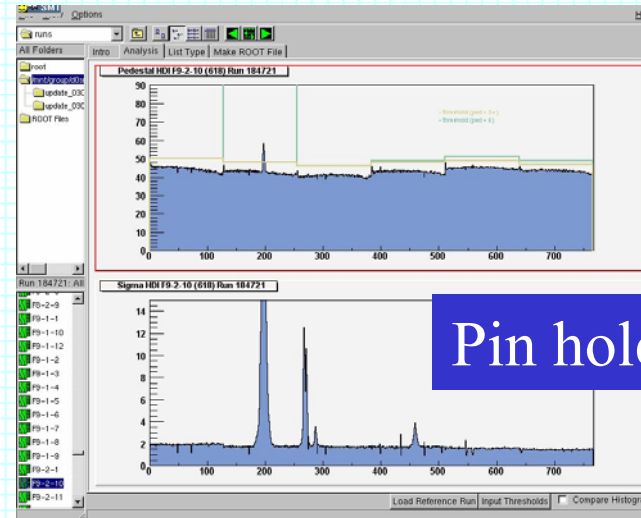
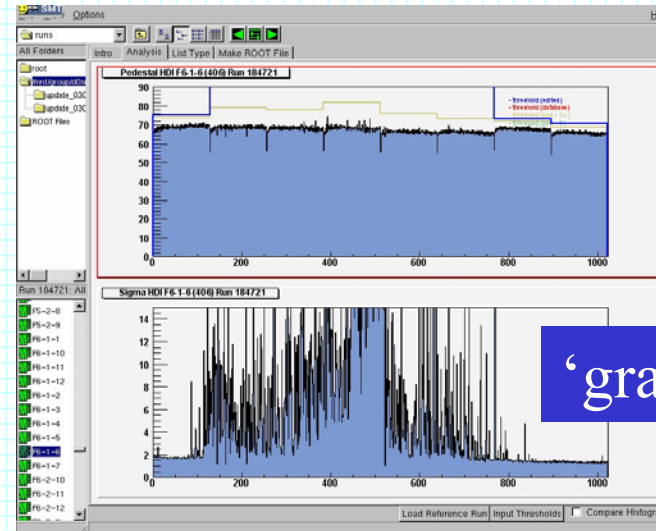
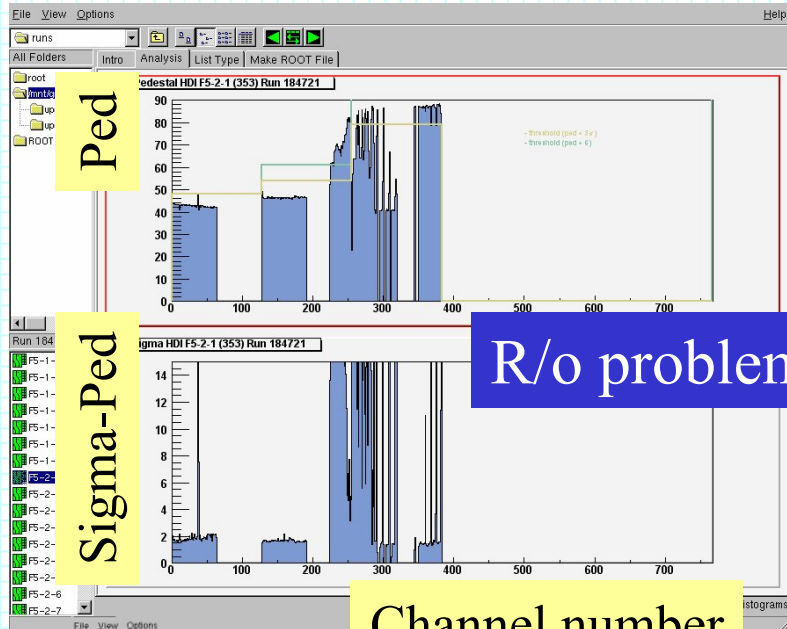
- 16% HDIs are NOT read out
- 8% problem in non accessible part
 - readout problems (preventing read out completely)
 - ‘no download’ = problem configuring SVXII
 - Low voltage trips
 - HV problem
 - Clock lines
- ~10% unstable

In $\frac{1}{2}$ of these we found shorts/open lines at the low-mass cables



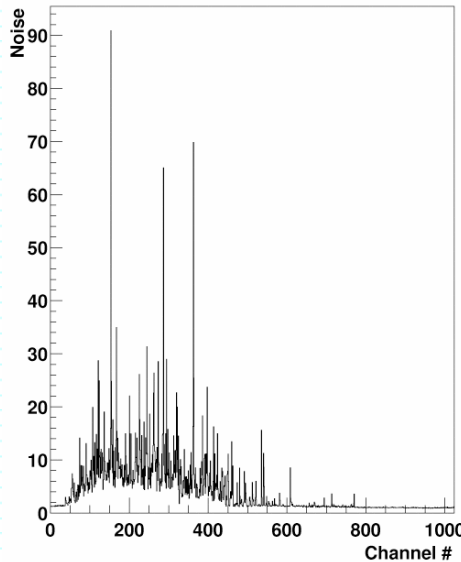


Problematic HDIs...

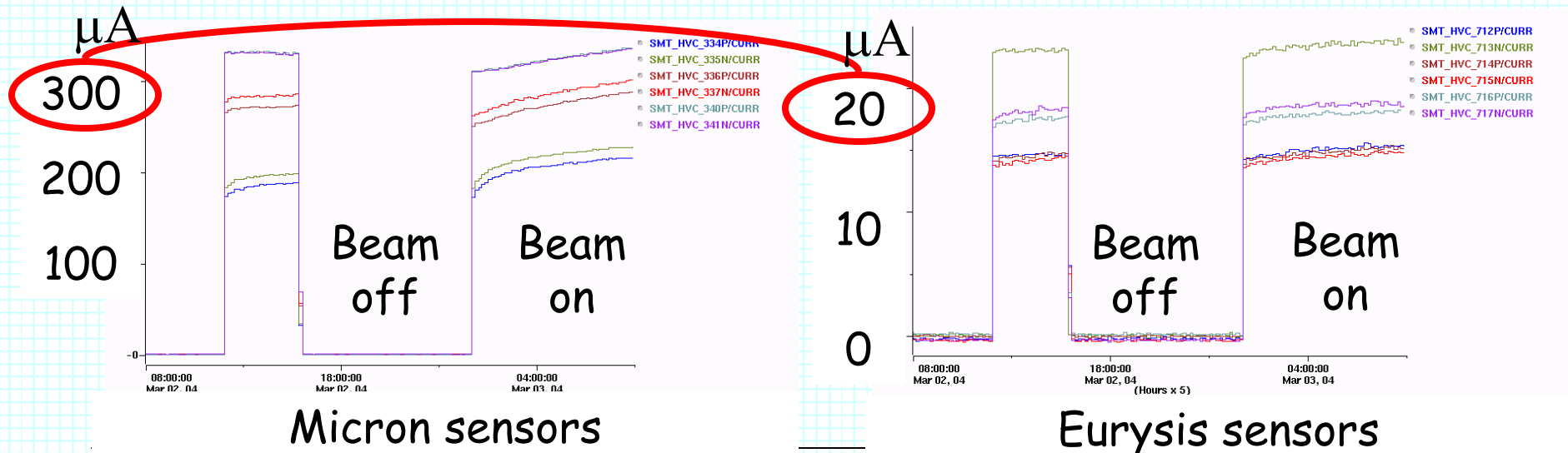




F-disk Noise



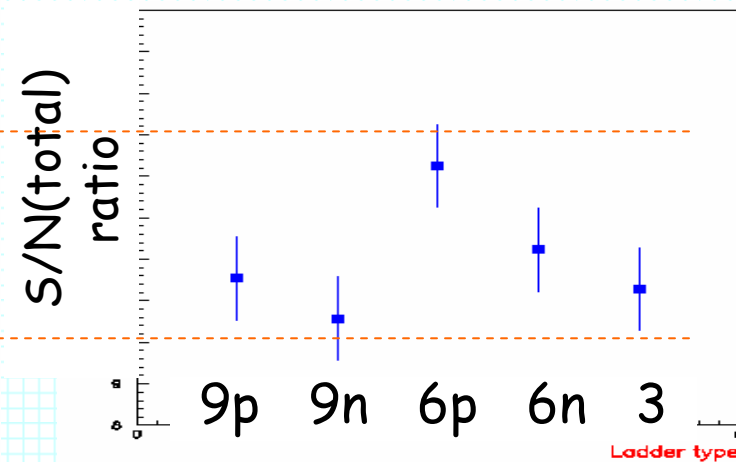
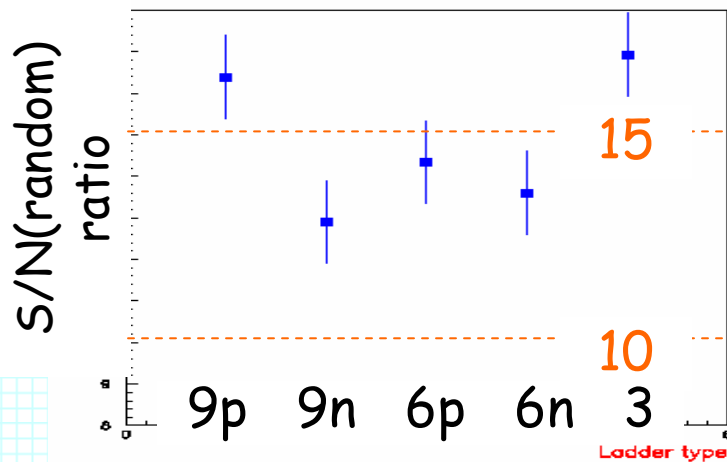
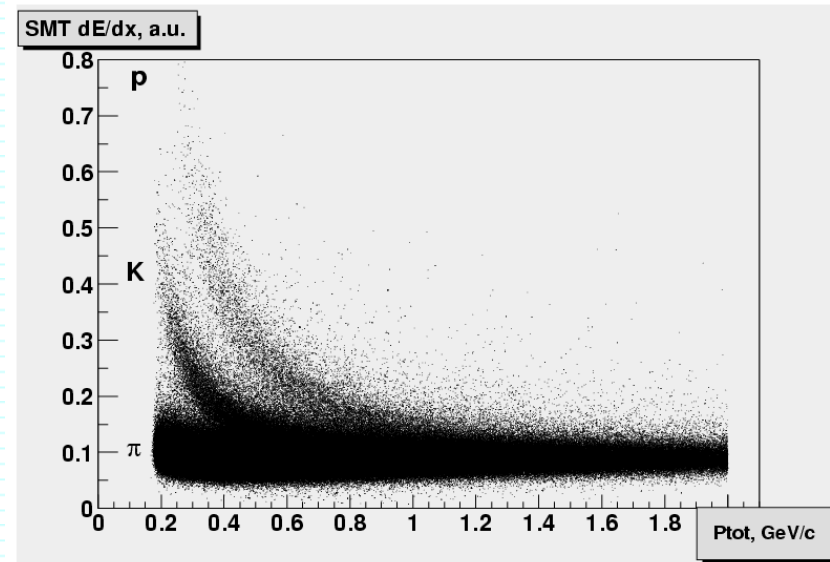
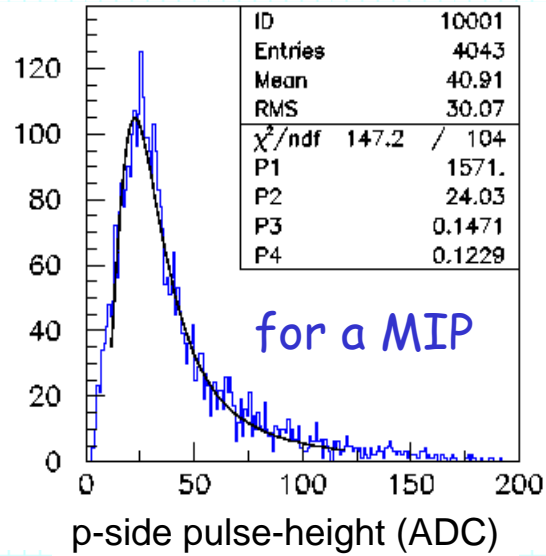
- 15% of the Micron r/o channels
- Looks like micro-discharge
- This appeared only after a several months operation
- Does not depend on bias scheme or temperature
- Charge-up effect, too





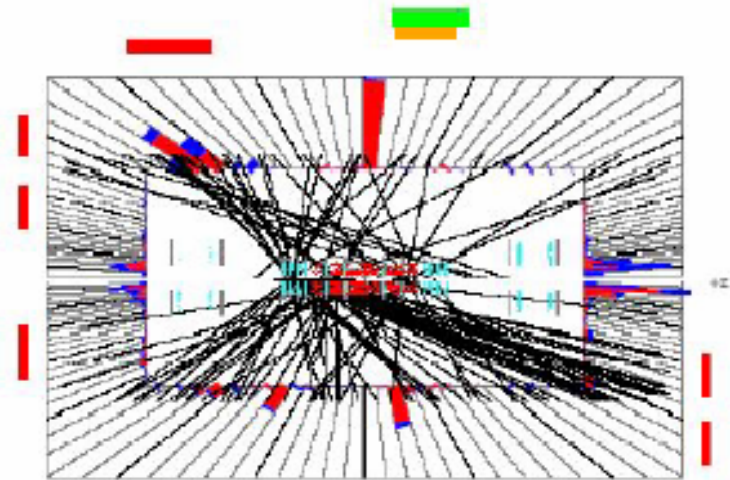
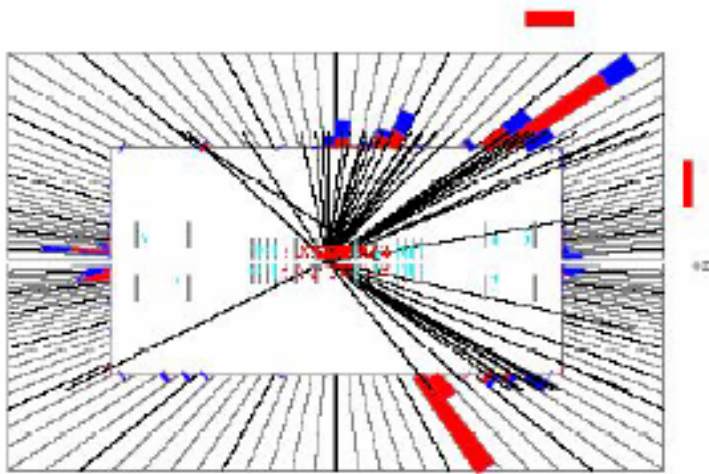


Performance



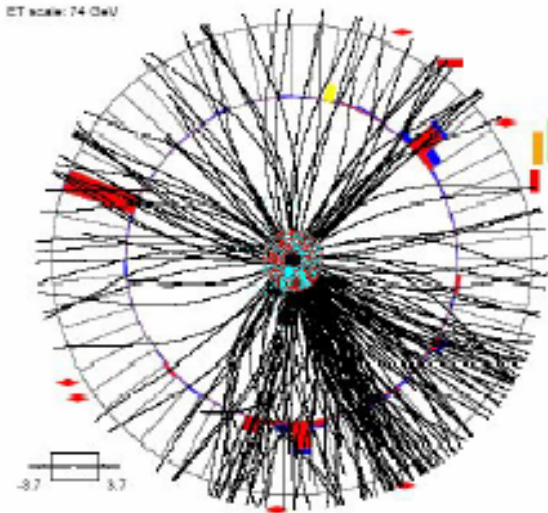
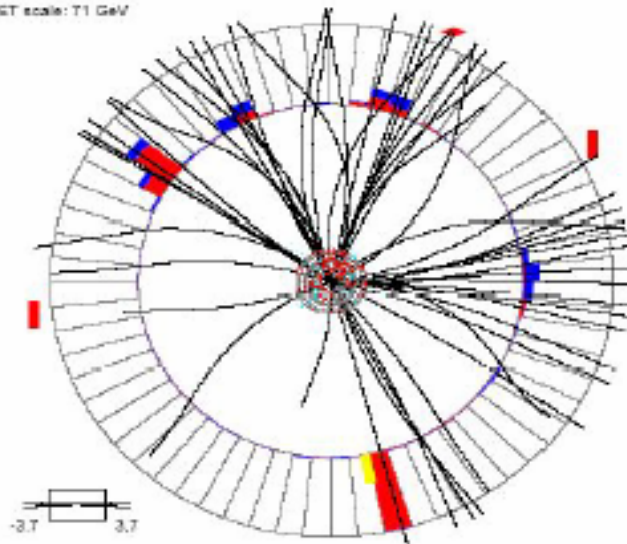


Tracking



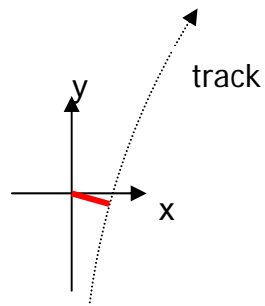
ET scale: 71 GeV

ET scale: 74 GeV





Tracking



Impact Parameter Resolution

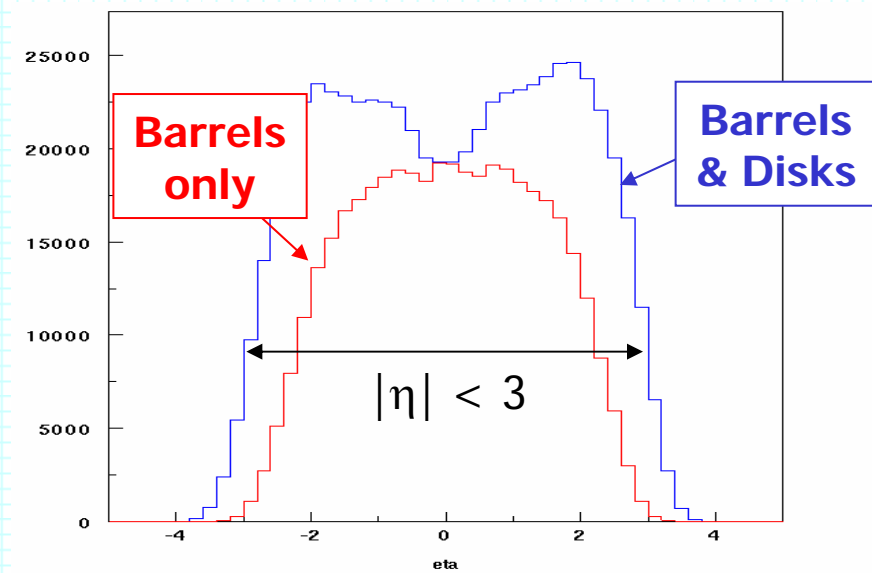
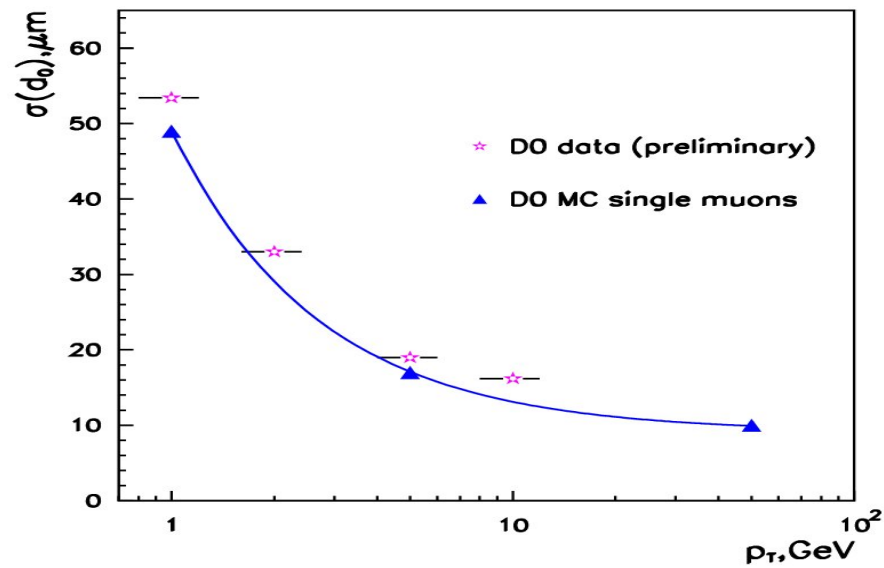
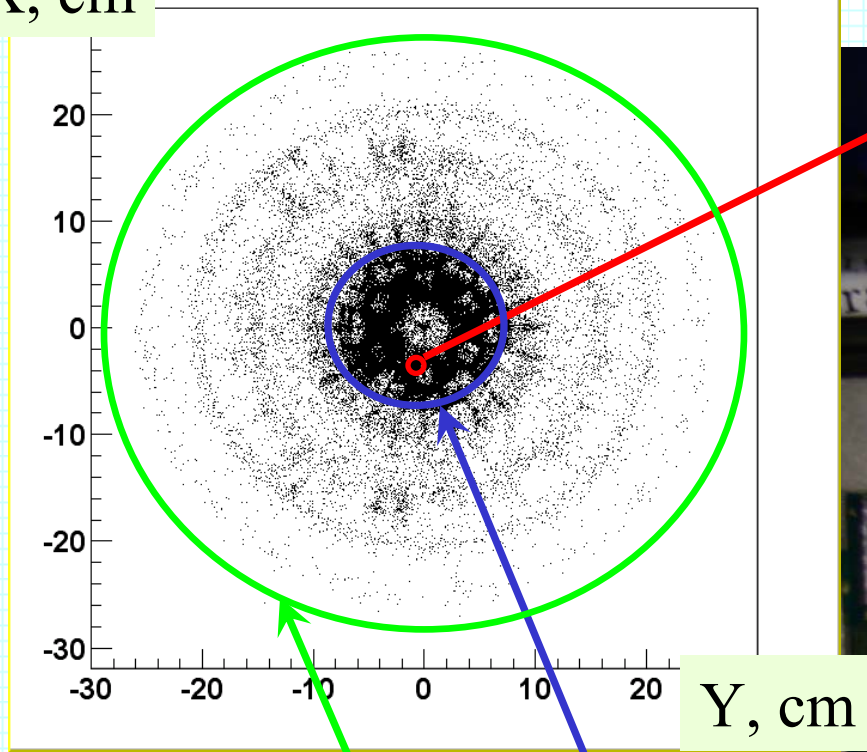




Image of Tracker from γ -conversions

$$\gamma \rightarrow e^+ e^-$$

X, cm

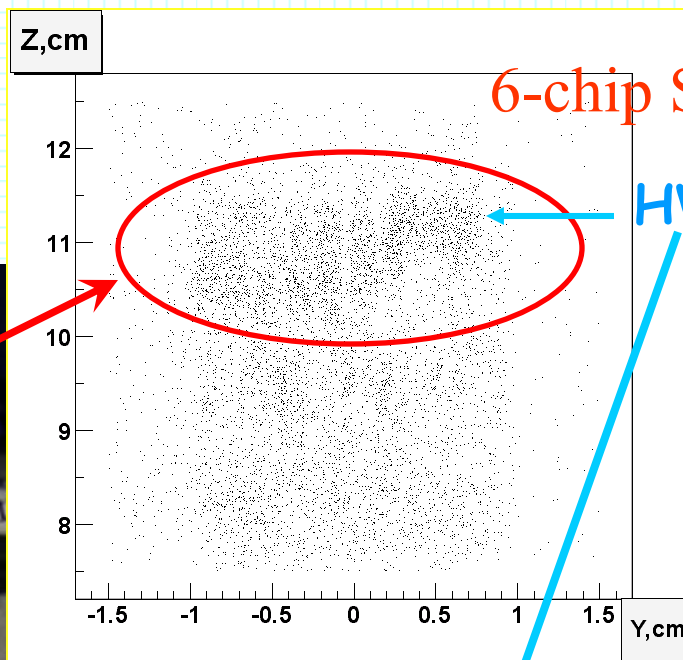


Y, cm

CFT

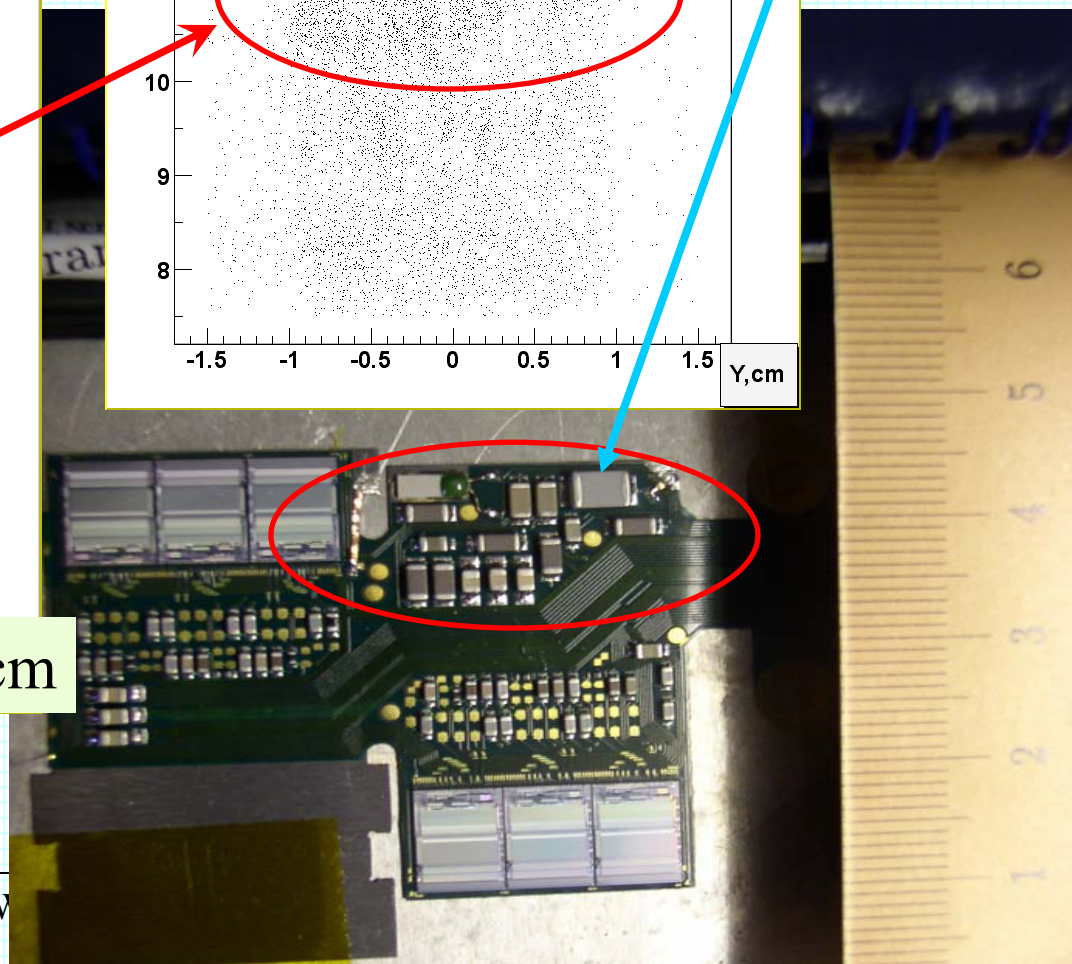
SMT

M.V



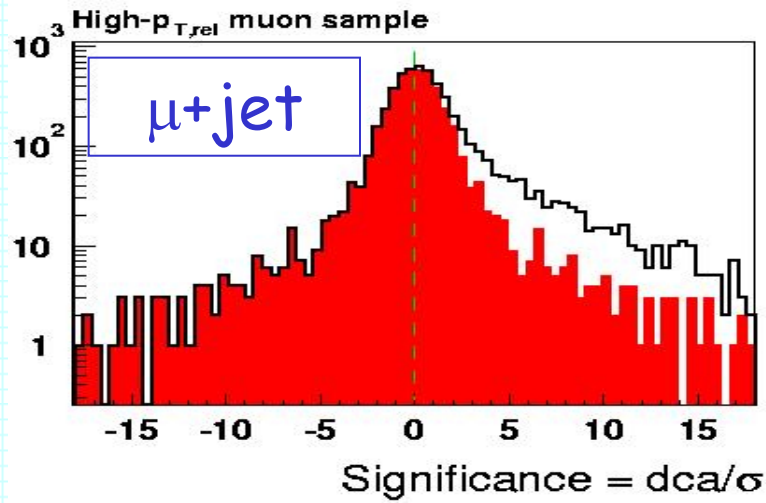
6-chip SMT HDI

HV cap

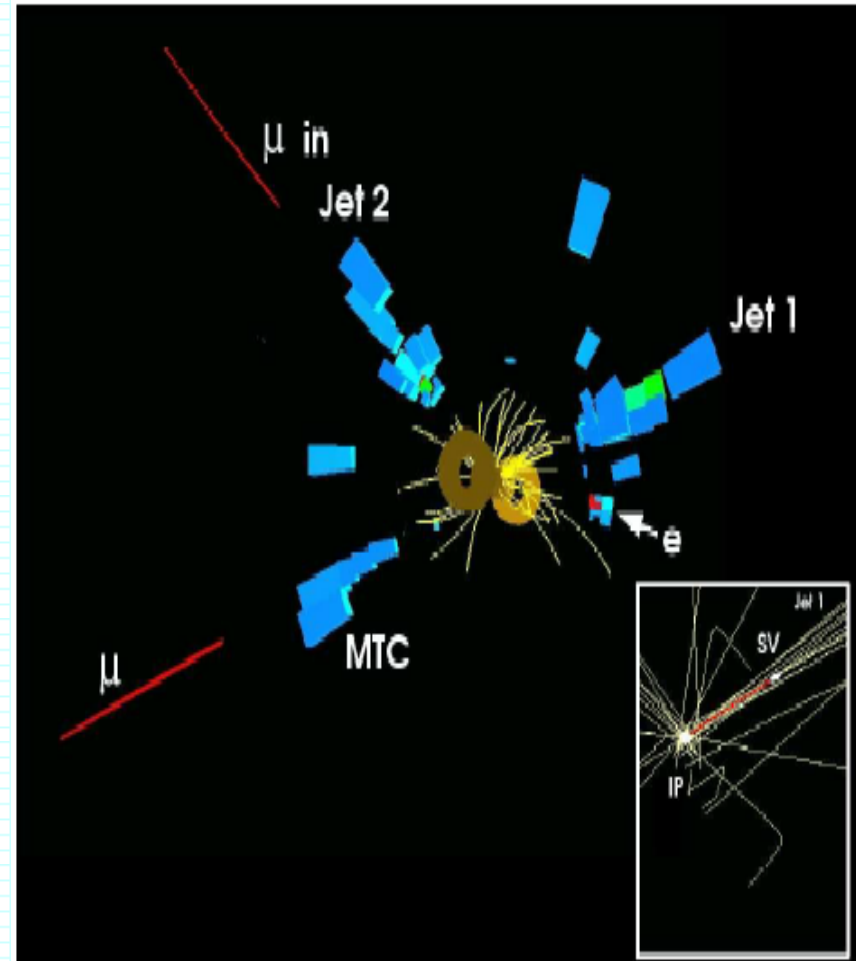
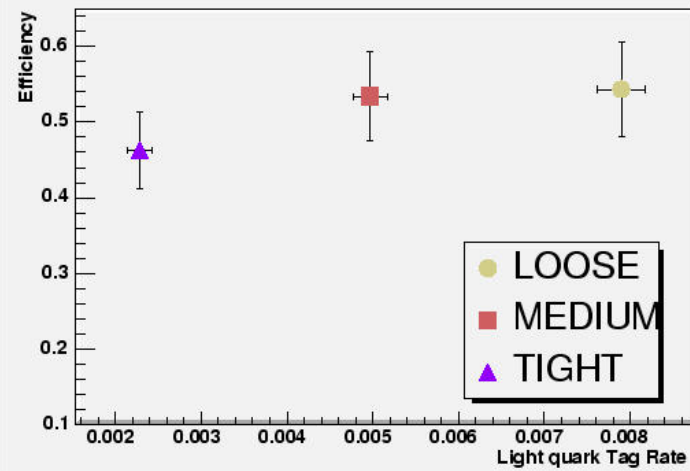




Vertexing



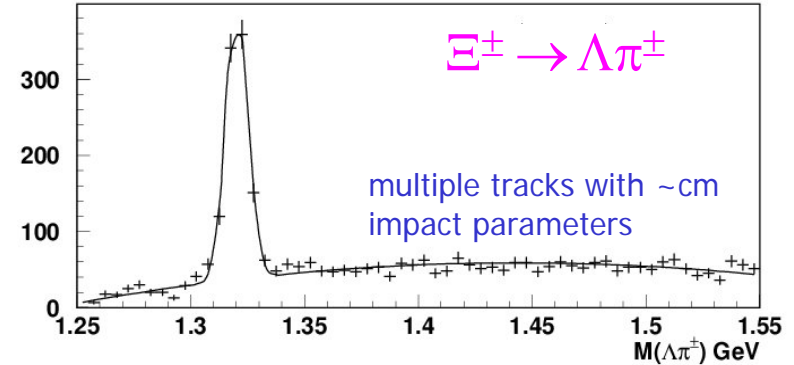
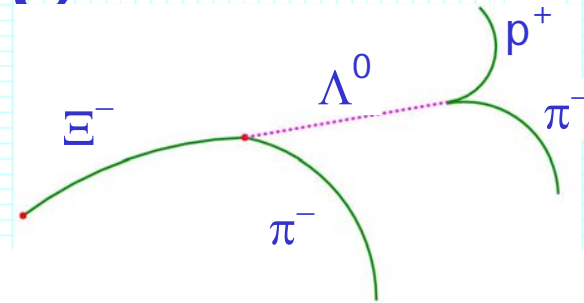
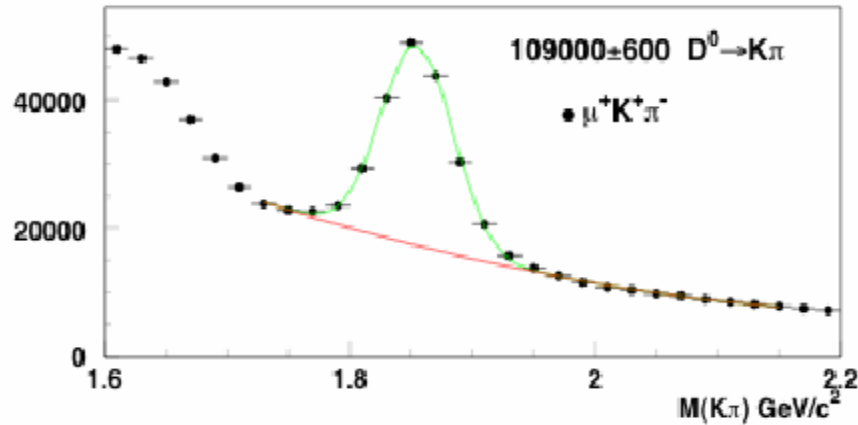
Central Region ($35 < p_T < 55$): b-tagging efficiency vs. light quark tagging efficiency



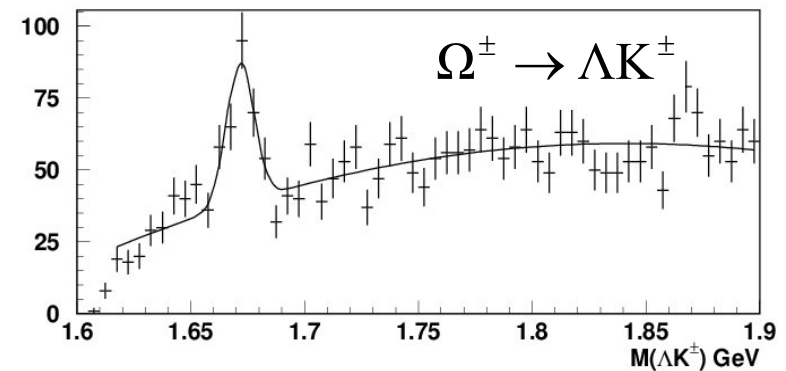
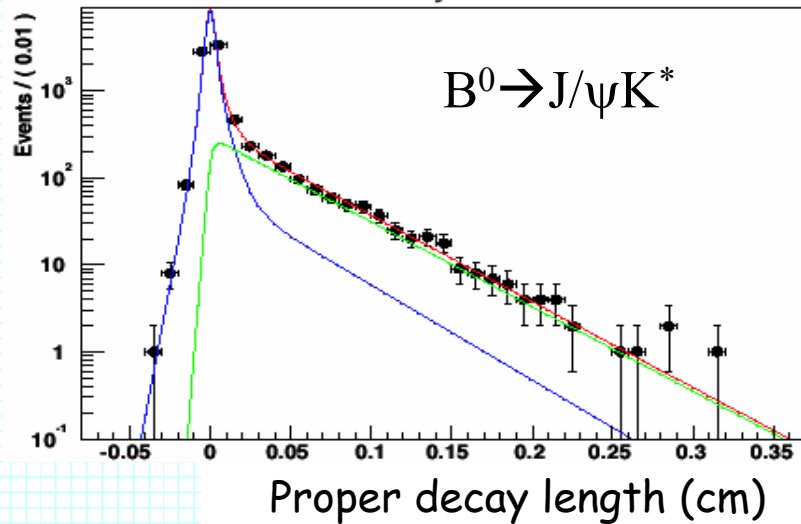


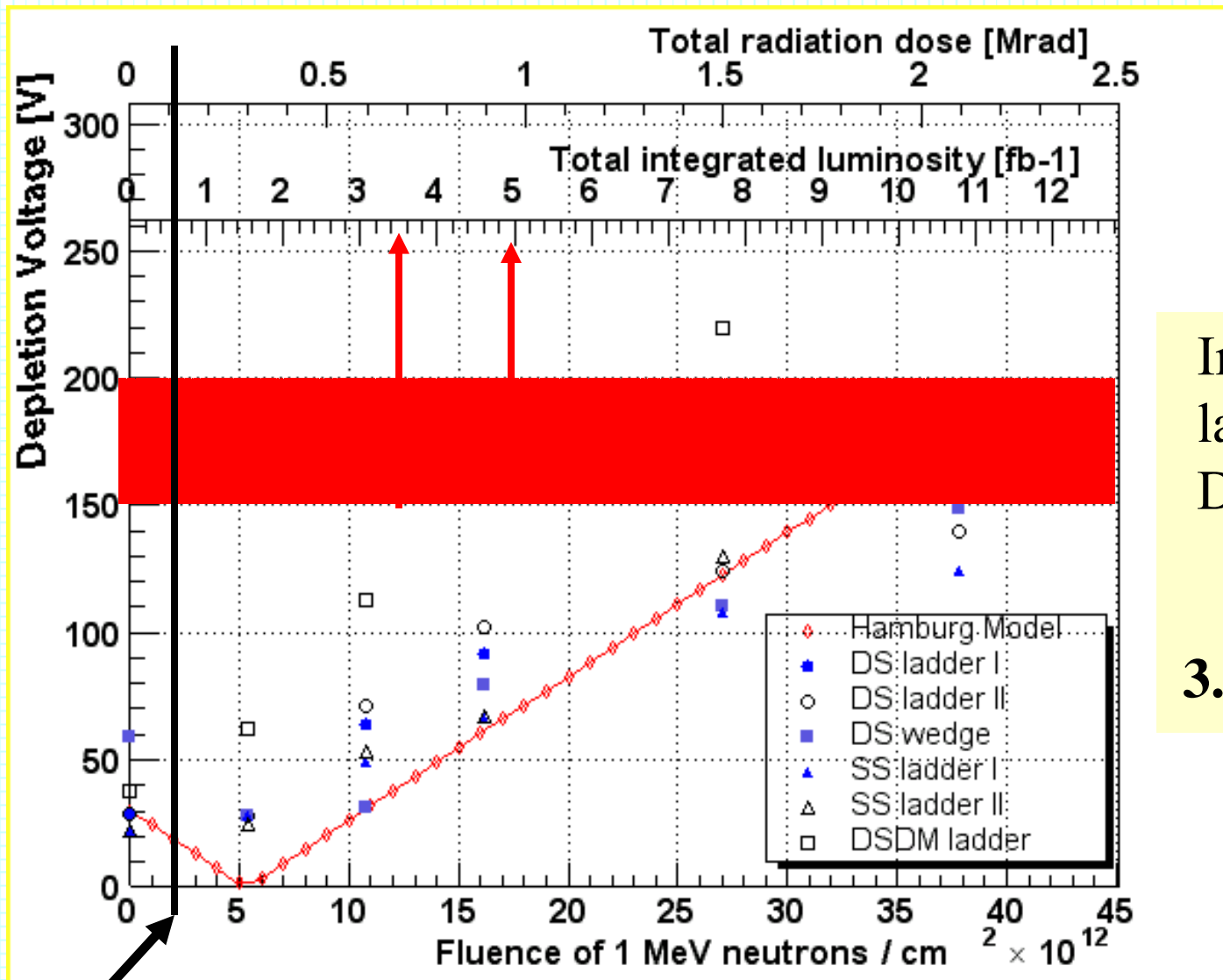
Vertexing

$$B \rightarrow \mu \bar{\nu} D^0 X$$



D0 Run II Preliminary





Innermost layers are DSDM

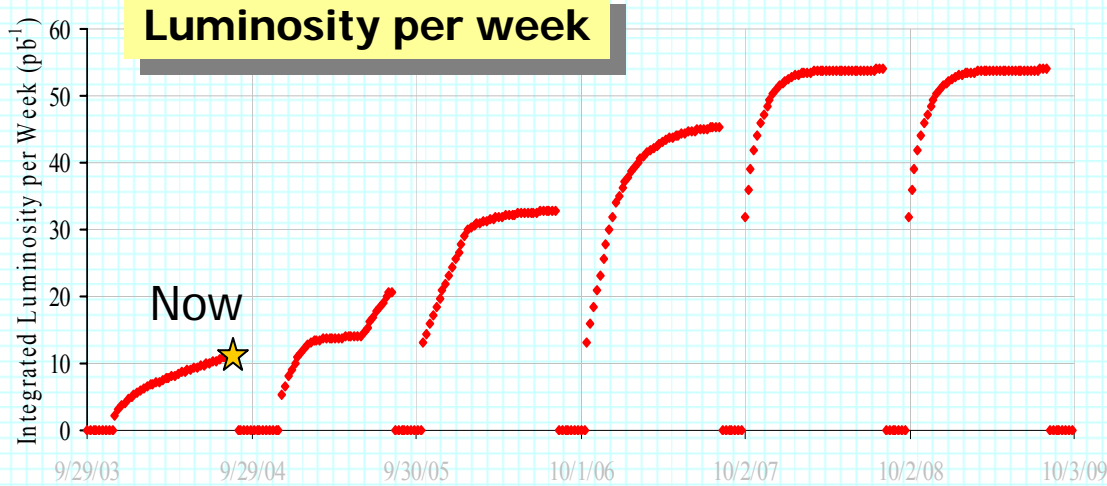


3.5fb⁻¹ to 5fb⁻¹

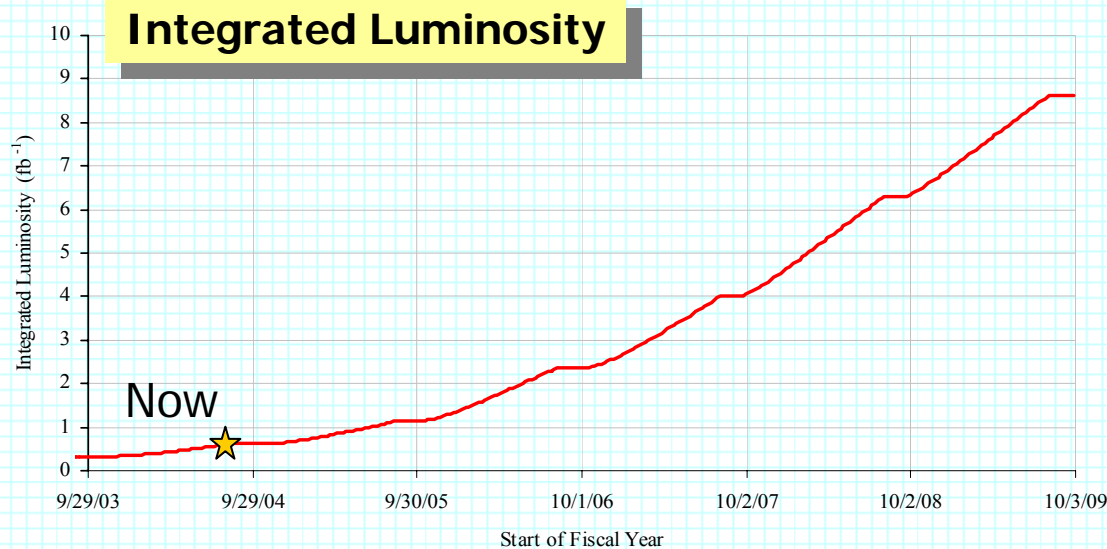
September 04



Tevatron Prospects



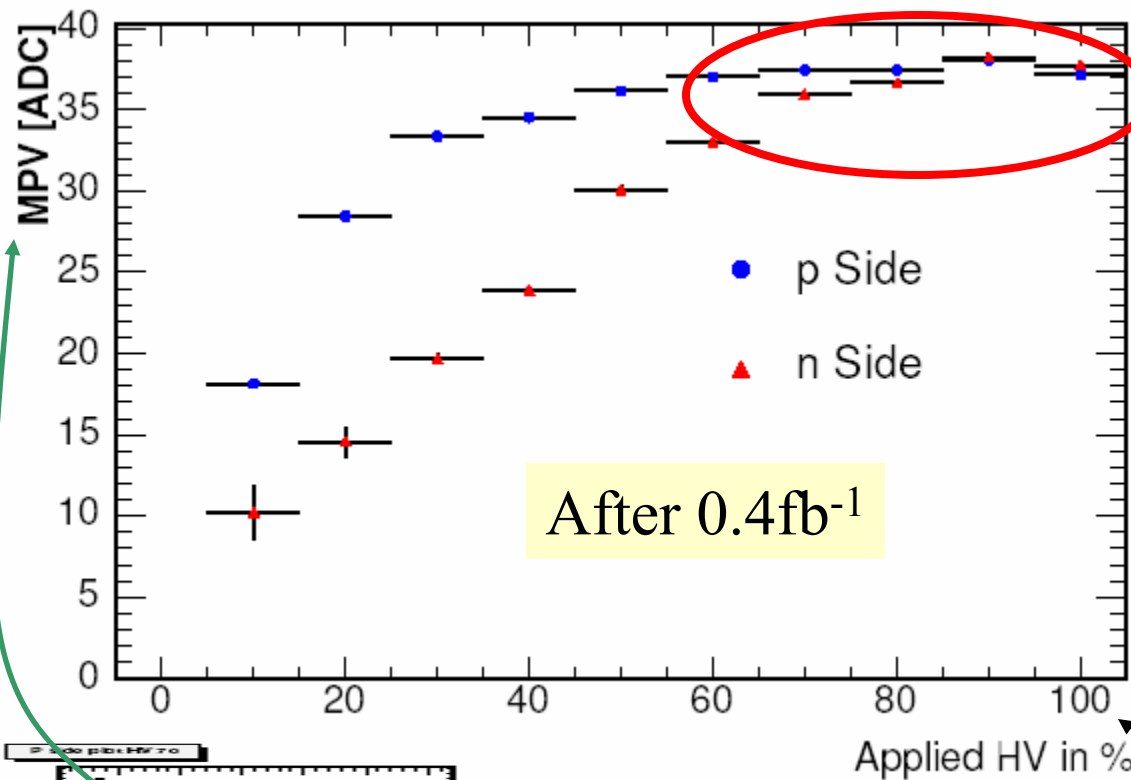
Major improvement will come from increasing the antiproton current: Recycler Ring, with electron cooling



Fiscal Year	Accumulated Luminosity	
	Design (fb^{-1})	Base (fb^{-1})
FY03	0.3	0.3
FY04	0.6	0.6
FY05	1.1	0.9
FY06	2.4	1.4
FY07	4.0	2.0
FY08	6.3	3.1
FY09	8.6	4.0

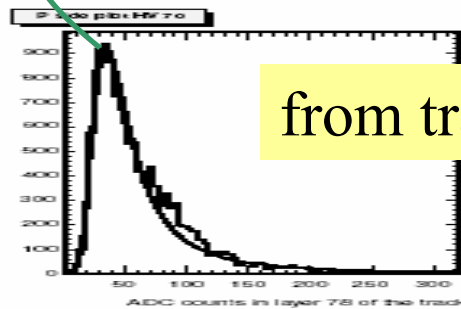


Depletion Voltage Measurement



No conclusion on reduced V_d

No type-inversion yet, as expected

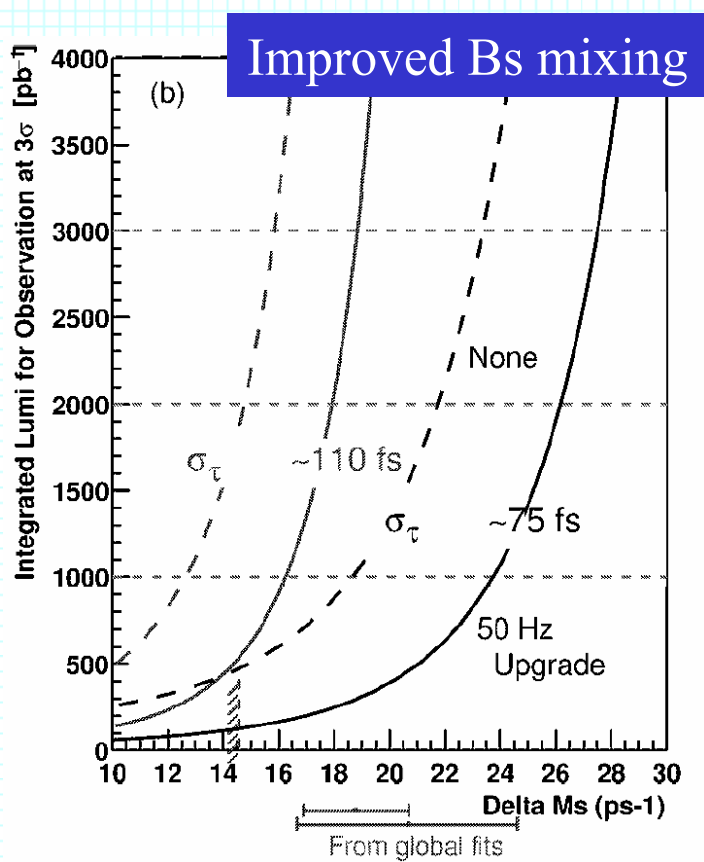


100% is the current operation voltage (10%-20% above V_d)

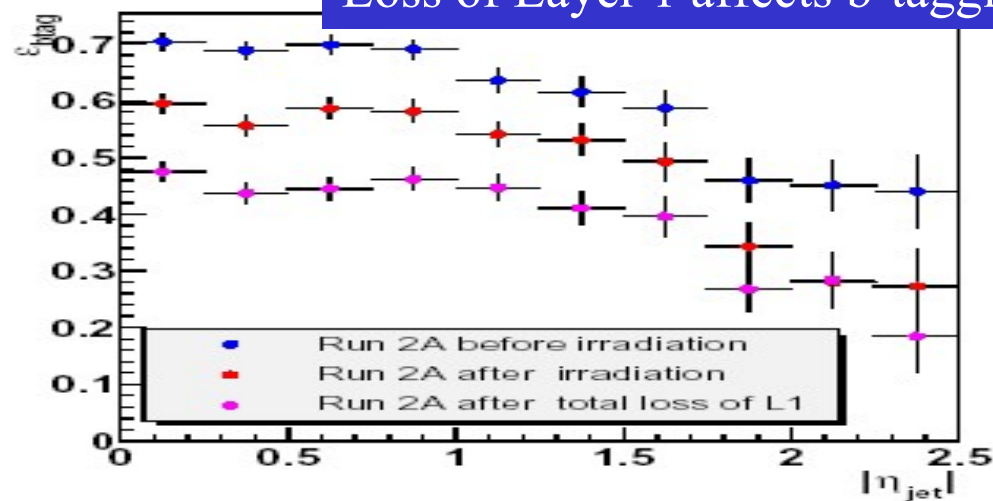


A new Layer 0

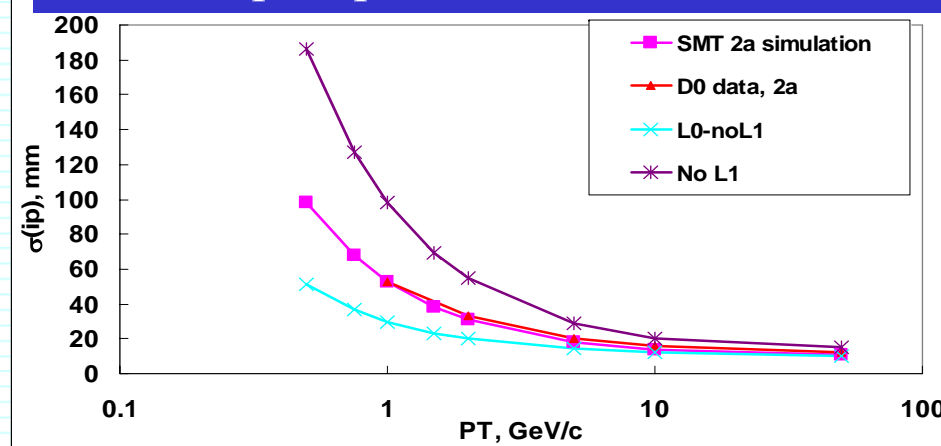
(Full replacement of the current silicon detector was cancelled last year)



Loss of Layer 1 affects b-tagging



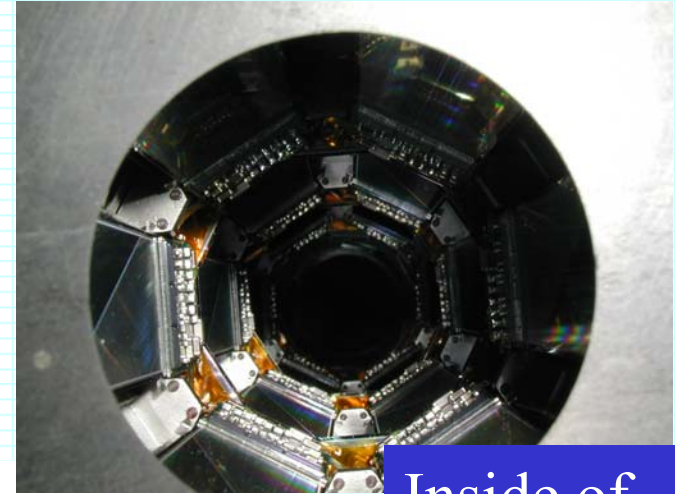
Better impact parameter resolution with L0



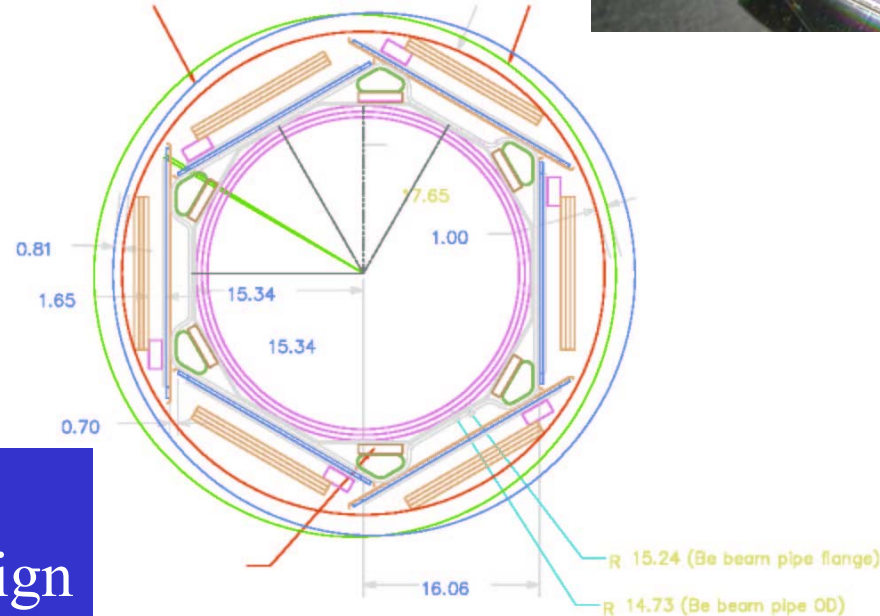


Layer 0 design

- Fits inside present silicon layers at $r \sim 1.6\text{cm}$ (**only 6.8mm gap !**)
- Layer 0 has 6-fold symmetry
- 4 sensors /z half (2x7cm, 2x12cm)
- 71 μm readout pitch (inner) and 81 μm (outer)
- 98.4% ϕ acceptance
- 48 hybrids
- SVX4 chip



Inside of the current detector



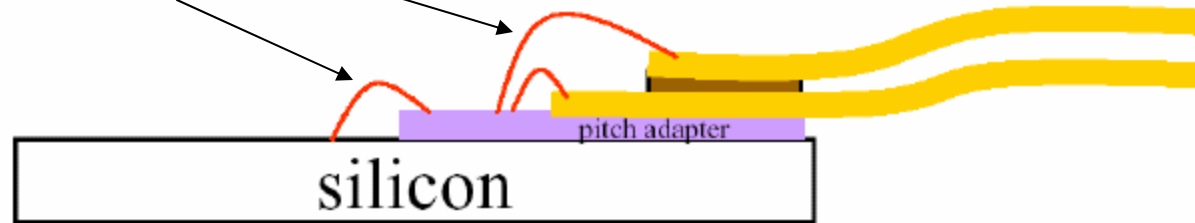
L0 design



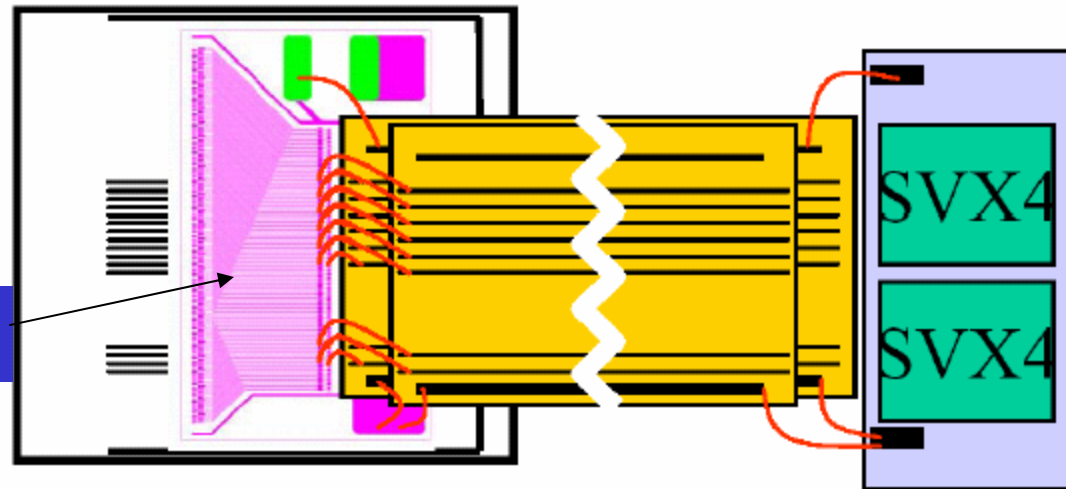
Readout channel

Wire bonds

Analog cables

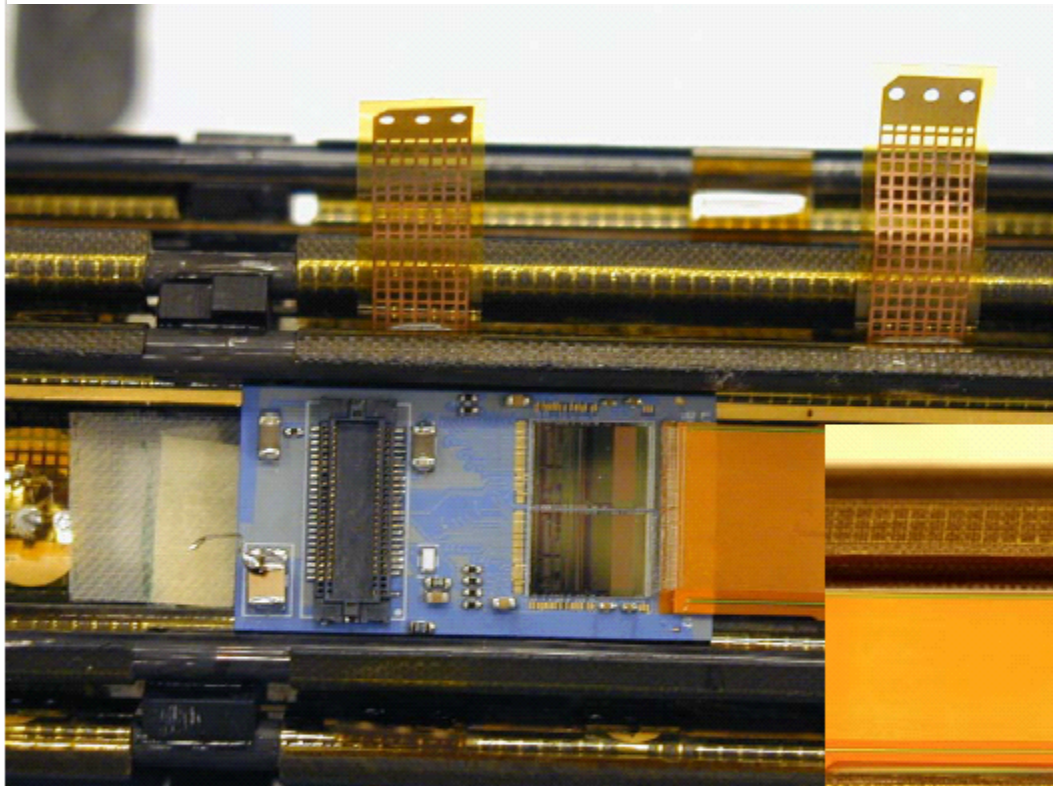


Pitch adapter

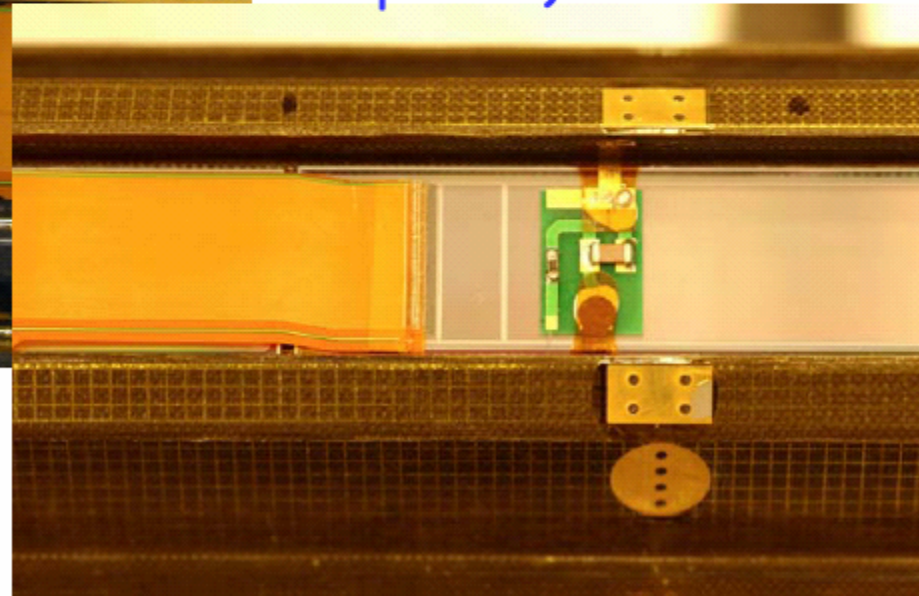




Layer 0 Grounding

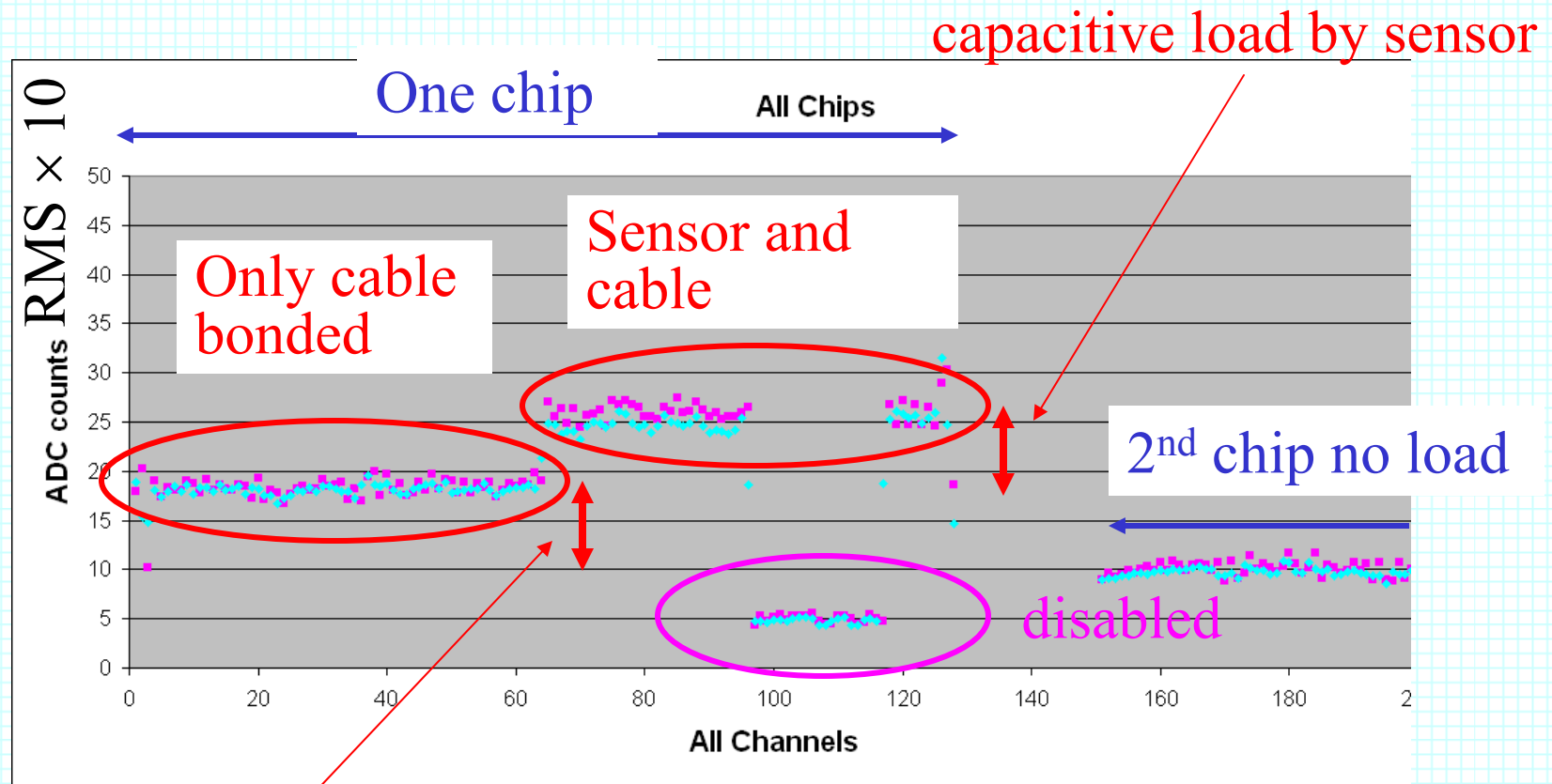


- Implements new grounding approach : laminated ground mesh covering all CF surface
- Excellent noise performance without Faraday cage (no pick-up noise)





Noise of L0



capacitive load by cable ($0.8\text{ADC} \sim 600e$)

- SVX4 ENC: $\text{const} + 41C/\text{pF} \rightarrow C = 15\text{pF}$ for $\sim 45\text{cm}$ as expected
- $1 \text{ M IP} \cong 22000e \rightarrow \text{S/N} \sim 12$



Conclusions

- D0 SMT operational since more than 2½ years
- Good tracking ($|\eta| < 3$; $\sigma = 16\mu\text{m}$) and vertexing (b-tagging; B lifetime)
- 85% active channels
- Expect the inner layer to succumb radiation after 3.5fb^{-1} to 5fb^{-1} (design is 8fb^{-1} by 2009)
- New Layer 0 being built (installed 2005)