Fully-Depleted, Back-Illuminated Charge-Coupled Devices Fabricated on High-Resistivity Silicon

Stephen E. Holland, Donald E. Groom, Nick P. Palaio, Richard J. Stover, Mingzhi Wei

Abstract— **Charge-coupled devices (CCD's) have been fabricated on high-resistivity, n-type silicon. The resistivity, on the order of 10,000 Ω-cm, allows for depletion depths of several hundred microns. Fully-depleted, back-illuminated operation is achieved by the application of a bias voltage to a ohmic contact on the wafer back side consisting of a thin in-situ doped polycrystalline silicon layer capped by indium tin oxide and silicon dioxide. This thin contact allows for good short wavelength response, while the relatively large depleted thickness results in good near-infrared response.**

Keywords— **Charge-coupled device, back illuminated, fully depleted, high-resistivity silicon.**

I. Introduction

THE large focal planes at astronomical telescopes require high quantum efficiency (QE), large format charge-coupled device (CCD) detectors. In order to achieve high QE, the standard scientific CCD is thinned and back illuminated [1]. Thinning is required because the relatively low resistivity silicon used to fabricate scientific CCD's limits the depth of the depletion region. In order to minimize field-free regions with resulting degradation in spatial resolution, the typical scientific CCD is thinned to about 20 μm. This process degrades red and near-infrared response due to the rapid increase in absorption length in silicon at long wavelengths. In addition, fringing patterns due to multiply-reflected light are observed in uniformly-illuminated images taken at near-infrared wavelengths where the absorption length exceeds the CCD thickness. The CCD described in this work achieves high quantum efficiency in the red and near-infrared by virtue of a thick depleted region made possible by the use of high-resistivity silicon substrates.

Extended red response is extremely important to the Supernovae Cosmology Project at Lawrence Berkeley National Laboratory (LBNL) due to the use of distant, high redshift supernovae for the determination of cosmological parameters [2]. Detection and follow-up spectroscopy of high redshift objects would greatly benefit from CCD's with improved near-infrared response.

We have reported results on a small prototype CCD with high QE extended to 1000 nm [3], [4]. In this work the physical operating principles and technology of this CCD are described along with results on large-format sensors.

S. Holland is with the Lawrence Berkeley National Laboratory, Berkeley, California, USA. E-mail: seholland@lbl.gov .

D. Groom and N. Palaio are with the Lawrence Berkeley National Laboratory, Berkeley, California, USA.

R. Stover and M. Wei are with the University of California Observatories, Santa Cruz, CA.

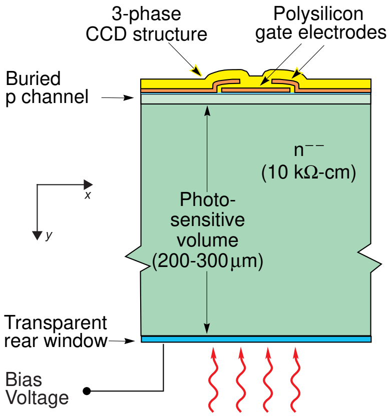

Fig. 1. Cross-sectional diagram of the CCD described in this work. The actual implementation of the substrate bias voltage connection is described in Section III.

II. Background

Scientific CCD's are typically used in applications requiring low level light detection. Hence dark current, noise and quantum efficiency are of primary importance. For astronomy applications the CCD's are often cooled to −120°C to −150°C to minimize dark current. In addition readout rates are relatively slow, typically 20–50 kpixels/sec, to minimize read noise [1]. The signal to noise ratio is further increased by the use of back illumination with correspondingly high quantum efficiency. Large format sensors are commonly used, and high charge transfer efficiency (CTE) is required.

Figure 1 shows a cross-section of the CCD considered in this work. A conventional three-phase, triple polysilicon gate CCD [5] with buried channel is fabricated on a high-resistivity n-type substrate. A substrate bias is applied to fully deplete the substrate, which is typically 200–300 μm thick. The biasing details are described in Section III. The CCD's described in this work are fabricated on 10,000–12,000 Ω-cm material, corresponding to a donor density N_D of approximately 3.6–4.3 × 10^{11} cm^{-3}. This high resistivity starting material allows for fully depleted operation at reasonable voltages.

The CCD described here is p-channel. The choice of p-channel over the more conventional n-channel was due to our previous experience with fabrication of charged-particle p-i-n detectors, where we found it more straightforward to produce low dark current devices via backside gettering techniques on n-type silicon [6]. The degraded readout speed resulting from lower hole mobility in a p-channel CCD is not a concern for the astronomy application due

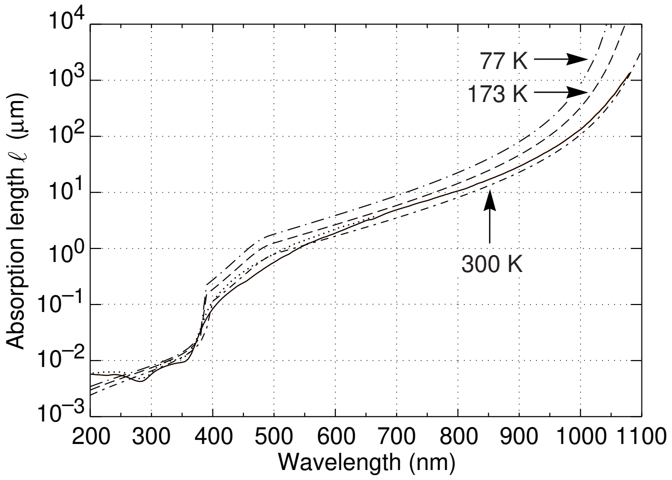

Fig. 2. Absorption length versus wavelength for silicon. Data and calculations (dashed lines) are taken from Reference [18]. Additional room temperature data (solid line) is taken from Reference [1].

to the relatively low readout rates. P-channel CCD's are presently under study for space applications due to the expected improvement in resistance to damage produced by high-energy protons in the space environment when compared to n-channel CCD's [7], [8], [9].

Previous n-channel "deep-depletion CCD's" [10], [11], [12], [13], [14] have 40–80 μm thick depletion regions, due to the use of more highly doped starting silicon and the lack of a substrate bias voltage. Early work on CCD's fabricated on high-resistivity n-type silicon was reported, although problems with high dark current were noted [15], [16]. The same group later described fully-depleted, deep-depletion n-channel CCD's with implanted backside layers [17]. In the prior work cited, the interest was primarily in extended x-ray response. As noted earlier our interest in a thick CCD is motivated by improved near-infrared response. Figure 2 shows calculated absorption length in silicon as a function of wavelength [18]. Absorption length is defined here as the reciprocal of absorption coefficient α defined in terms of attenuation of incident light intensity I_0 with depth y, *i.e.* $I(y) = I_0 e^{-\alpha y}$.

Given that silicon is an indirect-gap semiconductor, two regions are of interest. For photon energies above the direct bandgap energy of 2.5 eV, corresponding to a wavelength of approximately 500 nm, light absorption is highly efficient and the absorption coefficient is determined by available conduction band states [19], [20]. Hence the absorption coefficient for direct transitions α_d varies as the square root of energy as per the energy dependence of the conduction band density of states, *i.e.*

$$\alpha_d = A\sqrt{h\nu - E_{g,\mathrm{direct}}(T)} \qquad (1)$$

The temperature dependence is due to the band gap term $E_{g,\mathrm{direct}}(T)$ and is relatively weak in the direct gap regime. A is a constant, $h\nu$ is the photon energy, and T is the absolute temperature.

Below photon energies of 2.5 eV, phonons are required for momentum conservation and the absorption process becomes less efficient and more sensitive to temperature due to the phonon statistics. In the indirect absorption regime the absorption coefficient goes as [19], [20]

$$\alpha_i = \frac{B(h\nu - E_{g,\mathrm{indirect}} + E_p)^2}{\exp(E_p/kT) - 1} + \frac{B(h\nu - E_{g,\mathrm{indirect}} - E_p)^2}{1 - \exp(-E_p/kT)} \qquad (2)$$

where the terms are due to phonon absorption and emission, respectively. k is Boltzmann's constant, E_p is the phonon energy, and B is a constant. Equation 2 is valid for photon energies greater than $E_{g,\mathrm{indirect}} + E_p$ while only the phonon absorption term contributes to the absorption coefficient for photon energies of $E_{g,\mathrm{indirect}} \pm E_p$.

The net result is an absorption length that increases with wavelength as shown in Figure 2. At photon energies comparable to the indirect bandgap energy the absorption length can be more than 100 μm, requiring thick CCD's to achieve high QE in the near-infrared.

An advantage of a thick CCD fabricated on high-resistivity silicon is that the CCD clock levels can be set to optimize performance parameters such as charge transfer efficiency and well depth while the nearly independent substrate bias is used to achieve full depletion. A one-dimensional depletion-approximation solution to the Poisson equation for a thick CCD with applied substrate bias is given in Appendix A. The potential V_J at the buried-channel/substrate junction is approximately equal to the potential minimum $V_{\min}$ and is given by

$$V_J \approx V_G - V_{FB} - \frac{qN_A}{2\epsilon_{\mathrm{Si}}} {y_J}^2 \left(1 + \frac{2\epsilon_{\mathrm{Si}} d}{\epsilon_{\mathrm{SiO_2}} y_J}\right) \qquad (3)$$

which is independent of the substrate bias voltage V_{sub}. V_G is the applied gate voltage, V_{FB} is the flat-band voltage, q is the electron charge, N_A is the doping density in the p channel of depth y_J, d is the gate insulator thickness, and ϵ_{Si} and $\epsilon_{\mathrm{SiO_2}}$ are the permittivities of silicon and silicon dioxide, respectively.

This approximation is valid for $N_D \ll N_A$ and $y_N \gg y_J + (\epsilon_{\mathrm{Si}}/\epsilon_{\mathrm{SiO_2}})\, d$, where y_N is the thickness of the fully-depleted, n-type region with doping density N_D (see Figure 16 in Appendix A). For the CCD's considered here N_D is more than four orders of magnitude less than N_A, and therefore only a small fraction of the field lines from the channel are required to terminate in the substrate. Hence nearly all the field lines from the channel terminate in the gate, which is the physical interpretation of Equation 3. The third and fourth terms of Equation 3 are the voltage drops across the fully depleted channel and the voltage drop across the oxide when the channel is fully depleted. Equation 3 is a one-dimensional approximation to a decidedly two-dimensional problem, and it is shown in Appendix A that the effect of the barrier phases is to slightly raise the value of V_J when compared to the 1-d approximation. However, it is still true that the potential at the junction is a weak function of the substrate bias due to the large difference in doping between the channel and substrate and the use of a thick depleted substrate.

In addition, a thick CCD reduces fringing [21]. In thinned CCD's fringing arises due to multiple reflections at long wavelengths when the absorption length of the incident light is greater than the CCD thickness. Fringing as well as the loss of QE limits the usefulness of scientific CCD's at long wavelengths.

There are several drawbacks to a thick CCD, however. Charged-particle events from cosmic rays and terrestrial radiation sources will affect more pixels in a thick CCD [22]. Also, a larger volume for near-infrared response implies more volume for dark current generation and care must be taken during processing to minimize dark current. In addition, reduction of surface current due to interface states is not as straightforward as in a thinned CCD with no substrate bias, although as shown later surface dark current suppression can be done satisfactorily at cryogenic temperatures.

In low-f number optical systems where the light is incident at large angles from the normal, there will be depth of focus issues for long-wavelength light absorbed at significant depths, although the large refractive index of silicon helps in this regard by "straightening" the light. At the short wavelength end, the photogenerated holes must traverse nearly the entire thickness of the CCD, and spatial resolution is a concern. This is discussed in more detail in Section VI. In the next section the fabrication technology is described, followed by discussion of transistor behavior of buried channel MOS devices fabricated on high-resistivity silicon.

III. CCD Fabrication and Back-Illumination Technology

The CCD's discussed in this work were fabricated at the Lawrence Berkeley National Laboratory Microsystems Laboratory [3]. The starting material was 100 mm diameter, (100), high-resistivity, n-type silicon manufactured by Wacker Siltronic.

The gate insulator consists of 500 Å of thermally grown SiO_2 and 500 Å of low-pressure chemical vapor deposited (LPCVD) Si_3N_4. The triple polysilicon gate structures are plasma etched in Cl_2/HBr for high selectivity to the underlying Si_3N_4 layer. Single-level Al-Si is used for metallization. In-situ doped (phosphorus) polysilicon is used for extrinsic gettering [6], and this layer is deposited on the back side of the wafer early in the process and capped with Si_3N_4 to eliminate oxidation of the layer and possible autodoping during subsequent processing. A notch implant [23] is included in the process and is used in the serial register to confine small-signal charge packets to a 3 μm wide channel in the serial register, which is wider than the vertical channel to accommodate binning.

Figure 3 shows an example of a 100 mm diameter wafer fabricated at LBNL. The large devices in the center of the wafer are 2048 × 2048, 15 μm pixel CCD's. The vertical register is split into two equal regions allowing for frame store operation, although in most cases the two sets of vertical clocks are connected and the CCD is operated as a frame transfer device. The serial register located along one side of the CCD is similarly split, allowing for readout to either amplifier or to both for faster readout rates. The wafer also includes additional 15 and 24 μm pixel CCD's.

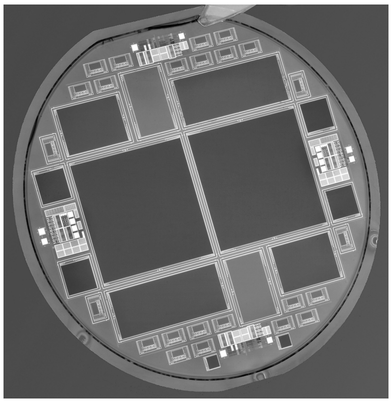

Fig. 3. 100 mm diameter wafer fabricated at LBNL. The two large CCD's in the center of the wafer are 2048 × 2048, 15 μm pixel, frame transfer CCD's.

Since the structure shown in Figure 1 is essentially a CCD merged with a p-i-n diode, we require a backside ohmic contact in order to apply the substrate bias needed to fully deplete the wafer thickness. This ohmic contact layer must be thin to allow for short-wavelength light transmission. In Figure 2 it can be seen that the absorption length is less than 0.1 μm for wavelengths less than about 400 nm, and becomes less than 100 Å at ultraviolet (UV) wavelengths.

Previous back-illumination techniques for conventional scientific CCD's include UV flooding [24] and laser annealing of an ion implanted backside layer [13], [25]. In both cases a built-in field is generated to overcome the native depletion layer at the backside surface for p-type silicon due to positive fixed oxide charge at the silicon-SiO_2 interface [1]. Laser annealing is required since the thinning step is performed on a finished wafer and the annealing temperature of the backside implant is limited to ≈ 475–525°C depending on the metallization used [26].

Since the devices fabricated on high-resistivity silicon can be made relatively thick, it is possible to create the backside layer as a high-temperature step before the Al is deposited. Bosiers *et al.* [17] were able to demonstrate conventional high-temperature annealing of an implanted backside p^+ layer by virtue of the use of relatively thick (150 μm and below) high-resistivity substrates that could be processed through the metallization step after the implant was annealed. Our technique involves removing the ≈ 1 μm thick n^+ polysilicon gettering layer before the contact mask. The wafers are sent to a commercial vendor for backside polishing to the final desired thickness. Polishing of the backside surface is required for an optical quality surface, and in our experience this is especially an issue for long-wavelength light.

After the polishing step the backside ohmic contact is formed by depositing a thin (≈ 20 nm) layer of in-situ doped (phosphorus) polysilicon [27]. This layer is deposited by LPCVD at 650°C using 1.5% PH_3 in SiH_4 as the source gas. A sacrificial oxide is then sputtered on the back side and the wafers are processed through the contact and metal

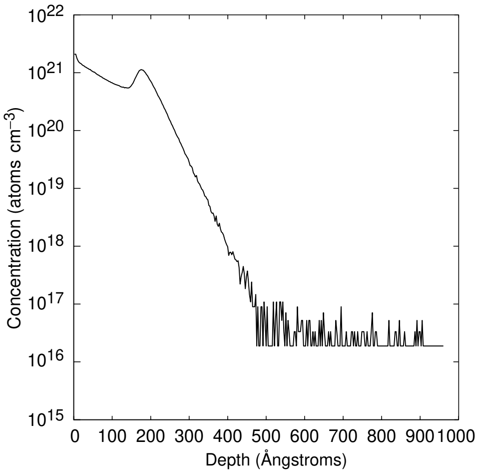

Fig. 4. Secondary ion mass spectroscopy depth profile of the thin back side ohmic contact used in this technology. The layer is fabricated by in-situ doped (phosphorus) polysilicon deposition. The detection limit for phosphorus was 1 $\times 10^{16}$ cm^{-3}.

steps. During these steps the wafers are thinner than standard. We have found that 200 - 300 μm thick, 100 mm diameter wafers can be processed with standard processing equipment. This becomes more challenging as one scales to larger diameter wafers. Modification of some automatic wafer handling equipment was required in order to avoid damaging the backside surface, as well as to minimize particle deposition on the back side. In addition, particle removal via scrubbing is used to reduce the final particle count on the back side of the wafer. If this is not done, uniformly illuminated images (flat fields) taken in the UV can show particle patterns from the various wafer handlers used in the process.

Figure 4 shows a secondary ion mass spectroscopy (SIMS) depth profile of the phosphorus concentration for a nominal 200 Å thick backside polysilicon film. The detection limit was 1 $\times 10^{16}$ cm^{-3} and the spatial resolution limit was 65 Å /decade. As can be seen in Figure 4 a very thin layer is possible with this technique. The peak in the phosphorus concentration could be due to phosphorus pile-up at the original polysilicon-silicon interface resulting from perhaps a native oxide layer present at that interface [28]. In general this is not desirable due to the potential for a built-in field that would oppose hole flow for carriers generated in the polysilicon layer, although poor collection efficiency is expected there because of low minority carrier lifetime due to Auger recombination.

It will be shown later that it is desirable to operate the CCD over depleted to minimize degradation in spatial resolution. In addition, the fairly large radial variation in resistivity for high-resistivity silicon [29] requires overdepleted operation to guarantee the elimination of field-free regions with correspondingly poor spatial resolution. A possible concern is the effect on dark current for overdepleted operation. Figure 5 shows measured dark current and inverse square capacitance $1/C^2$ measured on 2 mm^2 p-i-n diode test devices. Results are shown from wafers of

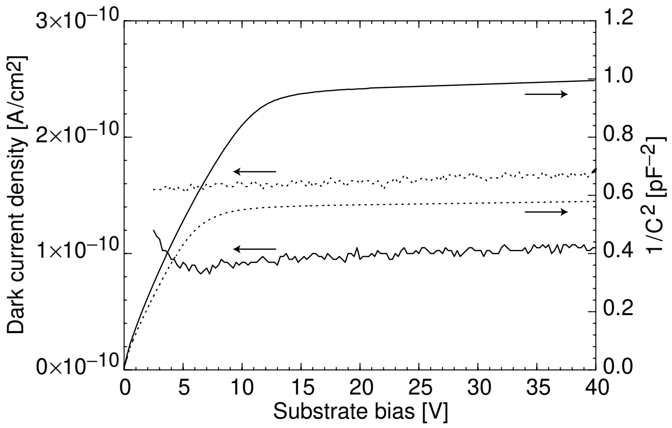

Fig. 5. Inverse square capacitance and reverse leakage current measured at room temperature on 2 mm^2 p-i-n diode test structures from CCD wafers. Data are shown for 200 μm (dotted lines) and 275 μm (solid lines) thick wafers.

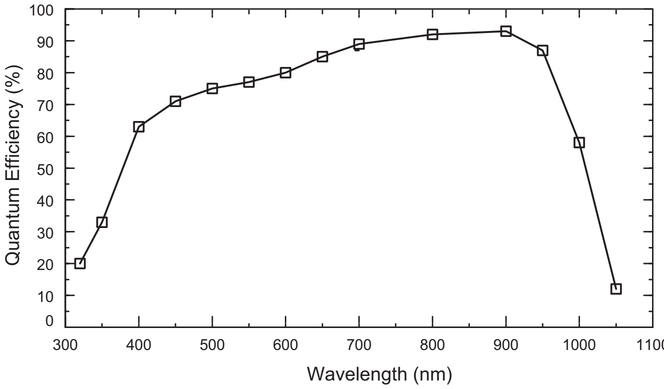

Fig. 6. Quantum efficiency measured on a 1980 $\times$ 800, 15 μm pixel back-illuminated, fully-depleted CCD. The measurement was performed at Lick Observatory and the operating temperature was $-130°$C. The thickness was $\approx$ 280 μm.

thickness $\approx$ 200 and 275 μm. These wafers went through the entire CCD process. The backside polysilicon thickness is $\approx$ 200 Å. The dark current at room temperature is less than 0.2 nA/cm^2, and does not increase significantly for bias voltages above that necessary for full depletion, where the $1/C^2$ curves approach a constant level. Therefore the gettering process is effective in maintaining low dark current for large depletion depths, and the thin polysilicon deposition step does not degrade the dark current.

After the 400°C sintering step the back side sacrificial oxide is removed and $\approx$ 600 Å of indium tin oxide (ITO) is deposited [27]. The ITO functions as part of an anti-reflection (AR) coating and improves the conductivity of the back side, where an equipotential is desired as described below. A second AR coating of $\approx$ 1000 Å of SiO_2 is added to form a 2-layer AR coating optimized for near-IR detection [21]. Figure 6 shows measured QE of an $\approx$ 280 μm thick, 1980 $\times$ 800, 15 μm pixel back-illuminated CCD with the two-layer AR coating. The QE exceeds 90% at near-infrared wavelengths, and is still $\approx$ 60% at a wavelength of 1 μm. For detailed discussion of QE modeling results for these CCD's the reader is referred to reference [21].

As a practical matter it is not convenient to make a direct electrical connection to the back side of the wafer as shown in Figure 1. Doing so would complicate the use of

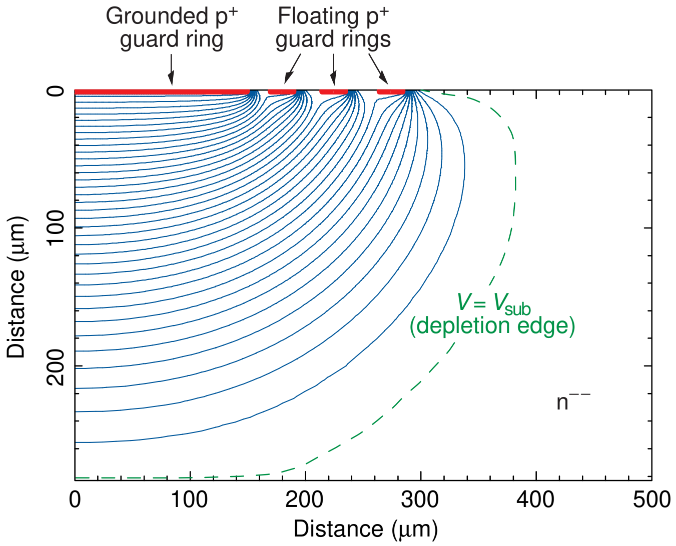

Fig. 7. Two-dimensional simulation of a p-i-n diode structure on high-resistivity silicon. The equipotential lines are spaced at 1V intervals. The substrate bias voltage was 35V and the substrate doping and thickness were 4×10^{11} cm^{-3} and 280 μm respectively.

insulating anti-reflecting coatings, for example. Instead, in the actual implementation the contact is made on the front side of the CCD. Figure 7 illustrates the technique used to bias the CCD. Shown in the figure is a two-dimensional simulation (Medici 4.0.1) of a p-i-n diode structure on a 280 μm thick high-resistivity, n-type substrate. The substrate doping used in the simulation was 4.0 $\times 10^{11}$ cm^{-3}. For convenience in the simulation the 35 V bias voltage was applied to the backside ohmic contact. Beyond the depletion edge the undepleted region is an equipotential at the applied substrate bias as long as the current flow in this region is negligible. In that case one can equivalently place an n$^+$ contact at the front side of the CCD in the undepleted region with the same result as shown in Figure 7, and apply the bias voltage more conveniently there. The function of the floating p$^+$ guard rings is to gradually drop the potential from the undepleted n region to the grounded p$^+$ guard ring that surrounds the CCD, thereby maintaining low electric fields at the surface [30], [31], [32].

Photo-generated electrons are directed by the field in the fully-depleted substrate to the backside ohmic contact where they flow laterally and are eventually drained through the undepleted substrate to the front-side n$^+$ contact located in the undepleted region. For low light level applications the dc voltage drop in the substrate due to the electron photocurrent is negligible. A 1 Mpixel CCD operating at 30 frames/sec with a high light level corresponding to 100 ke$^-$/pixel would have an electron photocurrent of only $\approx$ 0.5 μA, for example, while in low level light applications the photocurrent would be orders of magnitude smaller. The dc voltage drop in the backside ohmic contact resulting from lateral drift of electrons along the backside contact is minimized by the use of the ITO anti-reflecting layer that has a typical sheet resistance of 40 Ω/square. This biasing scheme was used in all the results presented in this paper.

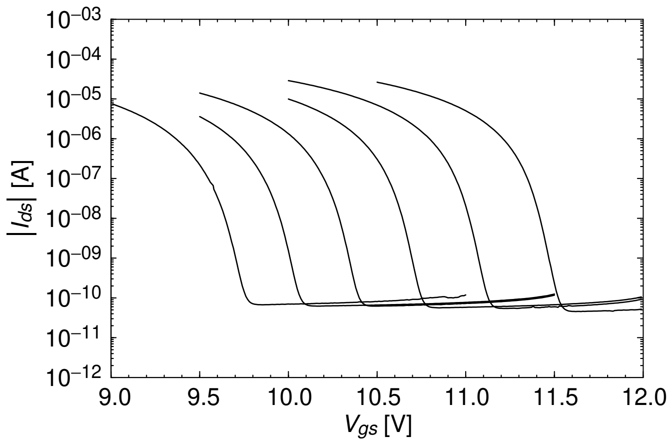

Fig. 8. Measured subthreshold characteristics of a 47/6 buried channel PMOSFET with 1.5 μm gate to source/drain spacing. The substrate bias varied from 25V (rightmost curve) to 75V (leftmost curve) in 10V steps. The temperature was $-128°$C, and the drain to source voltage was -1V.

IV. Transistor Performance

The CCD's described in this work have conventional floating diffusion amplifiers, and p-channel MOSFET's are used for reset and amplification. Given the relatively slow readout rates, the output source follower is buried channel to minimize $1/f$ noise [33], as is the reset transistor. For process simplicity, the transistors are fabricated directly in the high-resistivity substrate without the use of a well. We have found such transistors to give acceptable performance although future applications could require improvements in transistor characteristics. Several examples of active devices fabricated directly on high-resistivity silicon for high-energy physics applications have been reported [34], [35], [36], as well as early work on MOS transistors fabricated on high-resistivity silicon [37], [38].

The use of extremely low substrate doping in an MOS transistor leads to desirable features such as small bulk-junction capacitance and body effect, as well as undesirable features such as punchthrough and drain-induced barrier lowering. The latter two effects can be reduced somewhat by the application of the substrate bias used to fully deplete the substrate [3], [35]. In addition, the heavily doped source and drain regions can be offset from the gate to improve punchthrough characteristics [39], [40] as well as minimize overlap capacitance [10].

The small body effect realized for these transistors is demonstrated in Figure 8, which shows subthreshold characteristics measured on a 47/6 MOSFET with 1.5 μm gate to source/drain spacing at a temperature of $-128°$C for substrate bias voltages ranging from 25V to 75V. Over this 50V range in substrate bias the threshold voltage of the transistor is changed by only $\approx$ 1.8V, which can easily be accommodated in the CCD biasing. The data of Figure 8 were measured on a CCD with access to the gate electrode through the reset transistor. The 47/6 transistor is presently used for most single-stage, source-follower amplifier designs in this technology. The CCD was mounted in a

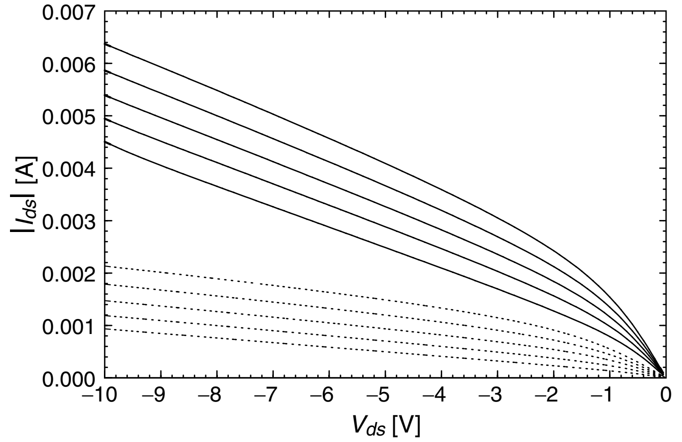

Fig. 9. Room temperature output characteristics of a 51/2 buried channel PMOSFET with 1.5 μm gate to source/drain spacing (lower curves, dotted) compared to a self-aligned transistor (upper curves, solid). The substrate bias was 25V. The gate voltage was varied from 7.5 to 3.5V in 1V steps.

commercially available cryogenic dewar. The high off-state leakage current is an artifact of the measurement, and is due to leakage current in the dewar wiring. This device had a boron channel implant dose of 1.3×10^{12} cm^{-2}. The measured subthreshold slope at $-128°$C is 50–56 mV/decade.

The effectiveness of a 1.5 μm source-drain to gate offset in improving the transistor characteristics is shown in Figure 9. Output characteristics of transistors with 2 μm channel length are shown. The self-aligned transistor has a significant threshold voltage change as well as higher output conductance when compared to the device with the 1.5 μm gap between the gate edge and heavily-doped source and drain.

Hence the transistor characteristics are adequate for scientific CCD applications even for devices fabricated on 10,000–12,000 Ω-cm silicon. In the next section we present data on CCD performance.

V. CCD performance

Figure 10 shows a far red/near infrared image of the Dumbbell Nebula M27 taken at the National Optical Astronomy Observatory WIYN 3.5–meter telescope [41] with a back-illuminated 2048 × 2048, 15 μm pixel CCD of the type shown in Figure 3. This is a false color image taken from exposures with three different filters; a narrow-band filter at the H-α line (6560 Å, blue in the image), a narrow-band filter at the [SIII] line (9532 Å, green in the image), and an intermediate band filter that detects HeII emission (1.0124 μm, red in the image).

For comparison a visible light image taken at the European Southern Observatory 8.2–meter Very Large Telescope (VLT) is shown in Figure 11 [42]. This image was taken with a commercially available, back-illuminated 2048 × 2048, 24 μm pixel CCD. The image is also generated from three filters, although in this case the filters are all in the visible range; a narrow-band filter centered at the [OIII] emission line (5010 Å, green in the image), a narrow-band filter centered at the H-α emission line (6560 Å, red in the image), and a broad band filter centered at 4290 Å (blue in the image).

The H-α detail is shown nicely in both images. The main difference in the images is the detection of background stars in the 1.0124 μm exposure, which are not seen in the image of Figure 11 due to absorption of the visible wavelengths of the background light in the dust and gas in the vicinity of the nebula. Imaging at ≈ 1 μm with high quantum efficiency and negligible fringing is a unique feature of a fully-depleted, thick CCD.

Figures 12 and 13 show charge transfer efficiency and noise results. Charge transfer efficiency was measured with an ^{55}Fe source [1] on a front-illuminated, 1478 × 4784, 10.5 μm pixel CCD. In this method the CCD is exposed to an ^{55}Fe radioactive source that emits K_α and K_β manganese x rays at energies of 5.9 and 6.5 keV, respectively. The x rays deposit a well defined amount of energy in the silicon, which on average is converted to 1620/1778 e$^-$ respectively for the K_α/K_β x rays. In Figure 12 each column of the CCD is read out in analog to digital units (ADU's), and all columns are stacked together in a single plot. The dark band is the cluster of K_α events and is used for both CTE determination and amplifier calibration. Events below this dark band are x-ray events where the charge was split into multiple pixels. The faint band above the K_α single-pixel events is the K_β band. The slope of the K_α band gives a global measure of CTE. Devices with poor CTE will show decreasing x-ray counts with increasing charge transfer distance (row number in Figure 12), or stated differently, a negative slope on a plot such as shown in Figure 12. The measurement is global in the sense that information regarding the column number of the x-ray event is not displayed in such a plot. Related to this, the serial CTE must be good in order to not affect the vertical CTE measurement. Serial CTE is determined in a similar fashion, with ADU counts plotted against column number. We typically observe no significant difference between serial and vertical CTE. The CTE defined in terms of pixel transfers determined from the data of Figure 12 was 0.9999987 at $-130°$C, and CTE's exceeding 0.999995 are typical for devices fabricated on high-resistivity silicon at LBNL. The data were truncated at ≈ 3700 rows due to decreasing x-ray counts resulting from the finite size of the x-ray source. Nonetheless, 3700 rows corresponds to a transfer length of ≈ 4 cm, and a CTE of 0.9999987 corresponds to less than 1% loss in signal after 4784 vertical charge transfers.

The read noise was previously reported to be 4–6 electrons [4], and has been improved to as low as ≈ 2 electrons by reducing the parasitic capacitance at the floating diffusion, as seen in Figure 13. Minimization of the area of the aluminum trace from the floating diffusion to the gate of the output 47/6 MOSFET accounts for most of the improvement noted in Figure 13. Charge to voltage conversion factors are estimated to be 2.0 and 3.5 μV/e$^-$ for the old and new amplifiers respectively. Even lower noise has been reported with the use of a buried contact technology to minimize the interconnect capacitance [13].

Dark currents of a few electrons per pixel per hour have been achieved at low temperatures. The importance of

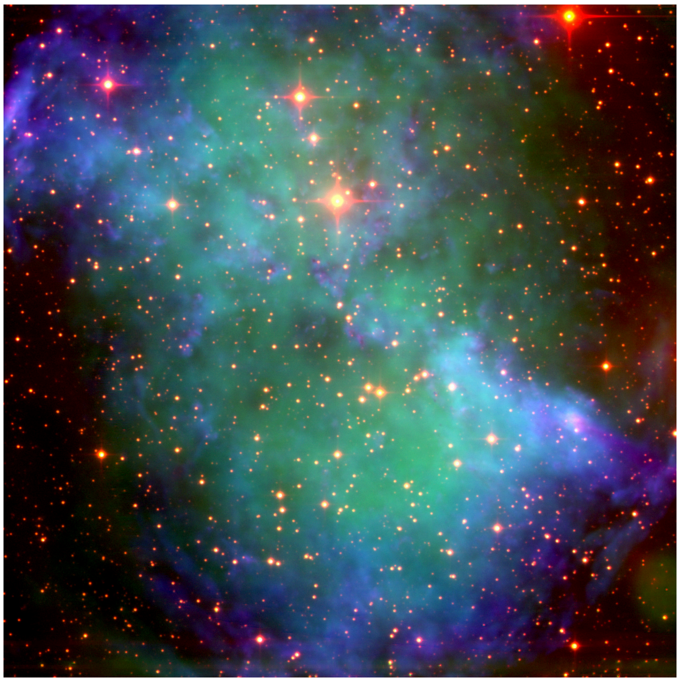

Fig. 10. Far red/near infrared image of M27 (Dumbbell Nebula) taken with a fully-depleted, back-illuminated 2048 × 2048, 15 μm pixel, high-resistivity CCD. The image was generated from exposures taken at three wavelengths (see text) at the National Optical Astronomy Observatory WIYN 3.5 meter telescope [41].

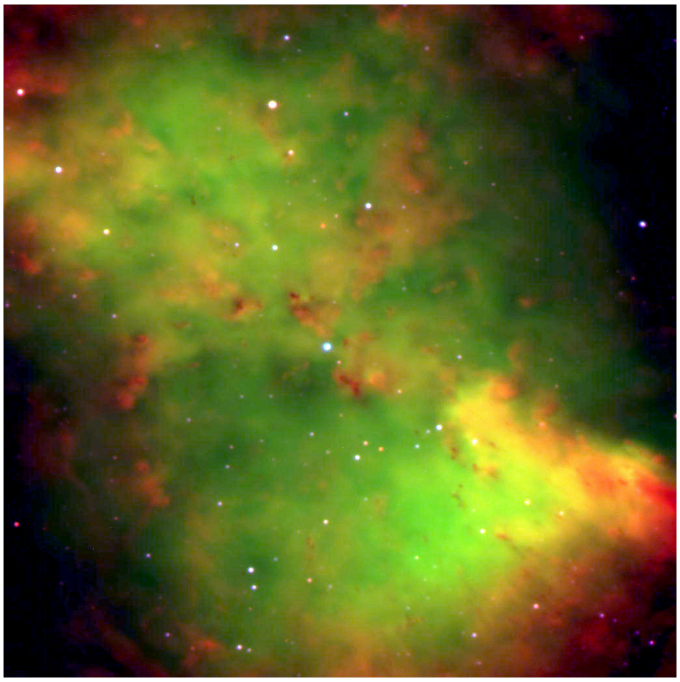

Fig. 11. Visible light image of M27 (Dumbbell Nebula) taken with a commercially available, back-illuminated 2048 × 2048, 24 μm pixel CCD. The image was generated from exposures taken at three wavelengths (see text) at the European Southern Observatory 8.2- meter Very Large Telescope (VLT) [42].

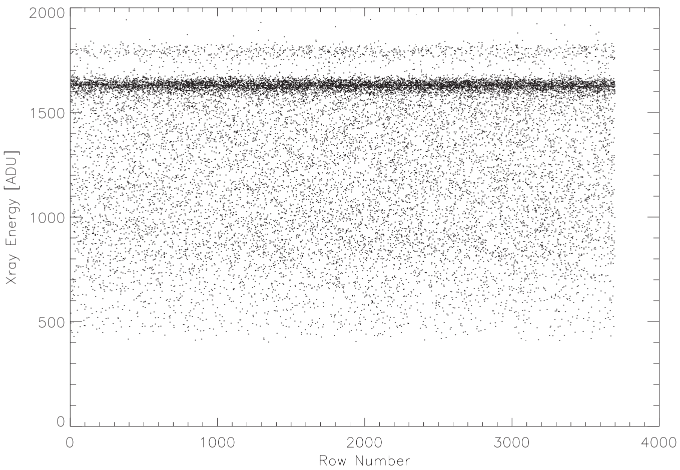

Fig. 12. Vertical charge transfer efficiency measured at −130°C on a 1478 × 4784, 10.5 μm pixel CCD.

gettering to achieve low dark current was previously described. Surface dark current arising from surface states at the silicon-silicon dioxide interface is also an important issue [43]. In typical scientific CCD's the surface dark current is reduced by operating the surface of the buried channel in inversion at least part of the clock cycle [44], [45], [46].

Supply of inversion layer carriers from the implanted channel stops located between channels is not straightforward when relatively large substrate bias voltages are applied, as in the case of the CCD's considered in this work. This is a drawback to the use of a substrate bias to fully deplete the CCD. Nonetheless, one can take advantage of the temperature dependence of the time constant for detrapping of charges trapped in interface states [47]. At the low operating temperatures considered here, the time constants are on the order of hours. Figure 14 shows experimental data taken at −150°C on a back-illuminated, 2048 × 2048 CCD. The CCD was exposed to a light level exceeding the full-well capacity, resulting in photogenerated holes trapped at interface states. This charge gradually detraps during subsequent frames, causing a residual image [1]. After 14 hours the CCD then goes through an "erase" cycle that consists of lowering the substrate bias to zero volts and increasing the positive vertical clock levels to a value sufficient to invert the surface with electrons from the channel stops. After the erase cycle the CCD is operated with the normal substrate bias voltage and more dark frames are taken. The erase cycle fills the interface states with electrons, and as shown in Figure 14 dark currents on the order of a few electrons per pixel per hour are then achieved at the cryogenic operating temperatures of interest for the astronomy application.

VI. Spatial Resolution

A concern for the fully-depleted, back-illuminated CCD is spatial resolution degradation resulting from lateral spreading via diffusion of the photogenerated charge during the transit from the back side of the device, where short-wavelength light is absorbed, to the CCD potential wells located as far as 300 μm away. We first analyze the charge spreading for the case of a fully-depleted p-i-n diode. The charge spreading is described by the point spread function (PSF), which is the impulse response of the optical system [48]. It can be shown that for carriers arriving at the potential wells at the same time that the solution to the continuity equation for the lateral charge spreading is

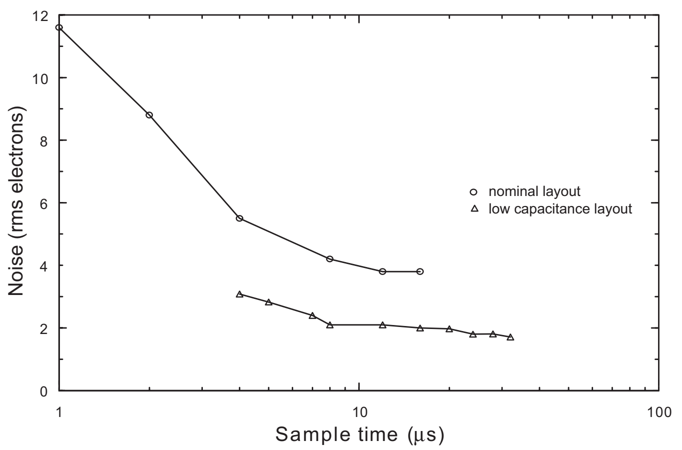

Fig. 13. Noise after double-correlated sampling versus sample time at $-130°$C comparing 47/6 output transistors with varying size metal interconnect between the floating diffusion and output transistor.

Gaussian [49]. The charge spreading is characterized by a standard deviation σ given by $\sqrt{2D\,t_{\rm tr}}$ where D is the diffusion coefficient and $t_{\rm tr}$ is the carrier transit time [50]. Assuming the fields are below the velocity saturation limit, the drift velocity of the holes is given by

$$v_{\rm DRIFT} = \frac{dy}{dt} = \mu_p E(y) = \mu_p(E_{\rm max} + \frac{\rho_n}{\epsilon_{\rm Si}} y) \qquad (4)$$

where $E(y)$ is the electric field and μ_p is the hole mobility. The expression for $E(y)$ given above is for the case of a simple p$^+$–n$^-$–n$^+$ structure that is overdepleted. $\rho_n = q\,N_D$ is the volume charge density in the depleted region. $E_{\rm max}$ is the field at the p-n junction and is given by

$$E_{\rm max} = -\left(\frac{V_{\rm appl}}{y_D} + \frac{1}{2}\frac{\rho_n}{\epsilon_{\rm Si}} y_D\right) \qquad (5)$$

where $V_{\rm appl}$ is the voltage drop across the drift region and is assumed to be larger than the depletion voltage, $\rho_n\,{y_D}^2/(2\,\epsilon_{\rm Si})$. The origin is taken at the p-n junction where $E = E_{\rm max}$, and the n$^+$ region begins at y_D, *i.e.* y_D is the thickness of the depleted region and $E(y_D) = E_D$.

Solving Equation 4 and making use of the Einstein relation $D/\mu_p = kT/q$ yields

$$\sigma_{od} = \sqrt{2D\,t_{\rm tr}} = \sqrt{2\frac{kT}{q}\frac{\epsilon_{\rm Si}}{\rho_n}\ln\frac{E_{\rm max}}{E_D}} \qquad (6)$$

The subscript indicates that this result is for an overdepleted region. An implicit assumption used in deriving Equation 6 is that the photons are absorbed at y_D, which is the worst case. At high fields σ_{od} approaches the constant-field result

$$\sigma_{od} \approx \sqrt{2\frac{kT}{q}\frac{{y_D}^2}{V_{\rm appl}}} \qquad (7)$$

which is independent of N_D, directly proportional to y_D, and proportional to $\sqrt{T}$ and $1/\sqrt{V_{\rm appl}}$. While the above derivation is for a simple p$^+$–n$^-$–n$^+$ structure, the results are also applicable to a fully depleted CCD. The field at the p-n junction of an overdepleted CCD is given by (see Appendix A)

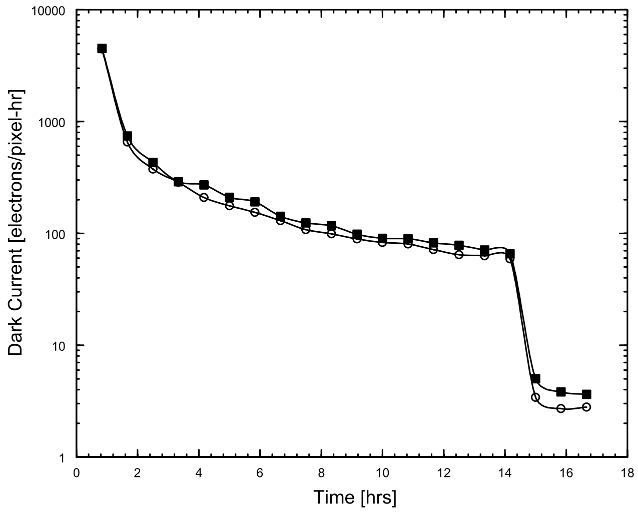

Fig. 14. Dark current versus time measured at $-150°$C for a back-illuminated, 2048 × 2048 CCD. At time zero the CCD is overexposed to light, resulting in a residual image that detraps with a long time constant at $-150°$C. After 14 hours the "erase" cycle described in the text is employed to erase the residual image and reduce the surface dark current by trapping electrons in the interface states. The open symbols are for dark current measured near the serial register, and the closed symbols are for measurements far from the serial register.

$$E_J \equiv -\frac{dV}{dy}(y_J) = -\left(\frac{V_{\rm sub} - V_J}{y_N} + \frac{1}{2}\frac{\rho_n}{\epsilon_{\rm Si}} y_N\right) \qquad (8)$$

which is of the same form as Equation 5. V_J is the potential at the buried channel junction located at y_J, $V_{\rm sub}$ is the substrate bias voltage, and y_N is the thickness of the lightly-doped, fully-depleted region. V_J was given earlier in Equation 3. From these equations the maximum field in the drift region depends on both applied voltages (V_G and $V_{\rm sub}$) and the channel implant dose $N_A y_J$.

Equations 3 and 8 are derived from a one-dimensional analysis. For CCD's on high-resistivity silicon the potentials are strongly two dimensional [11], [15], since a region exists below the buried channel implant where the field is significantly larger than predicted by Equation 8. As a practical matter the charge spreading in the high-field region is negligible and Equation 8 can still be used, but V_J is not the potential at the junction but an average potential where the field deviates from Equation 8.

We next derive the PSF for conventional back-illuminated scientific CCD's that typically have a region of zero electric field between the back side illumination surface and the CCD potential wells [1], [51]. The modulation transfer function (MTF) was theoretically analyzed for this case by Crowell and Labuda [52], where MTF is the magnitude of the Fourier transform of the PSF [48]. This work was later extended by Seib [53] to include the possibility of multiple reflections as would occur when the absorption depth of the incident light is larger than the thickness of the device. Details are given in Appendix B, where it is shown that for negligible recombination and light absorbed near the back surface such that the absorption depth is small compared to the field-free thickness, the MTF is given by

$$\mathrm{MTF}_{ff} \approx \frac{1}{\cosh(kL_{ff})} \tag{9}$$

where $k = 2\pi f$ where f is the spatial frequency and L_{ff} is the field-free thickness. The PSF is the inverse Fourier transform of the MTF and is then

$$\mathrm{PSF}_{ff} = \frac{1}{2L_{ff}(\cosh(\pi x/2L_{ff}))} \tag{10}$$

where x is the lateral dimension (see Figure 1). The rms standard deviation can be calculated from the Moment Theorem [54] and is given by

$$\sigma^2 = \frac{-F^{(2)}(0)}{4\pi^2 F(0)} + \frac{1}{4\pi^2}\left[\frac{F^{(1)}(0)}{F(0)}\right]^2 \tag{11}$$

where $F^{(n)}(0)$ is the n^{th} derivative of the Fourier transform F evaluated at the origin. Substitution of Equation 9 with $k = 2\pi f$ into the above yields the simple result

$$\sigma_{ff} = L_{ff} \tag{12}$$

and hence the rms standard deviation for the field-free case is just equal to the field-free thickness. This result was previously given based on the results of Monte Carlo simulations [55]. The above analysis is highly simplified, and is not rigorously valid given the fact that CCD's do not meet the shift invariance requirement for the use of Fourier transforms in the modeling of MTF and PSF [48], [54].

Nonetheless, it is informative to compare the rms standard deviations of charge spreading for the case of an overdepleted substrate (Equation 7) and where the field-free thickness dominates (Equation 12). Calculations of CCD depletion depth using the equations in Appendix A for a conventional CCD with no applied substrate bias show that the depletion depth is on the order of ≈ 8 μm for a substrate resistivity of 20 Ω-cm at a gate voltage of 10V with a uniform channel doping of 2×10^{16} cm^{-3}. Hence a typical 20 μm thick back-illuminated CCD fabricated on 20 Ω-cm silicon with no substrate bias could have a σ of about 12 μm. This can be improved with further thinning but at the expense of red response and fringing.

In the overdepleted case the lateral diffusion can be reduced by lowering the thickness and/or operating temperature, and by increasing the substrate bias. Figure 15 shows experimental data of charge spreading versus substrate bias voltage for an ≈ 300 μm thick CCD at -130°C. The charge spreading was measured by illuminating the CCD through a chrome-on-quartz pinhole mask that was placed directly on the back surface of the CCD. 400 nm light was used in order to maximize the transit distance of the photogenerated holes.

At a typical substrate bias voltage of 40V σ is about 8-10 μm, which would be comparable to the theoretical calculation given above for a conventional back-illuminated CCD fabricated on 20 Ω-cm silicon. Therefore, even though the CCD fabricated on high-resistivity silicon is much thicker than its low-resistivity counterpart, the spatial resolution can be comparable and in some cases better. Measurements at the Lick Observatory Hamilton Spectrograph on a 200 μm thick, 2048 $\times$ 2048, 15 μm pixel CCD give an overall PSF of ≈ 1.4 pixels full width at half maximum (FWHM), compared to a value of ≈ 2.1 pixels FWHM measured on a thinned, back-illuminated CCD [56].

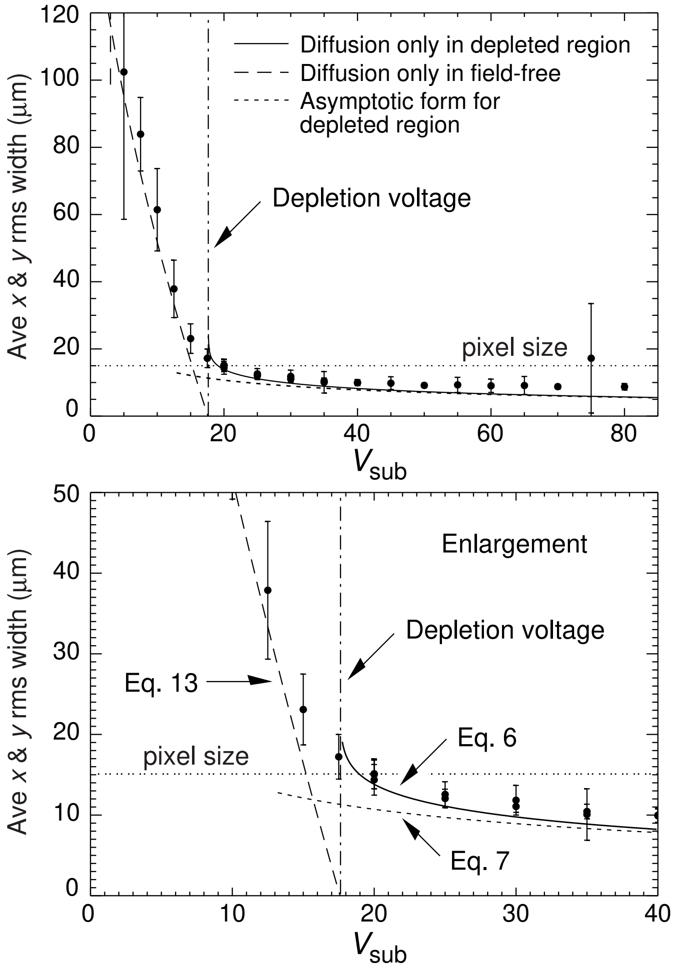

Fig. 15. Measured charge spreading σ using a pinhole mask placed directly on the back side of a back-illuminated CCD fabricated on high-resistivity silicon.

Figure 15 also includes theoretical curves for the charge spreading. Two parameters, the doping density N_D and potential at the buried channel junction V_J, are required for the theoretical curves shown in the Figure (Equations 6, 7, 8, and 3). These are determined from data taken below full depletion where the field-free thickness dominates the σ measurement, and where the field-free thickness varies with N_D and V_J as per simple p-n junction theory [57], *i.e.*

$$L_{ff} = y_N - \sqrt{\frac{2\epsilon_{\mathrm{Si}}}{qN_D}(V_{\mathrm{sub}} - V_J)} \tag{13}$$

A plot of $(y_N - L_{ff})^2$ versus V_{sub} should yield a straight line from which N_D and V_J can be determined.

VII. Summary

Fully-depleted CCD's fabricated on high-resistivity silicon have been shown to have improved characteristics at near-infrared wavelengths when compared to conventional scientific CCD's. Physical operating principles of the fully-depleted CCD have been presented along with technology issues and performance results. Trade-offs in terms of QE and spatial resolution as determined by device thickness and operating temperature can be analyzed based on the results given in this work and optimized for a given application.

VIII. Acknowledgements

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Appendix A: Derivation of potentials and fields for an overdepleted CCD

Figure 16 shows the cross-section of the CCD. The origin is taken at the silicon-SiO_2 interface. The gate insulator thickness is d, the junction depth is at y_J, and the thickness of the substrate is $y_J + y_N$. We treat the junction at the substrate - n^+ backside ohmic contact (not shown) as a one-sided step junction and neglect the voltage drop in the backside ohmic contact. The CCD is assumed to be overdepleted in what follows.

Poisson's equation in the various regions is

$$\frac{d^2V}{dy^2} = 0 \qquad -d < y < 0 \tag{A1}$$

$$\frac{d^2V}{dy^2} = \frac{qN_A}{\epsilon_{\rm Si}} \qquad 0 < y < y_J \tag{A2}$$

$$\frac{d^2V}{dy^2} = \frac{-qN_D}{\epsilon_{\rm Si}} \qquad y_J < y < (y_J + y_N) \tag{A3}$$

The solutions to Poisson's equation subject to the boundary conditions $V(-d) = V_G - V_{FB}$, $V(y_J + y_N) = V_{\rm sub}$, and continuity of electric field and potential at y =0 and y_J are

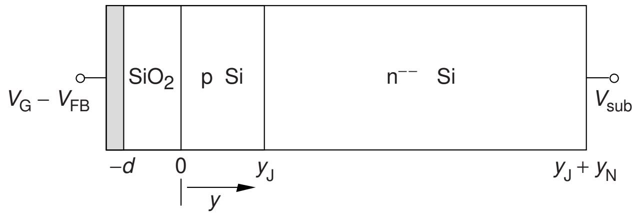

Fig. 16. CCD cross section.

$$V(y) = V_G - V_{FB} - E_{{\rm SiO}_2}(y + d) \qquad -d < y < 0 \tag{A4}$$

$$V(y) = V_{\rm min} + \frac{qN_A}{2\epsilon_{\rm Si}}(y - y_{\rm min})^2 \qquad 0 < y < y_J \tag{A5}$$

$$V(y) = V_J - \frac{qN_D}{2\epsilon_{\rm Si}}(y - y_J)^2 - E_J(y - y_J) \qquad y_J < y < (y_J + y_N) \tag{A6}$$

where $V_J \equiv V(y_J)$, $V_{\rm min} \equiv V(y_{\rm min})$, *i.e.* $y_{\rm min}$ is the location of the potential minimum. The corresponding electric fields are

$$E(y) = E_{{\rm SiO}_2} \qquad -d < y < 0 \tag{A7}$$

$$E(y) = -\frac{qN_A}{\epsilon_{\rm Si}}(y - y_{\rm min}) \qquad 0 < y < y_J \tag{A8}$$

$$E(y) = \frac{qN_D}{\epsilon_{\rm Si}}(y - y_J) + E_J \qquad y_J < y < (y_J + y_N) \tag{A9}$$

The electric fields are defined by

$$E_{{\rm SiO}_2} \equiv -\frac{dV}{dy}(0^-) \tag{A10}$$

$$E_J \equiv -\frac{dV}{dy}(y_J) = -\left(\frac{V_{\rm sub} - V_J}{y_N} + \frac{1}{2}\frac{qN_D}{\epsilon_{\rm Si}}y_N\right) \tag{A11}$$

where the boundary condition $V(y_J + y_N) = V_{\rm sub}$ was used to determine E_J from Equation A6. In terms of terminal voltages E_J is

$$E_J = \frac{V_G - V_{FB} - {V_{{\rm SiO}_2}}' - {V_p}' - {V_n}' - V_{\rm sub}}{y_N + y_J + (\epsilon_{\rm Si}/\epsilon_{{\rm SiO}_2})\, d} \tag{A12}$$

where

$${V_{{\rm SiO}_2}}' \equiv \frac{qN_A y_J d}{\epsilon_{{\rm SiO}_2}} \tag{A13}$$

$${V_p}' \equiv \frac{qN_A}{2\epsilon_{\rm Si}}{y_J}^2 \tag{A14}$$

$${V_n}' \equiv \frac{qN_D}{2\epsilon_{\rm Si}}{y_N}^2 \tag{A15}$$

$y_{\rm min}$, $V_{\rm min}$, and $E_{{\rm SiO}_2}$ are given by

$$y_{\rm min} = y_J + \frac{\epsilon_{\rm Si}}{qN_A}E_J \tag{A16}$$

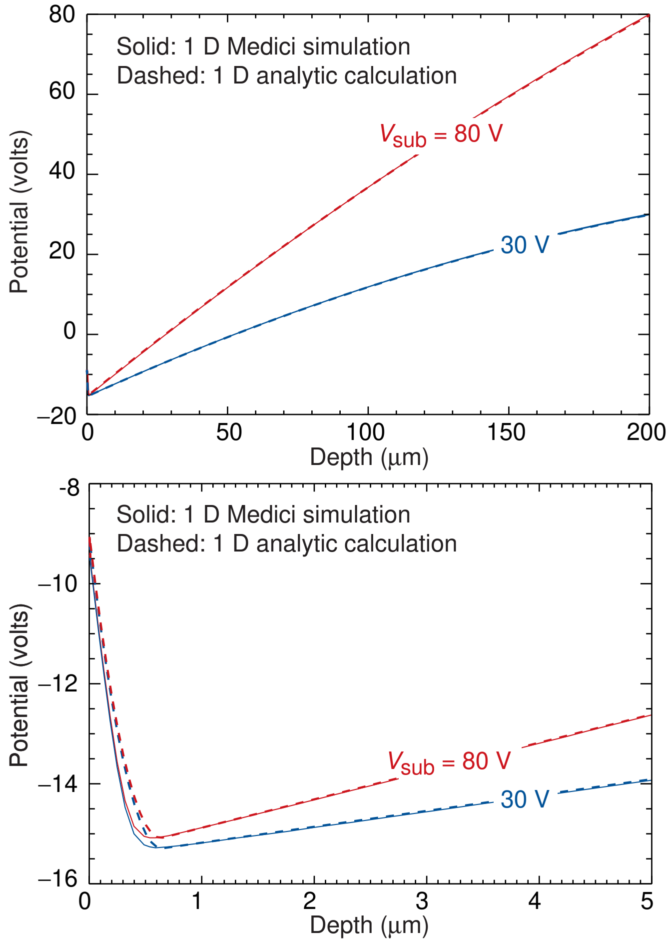

Fig. 17. Calculated and simulated potential versus depth for a CCD operated overdepleted. The calculations are based on the equations given in Appendix A, and the details of the one-dimensional simulation are described in the text. The calculations and simulations are nearly indistinguishable at the scale shown in the upper plot. The potential is plotted along the center line of the pixel.

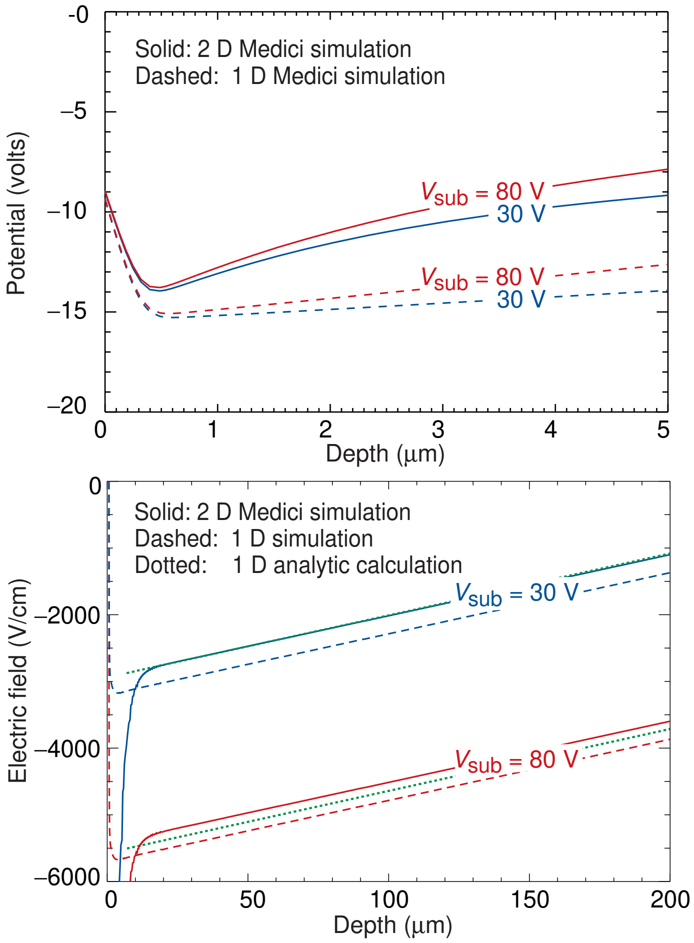

Fig. 18. Simulated potentials and electric fields versus depth for a CCD operated overdepleted. The dotted lines shown in the electric field plot were calculated from Equations A9 and A11 with V_J and y_N adjusted to give a good fit for the 30V case. The potential and field are plotted along the center line of the pixel.

$$V_{\min} = V_J - \frac{qN_A}{2\epsilon_{\mathrm{Si}}}(y_J - y_{\min})^2 \tag{A17}$$

$$E_{\mathrm{SiO_2}} = \frac{qN_A y_{\min}}{\epsilon_{\mathrm{SiO_2}}} \tag{A18}$$

For the CCD's considered here $y_N \gg y_J + (\epsilon_{\mathrm{Si}}/\epsilon_{\mathrm{SiO_2}})\,d$, and Equation 3 results from Equations A11 and A12. It also follows that if $y_N \gg y_J + (\epsilon_{\mathrm{Si}}/\epsilon_{\mathrm{SiO_2}})\,d$ then $N_D \ll N_A$ for the above derivation of potentials and fields to be valid. This can be seen from the the charge neutrality condition for field lines from the p-channel that terminate in the substrate just at full depletion, i.e.,

$$qN_A(y_J - y_{\min}) = qN_D y_N \tag{A19}$$

Figure 17 compares the potential calculated from the above equations to a one-dimensional simulation (Medici 4.0.1). The simulation cross section shown in Figure 1 was used and was generated from realistic process conditions that were input to the process simulator TSUPREM4. One-dimensional simulations were generated by biasing all phases in collection mode at -5V. Good agreement between the simulation and analytic model is observed except in the region to the left of the potential minimum. The discrepancy in this region is due to the fact that the uniform channel doping assumed in the analytic model does not realistically describe the simulated implanted channel. In order to constrain the analytic model it was required that the total integrated channel doping be the same as simulated (1.27×10^{12} cm^{-2}). The substrate doping and thickness were 6×10^{11} cm^{-3} and 200 μm, respectively, and the gate insulator was 41.7/50 nm SiO_2/Si_3N_4.

The interesting point to note from Figure 17 is the near insensitivity of the potential minimum to the applied substrate bias as predicted by Equation 3. As discussed above this is a result of the thick depleted region and large difference in doping between the channel and the high-resistivity substrate. The charge neutrality condition for the overdepleted case derived from Equations A11 and A16 with the substitution $V_n{}' + \Delta V$ for $V_{\mathrm{sub}} - V_J$ is

$$(y_J - y_{\min}) = \frac{N_D}{N_A} y_N + \frac{\epsilon_{\mathrm{Si}}}{qN_A}\frac{\Delta V}{y_N} \tag{A20}$$

where $V_n{}' = qN_D y_N^2/2\epsilon_{\mathrm{Si}}$ is the depletion voltage and ΔV is the voltage above full depletion. For typical values of N_D and N_A of 4×10^{11} cm^{-3} and 2×10^{16} cm^{-3}, respectively, Equation A20 predicts that only 0.6% of the field lines from the channel terminate in the substrate just at full depletion for y_J and y_N values of 1 and 300 μm, respectively. If the substrate is overdepleted by ΔV=50V only 1.7% of the field lines from the channel terminate in the substrate. Hence in this example nearly all the field lines from the channel terminate on the gate electrodes. The voltage drop across the channel, and therefore the potential minimum, is a weak function of the substrate bias voltage when $N_D \ll N_A$ and $y_N \gg y_J + (\epsilon_{\mathrm{Si}}/\epsilon_{\mathrm{SiO_2}})\, d$. The latter can be rewritten as $C_{DEPL} \ll C_S$ where $C_{DEPL} = \epsilon_{\mathrm{Si}}/y_N$ is the capacitance of the fully depleted n region and C_S is the capacitance of the series combination of the channel and gate insulator capacitors ($\epsilon_{\mathrm{Si}}/y_J$ and $\epsilon_{\mathrm{SiO_2}}/d$, respectively). In this context the coupling of the substrate bias to the channel is weak due to the capacitor voltage divider formed by C_{DEPL} and C_S.

One-dimensional simulations are compared to two-dimensional results in Figure 18. For the two-dimensional case the center gate electrode of Figure 1 was held at −5V while the other electrodes were biased in barrier mode at +3V. Electric fields were calculated by numerical differentiation of the simulated potentials. The effect of the positive barrier potentials is to raise the potential minimum by about a volt in this case and to increase the magnitude of the electric field over a depth of about 10 μm when compared to the one-dimensional case. As expected the insensitivity of the potential minimum to the applied substrate bias is still observed in the more realistic two-dimensional case.

The electric field calculations are needed to model the spatial resolution. As seen in Figure 18 the one-dimensional calculation overestimates the magnitude of the field. This can be easily corrected by adjusting V_J and y_N in Equations A9 and A11. This correction is shown as the dotted curves in Figure 18. As described in Section VI this is a reasonable simplification to the spatial resolution problem since negligible diffusion occurs in the high field region near the potential wells where the field is no longer described by Equation A11.

Appendix B: Derivation of PSF for a back-illuminated CCD with a field-free region

A back-illuminated photodiode array consisting of p$^+$ diodes on n-type silicon, with field-free thickness L_{ff} and total thickness (field-free and depleted depth) L_b was considered in the Crowell and Labuda analysis [52]. Surface and bulk recombination are characterized by surface recombination velocity S and minority carrier lifetime τ. $L_o = \sqrt{D\tau}$ is the diffusion length.

The continuity equation was solved with electron-hole pair generation due to a sinusoidal light source yielding a generation term of

$$G(x,y) = \frac{N_0}{2}\alpha(1-R)(1+\cos(kx))\exp(-\alpha y) \qquad \text{(B1)}$$

where N_0 is the peak photon flux, $k = 2\pi f$ where f is the spatial frequency, and R is the wavelength-dependent reflectivity, which can be determined from optical calculations [21].

The total hole flux $J_p(x)$ consisting of the hole diffusion current entering the depletion region plus the number of holes per unit time and area that are optically generated in the depletion region is given as

$$J_p(x) = (N_0/2)(\eta_0 + \eta_k \cos(kx)) \qquad \text{(B2)}$$

where

$$\eta_k = (1-R)\left[\frac{\alpha L_k}{\alpha^2 {L_k}^2 - 1} \times \gamma - \exp(-\alpha L_b)\right] \qquad \text{(B3)}$$

$$\eta_o = \eta_k \mid_{k=0} \qquad \text{(B4)}$$

$$\begin{aligned} \gamma \;&=\; \frac{2(\alpha L_k + SL_k/D) - (\beta_+ - \beta_-)\exp(-\alpha L_{ff})}{\beta_+ + \beta_-} \\ &-\; (\alpha L_k)^{-1}\exp(-\alpha L_{ff}) \end{aligned} \qquad \text{(B5)}$$

$$\beta_\pm = (1 \pm SL_k/D)\exp \pm (L_{ff}/L_k) \qquad \text{(B6)}$$

$$1/{L_k}^2(k) = (1/{L_o}^2) + k^2 \qquad \text{(B7)}$$

Note that η_o models the QE in the presence of surface and bulk recombination for the case of a field-free region at the back surface. A further refinement to the basic quantum efficiency model including an electric field at the back surface was given by Blouke *et al.* [51].

In order to simplify the above, we first neglect bulk recombination. This results in $1/L_k(k) \approx k$ with β now given by

$$\beta_\pm \approx (1 \pm S/(Dk))\exp \pm (kL_{ff}) \qquad \text{(B8)}$$

We further assume that the absorption length is small compared to L_{ff}, so that αL_{ff} and αL_b are large. Hence the exponential terms in Equations B5 and B3 are neglected, and γ becomes

$$\gamma \approx \frac{2\alpha}{k(\beta_+ + \beta_-)} + \frac{S}{Dk(\beta_+ + \beta_-)} \qquad \text{(B9)}$$

and substitution into Equation B3 yields

$$\frac{\eta_k}{(1-R)} \approx \frac{2}{\beta_+ + \beta_-} + \frac{S}{\alpha D(\beta_+ + \beta_-)} \qquad \text{(B10)}$$

where the approximation $\alpha^2 L_k^2 \approx \alpha^2/k^2 \gg 1$ was used (valid for the spatial frequencies of interest, i.e. $\approx$ Nyquist and below). The MTF neglecting surface recombination is then

$$\begin{aligned} \text{MTF}_{ff} &= \frac{\eta_k}{\eta_o} \\ &\approx \frac{1}{\cosh(kL_{ff})} \end{aligned} \quad \text{(B11)}$$

This result can be derived from Barbe's Equation 83 [58], given below, for the case of negligible recombination.

$$\text{MTF}_{ff} \approx \frac{\cosh(L_{ff}/L_o)}{\cosh(L_{ff}/L_k)} \quad \text{(B12)}$$

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