Pixel detector R&D at UH

Gianluca Alimonti

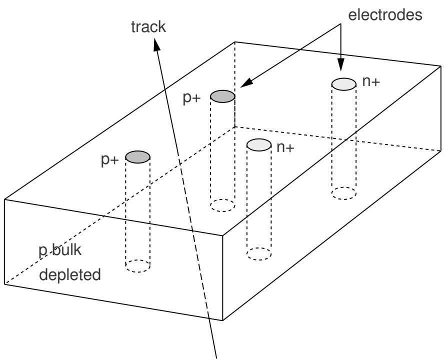
Physics and Astrophysics department
University of Hawaii
Honolulu, Hawaii 96822

Abstract. The goal is to develop a pixel detector with total thickness of $150\mu m$ with small pixel size of $40x60\mu m^2$. We fabricated dummy sensors and dummy readout chips with $50x100\mu m^2$ pixel size. They were thinned to about $100\mu m$ thick and sent out for bump bonding to AIT (Hong Kong). There were no misconnection with shorting probability of about 10^{-3}. It was found that an infrared microscope can diagnose the bump bonds as well as X-ray images. A pixel electronics that fits $50x100\mu m^2$ pixel size was developped and fabricated through MOSIS. The first round involved basic tests of analog functions and radiation hardness: they were mostly satisfactory.

3-D SENSORS

Silicon sensors with a three dimensional architecture [1,2], in which the n and p electrodes penetrate through the entire substrate, as shown in Fig. 1, have been successfully fabricated. This is allowed by the new plasma etch technology whose potential is shown in Fig. 1 where a wheel is etched in $300\mu m$ silicon.

To make the sensors two sets of narrow cylindrical holes are etched through a wafer using a plasma etcher designed for the new field of micro-machining. Each



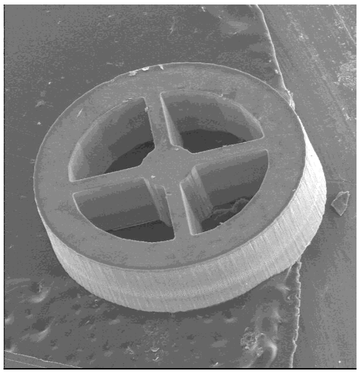


FIGURE 1. "3-D" pixel geometry and a wheel etched in $300\mu m$ of silicon.

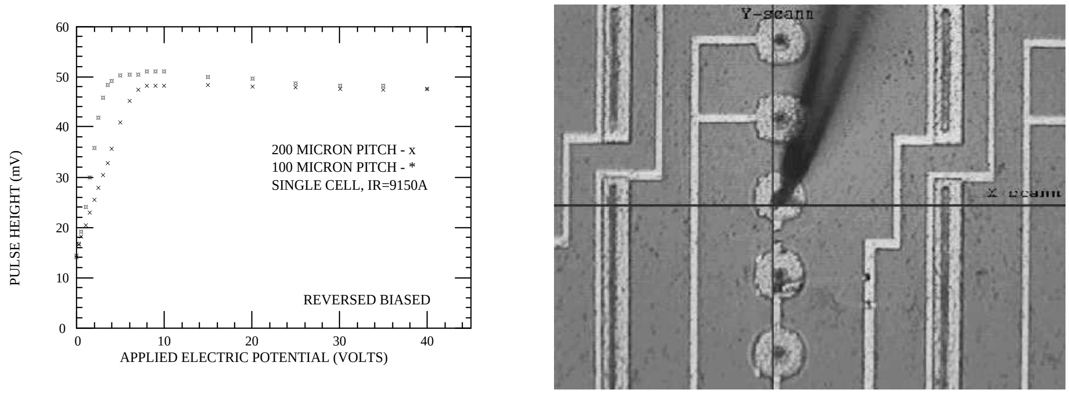


FIGURE 2. Depletion voltage for 3-D sensors and the setup for the active edge measurements.

set is then filled with n or p type polysilicon: this is done by exposing the wafer to silane gas keeping the pressure and the temperature low. Under these conditions, when a molecule does remain on the surfice of a hole, it is almost as likely to be at the bottom as at the top, thus producing a conformal layer. This is followed by the deposition of appropriate dopant gases such as P_2O_5 and B_2O_3, and by a final deposition of poly, which eventually fills the holes. Heating then lets the dopant diffuse into the single-crystal silicon and the low-leakage diode junction is thus formed.

As a result of this three dimensional architecture, the electrodes can be separated from each other by distances that are less than the substrate thickness: the maximum drift and depletion distances are then set by the elctrode spacing rather than the sensor thickness, thus allowing short collection time and low depletion voltages; on the left side of Fig. 2 is shown a depletion voltage around 5 Volts for a $100\mu m$ pitch cell and below 10 Volts for a $200\mu m$ pitch cell.

Even if no special hardening steps have been taken in the initial fabrication runs, these features from a three dimensional architecture produce an intrinsic resistance to the effects of radiation damage. After irradiation with 10^{14} 55 $Mev\ protons/cm^2$ the depletion voltage is around 20 Volts for a $200\mu m$ pitch sensor and the leakage current is still at a reasonable level even at room temperature.

Last, but not least, this kind of sensor can be sensitive up to the very edge having virtually no dead area: trenches can be etched and doped, just as holes can. Forming the sensor edges with doped trenches could be used to produce detectors with no dead regions near their edges. Trenches have been implanted in silicon and these devices behave as diodes with low leakage current, have a signal plateau at expected voltage and show a sensitive area that extends to the trench edge. Fig. 2 shows such a device where an isolated p electrode is connected to a pico-probe; the sensor is biased and x and y scanned with an IR light peaking at $820nm$. The FWHM of the signal collected by the pico-probe is in perfect agreement with the $75\mu m$ pitch of the p electrodes and the $290\mu m$ spacing between the trenches.

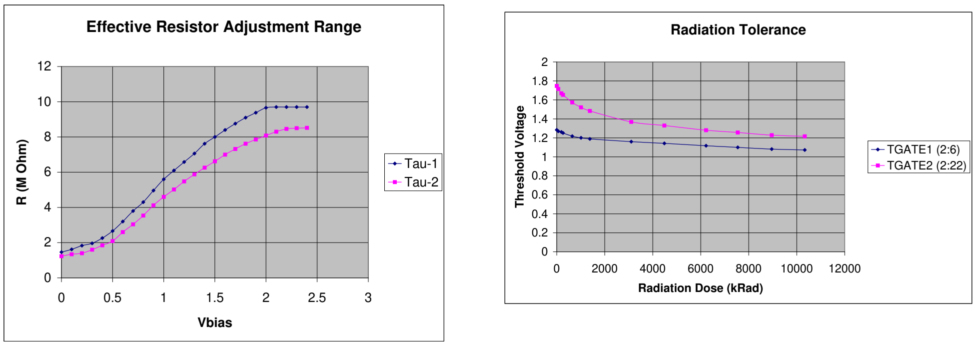


FIGURE 3. Test results: good analog performance on the left, excellent radiation hardness on the right.

SMALL FOOTPRINT ELECTRONICS

As part of the effort to improve the vertexing performance of the Belle detector [3], research on a pixel detector unpgrade has been ongoing. Motivation of the choice of readout scheme is that with a small input capacitance, a direct measurement of the voltage generated from the charge signal may be obtained. In this way the need for a preamplifier is removed, significantly reducing space and standing-power requirements. As an example, from a 100 μm thick sensor and a normally incident minimum ionizing particle the voltage generated from a complete charge collection is about 60 mV. Using a low power comparator this value may be converted into an encoded signal in a "quiet" environment, with a minimum of clocking and other noise present, over a portion of the available readout time. After encoding, the data is ripped out of the chip at maximum possible speed, as there are no longer any sensitive analog signals with which to have to be concerned.

Choice of the pixel size, $50x100\mu m$, was made at an early stage to allow sensor and readout electronics to decouple during the prototype stage. A prototype readout circuit has been fabricated in the HP $0.5\mu m$ CMOS process. Test demonstrating good analog performance and radiation hardness are found in Fig. 3, indicating that this technology should be able to function up to many MRad ^{60}Co $1Mev$ γ dose. Migration to $.25\mu m$ process is considered a necessity for obtaining optimal spatial utilization, better radiation tolerance and availability of future fabrication runs.

BUMP BONDING

Critical to the success of a hybrid detector approach is the ability to interconnect the sensor and the electronics reliably. To evaluate the process and difficulties of bump bonding fine pitch $(50x100\mu m)$ devices, a set of $300\mu m$ and $100\mu m$ thickness dummy sensor/detector pairs were fabricated and given to AIT to process. Dummy sensor/detector pairs were designed in such a way that after being bonded, pads

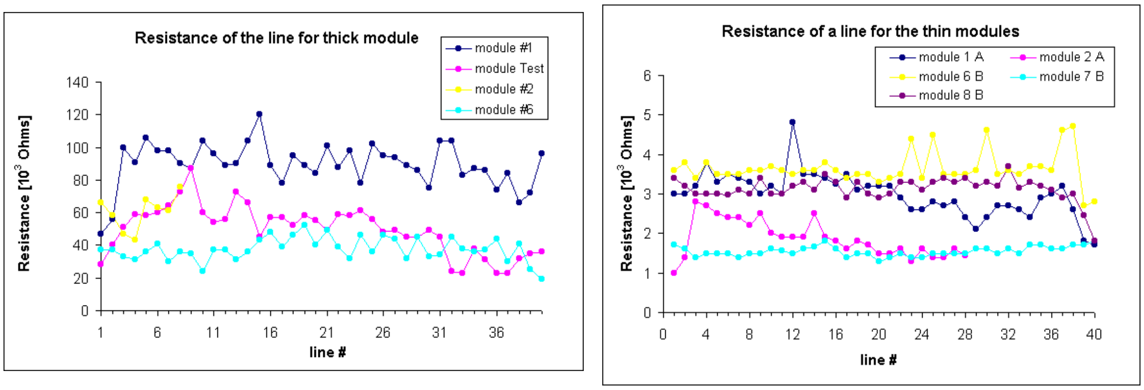


FIGURE 4. Resistance of 24 In bumps for thick (left) and thin modules.

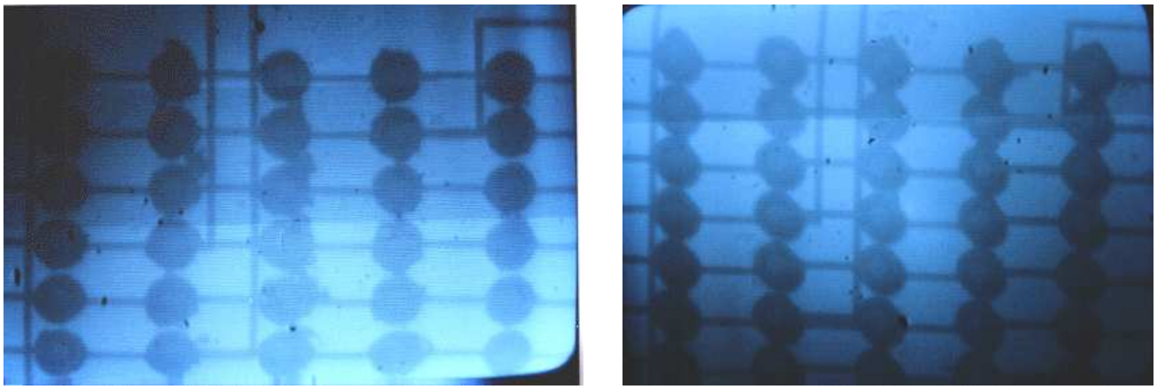


FIGURE 5. IR images of bonded chips: smashed on the left, misaligned on the right.

were available on the sides to allow the resistance measurement of lines with 24 bumps each. Results from thin and thick connectivity measurements are shown in Fig. 4. No open bump-to-bump connection was observed and, discarding the first 20% processed chips as considered being "learning" chips, the remaining 80% had a rate of inter-line shorts of about one in a thousand.

We found IR microscope images are a usefull tool to visualize problems that may arise after bonding as shown in Fig. 5.

REFERENCES

1. S.Parker, C.Kenney and J.Segal "3D - A proposed new architecture for solid-state radiation detectors" NIM-A 395 (1997) 328
2. S.Parker and C.Kenney "Silicon detectors with 3-D electrode arrays: fabrication and initial test results." IEEE Vol 46, No 4, Aug. 1999
3. G.S.Varner Belle note 278 "Design reference and functional description of the first Belle pixel readout IC".