Silicon Carbide Electronic Devices

The status of emerging silicon carbide (SiC) wide-bandgap semiconductor electronics technology is briefly surveyed. SiC-based electronic devices and circuits are being developed for use in high-temperature, high-power, and/or high-radiation conditions under which conventional semiconductors cannot function. Projected performance benefits of SiC electronics are briefly illustrated for several applications. However, most of these operational benefits of SiC have yet to be realized in actual systems, primarily owing to the fact that the growth techniques of SiC crystals are relatively immature and device fabrication technologies are not yet sufficiently developed to the degree required for widespread, reliable commercial use. Key crystal growth and device fabrication issues that limit the performance and capability of high-temperature and/or high-power SiC electronics are identified. The electrical and material quality differences between emerging SiC and mature silicon electronics technology are highlighted.

1. Properties of SiC

Silicon carbide occurs in many different crystal structures, called polytypes. A comprehensive introduction to SiC crystallography and polytypism can be found in Powell *et al.* (1993). Despite the fact that all SiC polytypes chemically consist of 50% carbon atoms covalently bonded with 50% silicon atoms, each SiC polytype has its own distinct set of electronic properties. While there are over 100 known polytypes of SiC, only a few are commonly grown in a reproducible form acceptable for use as semiconductors. The most common polytypes of SiC being developed for electronics are 3C-SiC, 4H-SiC, and 6H-SiC. 3C-SiC, also referred to as β-SiC, is the only form of SiC with a cubic crystal structure. The noncubic polytypes of SiC are sometimes ambiguously referred to as α-SiC. 4H-SiC and 6H-SiC are only two of many possible SiC polytypes with a hexagonal crystal structure. Similarly, 15R-SiC is the most common of many possible SiC polytypes with a rhombohedral crystal structure.

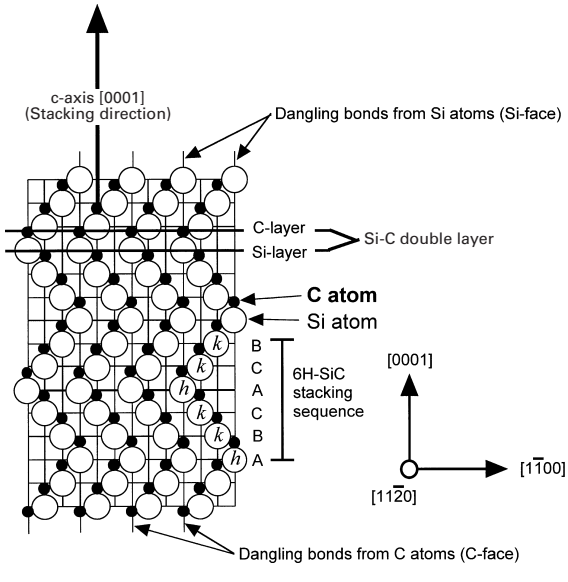

Figure 1
Schematic cross-section ((1120) plane) of the 6H-SiC polytype (reproduced by permission of IOP Publishing from "Semiconductor Interfaces, Microstructures, and Devices: Properties and Applications," 1993, pp. 257–93).

Because some important electrical device properties are nonisotropic with respect to crystal orientation, lattice site, and surface polarity, further understanding of SiC crystal structure and terminology is necessary. As discussed more thoroughly in Powell *et al.* (1993), different polytypes of SiC are actually composed of different stacking sequences of Si–C bilayers (also called Si–C double layers), where each single Si–C bilayer can simplistically be viewed as a planar sheet of silicon atoms coupled with a planar sheet of carbon atoms. The plane formed by a bilayer sheet of silicon and carbon atoms is known as the basal plane, while the crystallographic *c*-axis direction, also known as the stacking direction or the [0001] direction, is defined normal to Si–C bilayer plane. Figure 1 depicts schematically the stacking sequence of the 6H-SiC polytype, which requires six Si–C bilayers to define the unit cell repeat distance along the *c*-axis [0001] direction. The [1$\bar{1}$00] direction depicted in Fig. 1 is often referred to as the *a*-axis direction. The silicon atoms labeled "*h*" or "*k*" in Fig. 1 denote Si–C double layers that reside in "quasi-hexagonal" or "quasi-cubic" environments with respect to their immediately neighboring above and below bilayers. SiC is a polar semiconductor across the *c*-axis, in that one surface normal to the *c*-axis is terminated with silicon atoms while the opposite normal *c*-axis surface is terminated with carbon atoms. As shown in Fig. 1, these surfaces are referred to as the "silicon face" and "carbon face," respectively.

Owing to the differing arrangement of silicon and carbon atoms within the SiC crystal lattice, each SiC polytype exhibits unique electrical and optical properties. Some of the more important semiconductor electrical properties of the 3C, 4H, and 6H silicon carbide polytypes at room temperature are given in Table 1. More detailed electrical properties can be found in Choyke *et al.* (1997) and Pensl *et al.* (1998) and references therein. Even within a given polytype, some important electrical properties are nonisotropic, in that they are strong functions of crystallographic direction of current flow and applied electric field (e.g., electron mobility for 6H-SiC). Dopants in SiC can incorporate into energetically nonequivalent quasi-hexagonal (*h*) C-sites or Si-sites, or quasi-cubic (*k*)

Table 1
Comparison of properties of selected SiC polytypes with silicon and GaAs ($T = 300\,\mathrm{K}$).

Property	Silicon	GaAs	4H-SiC	6H-SiC	3C-SiC
Bandgap (eV)	1.1	1.42	3.2	3.0	2.3
Relative dielectric constant	11.9	13.1	9.7	9.7	9.7
Breakdown field at $N_D = 10^{17}\,\mathrm{cm}^{-3}$ ($\mathrm{MV\,cm}^{-1}$)	0.6	0.6	$\parallel c$-axis: 3.0	$\parallel c$-axis: 3.2, $\perp c$-axis: > 1	> 1.5
Thermal conductivity ($\mathrm{W\,cm}^{-1}\mathrm{K}^{-1}$)	1.5	0.5	3–5	3–5	3–5
Intrinsic carrier concentration (cm^{-3})	10^{10}	1.8×10^{6}	$\sim 10^{-7}$	$\sim 10^{-5}$	~ 10
Electron mobility at $N_D = 10^{16}\,\mathrm{cm}^{-3}$ ($\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$)	1 200	6 500	$\parallel c$-axis: 800, $\perp c$-axis: 800	$\parallel c$-axis: 60, $\perp c$-axis: 400	750
Hole mobility at $N_A = 10^{16}\,\mathrm{cm}^{-3}$ ($\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$)	420	320	115	90	40
Saturated electron velocity ($10^7\,\mathrm{cm\,s}^{-1}$)	1.0	1.2	2	2	2.5
Donor dopants and shallowest ionization energy (meV)	P: 45, As: 54	Si: 5.8	N: 45, P: 80	N: 85, P: 80	N: 50
Acceptor dopants and shallowest ionization energy (meV)	B: 45	Be, Mg, C: 28	Al: 200, B: 300	Al: 200, B: 300	Al: 270
Commercial wafer diameter as of 1999 (cm)	30	15	5	5	None

Sources: Sze (1981), Harris (1995), Choyke *et al*. (1997), Pensl *et al*. (1998) and references therein.

C-sites or Si-sites (only Si-sites are labeled *h* or *k* in Fig. 1). While all dopant ionization energies associated with various dopant incorporation sites should normally be considered for utmost accuracy, Table 1 lists only the shallowest ionization energies of each impurity.

For comparison, Table 1 also includes comparable properties of silicon and GaAs. Because silicon is the semiconductor employed in most commercial solid-state electronics, it is the yardstick by which other semiconductor materials must be evaluated against. To varying degrees the major SiC polytypes exhibit advantages and disadvantages in basic material properties compared to silicon. The most beneficial superior material properties of SiC over silicon listed in Table 1 are its wide bandgap energy, exceptionally high breakdown electric field, high thermal conductivity, and high carrier saturation velocity. The electrical device performance benefits that each of these properties enable are discussed in the next section, as are system-level benefits enabled by improved SiC devices.

2. *Electronics Benefits of SiC*

The wide bandgap energy and low intrinsic carrier concentration of SiC allow it to maintain semiconductor behavior at much higher temperatures than silicon, which in turn permits SiC semiconductor device functionality at these much higher temperatures. Semiconductor electronic devices function in the temperature range where intrinsic carrier concentrations are negligible so that conductivity is controlled by intentionally introduced dopant impurities. Furthermore, the intrinsic carrier concentration, n_i, is a fundamental prefactor to well-known equations governing undesired junction reverse-bias leakage currents. As temperature increases, intrinsic carriers increase exponentially so that undesired leakage currents grow unacceptably large, and eventually at still higher temperatures, the semiconductor device operation is overcome by uncontrolled conductivity as intrinsic carriers exceed intentional device dopings. Depending on specific device design, the intrinsic carrier concentration of silicon generally confines silicon device operation to junction temperatures less than 300 °C. The much smaller intrinsic carrier concentration of SiC theoretically permits device operation at junction temperatures exceeding 800 °C, and 600 °C SiC device operation has been experimentally demonstrated for a few prototype SiC devices.

The high breakdown field and high thermal conductivity of SiC coupled with high operational junction temperatures theoretically permit extremely high power densities and efficiencies to be realized. The high breakdown field of SiC relative to silicon enables the blocking voltage region of a power device to be roughly 10 times thinner and 10 times more heavily doped, permitting roughly a 100-fold decrease in the blocking region resistance. For device topology reasons discussed in Bhatnagar and Baliga (1993) and Chow *et al*. (1998), the high breakdown field and wide energy bandgap of SiC also enable much faster power switching than is possible in comparably volt-amp rated silicon power-switching devices. Therefore, SiC-based power converters can operate at higher switching frequencies with much greater efficiency (i.e., less

switching energy loss). Higher switching frequency in power converters is highly desirable because it permits use of smaller capacitors, inductors, and transformers, which in turn can reduce overall system size and weight.

While the smaller on-resistance and faster switching of SiC help minimize energy loss and heat generation, the higher thermal conductivity enables more efficient removal of waste heat energy from the active device. Because heat energy radiation efficiency increases greatly with increasing temperature difference between the device and the cooling ambient, the ability of SiC to operate at high junction temperatures permits much more efficient cooling to take place, so that heatsinks and other device-cooling hardware (i.e., fan cooling, liquid cooling, air conditioning, etc.) typically needed to keep high-power devices from overheating can be made much smaller or even eliminated.

While the preceding discussion has focused on high-power switching for power conversion, many of the same arguments can be applied to devices used to generate and amplify radio-frequency (RF) signals used in radar and communications applications. In particular, the high breakdown voltage and high thermal conductivity coupled with high carrier saturation velocity allow SiC microwave devices to handle much higher power densities than their silicon or GaAs RF counterparts, despite the disadvantage in low-field carrier mobility of SiC (Table 1) (Weitzel and Moore 1998). The high power density reduces the number of devices required to generate large total RF powers needed for fixed-base high-power RF transmission applications, thus minimizing RF matching difficulties and cooling requirements to reduce the overall system size and cost. SiC RF transistors are not well suited for low-power products, such as handheld cell telephone units.

Uncooled operation of high-temperature and/or high-power SiC electronics would enable revolutionary improvements in aerospace systems. Replacement of hydraulic controls and auxiliary power units with distributed ''smart'' electromechanical controls and sensors capable of harsh-ambient operation will lead to substantial jet-aircraft weight savings, reduced maintenance, reduced pollution, higher fuel efficiency, and increased operational reliability. SiC high-power solid-state switches will also afford large efficiency gains in electric power management and control. Performance gains from SiC electronics could enable the public power grid to meet the increased consumer electricity demand without building additional generation plants, and improve power quality and operational reliability through ''smart'' power management. More efficient electric motor drives, enabled by improved SiC power devices, will benefit industrial production systems as well as transportation systems such as diesel–electric railroad locomotives, electric mass-transit systems, nuclear-powered ships, and electric automobiles and buses.

Hostile environment SiC semiconductor devices and ICs offer little advantage if they cannot be reliably packaged and connected to form a complete system capable of operating in such environments. With proper materials selection, modifications of existing IC packaging technologies appear feasible for non-power SiC circuit packaging up to 300 °C. Prototype electronic packages that can withstand over 1000 hours of heat soaking without electrical bias at 500 °C have been demonstrated (Salmon *et al.* 1998). Harsh environment passive components, such as inductors, capacitors, and transformers, must also be developed for operation in demanding conditions before the full system-level benefits of SiC electronics can be successfully realized.

3. SiC Crystal Growth

At the start of the semiconductor electronics era, SiC was considered an early transistor material candidate along with germanium and silicon. However, reproducible wafers of reasonable consistency, size, quality, and availability at acceptable cost are a prerequisite for commercial mass production of semiconductor electronics. Because SiC sublimes instead of melting at reasonably attainable pressures, SiC cannot be grown by conventional seeded melt-growth techniques such as those employed in the manufacture silicon wafers. This prevented the realization of SiC crystals suitable for mass production of electronics until the late 1980s. Prior to 1980 experimental SiC electronic devices were mostly confined to small (typically $\sim 1\,\mathrm{cm}^2$), irregularly shaped SiC crystal platelets grown as a by-product of the Acheson process for manufacturing industrial abrasives (Acheson 1892) or by the Lely process (Lely 1955).

There have also been numerous efforts, some of which are still ongoing, to grow heteroepitaxial single-crystal 3C-SiC layers on top of large-area wafer substrate materials such as silicon or sapphire. These efforts have always resulted in SiC layers with high densities of structural defects. While some limited semiconductor electronic devices and circuits have been implemented in 3C-SiC grown on silicon, the performance benefits of these electronics are severely limited to the point where almost none of the operational benefits of SiC over silicon have been realized.

Tairov and Tsvetkov (1978) established the basic principles of a modified seeded sublimation growth process for 6H-SiC. This process, also referred to as the modified Lely process, was a breakthrough for SiC in that it offered the first possibility of reproducibly growing acceptably large single crystals of SiC that could be cut and polished into mass-produced SiC wafers. The growth process is based on heating polycrystalline SiC source material to $\sim 2400\,^{\circ}\mathrm{C}$ under conditions where it sublimes into

the vapor phase and subsequently condenses onto a cooler SiC seed crystal. This produces a somewhat cylindrical boule of single-crystal SiC that grows taller at a rate of a few millimeters per hour. The preferred orientation of the growth in the sublimation process is such that vertical growth of a taller cylindrical boule proceeds along the [0001] crystallographic *c*-axis direction (i.e., vertical direction in Fig. 1). Circular "*c*-axis" wafers with surfaces that lie normal (perpendicular) to the *c*-axis can then be sliced from the roughly cylindrical boule. Other growth orientations (such as along the *a*-axis) are also being investigated, but are not nearly as available and well developed as *c*-axis-grown wafer material.

After further development of the sublimation growth process, mass-produced sublimation-grown wafers (6H-SiC polytype, 2.5 cm diameter) became commercially available in 1989 (Cree Inc., Durham, NC, http://www.cree.com). The vast majority of SiC semiconductor electronics development has taken place since then. Other companies have subsequently entered the SiC wafer market, and sublimation-grown wafers of the 4H-SiC polytype have also been widely commercialized. *n*-Type, *p*-type, and semi-insulating SiC wafers of 2.5 cm to 5 cm in diameter are commercially available, and prototype wafers as large as 10 cm in diameter have been grown in the laboratory.

Wafer size, cost, and quality are all very critical to the manufacturability and process yield of mass-produced semiconductor microelectronics. Compared to commonplace silicon and GaAs wafer standards, 4H- and 6H-SiC wafers are small, expensive, and generally of inferior quality. However, such disparities are expected considering that silicon and GaAs wafers have undergone decades of commercial process refinement, and that SiC is an extraordinarily hard material making it very difficult to properly saw and polish.

Most SiC electronic devices are not fabricated directly in sublimation-grown wafers, but are instead fabricated in much higher quality epitaxial SiC layers that are grown on top of the sublimation-grown wafer. Therefore, the controlled growth of high-quality epilayers directly impacts on the realization of SiC electronic devices and circuits. An interesting variety of SiC epitaxial growth methods, ranging from liquid-phase epitaxy, molecular beam epitaxy, and chemical vapor deposition (CVD), have been investigated (Choyke *et al*. 1997, Pensl *et al*. 1998). The CVD growth technique is generally accepted as the most promising method for attaining epilayer reproducibility, quality, and throughputs required for mass production.

In the simplest terms, variations of SiC CVD are carried out by heating SiC substrates in a chamber with flowing silicon- and carbon-containing gases that decompose and deposit silicon and carbon onto the wafer allowing an epilayer to grow in a well-ordered single-crystal fashion under well-controlled conditions. Conventional SiC CVD epitaxial growth processes are carried out at substrate growth temperatures between 1400 °C and 1600 °C at pressures from 0.1 atm to 1 atm resulting in growth rates of the order of micrometers per hour (Powell and Larkin 1997). Higher temperature (up to 2000 °C) SiC CVD growth processes are also being pioneered to obtain higher SiC epilayer growth rates of the order of hundreds of micrometers per hour (Kordina *et al*. 1997).

Homoepitaxial growth, whereby the polytype of the SiC epilayer matches that of the SiC substrate, is accomplished by step-controlled epitaxy (Kimoto *et al*. 1997). Step-controlled epitaxy is based on growing epilayers on an SiC wafer polished at an angle (called the "tilt angle" or "off-axis angle") of typically 3–8° off the (0001) basal plane, resulting in a surface with atomic steps and flat terraces between steps as depicted schematically in Fig. 2. When growth conditions are properly controlled and there is a sufficiently short distance between steps, silicon and carbon adatoms impinging onto the growth surface find their way to steps where they bond and are incorporated into the crystal. Thus, ordered lateral "step flow" growth takes place which enables the polytypic stacking sequence of the substrate to be exactly mirrored in the growing epilayer. When growth conditions are not properly controlled or when steps are too far apart (as can occur with SiC substrate surfaces that are polished to within less than 1° of the basal plane), growth adatoms can nucleate and bond in the middle of terraces instead of at the steps, which leads to growth of poor-quality 3C-SiC (Kimoto *et al*. 1997, Powell and Larkin 1997). It is impractical to intentionally vary the polytype of SiC epilayers, so that heterojunction device structures have not been demonstrated using single-crystal SiC–SiC heterojunctions.

It is important to note that most as-grown SiC epilayers contain varying densities of undesirable defects and surface morphological features which affect SiC device processing and performance to varying degrees (Neudeck 2000). Micropipes and closed-core screw dislocations originating in *c*-axis substrates propagate through subsequently grown epilayers. Nonideal epilayer surface features commonly observed include "triangular inclusions," "growth pits," and macrosteps formed by coalescence of multiple SiC growth steps (i.e., "step bunching") during epitaxy. Pregrowth wafer polishing as well as growth initiation procedures have been shown to have a strong impact on the formation of undesirable epitaxial growth features (Powell and Larkin 1997). Continued reduction of these defects will clearly help pave the way for increasingly capable SiC devices, especially devices for very high-power applications.

In situ doping during CVD epitaxial growth is primarily accomplished through the introduction of nitrogen (usually N_2) for *n*-type and aluminum (usually trimethyl- or triethylaluminum) for *p*-type epilayers. Some alternative dopants such as phos-

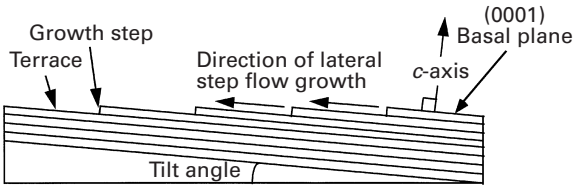

Figure 2
Cross-sectional schematic representation of "off-axis" polished SiC surface used for homoepitaxial growth. When growth conditions are properly controlled and there is a sufficiently short distance between steps, silicon and carbon adatoms impinging onto the growth surface find their way to steps where they bond and are incorporated into the crystal. Thus, ordered lateral "step flow" growth takes place, which enables the polytype stacking sequence of the substrate to be exactly mirrored in the growing epilayer (reproduced (with modifications) by permission of IOP Publishing from "Semiconductor Interfaces, Microstructures, and Devices: Properties and Applications," 1993, pp. 257–93).

phorous, boron, and vanadium have also been investigated for *n*-type, *p*-type, and semi-insulating epilayers, respectively. While reasonable variation in epilayer doping can be achieved by strictly varying the flow of dopant gases, the site competition doping method (Larkin 1997) has enabled a much broader range of SiC doping to be accomplished. In addition, site competition epitaxy has also made moderate epilayer dopings more reliable and repeatable. Commercial epilayer thickness and doping tolerances are specified at 25% and 50%, respectively, while doping uniformities of 7% and thickness uniformities of 4% over 30 mm wafers have been reported in developmental research (Burk and Rowland 1997).

4. SiC Device Fabrication

In order to minimize the development and production costs of SiC electronics, it is essential that SiC device fabrication takes advantage of existing silicon and GaAs wafer processing infrastructure as much as possible. Most of the steps necessary to fabricate SiC electronics starting from SiC wafers can be accomplished using somewhat modified commercial silicon electronics processes and fabrication tools. While 4H-SiC and 6H-SiC device processing methods are discussed in this section, these processes are generally applicable to other polytypes of SiC, except for the case of 3C-SiC grown on silicon where all processing temperatures need to be kept below the melting temperature of silicon ($\sim$ 1400 °C).

4.1 Patterned Doping by Ion Implantation

The fact that diffusion coefficients of most dopants in SiC are negligibly small below $\sim$ 1800 °C is excellent for maintaining device junction stability, because dopants do not undesirably diffuse as the device is operated for long times at high temperatures. Unfortunately, however, this characteristic also precludes the use of conventional dopant diffusion, a highly useful technique widely employed in silicon microelectronics manufacturing, for patterned doping of SiC. Therefore, laterally patterned doping of SiC is almost exclusively carried out by ion implantation. This somewhat restricts the depth that most dopants can be implanted to less than 1 μm using conventional dopants and implantation equipment. Compared to silicon processes, SiC ion implantation requires a much higher thermal budget to achieve acceptable dopant implant electrical activation. Summaries of ion implantation processes for various dopants can be found in (Pensl *et al.* 1998). Most of these processes are based on carrying out implantation at elevated temperatures ($\sim$ 500–800 °C) using a patterned high-temperature masking material. The elevated temperature during implantation promotes some lattice self-healing during the implant, so that damage and segregation of displaced silicon and carbon atoms does not become excessive, especially in high-dose implants often employed for ohmic contact formation. Co-implantation of carbon with *p*-type dopants has been shown to improve the electrical conductivity of high-dose *p*-type layers (Zhao *et al.* 1997).

Following ion implantation, the patterning mask is generally stripped prior to carrying out a very high-temperature ($\sim$ 1200–1800 °C) anneal, the purpose of which is to achieve maximum electrical activation of dopant ions. At higher implant anneal temperatures, the SiC surface morphology can seriously degrade as damage-assisted sublimation etching of the SiC surface begins to take place (Capano *et al.* 1998). Because sublimation etching is driven primarily by loss of silicon from the crystal surface, annealing in silicon overpressures can be used to prevent surface degradation during high-temperature anneals. Such overpressure is often achieved by close proximity solid sources, such as using an enclosed SiC crucible with SiC lid and/or SiC powder near the wafer, or by annealing in a silane-containing atmosphere.

4.2 Contacts

All useful semiconductor electronics require conductive signal paths in and out of each device as well as conductive interconnects to carry signals between devices on the same chip and to external circuit elements that reside off-chip. While SiC itself is theoretically capable of high-performance operation under extreme conditions, such functionality is useless without contacts and interconnects that are also capable of operation under the same conditions to enable complete circuit functionality. The durability and reliability of metal–semiconductor contacts and interconnects are one of the main factors limiting the

operational high-temperature limits of SiC electronics. Most reported SiC metallizations appear sufficient for long-term device operation at temperatures up to 300 °C. Depending on the device structure and application, SiC Schottky diode reverse leakage currents generally become excessive at temperatures greater than 400 °C. SiC ohmic and Schottky contacts to meet the demanding requirements needed for harsher environment operation (i.e., temperatures > 400 °C, high current densities, and/or oxidizing environments) are a challenging topic of ongoing research activity.

Specific overviews of SiC metal–semiconductor contact technology can be found in Porter and Davis (1995), Crofton *et al.* (1997), and Saxena and Steckl (1998). There are both similarities and a few differences between SiC contacts and contacts to conventional narrow-bandgap semiconductors (e.g., silicon, GaAs). The same basic physics and current transport mechanisms that are present in narrow-bandgap contacts, such as surface states, Fermi pinning, thermionic emission, and tunneling, also apply to SiC contacts. A natural consequence of the wider bandgap of SiC is higher effective Schottky barrier heights. Analogous to narrow-bandgap contact physics, the microstructural and chemical state of the SiC–metal interface is crucial to contact electrical properties. Therefore, premetal deposition surface preparation, metal deposition process, choice of metal, and postdeposition annealing can all greatly affect the resulting performance of metal–SiC contacts. Because the chemical nature of the starting SiC surface is strongly dependent on surface polarity, it is not uncommon to obtain significantly different results when the same contact process is applied to the silicon face surface as opposed to the carbon face surface. While Schottky contact barrier height does somewhat depend on metal–semiconductor work-function difference, the dependence is weak enough to suggest that surface state charge also plays a significant role in determining the effective barrier height of SiC Schottky junctions. Undesired nonuniformities in SiC surface properties owing to crystal defects and surface structure variations are widely suspected as the cause of uneven current flow and higher-than-expected leakage curr-barrier heights extracted by *C–V* methods typical in experimental SiC Schottky diodes. Thus, barrier heights extracted by *C–V* methods typically are higher than those extracted by *I–V* measurements.

While SiC specific ohmic contact resistances at room temperature are generally higher than in contacts to narrow-bandgap semiconductors, they are nevertheless sufficiently low for most envisioned SiC applications. Lower specific contact resistances are usually obtained to *n*-type 4H- and 6H-SiC ($\sim 10^{-4}$–$10^{-6}\ \Omega\text{cm}^2$) than to *p*-type 4H- and 6H-SiC ($\sim 10^{-3}$–$10^{-5}\,\Omega\text{cm}^2$). Consistent with narrow-bandgap ohmic contact technology, it is easier to make low-resistance ohmic contacts to heavily doped SiC. Regardless of doping, it is common practice with SiC to thermally anneal ohmic contacts to obtain the minimum possible contact resistance. Most SiC ohmic contact anneals are performed at temperatures around 900–1000 °C in nonoxidizing environments. Depending on the contact metallization employed, this anneal generally causes limited interfacial reactions (usually metal carbide or metal silicide formation) that broaden and/or roughen the metal–semiconductor interface.

4.3 Patterned Etching

At room temperature, no known wet chemical etches single-crystal SiC. Therefore, most patterned etching of SiC for electronic devices and circuits is accomplished using dry-etching techniques. Yih *et al.* (1997) give an excellent summary of dry SiC etching results. The most commonly employed process involves reactive ion etching (RIE) of SiC in fluorinated plasmas. Sacrificial etch masks (often metals) are deposited and photolithographically patterned to protect desired areas from being etched. The SiC RIE process can be implemented using standard silicon RIE hardware, and typical 4H- and 6H-SiC RIE rates are of the order of hundreds of angstroms per minute. Well-optimized SiC RIE processes are typically highly anisotropic with little undercutting of the etch mask, leaving smooth surfaces. One of the keys to achieving smooth surfaces is preventing ''micromasking'' where masking material is slightly etched and randomly redeposited onto the sample, effectively masking very small areas on the sample that were intended for uniform etching. This can result in ''grass''-like etch residue features being formed in the unmasked regions, which is undesirable in most cases. In special cases, RIE under conditions promoting micromasking is useful in greatly roughening the SiC surface to reduce the contact resistance of subsequently deposited ohmic metallizations.

While RIE rates are sufficient for many electronic applications, much higher SiC etch rates are necessary to delineate features of the order of tens to hundreds of micrometers deep that are needed to realize advanced sensors, microelectromechanical systems (MEMS), and some very high-voltage power device structures. High-density plasma dry-etching techniques, such as electron cyclotron resonance (ECR) and inductively coupled plasma (ICP), have been developed to meet the need for deep etching of SiC. Residue-free patterned etch rates exceeding $1000\,\text{Å}\,\text{min}^{-1}$ have been demonstrated (Yih *et al.* 1997).

Patterned etching of SiC at very high etch rates has also been demonstrated using photoassisted and dark electrochemical wet etching (Shor *et al.* 1997). By choosing proper etching conditions, this technique has demonstrated a very useful dopant-selective etch-stop capability. However, there are major incompatibilities of the electrochemical process that make it undesirable for VLSI mass production, including extensive pre-

etching and postetching sample preparation, etch isotropy and mask undercutting, and somewhat nonuniform etching across the sample.

4.4 Metal–Oxide–Semiconductor (MOS) Technology

The vast majority of semiconductor integrated circuit chips in use rely on silicon metal–oxide–semiconductor field effect transistors (MOSFETs), whose electronic advantages and operational device physics are summarized in other articles of this encyclopedia. Given the extreme usefulness and success of MOSFET-based electronics in silicon, it is naturally desirable to implement high-performance inversion channel MOSFETs in SiC. Like silicon, SiC forms a thermal SiO_2 oxide when it is heated to high temperatures in an oxygen environment. While this enables SiC MOS technology to somewhat follow the highly successful path of silicon MOS electronics, there are nevertheless important differences in insulator quality and device processing that prevent SiC MOSFETs from realizing their full potential. While the following discussion attempts to quickly highlight key issues facing SiC MOSFET development, more detailed insights can be found in Afanasev *et al*. (1997), Brown *et al*. (1997), Cooper (1997), and Ouisse (1997). In highlighting the difficulties facing SiC MOSFET development, it is important to keep in mind that early silicon MOSFETs faced similar developmental challenges that took many years of dedicated research to overcome successfully.

From a purely electrical point of view, there are two prime operational deficiencies of SiC oxides and MOSFETs compared to silicon MOSFETs. First, effective inversion channel mobilities in most SiC MOSFETs are much lower (typically well under $100\,cm^2V^{-1}s^{-1}$ for inversion electrons) than one would expect based on silicon inversion channel MOSFET carrier mobilities. This seriously reduces the transistor gain and current-carrying capability of SiC MOSFETs, so that they are not nearly as advantageous as theoretically predicted. Second, SiC oxides have not proved to be as reliable as well-developed silicon oxides, in that SiC MOSFETs are more prone to threshold voltage shifts, gate leakage, and oxide failures than comparably biased silicon MOSFETs. The excellent works by Cooper (1997) and Brown *et al*. (1997) discuss noteworthy differences between the basic electrical properties of *n*-type vs. *p*-type SiC MOS devices. SiC MOSFET oxide electrical performance deficiencies appear to be mostly attributable to differences between silicon and SiC thermal oxide quality and interface structure that cause the SiC oxide to exhibit undesirably higher levels of interface state densities ($\sim 10^{11}$–$10^{12}\,eV^{-1}cm^{-2}$), fixed oxide charges ($\sim 10^{11}$–$10^{12}\,cm^{-2}$), charge trapping, carrier oxide tunneling, and roughness-related scattering of inversion channel carriers. SiC surfaces are well known to be much rougher than silicon surfaces, owing to off-angle polishing needed to support SiC homoepitaxy as well as step-bunching that can occur during SiC homoepilayer growth. The wide bandgap of SiC reduces the potential barrier impeding tunneling of carriers into SiC thermal oxides, so that perfectly grown oxides on atomically smooth SiC are not be as reliable as silicon thermal oxides (Agarwal *et al*. 1997). Therefore, it is highly probable that alternative gate insulators will have to be developed for optimized implementation of inversion channel SiC FETs for the most demanding high-power and/or high-temperature electronic applications.

5. Prototyping and Production of SiC Electronic Devices

This section briefly summarizes a variety of experimentally realized SiC electronic devices broken down by major application areas. The operational performance of experimental SiC devices is compared to that predicted theoretically as well as the capabilities of existing silicon and GaAs devices. SiC process and materials technology issues limiting the capabilities of various SiC device topologies are highlighted as key issues to be addressed in further SiC technology development.

5.1 Optoelectronics and Sensors

The wide bandgap of SiC is useful for realizing short-wavelength blue and UV optoelectronics. 6H-SiC-based blue *p–n* junction light emitting diodes (LEDs) were the first SiC-based devices to reach high-volume commercial sales. These epitaxially grown, dry-etch, mesa-isolated *p–n* junction diodes were the first mass-produced LEDs to cover the blue ($\sim$ 250–280 nm peak wavelength) portion of the visible spectrum. Because the bandgap of SiC is indirect (i.e., the conduction minimum and valence band maximum do not coincide in crystal momentum space), luminescent recombination in the LEDs is governed by inherently inefficient indirect transitions mediated by impurities and phonons. Therefore, the efficiency of SiC blue LEDs is limited to well below 1%. While commercially successful from 1989 to 1995, SiC-based blue LEDs have been totally replaced by the emergence of much brighter, more efficient direct-bandgap GaN blue LEDs.

SiC has proved to be much more efficient at absorbing short-wavelength light, which has enabled the realization of SiC UV-sensitive photodiodes that serve as excellent flame sensors in turbine-engine combustion monitoring and control (Brown *et al*.

1998). The wide bandgap of 6H-SiC is useful for realizing low photodiode dark currents, as well as sensors that are blind to undesired near-IR wavelengths produced by heat and solar radiation. Commercial SiC-based UV flame sensors, again based on epitaxially grown, dry-etch, mesa-isolated 6H-SiC p–n junction diodes, have successfully reduced harmful pollution emissions from gas-fired ground-based turbines used in electrical power generation systems.

The high-temperature capabilities of SiC allow the production of catalytic metal–SiC and metal–insulator–SiC (MIS) prototype gas sensor structures with great promise for combustion engine emission monitoring applications (Lloyd Spetz *et al*. 1997, Hunter *et al*. 1998). High-temperature operation of these structures, not possible with silicon, enables rapid detection of changes in hydrogen and hydrocarbon content to sensitivities of parts per million in very small sensors that could easily be placed unobtrusively anywhere in an engine. Once they have been more fully developed, these sensors could assist in active combustion control to reduce harmful pollution emissions from automobile and aircraft engines. While generally beyond the scope of this article, SiC is also likely to play a significant role in emerging MEMS applications (Mehregany *et al*. 1998).

5.2 RF Electronics

The main use of SiC RF devices appears to be in high-frequency solid-state high-power amplification at frequencies from around 600 MHz (UHF band) to perhaps around 10 GHz (X band). As discussed by Weitzel and Moore (1998), the high breakdown voltage and high thermal conductivity coupled with high carrier saturation velocity allow SiC RF transistors to handle much higher power densities than their silicon or GaAs RF counterparts, despite the disadvantage of SiC in low-field carrier mobility (Table 1). The higher breakdown field of SiC permits higher drain breakdown voltage, allowing RF operation at higher drain biases, which leads to higher SiC MESFET output power densities. The higher thermal conductivity of SiC is also crucial in minimizing channel self-heating so that phonon scattering does not seriously degrade channel carrier velocity and current. Similar RF output power arguments can be made for SiC-based static induction transistors (SITs). While 4H-SiC MESFETs for high-power RF applications are now commercially available, increasingly beneficial SiC RF transistors should continue to evolve as SiC crystal quality and device processing technology continue to improve.

In addition to high-power RF transistors, SiC mixer diodes show excellent promise for reducing undesired intermodulation interference in RF receivers (Fazi and Neudeck 1998). More than 20 dB dynamic range improvement has been demonstrated using non-optimized SiC Schottky diode mixers. Such dynamic range improvement could prove particularly beneficial to RF systems where numerous receivers and high-power transmitters are closely located, such as on a commercial passenger aircraft or military surface ship.

5.3 High-temperature Devices and ICs

Commercially available silicon-on-insulator circuits can perform complex digital and analog signal-level functions up to 300 °C when high-power output is not required. Thus, aside from ICs where it is advantageous to combine signal-level functions with high-power or unique SiC sensors/MEMS onto a single chip, more expensive SiC circuits solely performing low-power signal-level functions appear largely unjustifiable for low-radiation applications at temperatures below 250–300 °C. In high-power systems, junction self-heating and high electrothermal stress mean silicon devices cannot function above 100–200 °C. Thus, the transition to SiC is necessary at lower temperatures in high-power applications.

Achieving long-term operational reliability is the primary ongoing challenge of realizing 300–600 °C SiC devices and circuits. IC device technologies covered in other articles in this encyclopedia that have been used to successfully implement circuits in silicon and GaAs are to varying degrees candidates for use as a basis for SiC integrated circuits at $T > 300$ °C. High-temperature gate-insulator reliability, discussed in Sect. 4, is needed for the successful realization of MOSFET-based integrated circuits. Gate-to-channel Schottky diode leakage limits the peak operating temperature of SiC MESFET circuits to around 400 °C. Prototype bipolar SiC transistors exhibit poor gains, but improvements in SiC crystal growth and surface passivation could greatly improve SiC BJT gains to make SiC bipolar devices a more viable technology (Wang *et al*. 1996). As discussed previously, a common obstacle to all technologies is reliable long-term operation of contacts, interconnects, passivation, and packaging at $T > 300$ °C. Robust circuit designs that accommodate large changes in device operating parameters with temperature will be necessary for circuits to function successfully over the very wide temperature ranges (as large as 650 °C spread) enabled by SiC. Device behaviors that have traditionally been unimportant to design and simulation of silicon-based device and circuits, such as freezeout of incompletely ionized dopant atoms, must now be included for proper design and simulation of SiC devices and circuits. Because of carrier freezeout effects, it may prove difficult to realize SiC-based ICs operational at temperatures much lower than -55 °C.

Because signal-level circuits are operated at relatively low electric fields well below the electrical failure voltage of most micropipes, micropipes affect signal-

level circuit process yields to a much lesser degree than they affect high-field power device yields. Small-scale prototype logic and analog amplifier SiC-based ICs have been demonstrated using SiC variations of common device topologies (Harris *et al*. 1994, Xie *et al*. 1994, Diogu *et al*. 1996, Brown *et al*. 1997, Ryu *et al*. 1998). These prototypes are not commercially viable, largely owing to their high cost, unproven reliability, and limited temperature range that is mostly covered by silicon-on-insulator circuitry. However, increasingly capable and economical SiC integrated circuits will continue to evolve as SiC crystal growth and device fabrication technology continue to improve. Nonidealities in SiC epilayers, such as variations in epilayer doping and thickness, surface morphological defects, and slow charge trapping/detrapping phenomena causing unwanted device I–V drift, limit the yield, size, and manufacturability of SiC high-temperature ICs (Brown *et al*. 1997).

5.4 *High-power Switching*

While SiC devices offer large potential benefits to high-power systems, solid-state devices in these systems are also the most susceptible to deficiencies in SiC material quality and process variations. This is primarily because these devices operate at high electric fields and high current densities that place the greatest electrical stresses on the semiconductor and surrounding device materials. Prototype SiC devices have demonstrated excellent area-normalized performance often well beyond (more than 10 times) the theoretical power density of silicon power electronics. However, the presence of crystal defects such as micropipes has prevented scale-up of small-area prototypes to large areas that can reliably deliver high total operating currents in large-scale power systems. Since the early 1990s SiC micropipe densities have dropped from hundreds to several tens per square centimeter of wafer area, resulting in corresponding improvements in peak SiC device operating currents from less than 1 A to several tens of amps. However, further defect reductions of at least an additional order of magnitude will be necessary before commercially viable power device yields at these current ratings can be expected.

In addition to micropipes, the density of nonhollow core (elementary) screw dislocation defects in SiC wafers and epilayers has been measured to be of the order of several thousand per square centimeter of wafer area. While these defects are not nearly as detrimental to device performance as micropipes, experiments have shown that they degrade the local material properties such as breakdown field and minority carrier lifetime (Neudeck 2000). While localized breakdown is well known to degrade silicon device reliability in high-power switching applications, the exact impact on SiC high-power switching devices remains to be quantified. The electrical significance of other dislocation defects, if any, also remains to be ascertained.

For SiC power devices to function successfully at high voltages, peripheral breakdown owing to edge-related electric field crowding must be avoided through careful device design and proper choice of insulating/passivating dielectric materials. The peak voltage of most prototype high-voltage SiC devices has been limited by edge-related breakdown (often destructive), especially in SiC devices capable of blocking multiple kilovolts. In addition, most testing of multikilovolt SiC devices has required the device to be immersed in specialized high-dielectric fluids or gas atmospheres to minimize damaging electrical arcing and surface flashover at device peripheries. A variety of edge termination methods, many of which were originally pioneered in silicon high-voltage devices, have been applied to prototype SiC power devices with varying degrees of success. The higher voltages and higher local electric fields of SiC power devices will place larger stresses on packaging and on-wafer insulating materials, so it is unclear whether traditional materials used to insulate/passivate silicon high-voltage devices will prove sufficient for reliable use in SiC high-voltage devices, especially if those devices are to be operated at high temperatures.

The high-power diode rectifier is a critical building block of power conversion circuits. The most important SiC diode rectifier device design tradeoffs roughly parallel well-known silicon rectifier tradeoffs, except for the fact that numbers for current densities, voltages, power densities, and switching speeds are typically much higher in SiC. The high breakdown field of SiC and wide energy bandgap permit operation of SiC metal–semiconductor Schottky diodes at much higher voltages (i.e., kilovolts) and current densities than is practical with silicon-based Schottky diodes. For blocking voltages up to around 3 kV, unipolar SiC Schottky rectifiers appear to offer lower turn-on voltages ($\sim$ 1–2 V vs. $\sim$ 3 V) and faster switching speeds (owing to no appreciable minority carrier injection/charge storage) than SiC p–n junctions (Chow *et al*. 1998). In rectifiers that block over $\sim$ 3 kV, bipolar minority carrier charge injection (i.e., conductivity modulation) should enable SiC p–n diodes to carry higher current densities than unipolar Schottky diodes whose drift regions conduct solely using dopant-atom majority carriers. Hybrid Schottky/p–n rectifier structures first developed in silicon that combine p–n junction reverse blocking with low Schottky forward turn-on should prove extremely useful to realizing application-optimized SiC rectifiers (Dahlquist *et al*. 1998, Held *et al*. 1998). As with silicon bipolar devices, reproducible localized control of minority carrier lifetime will be important in optimizing switching speed vs. ON-state current density performance. SiC minority carrier lifetimes of the order of several microseconds have been measured in high-quality epilayers (Kordina *et al*. 1996), and

lifetime reduction via intentional impurity incorporation and introduction of radiation-induced structural defects appears feasible.

Three terminal power switches that use small drive signals to control large voltages and currents are also critical building blocks of high-power conversion circuits. As summarized by Chow *et al*. (1998), a variety of prototype three-terminal SiC power switches have been demonstrated. For the most part SiC solid-state switches are based on well-known silicon device topologies, like the thyristor, vertical and lateral channel MOSFETs, IGBTs, etc., that try to maximize power density via vertical current flow using the substrate as one of the device terminals. Because these switches all contain high-field junctions responsible for blocking current flow in the off state, their maximum operating currents are primarily restricted by the material quality deficiencies discussed previously.

Silicon power MOSFETs and IGBTs are extremely popular in power circuits largely because their MOS gate drives are well insulated and require little drive signal power, and the devices are ''normally off'' in that there is no current flow when the gate is unbiased at 0 V. However, as discussed previously, the performance and reliability of SiC power device structures with inversion channel MOS field-effect gates (i.e., MOSFETs, IGBTs, etc.) are limited by poor inversion channel mobilities and questionable oxide reliability at high temperatures. Thus, SiC device structures that do not rely on high-quality gate oxides, such as the thyristor, appear favorable for more immediate realization, despite some nontrivial drawbacks in operational circuit design and switching speed.

Some nontraditional power switch topologies have been proposed to somewhat alleviate SiC oxide and material quality deficiencies while maintaining normally off insulated gate operation. Lateral and vertical doped-channel power SiC MOSFETs and JFETs that can be completely depleted by built-in potentials at zero gate bias so that they are ''normally off'' have been demonstrated. With the assistance of lateral surface electric field tailoring techniques, Baliga (1996) has suggested that lateral-conduction SiC power devices could deliver better power densities than traditional vertical SiC power device structures. Baliga also proposed advantageous high-voltage switching by pairing a high-voltage SiC MESFET or JFET with a lower voltage silicon power MOSFET.

6. Further Information

Many of the articles in the Semiconducting Devices section of this encyclopedia contain useful background on a variety of basic semiconductor device structures, the SiC versions of which are described in this article. In addition to the works referred to in this article, the reader should consult the proceedings from the latest International Conference on Silicon Carbide and Related Materials (held in October 1999), which was published as *Materials Science Forum* Volumes 338–42 by Trans Tech Publications (http://www.ttp.ch) in 2000.

See also: Silicon Carbide; Contacts for Compound Semiconductors: Ohmic Type; Contacts for Compound Semiconductors: Schottky Barrier Type; Devices for High-frequency Applications; Junction Field Effect Transistors; Light Emitting Diodes; Metal Oxide–Semiconductor Field Effect Transistors; Point Defects and Impurities in Silicon Carbide and Group III-Nitrides; Bulk Crystals: Vapor Growth; Silicon Carbides, Bulk; Chemical Vapor Epitaxy of Silicon Carbide

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