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Run 2b Silicon Working Group Report: Findings and Recommendations

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Abstract

We present results of studies dedicated to understanding the longevity of the CDF Run 2a silicon detectors and our options for upgrading these detectors to enable continued high luminosity data-taking in Run 2b.

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1 Introduction

In recent years, a series of workshops and studies [1, 2, 3] have shown that the collider experiments at Fermilab have the potential to make major physics discoveries and perform significant measurements in the period prior to the start of high luminosity running at the CERN Large Hadron Collider (LHC)[4]. These may include a discovery of the Higgs boson or SUSY partners, precision studies of the CKM matrix elements, and significant advances in QCD, top, and electroweak physics.

Many of these opportunities can only be realized with a significant increase in integrated luminosity beyond that which was originally planned for Run 2. At present, the Laboratory defines Run 2a as 2.2 fb^{-1} delivered to each of the collider detectors. The additional luminosity required to search for the Higgs in a significant mass range, would be acquired in a Run 2b. The laboratory has issued a memorandum [5] stating a goal of providing a total integrated luminosity of 15 fb^{-1} per experiment by 2007.

In preparation for Run 2, the CDF and D0 collider detectors have undergone significant upgrades to improve their performance and make them compatible with high luminosity running conditions. Both experiments will install extensive silicon tracking systems. These systems were largely designed in the early to middle 1990's to operate with a specified integrated luminosity of 2 fb^{-1}. The sensor and electronic designs made use of the best available radiation resistant technology at that time. Extrapolations to the doses expected in the present Run 2b scenario indicate that the existing systems cannot be guaranteed to survive that run. On the other hand, radiation hardened (rad-hard) sensor and electronic technologies have evolved, and new components conceived and built today could survive well beyond the Run 2b luminosity specification.

It is the purpose of this report to examine the effects of Run 2b conditions on the CDF silicon systems and to explore options for ensuring the performance required to exploit the physics opportunities of the much higher luminosity now expected from the Tevatron Collider. We remind the reader that the characteristics of the CDF Run 2a silicon tracker which are essential to the CDF physics program and which must be preserved in Run 2b are silicon only (standalone) tracking in the pseudorapidity range $1 < |\eta| < 2$, 3D tracking and vertexing, excellent impact parameter resolution, (especially in r-ϕ), and compatibility with a displaced track trigger (SVT). The CDF Run 2a silicon detector is made up of 3 subsystems: Layer 00 (L00), SVXII, and ISL. A transverse view of the system is shown in Figure 1. The basic parameters of the three silicon detectors are included in Table 1. The innermost layers are shown in Figure 2. For more details about the CDF Run 2a silicon tracker, an overview of the system is available on-line at:

http://www-cdf.fnal.gov/upgrades/silicon/cdf_runii_silicon.html

This report is organized as follows. In the remainder of this introductory section we will present the basic issues and summarize the findings and recommendations of the CDF Run 2b Silicon Working Group. The remaining sections revisit each issue in more detail. Section 2 is a discussion of the predicted lifetimes of the various components. Section 3 considers the layout and mechanical design of a possible replacement system. Material impact is discussed in Section 4. The possibility of a partial replacement is explored in Section 5. Component issues, the readout chip, the hybrids, and the port-cards, are discussed in Sections 6-9. A

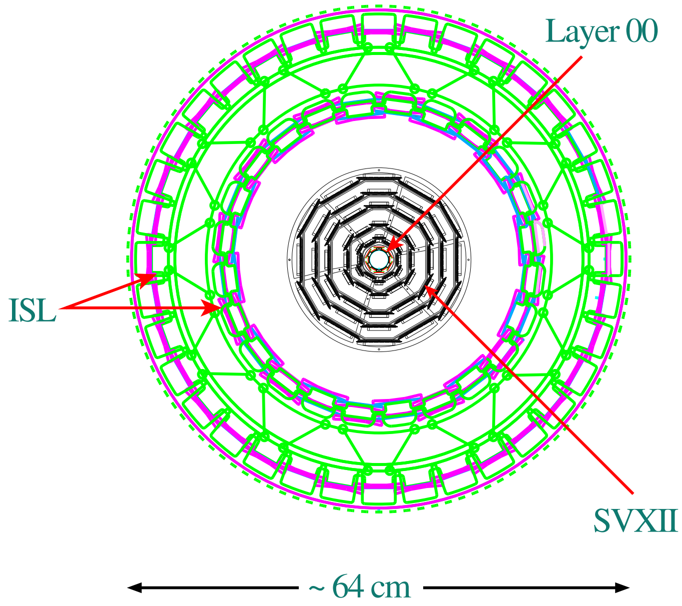

Figure 1: *Schematic transverse cross-sectional view of the Run 2a silicon detector layers.*

CDF Silicon	L00	SVX II	ISL	Overall
No. of Layers	1	5	2	8
Length	0.9 m	0.9 m	1.9 m	1.9 m
Channels	13,824	405,504	303,104	722,432
Modules	48 (SS)	360 (DS)	296 (DS)	704
Readout Length	14.8 cm	14.5 cm	21.5 cm	
Inner/Outer Radii	1.35/1.65 cm	2.5/10.6 cm	20/28 cm	1.35/28 cm

Table 1: Description of the CDF II Silicon tracker. Note that SS (DS) refers to single (double) sided sensors.

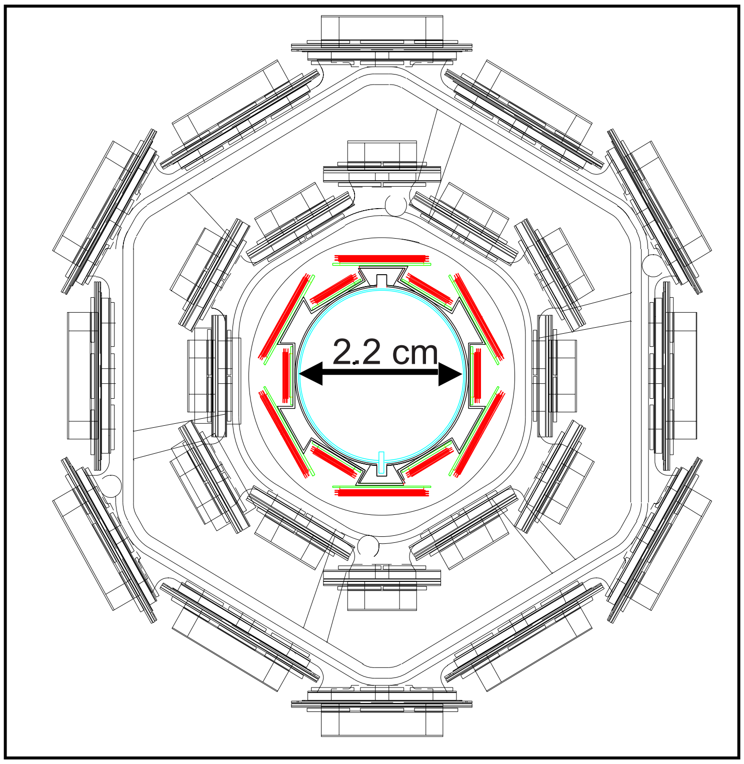

Figure 2: *Transverse cross-sectional view of the innermost two layers of SVXII and L00.*

pixel option for a replacement of L00 has been studied by a subgroup and is described in Section 10. Finally costs, schedules, and conclusions are presented in Sections 11-13.

1.1 Run 2b Silicon Workshops

To explore issues and options for upgrading the Run 2a CDF silicon system for Run 2b, a series of four one-day meetings were held at FNAL between March and August, 2000. The goals of these meetings, which were all of equal priority, are listed below.

- To understand the lifetimes of the silicon detectors and front-end electronics, layer by layer, and to investigate whether other components of the DAQ may be vulnerable to damage or failure for the radiation levels expected during Run 2b.
- To develop the specifications and the basic design of any needed upgrade such that a worst case lifetime would exceed 15 fb^{-1} and would include significant safety factors *whenever this can be achieved without adding substantially to schedule risk or cost.*
- To understand the trade-offs between longevity and physics capabilities of any needed upgrade. To this end we set the Run 2a detector performance as our minimum standard and seek to improve performance *whenever this can be achieved without adding substantially to schedule risk or cost.*
- To identify those components of an upgrade which have long development and production lead times in order to get them started as soon as possible.
- To understand the current state of the art in rad-hard and other relevant technical developments which may be of use to a new system.
- To analyze relevant aspects of the Run 2a design and construction experience, benefit from successes, and develop simple efficient assembly methods to streamline any necessary production.

The lifetimes of each layer of silicon were considered and are discussed in more detail in Section 2. We believe that the criteria for Run 2b could result in the ultimate need to replace L00 and the inner three layers of SVX-II (L0,L1 and L2). The need to replace L2 came as something of a surprise. It is the result of a peculiarity of the operation of Micron double-sided detectors and is discussed in more detail in Section 2. (L4 was also manufactured by Micron and indeed may also die pre-maturely, but this requires further study.) We also concluded that SVX-II L3, probably L4, and all of ISL, should survive to an integrated luminosity of 15 fb^{-1}. The port-cards were also considered, and it appears that some components may see operational problems develop in Run 2b.

The Run 2b Memorandum from the Fermilab Directorate [5] specifies not only the total integrated luminosity of Run 2b, but also the date and duration of the shutdown period for installation of these upgrades. The installation of Run 2b upgrades will take place during a shutdown [6] lasting 6 months starting from some time in late 2003 or early 2004. Our current understanding of the lifetimes of Run 2a components and the schedule guidance we received from the FNAL directorate were the primary constraints in our consideration of possible upgrades for Run 2b.

1.2 Run 2a Lessons

There are a number of aspects of the Run 2a system and experience which provide guidance for any future effort.

- **Front End Readout Chip** The SVX3D chip was the result of a development process which became extended partially due to evolving specifications. The original requirements did not include dead-timeless operations and a major effort was needed to realize this new goal. The particular foundry used, Honeywell, experienced significant delays and yield/reliability problems with their rad-hard process. Extraordinary diagnostic and quality assurance (QA) efforts were required to screen and sort these chips. Significant effort was also spent on rework of hybrids and modules due to latent chip problems. While sufficiently rad-hard for the needs of Run 2a, this chip will not survive Run 2b at small radii and insufficient quantities of are on hand for even a small silicon replacement. *If a new readout chip is required, the specifications need to be close to SVX3D, frozen rapidly, and the chip should not be produced with Honeywell, (see later discussion of 0.25 μm processes now available commercially).*

- **Double-sided sensors:** The choice of double-sided sensors was not expected to be a problem. It turned out that they were more difficult to produce than had been anticipated. Hamamatsu and Micron, who each produced roughly half of the CDF sensors, encountered a number of problems that resulted in significant delays in deliveries. In addition, double-sided silicon is not particularly rad-hard. This is because the high voltages which must be applied to fully deplete them after radiation damage has occurred are difficult to tolerate in a complex double-sided structure and compromise the AC coupling oxide layers. *Double-sided sensors are not a viable option for a new system.*

- **Multiplicity of designs:** There were 5 distinct SVX-II layers plus 2 types of ISL modules and 2 types of L00 modules. This resulted in 13 distinct hybrid types plus cables, and various other items such as gang cards, mezzanine cards, fingers, jumpers, etc. All of this required special fixturing and assembly and test procedures. *We should emphasize the use of standard and/or universal components as much as possible*

- **Hybrids mounted on silicon:** The SVX-II detector has all of the front-end electronics hybrids mounted directly on the silicon. This has the great advantage that one can reduce the gap between barrels to improve acceptance. The drawback is that it makes ladder fabrication much more difficult and it increases somewhat the amount of material in the tracking volume. The ISL detector did not mount the hybrids on the silicon and this led to a much shorter module assembly time, in spite of the fact that double-sided silicon and hybrids were used. New techniques, such as the fine pitch signal cables used for L00, offer the possibility of moving the hybrids away from the silicon while maintaining hermeticity. *If possible we should utilize available methods to keep hybrids out of the tracking volume, particularly at small radii. We should keep module designs as simple as possible.*

- **Optical readout:** The Run 2a detector uses an optical fiber readout from inside the tracking volume via Dense Optical Interface Modules (DOIM's) mounted on the port-cards. The advantage of this scheme is a clean signal and reduced potential for pick-up on other detector components. The drawback is that the DOIM's use a lot of power and are radiation sensitive. In addition, they were difficult to fabricate and may not be available in the future. *A new system must consider wire transmission lines as an alternative to optical methods and understand the possible consequences of Cu on the material budget.*

1.3 Run 2b silicon options

The conceptual design of a silicon detector for Run 2b is driven by physics goals, radiation damage issues, technological constraints, cost, and schedule. In particular, we would like to retain or improve the performance of the detector, increase its radiation hardness, and most importantly, avoid design choices, such as those discussed above, which could lead to difficulties or delays. These considerations suggest a natural subdivision of the silicon into four radially distinct segments.

1. The ISL detector at large radius.
2. An "outer section" of silicon strips immediately inside the ISL in a region where the radiation dose corresponding to an integrated luminosity of $\sim$15 fb^{-1} is not high enough to require sensors which are operated at extremely high bias voltages and which may require direct cooling.
3. An "inner section" of silicon strips, where the radiation dose will be sufficiently high that only single-sided, high voltage, directly cooled sensors would last for the entire Run 2b.
4. A beam-pipe layer.

The following are what we have found to be the most attractive possibilities for these 4 segments:

1. Keep the ISL detector exactly as it is. The radiation dose rates at the radii of the ISL layers are low enough that we believe the ISL silicon and front-end electronics will last well beyond an integrated luminosity of $\sim$15 fb^{-1}.
2. The outer section should be mechanically separated from the inner section since the latter must be very different from the Run 2a SVX-II in order to survive Run 2b radiation. For the outer section we then have two clear options. We can either design and build something completely new or we can recycle the ladders from the outer two layers of SVX-II.
3. The inner section will be a new system. We will use single-sided micro-strips. To obtain stereo views we would mount two single-sided ladders back-to-back. The ladders would include direct cooling of the silicon
4. For the beam-pipe layer, we can either build a replica of the present L00 with components that are more rad-hard, or design and build a pixel layer.

In summary, we see two possible ways to deal with radiation damage to SVX-II and two ways that we can replace L00. There was a strong consensus in the working group for the separation of the SVX-II replacement into two mechanically distinct radial sections. The option in which we would build a completely new outer section is referred to as the "full replacement scenario" since it implies that all of SVX-II would be replaced. The option in which we make new mechanical supports and re-use ladders from the outer layers of SVX-II is called the "partial replacement scenario".

Replacing L00 is not a major issue since it is a small system and assembly was rapid. A similar or identical micro-strip replacement could be built at low cost and in a very short time. We recommend that this be done as a fallback even if it is decided to pursue pixels. With regard to the latter, it is important to understand the potential benefits and costs, and the likelihood of success on the required time-scale of such a project. If it can be demonstrated that pixels will significantly improve CDF tracking, have a good chance of being ready on time, and CDF can afford them, then they should be pursued. In this note we present a preliminary discussion of pixels. More detail will be required to make a decision. An R&D program in FY01, as described in section 12, would provide the information that we need.

1.4 SVX-II replacement scenarios: The issues.

Regarding the two options available for replacing SVX-II, there are a number of important issues that have to be addressed. We summarize these issues here, and delve more deeply into them in the remainder of this note.

1. **Partial replacement scenario.**

   In this scenario we retain as much of the Run 2a detector as possible. The Run 2b Working Group agreed to the following points:

   - Our best estimates of detector lifetimes now indicate that SVX-II layers L0, L1, and L2 cannot be guaranteed to last for 15 fb^{-1}. We must therefore assume that they will need to be replaced.
   - The very short shutdown period of 6 months that the laboratory envisions requires as much pre-construction as possible. We therefore need to prepare a new ladder support structure that would have the new inner layers installed prior to extracting the Run 2a silicon. The two layers which are retained from SVX-II would be transferred to new bulkheads containing support ledges and cooling for only these two layers.
   - In order to have greater longevity, the replacement layers would need to use single-sided silicon, which could be placed back-to-back for stereo views. However, the full radiation hardness of these detectors is only possible if the silicon is directly cooled and can be biased to high voltages. As a result, direct cooling of the sensors needs to be integrated into the mechanical supports *a la* LHC tracking systems. This point, in fact, drives the likely need for a new mechanical support concept to replace the SVX-II bulkheads.

- We need to understand in as much detail as possible how many L3 and L4 ladders may be damaged or otherwise need replacement when we transfer ladders from SVX-II to the new system. These new ladders would require that new orders be placed for double-sided silicon and new pairs of SVX-II hybrids. These should be ordered and built soon, while parts remain available and while experienced technicians are still in place.
- We must prepare a detailed estimate of the time, resources, and risks involved in this scenario based upon a list of all of the tasks involved, starting from extraction of the Run 2a detector at B0, through the installation of the Run 2b detector. The schedule, cost, and associated risks are discussed in more detail in later sections of this note.

2. **Full replacement scenario.**

   In this scenario we would build a replacement system for all of SVX-II. The Run 2b Working Group agreed to the following points:

   - The innermost region of the system, out to $\sim$ 6 cm, could be identical to that planned for the partial replacement scenario.
   - The detector should be fully assembled and ready for installation inside the ISL by the time of the Run 2b shutdown.
   - To allow for rapid construction and a minimum of development time, only a few universal ladder types should be used. A single ladder type could then be used on different layers while maintaining the 60 degree symmetry required for the SVT.
   - For this option, we would explore simple new mechanical support schemes with integrated cooling such as the CMS rod or shell concepts. These schemes would greatly simplify the final installation and alignment processes
   - We must also prepare a detailed estimate of the time, resources, and risks involved in this scenario. We believe that this option would minimize the shutdown by virtue of the fact that a full replacement could be installed in the ISL immediately after removal of SVX-II.

For both scenarios there exist a number of components in common. These are listed here, and discussed in greater detail later in this note.

- Front-end chips:
  - We have estimates for purchasing more Honeywell SVX3D chips [7]. The cost of 28k$ - 32.5K$ per wafer is extremely high, and we remain concerned about reliability, yield, and the schedule risks involved in this option. Furthermore, the Honeywell process is not sufficiently rad-hard for use at very small radii.
  - In the time since the Run 2a system was designed, new 0.25 μm ("deep sub-micron") processes have become available commercially. While not sold as rad-hard, they have in fact been shown to be extremely radiation resistant and are in use currently for a number of HEP projects (FNAL FPIX, CMS APV25 etc).

A new deep sub-micron chip could be developed to replace the SVX3D. This would require a fair amount of translation and development work. The cost of development and production of these chips is however much lower than for the original SVX3D chip. In addition, many groups have found development in this technology to be more rapid than with other processes. Preliminary simulations carried out within the Working Group indicate that this chip would have significantly lower noise than the present SVX3D. LBNL has begun some translation and prototyping work which is discussed in this note along with a more detailed discussion of the chip issue in general.

- Hybrids: For either scenario we will need many new hybrids. Those for the outer layers in a full replacement could be ceramic, double-sided hybrids similar to those used in the ISL. For the inner layers, which are common to both scenarios, the hybrids would need to be single-sided and could be similar to the existing L00 hybrids. In both regions we could also benefit from new high density processes to reduce material and perhaps cost.
- Port-card components: DOIM based port-cards will need to be replaced in either scenario and may be hard to produce in the future. We therefore consider an alternate scheme for this component of the readout system.

1.5 Conclusions and a proposed course of action.

The innermost layers of the Run 2a silicon tracker will almost certainly not survive to 15 fb^{-1}. It is less clear exactly how long they will survive, or in exactly what order they will fail. It will be important to integrate at least 0.5 fb^{-1} (and preferably 1 - 2 fb^{-1}) of luminosity in order to refine the expected lifetimes. In the meantime it is extremely important that development work begins as soon as possible.

The Run 2b Working Group recommends the development of a deep sub-micron replacement for the SVX3D chip for the following reasons. Firstly, all of the likely replacement scenarios we now foresee will require substantially more chips than we have in hand. Secondly, the vendor for our chips in Run 2a has indicated that they cannot guarantee any reasonable yield, price, or schedule for additional chips. Thirdly, a new chip could be developed in sub-micron technology that would be less risky, more rad-hard, and lower noise. These benefits would provide flexibility and contingency to any new detector project, thereby enhancing the probability of completing a replacement detector on schedule. *We therefore need the FNAL PAC and the Laboratory to take decisive and immediate steps to support our present efforts to develop a new chip. We cannot otherwise ensure that CDF will be prepared for data-taking in Run 2b.*

The next most important issues are the development of the mechanical support structures with integrated cooling, and the prototyping of hybrids, universal ladder types, and port-cards. The ideas we present in this note for simple hybrids, ladders and port-cards should be prototyped beginning in FY01 to assure that the final designs are simple, robust, and easy to manufacture and use.

It is essential to the success of this endeavor to have working hybrids in quantity by early 2003 if we are to install a new system in 2004. This means we need all production chips by this time. Simple single-sided ladders would be used and these can be built rapidly. Robotic ladder assembly systems developed for CMS will already be in operation at the FNAL silicon detector center (SiDet) for the US CMS silicon tracker project. Such a system could be adapted for use in CDF. Even without such a system we estimate that of order 1000 single-sided modules could be built and wire-bonded by a team of 6 technicians in 26 weeks.[17] If we develop and prepare all mechanical supports while we are developing the chips and preparing to start module assembly, we will have roughly one year for production of modules and the final assembly of the system. Note that the assembly of the Run 2a CDF silicon detectors took roughly one year from the time that production electronics and silicon components began to arrive at FNAL in quantity. The goal of our development effort would be to ensure that all of the key quantities required for a silicon replacement would be available a year before the targeted shutdown in 2004.

In summary, based upon currently available information, the Working Group has concluded that there is insufficient margin to guarantee that the innermost 4 layers of the present system will survive Run 2b. For reasons which are discussed in more detail in the remainder of this document, the Working Group concludes that the best scenario for recovery from the loss of these layers would be to replace L00 and all of SVX-II. This conclusion is motivated by the significant complications associated with trying to reconcile the Run 2a geometry with the requirements of operating single sided rad-hard micro-strips, and the extremely long and risky shutdown that would be required if we were to reuse any portion of the SVX-II detector. A considerable amount has been learned from the Run 2a experience that we intend to profitably apply to a simplified system design and streamlined construction process. We firmly believe that this can make a full replacement feasible on the necessary time-scale provided that critical R&D begins in FY01.

While there will be time to revise this conclusion as new information is obtained, it is imperative to begin immediately certain developments (chips and mechanics) for this full replacement to be possible. Present knowledge indicates that failure to make such an investment in FY01 will leave CDF without critical physics capabilities in Run 2b.

[17] We have worked with FNAL management to understand the implications that Run 2b CDF and D0 silicon projects would have for laboratory resources. It was concluded that SiDet has adequate capacity to accommodate these projects together with those already scheduled for the period up to 2004.

2 Run 2 Silicon Detector Lifetimes

The silicon systems for CDF II were designed to record 2 fb^{-1} of data on tape at $\sqrt{s} = 2.0$ TeV. We take this to correspond to 2.2 fb^{-1} of delivered luminosity.[18] Conservative lifetime estimates were made during the SVX-II design in order to be certain that the device would not fail at 2.2 fb^{-1}. It is clear that if SVX-II is guaranteed to last 2.2 fb^{-1} it will be operable beyond that point. The question that we now ask is exactly how long can we be confident it will survive. To answer this, we must look at all elements of the silicon system and estimate useful lifetimes based on known, as-built operational characteristics together with available data on radiation damage. It is critical to explore the expected lifetime range allowed by uncertainties in the available information. We revisit several results from previous studies of SVX-II radiation damage [9, 10, 11] in the context of investigating the allowed range for lifetime predictions.

There are factors which influence the lifetimes of CDF silicon that can be understood and predicted quantitatively, while others are more intangible and lead to more qualitative predictions. We have adopted the following prescription for our calculations. We carry out an analysis of detector lifetimes at each radial layer of our system using all of the most relevant data and theoretical models currently available to us. This is essentially the best that we can do in a systematic way. However, in spite of the quantitative appearance of these calculations, we are not terribly confident that the results are meaningful. In particular, there are many unknowns related to the Tevatron/CDF environment and the extended running period associated with Run 2. To account for such things in a quantitative manner is essentially impossible. Instead we adopt a convention, now used by other HEP experiments, and introduce an engineering safety factor. The safety factor is used to inflate the quantitative uncertainties.

The basic "observables" that we use to calculate lifetimes are leakage current and particle fluence. The expectations for these quantities for Run 2 are based on Run 1 data plus published results on silicon radiation damage. There are several systematic uncertainties associated with these predictions which we characterize with $\pm error$ figures in the tables to follow. These $errors$ reflect the allowed range of the predictions and are not standard deviations.[19] Based on these quantities we then predict useful lifetimes. However, lifetimes are in general not linear functions of the "observable" quantities and it can be misleading to try to convert the quoted uncertainties into lifetime errors. Instead, we give "central value lifetimes", which are calculated using the central values of the relevant observables, as well as "safe lifetimes", which are calculated by adjusting the central value by an amount resulting from 1.5× uncertainty for each relevant observable. The factor of 1.5 is the engineering safety factor discussed above. The idea is that components should survive up to the safe lifetime with good probability. Note that often the central value lifetime is not very well constrained by available predictions, and so the safe lifetime can be significantly different.

We evaluate the lifetime of each silicon layer by looking separately at thermal runaway due to leakage current, signal to noise performance, and required operating voltage. Each

[18] For the rest of this section, luminosity always refers to delivered luminosity, which is the relevant quantity for radiation damage.

[19] Interpreted statistically they should be viewed as between 2σ and 3σ, in the sense that they should contain the true value with high probability.

is capable of rendering a layer useless by a different mechanism, and it is not a priori clear which mechanism is the "killer". Finally, the lifetime of the port-cards is estimated.

2.1 Leakage Current and Neutron-Equivalent Fluence

Silicon sensors are damaged by radiation primarily through nuclear reactions in the bulk. The damage leads to both an increase in leakage current and a change in dopant concentration, which in turn changes the depletion voltage. Both leakage current and depletion voltage change linearly with radiation dose. However, leakage currents can be monitored and the rate of change can be easily determined after a small dose, whereas depletion voltage is more difficult to measure and larger doses are typically required for good understanding of the voltage shift with integrated luminosity.

Data from Run 1 provide a direct normalization of leakage current vs. integrated luminosity for CDF at the Tevatron [13]. The observed leakage currents in the 4 layers of SVX and SVX' are well fit by the empirical formula

$$I_L = I_0 \times V_s \times r^{-1.7} \times \mathcal{L} \tag{1}$$

where I_L is the leakage current for one strip, V_s is the strip volume in cm^3, r is the radial location of the silicon in cm, and $\mathcal{L}$ is the integrated luminosity in fb^{-1}. The normalization constant I_0, however, is not unambiguously determined from the data. While the statistical uncertainty of the measurements is negligible, Run 1a and Run 1b data disagree at the 25% level for the same operating temperature. In addition, tor the latter part of Run 1b the silicon temperature was reduced from 24^{o}C to 21^{o}C, which should have reduced the rate of increase of leakage currents by a factor of 1.39 [12]. No such change in the rate of increase of L0 leakage current was observed although the instantaneous leakage current did drop by 20% following the temperature change. Finally, available Run 1 leakage current measurements come from wedges at the top and bottom (in ϕ) of the SVX' and SVX, respectively. Radiation monitoring devices, (such as PIN diodes), used in those runs indicated that there existed an azimuthal dependence of the dose such that the radiation in the horizontal plane was approximately 10% higher than in the vertical plane. Such a dependence is reasonably expected because the colliding beams are bent in the horizontal plane. Taking all these effects into account we assign $I_0 = (1.19 \pm 0.46)$ mA at 24^{o}C and averaged over ϕ. Modulo the small ϕ correction, this range of values properly reflects the uncertainties associated with our Run 1 measurements.

Returning to Eq. (1), note that naively one would expect radiation dose and therefore damage to fall as r^{-2}. The decrease is slower because of particles generated by secondary interactions in the detector material. The radial dependence for Run 2 could be different because there is more material in the Run 2 silicon system than there was in Run 1. However, without a detailed simulation of the generation of secondary particles in the inner detector material, it is difficult to make a comparison between Run 1 and Run 2. We assume that the radial dependence seen in Run 1 applies to Run 2 at the radius of L0, as the material inside of L0 is both small and comparable between the two runs. Outside of L0 we increasingly inflate the I_0 uncertainty with radius (10% per cm outside L0), due to the different Run 1 and Run 2 material distributions

Run 2 Layer	Radius (cm)	Run 2 I_L ($\mu A/\text{fb}^{-1}$)
L00	1.35	0.32 ± 0.17
L0	2.54	0.35 ± 0.14
L1	4.12	0.16 ± 0.07
L2	6.52	0.072 ± 0.040
L3 ϕ	8.22	0.048 ± 0.030
L3 Z	8.22	0.072 ± 0.045
L4	10.10	0.038 ± 0.027

Table 2: Expected leakage current increase in Run 2 silicon layers extrapolated from Run 1 data.

Using equation (1) one can obtain a prediction for the leakage currents in Run 2 *at the same silicon temperature.* At the temperatures in question leakage current in silicon approximately doubles every 8^{o}C. In addition, rising temperatures increase the annealing rate, which acts to decrease leakage current over time in the early stages of radiation exposure. We ignore this effect, which should be small for the temperatures in question. Using a Run 1 silicon temperature of 24^{o}C and Run 2 temperatures of 16^{o}C and 5^{o}C for SVX-II and L00 respectively, we predict the strip leakage current increases given in Table 2. For all but L00 the uncertainties given are the uncertainty in I_0 inflated at large radii as stated above. For L00 there is a significant uncertainty from the $r^{-1.7}$ extrapolation. By fitting the Run 1 data points with different functional forms we find that the fit extrapolation at the L00 radius can vary by 30%. We therefore scale the L00 I_0 uncertainty by a factor of 1.3.

The observed leakage currents in Run 1 have also been used to obtain a normalization of neutron-equivalent fluence vs. integrated luminosity. The neutron-equivalent fluence Φ_n, will be needed later in order to calculate the changes in depletion voltage (V$_{dep}$) expected for Run 2. The leakage current increase at 20^{o}C (I_L^{20}) in a silicon diode of volume V_s is given by,

$$I_L^{20} = \alpha \Phi_n V_s \tag{2}$$

where α is the damage constant. A range of values for α can be found in the literature. We use $(3 \pm 1) \times 10^{-17} A/cm$ [9, 13, 14] to cover the range of commonly used values. The predicted fluences for Run 2 are given in Table 3. These values were obtained by scaling the Table 2 values to 20^{o}C (from 16^{o}C to 20^{o}C currents scale by 1.4), dividing by the damage constant and the strip volume, and multiplying the uncertainties by 1.3 to include the damage constant uncertainty. Note that the bulk radiation damage at the Tevatron is primarily due to pions and protons, but we express the fluence in terms of an equivalent number of 1 MeV neutrons because this is the convention for radiation damage studies. The choice of this convention does not affect our predictions. Note also that we show uncertainties as symmetric, whereas in reality some of the effects considered can only act to increase dose (for example the increased material in Run 2 can only give rise to more secondary particles). Thus, for example, the L4 entry in Table 3 may be more complete as $0.66^{+0.60}_{-0.40}$, but since the lower uncertainty is never used we keep symmetric notation for simplicity.

Run 2 Layer	Radius (cm)	Run 2 Φ_n ($\times 10^{12} cm^{-2}$/fb^{-1})
L00	1.35	18 ± 12
L0	2.54	6.0 ± 3.1
L1	4.12	2.8 ± 1.7
L2	6.52	1.2 ± 0.9
L3	8.22	0.83 ± 0.68
L4	10.10	0.66 ± 0.60
L6	20.0	0.18 ± 0.18
L7	22.0	0.15 ± 0.15
L8	28.0	0.10 ± 0.10

Table 3: Expected 1 MeV neutron-equivalent fluence in Run 2 silicon layers. Layers 6 and 8 are the forward/backward ISL layers and L7 is the central ISL.

2.2 Lifetime Due To Thermal Runaway

Thermal runaway is a potential issue only for SVX-II, for which the sensors are not directly cooled.[20] As indicated in the previous section, leakage current in silicon is strongly dependent on the operating temperature. Therefore, if the heat generated by the leakage current is sufficient to raise the silicon temperature, the temperature rise will in turn increase the current, triggering a positive feedback state known as thermal runaway. Thermal runaway would never lead to thermal breakdown or pose a safety hazard, because the bias voltage supplies cannot deliver much power and the voltage is supplied though a series resistor of order 10 KΩ, which further limits power delivery. However, thermal runaway would render a ladder inoperable.

Detailed simulations to predict the onset of thermal runaway were carried out during the SVX-II design [15, 16]. For our purposes we summarize the results of these simulations with one number,

$$I_{\text{runaway}} = 3.4\mu A/\text{strip} \tag{3}$$

which is the leakage current necessary to trigger thermal runaway, starting from a silicon operating temperature of 15^{o}C. The onset of thermal runaway is rather sudden, such that as the leakage current increases the silicon temperature does not rise appreciably, until near the runaway current. This sudden onset is what allows us to characterize the runaway current by a critical current (while once runaway is reached the leakage current is not well defined). It also allows us to ignore internal heating of the silicon when considering shot noise due to leakage current in the next section.

Using the above value of I_{runaway} Table 2 can be used to obtain the thermal runaway lifetime for each layer, given in Table 4.

[20] L00 sensors are directly cooled while ISL sensors are not. The leakage currents at ISL radii are too small for cooling to be required.

Layer	Thermal Runaway Central Value Lifetime (fb^{-1})	Thermal Runaway Safe Lifetime (fb^{-1})
L0	9.7	6.1
L1	21	13
L2	47	26
L3	71	36
L4	89	44

Table 4: Integrated luminosity values at which each layer is expected to reach thermal runaway. Column 2 uses central values pf leakage current given in Table 2. The safe lifetimes are based upon estimates of the currents obtained from the central values by adding uncertainties after inflating them by the safety factor.

2.3 Lifetime Due To Noise

From a performance standpoint, the main effect of leakage current is to add noise. Before irradiation, the sensor leakage current is very small and the dominant noise contribution is from the capacitive load on the amplifier. After irradiation a shot noise contribution, which scales as square root of the leakage current, can become significant. Additionally, the capacitive noise also increases because the SVX3D chip noise performance degrades with ionizing radiation dose (see section 6).

The ionizing radiation dose for the electronics does not scale radially exactly like the neutron-equivalent fluence because low energy secondary photons can have a very large effect on ionizing radiation dose, while they do not cause bulk damage. The degradation of the SVX readout chip seen in Run 1 has been used to obtain a normalization for ionizing dose vs. luminosity [19],

$$D = 2.8r^{-1.5} \tag{4}$$

where D is the dose rate in MRad/fb^{-1} and r is the chip radial location in cm. Different methods of calculating ionizing dose give different values. The Run 1a and Run 1b values do not agree very well. We therefore assign a 30% uncertainty to this estimate at r= 3cm to cover the spread, and again we increase the uncertainty with radius. For the Run 2 SVX3D chip noise increase we use 7%/MRad (Figure 16).

Table 5 gives a summary of the un-irradiated noise level of different SVX-II layers, together with the integrated luminosity values at which the signal to noise (S/N) would decrease to 8/1 for $r-\phi$ layers used in the SVT trigger and 6/1 for L00 and stereo layers. These S/N cut-offs are motivated by the requirements of standalone silicon tracking and Run 1 studies showing the effect of S/N degradation on b-tagging efficiency.

In our studies of Run 1a SVX performance [20] we found that the S/N ratio at the end of Run 1a on the innermost layer of the detector was effectively 2.7/1 when all operational effects were taken into account. At this low value the b tagging efficiency dropped to 70% of what it had been at the start of the run. Remarkably, b tag efficiency did not degrade at all until the S/N ratio on the innermost layer dropped below 4/1. We note however that the innermost tracking layer was not required for the formation of tracks. The central tracking chamber (CTC) was used for our tracking pattern recognition in Run 1 and the silicon was predominantly used to improve track parameters. We can expect similar results for Run 2 in the central region where the COT is located. However, the use of the silicon as a standalone tracking device in the region $1 < |\eta| < 2$ means that poor hit efficiency on even a few layers will seriously hurt tracking efficiency. We know from early design studies [21] that the SVX-II and ISL together provide enough information to form tracks with good efficiency and purity. L00 was added to improve track parameters and was not seen to be an essential tool in the tracking pattern recognition itself. It is for this reason that we are willing to accept a lower S/N ratio on L00.[21] Online sparsification thresholds and secondary vertex triggering further complicate matters. The SVT requirement of 4 out of 5 SVX-II layers also makes the single layer hit efficiency critically important. To determine the lowest S/N level we could comfortably tolerate in SVX-II and ISL layers we studied the degradation in hit efficiency due to radiation damage by adding real clusters, measured with a β source, to data taken from an SVX-II wedge. We find that the single hit efficiency remains stable at about 97% for signal to noise ratios down to about 8/1 but falls to 94% at 6/1 and 87% at 4/1. These calculations indicate that we can expect reasonably good tracking efficiency even a bit below 8/1. However, they do not take into account the possibility of additional, unexpected noise sources that could appear during data-taking with the full system. It is our conclusion that an S/N ratio of 8/1 for the SVX and ISL layers is the lowest value that we can safely assume will yield acceptable tracking performance.

The noise evolution was calculated according to reference [22] (which takes into account correlated sampling) assuming a constant 0-90% amplifier rise-time of 70 ns and an integration time (sampling time) of 108 ns. With these parameters a simplified shot noise expression is

$$ENC_{shot} = 900e^{-} \times \sqrt{I_L(\mu A)} \tag{5}$$

For the signal we use 20,000 electrons regardless of radiation dose. Note that in all cases the SVX3D chip noise dominates the lifetime. For L00 the SVX3D chips have been loaded on hybrids with a high pre-amp current configuration, which is expected to lead to reduced noise at the expense of extra power dissipation. Studies done for L00 [23] suggest that after irradiation the higher pre-amp current could result in signal to noise improvements of order 25%. However, the SVX3D performance in this configuration has not been extensively studied, and we therefore use as the L00 chip noise 90% of the standard configuration chip noise for the L00 capacitive loads. These loads are taken to be 30pF, 35pF, and 32pF for the hybrids placed at 3cm, 5cm, and 7cm radius, respectively. The fraction of L00 channels with hybrids at these radii are 10%, 10%, and 80%, respectively.

2.4 Lifetime Due To Depletion Voltage

Independent of leakage currents, radiation damage changes the dopant concentration of the silicon, which in turn changes the depletion voltage. Because the SVX-II sensors are double-sided, they must be fully depleted in order to be operated at all. If they are not fully depleted

[21] One can argue that the same may be true for L0 of SVX-II in which case we could assume a lower S/N cut-off here as well. Our estimated lifetime of L0 would then extend a bit further, up to the point at which it can no longer be depleted. It will be seen that this represents a fairly small lifetime gain.

Layer	Un-irradiated Noise (e^-)	S/N Limit Central Value Lifetime (fb^{-1})	S/N Limit Safe Lifetime (fb^{-1})	Shot Noise (e^-) (central)	Chip Noise (e^-) (central)
L00-3cm	2,200	9.0	6.0	1,527	2,947
L00-5cm	2,100	15	9.0	1,972	2,652
L00-7cm	2,400	13	8.0	1,836	2,730
L0 ϕ	1,600	6.5	4.3	1,354	2,115
L0 Z	2,000	9.0	6.0	1,597	2,872
L1 ϕ	1,600	14	8.5	1,347	2,125
L1 Z	2,000	20	12.5	1,610	2,937
L2 ϕ	1,700	25	14.5	1,207	2,200
L2 Z	1,700	> 40	33	1,527	2,501
L3 ϕ	1,600	> 40	23	1,247	2,132
L3 Z	2,000	> 40	31	1,527	2,532
L4 ϕ	1,700	> 40	27	1,110	2,115
L4 Z	1,700	> 40	> 40	1,110	2,115

Table 5: Signal to noise estimates based on contributions from leakage (shot) and SVX3D (capacitive) noise. The right two columns give the individual shot noise and chip noise contributions at the luminosity of column 3 for central value damage estimates.

the strips on the ohmic side remain effectively shorted together (note that after type inversion the ohmic side will be the ϕ side). Furthermore, because the electronics on both sides of the sensor are referenced to a common ground, the applied bias voltage must be "held off" by the coupling capacitors. The coupling capacitors are rated to withstand 100V, but due to micro-discharge they are limited to 85V in Hamamatsu sensors (Layers 0, 1 and 3). This means that Hamamatsu sensors cannot be operated if their depletion voltage exceeds 160V (10V over depletion is needed for operation [24], for a total of 170V bias: +85V on one side and -85V on the other). For Micron sensors (Layers 2 and 4), due to processing problems at the junction side, voltage can be applied only from the ohmic side. Since they have a lower depletion voltage than the Hamamatsu sensors (between 20 and 40V) systematic tests have been carried out on all Micron sensors at 60V (on the ohmic side). This should be considered the maximum safe voltage at which to operate them. Figure 3 shows how noisy strips develop in a Micron sensor as bias voltage is applied to the junction side.

Unfortunately we do not have a direct depletion voltage vs. luminosity calibration from Run 1. We are therefore required to first estimate the neutron-equivalent particle fluence expected per fb^{-1}, and then calculate the resulting depletion voltages with a model. This introduces significant uncertainties. Unlike for the leakage current, the time and temperature details during and after irradiation affect depletion voltages significantly.

Depletion voltages are modeled using the full parameterization of beneficial and reverse annealing [25, 11]. For a planar diode, the depletion voltage is given by

$$V_{planar} \propto d^2 \cdot |N_{eff}| \tag{6}$$

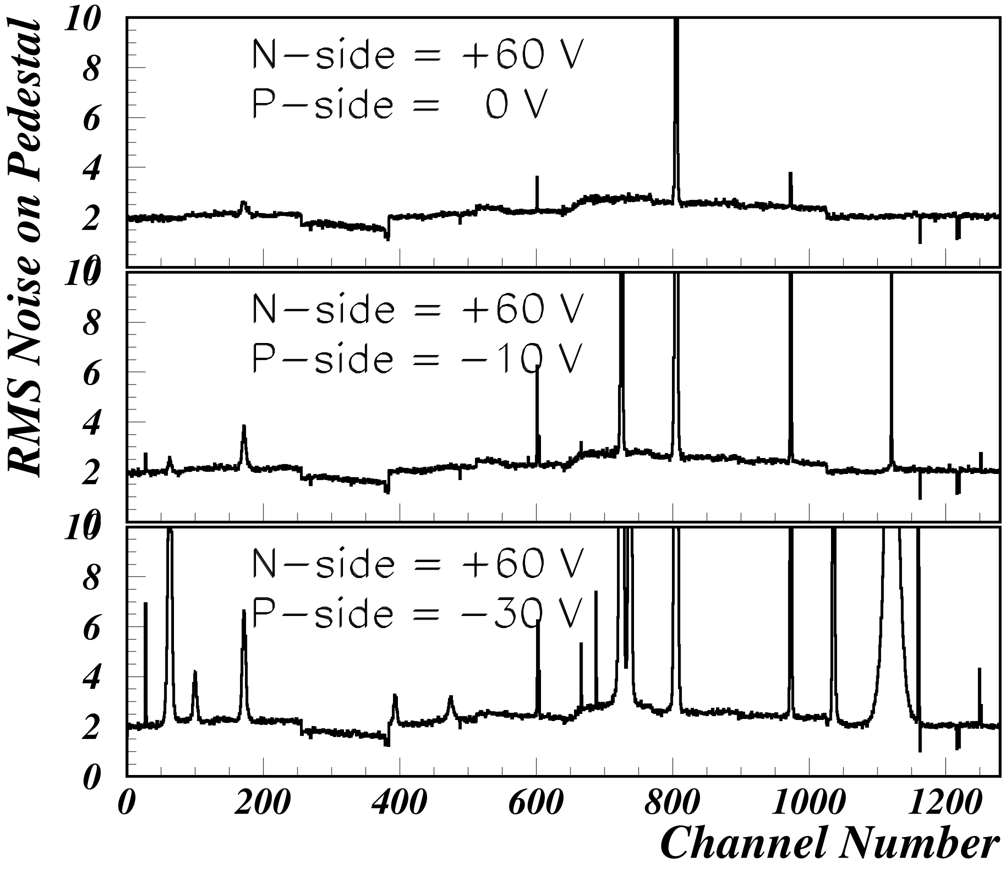

Figure 3: RMS noise on pedestal for an SVX-II ladder with Micron sensors (Layer 2). The top plot shows a properly functioning ladder, with the p-side at ground. The noise is approximately 2 ADC counts, as expected from the capacitive load on the amplifier. There are a few known bad channels. The middle and bottom plots show the development of noisy channels due to micro-discharge as the p-side bias is increased to -10V and -30V, respectively. A typical signal will be approximately 30 ADC counts.

Parameter	Unit	value
g_Y	(10^{-2}cm^{-1})	4.6 $\pm$0.3
g_C	(10^{-2}cm^{-1})	1.77$\pm$0.07
N_{C0}	(10^{11}cm^{-3})	5.0 $\pm$0.2
c	(10^{-13}cm^{2})	2.0
E_a	(eV)	1.31$\pm$0.04

Table 6: Measured values for the relevant bulk radiation damage constants [25, 11]. These constants are used to model depletion voltage versus fluence.

where N_{eff} is the effective doping concentration and d is the diode thickness, and

$$\Delta N_{eff}(\Phi, t, T) \approx N_C(\Phi) + N_y(\Phi, t, T). \tag{7}$$

where t is time, T is temperature, N_C is a stable defect term, and N_y is a reverse annealing term. These two terms are parameterized as follows:

$$N_C(\Phi) = N_{C0}(1 - e^{-c\Phi}) + g_C \tag{8}$$

$$N_Y(\Phi, t, T) = N_{X0}(\Phi)\left(1 - \frac{1}{1 + N_{X0}(\Phi)k_0 e^{-E_a/k_B T}t}\right). \tag{9}$$

where N_{X0} is the initial concentration of defects that leads to the formation of second-order defects (denoted by N_Y), k_0 is the generalized frequency factor, k_B is the Boltzmann constant, and the remaining parameters are given in Table 6.

The equations above and the constants in Table 6 are combined with a model for the fluence and for exposure times and temperatures to estimate a voltage. The nominal operating conditions assumed are, for SVX-II: 15°C operation and one week per year at 20°C, and for L00: 5°C operation and one week per year at 20°C. The results are summarized in Table 7. Figure 4 shows the output of the model for nominal conditions for SVX-II L1. After inversion one can easily distinguish in the figure the steps in depletion voltage corresponding to the warm (20°C) periods. Because of the importance of time and temperature, a model of integrated luminosity vs. time is necessary to make predictions. The model used here is given in Table 8. We do not explicitly include an uncertainty in the operating temperature. Instead, Table 7 includes a column showing the effect on lifetimes of a 2^o higher operating temperature. The effect is small and operating temperature variation is therefore reasonably covered by our engineering safety factor.

2.5 Port-card Lifetime

The port-card components that we expect to cause the first serious operational problems as a result of radiation damage are the DOIMs. A small sample of DOIMs were irradiated with 63 MeV protons up to total doses ranging from 200 krad to 1 Mrad. The performance of the DOIMs after various irradiation doses is seen in Figure 5. Radiation hardness behavior varied from DOIM to DOIM by as much as 20%. At high enough doses, the DOIMs appear to

Layer	Initial V_{dep} (V)	Inversion Point Central (fb^{-1})	Safe (fb^{-1})	Lifetime Central (fb^{-1})	Safe (fb^{-1})	Safe, Warm (fb^{-1})
L00	-55	1.6	0.8	12.2	7.4	6.6
L0	-60	2.9	1.6	10.0	5.6	5.3
L1	-60	5.9	3.1	20.9	10.9	10.3
L2	-30	7.5	3.5	22.7	10.7	10.0
L3	-60	20.0	8.9	> 50.0	30.0	27.7
L4	-30	10.3	4.3	33.0	14.0	13.2
L6	-80	> 50	25.5	> 100	> 50	> 50
L7	-80	> 50	30.7	> 100	> 50	> 50
L8	-30	> 50	22.5	> 100	> 50	> 50

Table 7: Expected depletion voltage evolution per layer. The lifetime is the point at which the depletion voltage plus 10V overvoltage equals the maximum bias that can be applied. For L00 a maximum of 600V is assumed. (In reality most of the L00 sensors can sustain up to 700V bias but low profile bypass capacitors rated to 630V were used in the L00 hybrids which explains the limit of 600V in our lifetime calculations. Another comment to be made about L00 is that the power supplies do not currently go beyond 500V. If it became desirable to operate L00 for the longest possible time, the small number of existing L00 power supplies would need to have a new daughter board installed.) The initial depletion voltages are negative to indicate before type inversion. The last column calculates the safe lifetime in the usual way but assumes an operating temperature 2^{o}C higher than nominal.

Date	Time in Stores (hr)	Initial Luminosity ($cm^{-2}sec^{-1}$)	Average Luminosity ($pb^{-1}hr^{-1}$)	Luminosity ($fb^{-1}yr^{-1}$)	Integrated Luminosity ($fb^{-1}yr^{-1}$)
2001	2500	0.82	0.20	0.50	0.5
2002	3500	1.51	0.30	1.05	1.6
2003	2500	1.34	0.30	0.75	2.3
2004	3500	2.27	0.50	1.75	4.1
2005	4000	3.26	0.70	2.80	6.9
2006	4500	3.91	0.80	3.60	10.5
2007	5000	4.95	0.90	4.50	15.0

Table 8: Luminosity model used for calculating depletion voltage evolution. A six month shutdown is included in 2003.

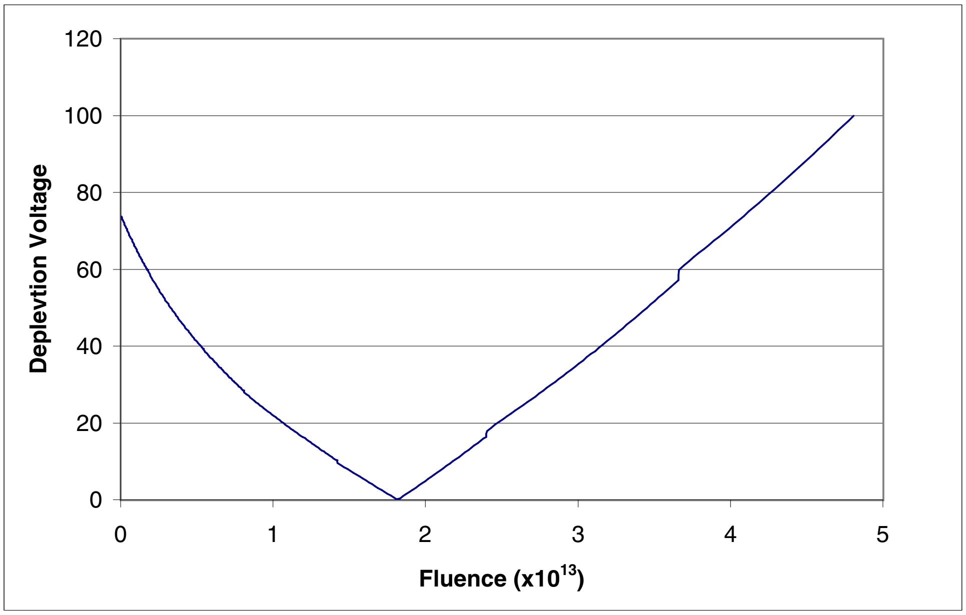

Figure 4: Results of depletion voltage model for SVX-II Layer 1, using nominal conditions and the central value expected fluence at the L1 radius.

cease functioning. We estimate from these studies that a reasonable estimate of the dose at which we expect this to occur is 800±100 krad. From Eq. (4) the ionizing dose at the SVX-II port-card radius of 14 cm is 53 kRad/fb^{-1} (to which we assign a 60% error). This yields an SVX-II port-card central value lifetime of 15 fb^{-1}, and a safe lifetime of 5.7 fb^{-1} after application of uncertainties and the engineering safety factor. For the ISL/L00 port-cards, the corresponding values are 14.6 and 39 fb^{-1}.

There may be an additional issue for L00 port-cards, where we have to consider degradation of the dielectric causing possible problems with HV bias. Recall that the port-card was designed before there was a L00 project. The specifications for the HV lines was 200V. After irradiation, L00 ladders will be biased up to much high voltages. All L00 port-cards/ladders are tested with 600V but this is still a concern after irradiation occurs.

We also estimated the lifetime of the power transistors used in the analog voltage regulators and the DOIMs on the port-card that send data to the crate electronics. Samples from two different lots of power transistors were irradiated with 63 MeV protons. The initial gain of all transistors was 200. After an ionizing dose of 400 kRad (silicon equivalent) the gain of lot 1 decreased to 40 whereas the gain of lot 2 decreased to 20. All transistors used on the present port-cards were taken from lot 1. The voltage regulator design requires a power transistor gain greater than 10. However, the circuit has not been tested with a gain as low as 10. We therefore assume that the voltage regulators will cease to function after a dose of (600 ± 200) kRad. However, tests have shown that these regulators are redundant and the system will function reliably without them.

2.6 Collider Backgrounds

The Tevatron for Run 2 is not the same collider that it was for Run 1. The beam structure and the hardware configuration in B0 will be significantly different. The extrapolation from Run 1 data is based on the assumption that $p\bar{p}$ collisions are the dominant source of radiation. However, other sources that depend on single beam currents, such as beam-gas and beam-wall interactions, may be significant. Any such sources are not taken into account in our extrapolation. Given the data collected during Run 1 and available simulation tools it is not possible for us to make an intelligent prediction of collider backgrounds in Run 2. The potential for such effects that we cannot estimate is the main justification for an engineering safety factor. The specific choice of 1.5 for this factor is based on common practice [29, 30].

2.7 Improving Estimates With Run 2 Data

The main uncertainties in our layer lifetime estimates come from

1. Discrepancies in Run 1 measurements
2. Radial dependence of neutron equivalent fluence,
3. Radial dependence of ionizing dose,
4. Damage coefficient α,
5. New running conditions.

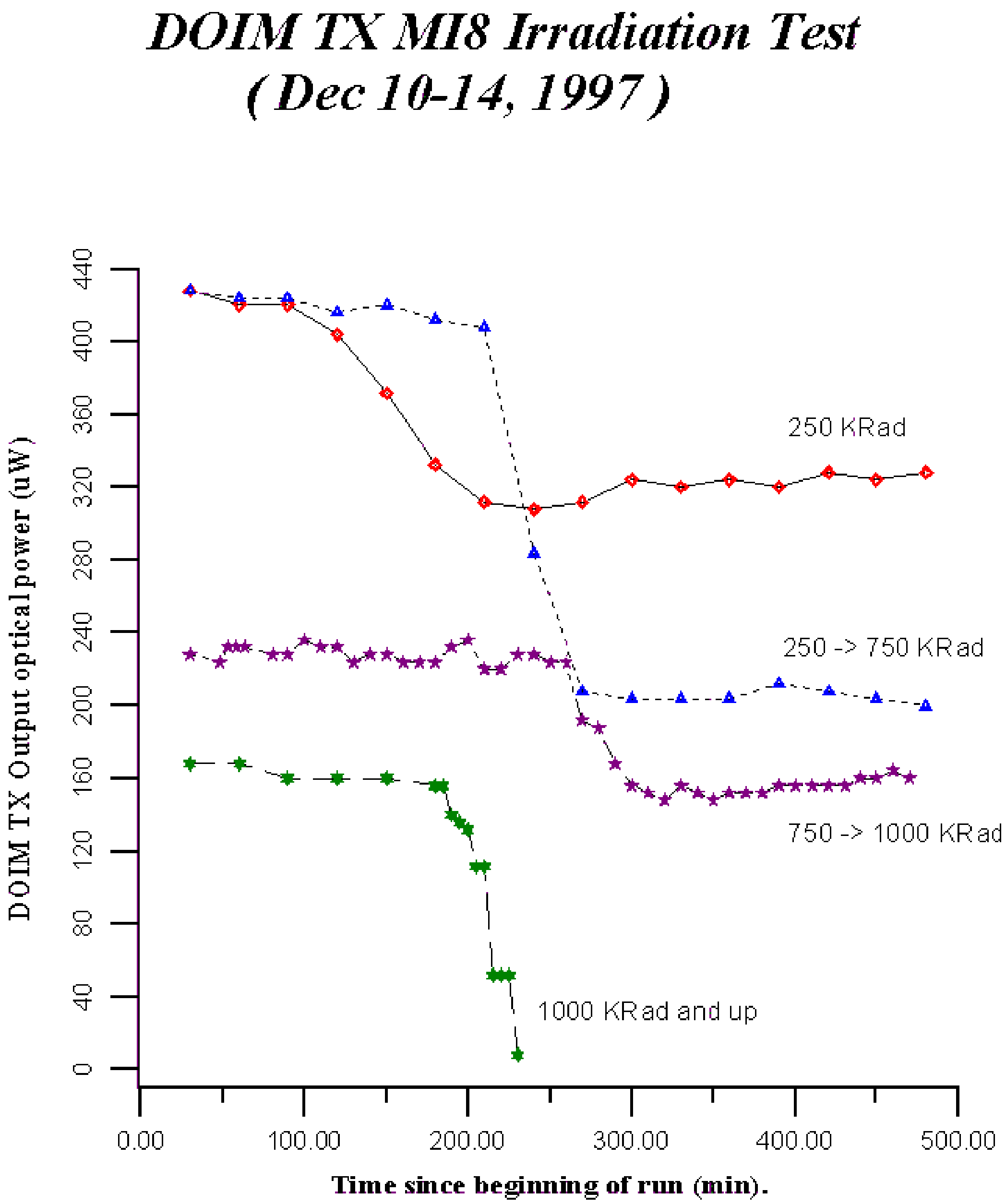

Figure 5: Results of irradiation of DOIMs.

Items 1, 2 and 5 will be measured in Run 2 as soon as a luminosity equivalent to Run 1 is integrated. This will remove practically all uncertainty in leakage current and neutron-equivalent fluence radial scaling, and will allow for a less conservative safety factor. Unfortunately the same cannot be said for item 2, because the radiation resistance of SVX3D chips means that no change will be measurable after a small dose. Radial dependence of ionizing damage will therefore probably remain uncertain for a long time. However, the initial (zero dose) signal to noise performance will be well measured almost immediately, removing smaller uncertainties. The damage coefficient is needed in order to calculate the evolution of depletion voltage. However, eventually it will be possible to normalize depletion voltage shift directly to integrated luminosity. This will allow us to dispense with the damage constant altogether. Unfortunately depletion voltage is hard to measure in the detector. Much easier to measure is the point at which type inversion occurs. Since L00 is expected to invert at 0.8-1.6 fb^{-1}, this is the point at which uncertainty 3 will be completely removed. However, already after 0.5 fb^{-1} we should have some information on the rate of change of the depletion voltage that can be used to make a more informed decision about the scale of required Run 2b Silicon upgrades.

For the port-cards the lifetime range allowed by present data is very broad. However, once Run 2a begins, the light output of the DOIMs is expected begin to decrease measurably with accumulated dose, and therefore a precise lifetime estimate for the port-card should become available quite soon.

Finally, it would be profitable to investigate further the behavior of Micron sensors by irradiating spare ladders left over from SVX-II and ISL construction. In particular, one would irradiate ladders beyond type inversion in order to check whether it is still necessary to restrict the bias voltage to one side only (as we have assumed).

2.8 Conclusion

Radiation affects both signal to noise performance and sensor operation requirements. While both are radiation effects, their dependence on integrated luminosity is different, as is our ability to predict them. We have therefore estimated the lifetime for each layer independently from internal heating due to leakage current, signal to noise, and depletion voltage shift. The results that dominate the lifetimes are summarized in Table 9. Where signal to noise degradation is dominant the safe lifetime due to depletion voltage is also given, since signal to noise lifetimes are soft in the sense that it is possible to relax them by accepting worse performance. On the other hand the shifting depletion voltage imposes a hard limit on detector operation.

Finally we would like to note that L00 reaches its V_{dep} limit[22] at roughly 50% more luminosity than L0. As discussed in the L00 proposal submitted to the PAC in 1999 [31], L00 thus provides for the possibility of extending the useful lifetime of the CDF Run 2a silicon. At the time of the L00 proposal it was further stated that it may be possible to maintain

[22] Actually 10% of L00 reaches its S/N limit of 6/1 at roughly 6.0 fb^{-1}. We have determined that this does not seriously affect the performance of the overall system. In particular, this portion of L00 corresponds to roughly 7% of unique coverage and would still provide significant, albeit degraded, b-tagging efficiency at lower S/N. For instance, even a 30% reduction in b tag efficiency in this region would cause a loss of only 2% of b-tagging overall.

Layer	Safe Lifetime (fb^{-1})	Cause of Death
L00	7.4	V_{dep}
L0	4.3 (5.6)	S/N (V_{dep})
L1	8.5 (10.9)	S/N (V_{dep})
L2	10.7	V_{dep}
L3	23 (30)	S/N (V_{dep})
L4	14	V_{dep}
L6	> 40	n/a
L7	> 40	n/a
L8	> 40	n/a
SVX-II port-cards	5.7	DOIM
ISL & L00 port-cards	14.6	DOIM

Table 9: Safe lifetimes for each layer of SVX-II as defined in the text. In the "Cause of Death" column S/N stands for signal to noise and V_{dep} for depletion voltage.

good performance of the CDF silicon by replacing only L00 when it stopped functioning. This strategy is no longer seen to be viable for Run 2b. As seen in Table 9, our current understanding of the longevity of the Run 2a silicon indicates that many layers of SVX-II may have to be replaced in order to guarantee survival to 15 fb^{-1} integrated luminosity. A L00 replacement on its own cannot provide useful data in the absence of operating silicon at the innermost 2 or 3 layers of SVX-II. As discussed above, biasing problems for L2 and L4 may lead to a fore-shortening of the useful lifetimes of these layers that was not appreciated at the time of the L00 proposal.

3 Layout Examples

As discussed in the Introduction, two scenarios for the Run 2b silicon tracking systems have been considered, a partial and a full replacement. In both cases the the Run 2a ISL would be retained. We also decided that the replacements for the small radius layers could be the same in both scenarios so that they only differ in the radial region from about 6 cm to 20 cm. In this section we describe the basic concepts currently under consideration. We emphasize that these are not final designs but rather conceptual examples to illustrate how new requirements and technologies can be integrated into practical layouts.

Given the technical requirements and time constraints on this project it is important to apply simple and efficient methods, and to benefit from existing experience. We seek a design which will meet radiation specifications with the lowest practical mass while not degrading the Run 2a performance standard. We have been strongly influenced by our experience in the Run 2a projects and the ongoing developments for the large silicon trackers at the LHC. Some of these elements are listed below.

- Simplify module design and variety: Following ISL and the LHC trackers we propose simple module designs and a minimum number of module types. We consider also the use of automated assembly methods similar to the gantry based system of CMS [32], to streamline production. CMS plans to construct some 17,000 modules, covering 223 m^2, in just a two year period by applying automated methods.
- Remove hybrids and port-cards from the tracking volume: Following L00 we will apply low-mass, fine-pitch cables to carry signals from the sensors to hybrids which are located outside the tracking volume. A potential benefit of this approach is that it allows one to increase the number of readout chips associated with the 90^o strips to reduce or eliminate troubling ambiguities. Following ISL, we also have a scheme to place the port-cards well outside the tracking volume.
- Integrate cooling and mechanical supports: Both L00 and the LHC designs require integrated cooling and support structures. In both cases this is necessary to maintain the required low temperatures on the detectors. In addition, the large scale of the LHC designs leads to cooling which runs parallel to the beam line rather than azimuthally about the bulkheads as in the short barrel designs of SVX and SVX-II. In particular, the CMS group have developed Carbon fiber support cylinders with integrated cooling for their inner tracker and a system of "rods" for their outer silicon layers. The rods are extremely attractive as they enable rather simple installation and maintenance, via direct access for insertion and extraction of all layers of the outer barrel [33]. In addition, they are able to achieve good mechanical alignment.

3.1 The Inner Section

The small radius region of the tracker is the most critical part of the Run 2b silicon system in several respects. First of all, the resolution on important track parameters is largely dominated by the hit resolution, radial position, and material content of the innermost layers of the tracker. Secondly, in Run 2b these layers will integrate large radiation doses to require the use of single sided micro-strips or pixels, with direct cooling. This situation is already familiar from the Run 2a L00 detector which uses single sided, rad-hard micro-strips at small radius. The silicon is directly cooled to $\leq\ 5^{o}$C with four 2 mm diameter pipes integrated with the C-fiber supports for the sensors.

The L00 front end electronics are placed away from the silicon, cooled separately, and connected via low mass fine pitch signal cables to the sensors. This results in a small cooling system for the sensors minimal mass in the tracking volume. The front end electronics are also placed at a larger radius than the sensors which minimizes their radiation dose. The L00 C-fiber supports contain some layers which are of relatively high thermal conductivity. The fiber orientations of the layers were chosen to efficiently carry heat to the four cooling tube locations while simultaneously providing mechanical rigidity and precision. The L00 techniques are described in more detail in the L00 proposal [34] and other documentation which is available from the L00 web-site [35].

In preparing a conceptual design for the Run 2b inner layers, we would leverage our L00 experience. An innermost beam-pipe layer can be similar to, or a copy of, the present L00 system. As mentioned earlier, an alternative could be to use pixels. Section 10 contains a technical discussion of the pixel layer concept. In either case we would purchase a new Be beam-pipe so that we could pre-assemble the new inner section before the Run 2a detector is extracted from the collision hall.

For the larger radius layers of the inner section additional molded C-fiber shells with integrated cooling pipes would be used. For these larger shells, a sandwich of Carbon fiber/honeycomb/Carbon fiber can be applied to increase stiffness. These will support pairs of back to back single sided sensors, placed on both the inside and outside surfaces. One of the pair would have strips parallel to the beam line (axial sensor) while the other could be a 90^{o} stereo sensor with a double-metal structure. Since the detectors are single sided, the cost of the silicon is relatively low [39]. Low mass, fine pitch cables would again carry the signals to front end electronics located outside the tracking volume. All detector pairs and hybrids would be one of two universal designs in this scheme.

Figure 6 shows a schematic layout of the inner region of the silicon tracker. The beam-pipe layer is identical to L00. The next two layers are each made up of two separate polygonal support shells to facilitate mounting on both surfaces while providing space for the passage of the fine pitch signal cables. In figure 7 we show a close up view of the silicon mounted on the support structure.

As in the L00 case, this design has the advantage of minimal mass within the tracking volume associated with electronics and cooling elements. This more than compensates for the increase in mass that comes with using two single sided sensors instead of one double sided sensor, (see the discussion on material in the section 4).

With regard to assembly and alignment, all the silicon would be placed and aligned on half cylinders prior to assembling half-cylinders into whole cylinders. The completed cylinders would be supported from their ends and could be adjusted as solid objects until all layers are concentric and parallel. This would have to be done to the level necessary to satisfy SVT triggering requirements.

The lightweight signal cables used in L00 were manufactured at CERN [36] at modest cost. If they had been made by a commercial U.S. vendor, they would have been expensive

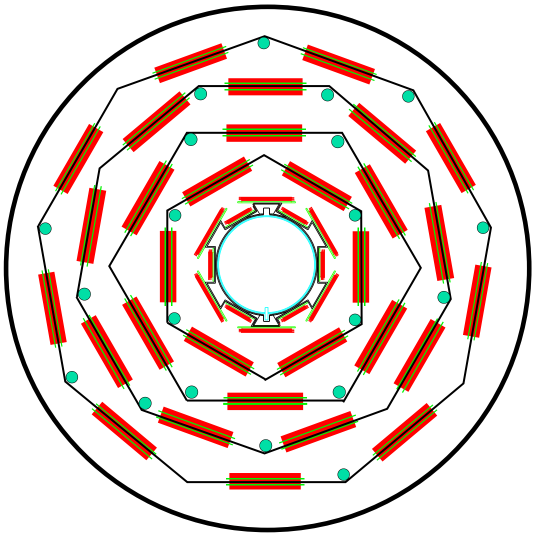

Figure 6: *Transverse cross-sectional view of a schematic layout for the small radius Run 2b silicon detector layers.*

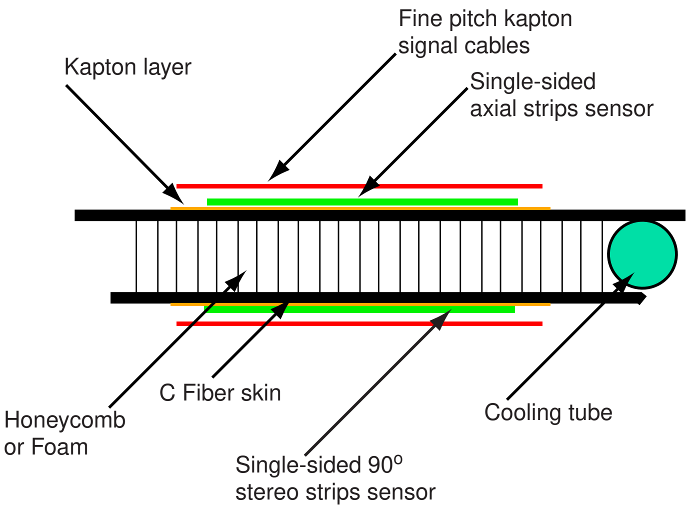

Figure 7: *Close up of the transverse cross-sectional view for the inner section silicon detectors mounted on their support shells.*

[37]. It will be important to find a capable low cost vendor because CERN may not be able to handle the volume required for the Run 2b system. We are currently in the process of qualifying a Japanese company [38]. One advantage for the inner layers at radii slightly larger than L00 is the existence of ample space to route the cables (along the polygonal faces) with correspondingly larger strip-line pitch. This both simplifies the fabrication of the cables and reduces the capacitance, resulting in a larger signal-to-noise ratio.

3.2 The Outer Section

In the partial replacement scenario we would try to retain as much of the Run 2a detector as possible. The outermost two double-sided layers of the SVX-II detector (L3, L4) would be reused by installing them on a two-layer Beryllium bulkhead support structure similar to those used in Run 2a. In the full replacement scenario, we would build new modules and a new support structure. In this case, the modules would all be single sided and therefore could be constructed rapidly. Again, axial-stereo views would be obtained by installing an axial module back-to-back with a stereo module. We describe these two concepts in greater detail here.

3.2.1 Partial replacement scenario

The sequence of tasks required during the shutdown, and the duration of the shutdown required in the partial replacement scenario is discussed in more detail in Section 5. In this scenario, the outermost two layers of SVX-II (L3, L4) could be reused. Probably the most obvious approach would be to build new rad-hard ladders to fit on the existing bulkheads for the inner layers. In this case we could either order a replacement set of bulkheads using the original designs or we could un-stack and reload the existing bulkheads during the shutdown. In practice however, the new inner layers, in order to be rad-hard, must be constructed from single sided sensors and have direct cooling to the silicon. These new ladders will be thicker than the present ones and will not fit on the present bulkheads. The Run 2a system is also not designed to distribute cooling inside the barrels. There would be significant difficulties associated with retro-fitting the current bulkhead designs to accommodate this possibility.

As a consequence of these issues, we decided to design a new inner section, as described above, and to install this inside a new two-layer bulkhead structure that would reuse the outer two layers of SVX-II. The plan would be to complete the inner section ahead of the shutdown. The outer layers of SVX-II would be transfered to the new bulkheads during the shutdown. The entire sequence of shutdown maneuvers is discussed in the next section. We recently received a quotation of 40k$ each for producing new two-layer bulkheads with the geometry shown in Figure 8. We would need to order a minimum of 6. This design would result in one fewer layer than the current SVX-II which may not be acceptable. This could be remedied by adding a layer outside L4 in the region previously occupied by the Run 2a port-cards. (The issues associated with port-cards in Run 2b are discussed in section 9 of this note).

There are at least three significant risks associated with this scenario which are discussed in more detail in the next section. The first is that the final assembly schedule would be entirely time-critical since much of the key work would have to be done during the shutdown when no data taking is possible. The second is that an unknown number of ladders could be bad by this time, or they could be damaged during their removal from SVX-II. Additional spares would have to be made which is non-trivial. Thirdly, the estimated shutdown period, which is discussed in more detail in section 5, would be unacceptably long.

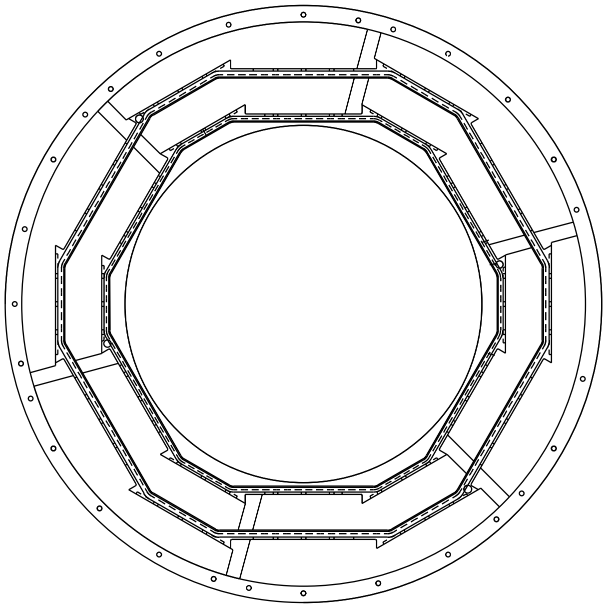

Figure 8: *Two layer Beryllium bulkhead design.*

3.2.2 Full replacement scenario

There are several advantages to a full replacement of the L00/SVX-II system. The primary one is that it decouples the effort from the shutdown schedule. In addition, we believe the installation can be achieved in a six month shutdown. Additional advantages are that the layout may be re-optimized, new low mass technologies can be applied, and the risk of damage to the remaining double sided ladders is removed.

In the case of a full replacement, the inner layers would be the same as those described earlier in this section, with hybrids mounted outside the tracking volume. The new outer layers would be based upon a single universal ladder type composed of back-to-back axial and small angle stereo single sided sensors. In the Run 2a system, a large radial gap exists between SVX-II and ISL. We would seek to distribute up to three new outer layers in the space between radii of 6 cm and 20 cm.

Using a fine pitched sensor, we could opt to bond a varying subset of the strips from layer to layer thereby optimizing the sampling and the channel count. The use of floating intermediate strips is known to result in improved resolution. A universal double sided hybrid could be used with different numbers of chips mounted for each of the layers. A set of three simple fanout designs would be required to mate the hybrids appropriately to each layer. Alternatively we could sample at each layer with constant granularity, as has been done in SVX and SVX-II.

In this design the hybrids would be mounted adjacent to the silicon. The modules would be placed longitudinally on extended support frames modeled after the "rod" concept developed for CMS. This is illustrated in Figure 9 and Figure 10. The rods could integrate the cooling of the silicon if desired so that these layers would also be capable of very high luminosity operation. (For 15 fb^{-1} it may not be necessary to directly cool the sensors at these radii.)

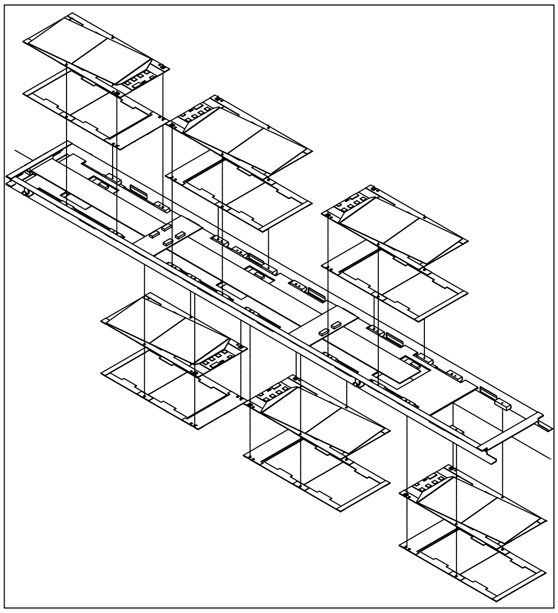

Figure 9: *An exploded view of a CMS outer barrel rod is shown. The basic support structure is a carbon fiber beam with integrated cooling. Modules are mounted to either side of the beam. The modules have the electronics hybrids mounted off the silicon. As a result, adjacent modules are staggered radially to allow silicon from one module to cover the hybrid region of its neighbor. This is done to obtain continuous coverage.*

We would plan to have 6-fold readout segmentation in z as is currently the case for SVX-II and L00 as seen in Figure 12, (labeled "Run 2a Detector"). In order to have the same acceptance as SVX-II when the outermost layers are at larger radius, it is necessary to make these layers longer as seen in Figure 12, (labeled "Run 2b"). Note however that in Run 2b it is expected that the luminous region will be shorter as a result of a crossing angle for the intersecting proton and anti-proton beams. As a result it would be possible to retain our Run 2a acceptance with a shorter replacement detector. This is made clear in Figure 13. The SVX-II detector in Run 2a has a half-length of 45 cm and the Run 2a luminous region will likely be $\sim$ 30 cm corresponding to $\sim$65% acceptance for two b jets in top events. For a luminous region of 15 cm, the acceptance increases to $\sim$ 85%. Alternatively, one could retain 65% acceptance while reducing the detector length to $\sim$40 cm. Note that the cost of the replacement detector would not be very different for this choice and so we would plan

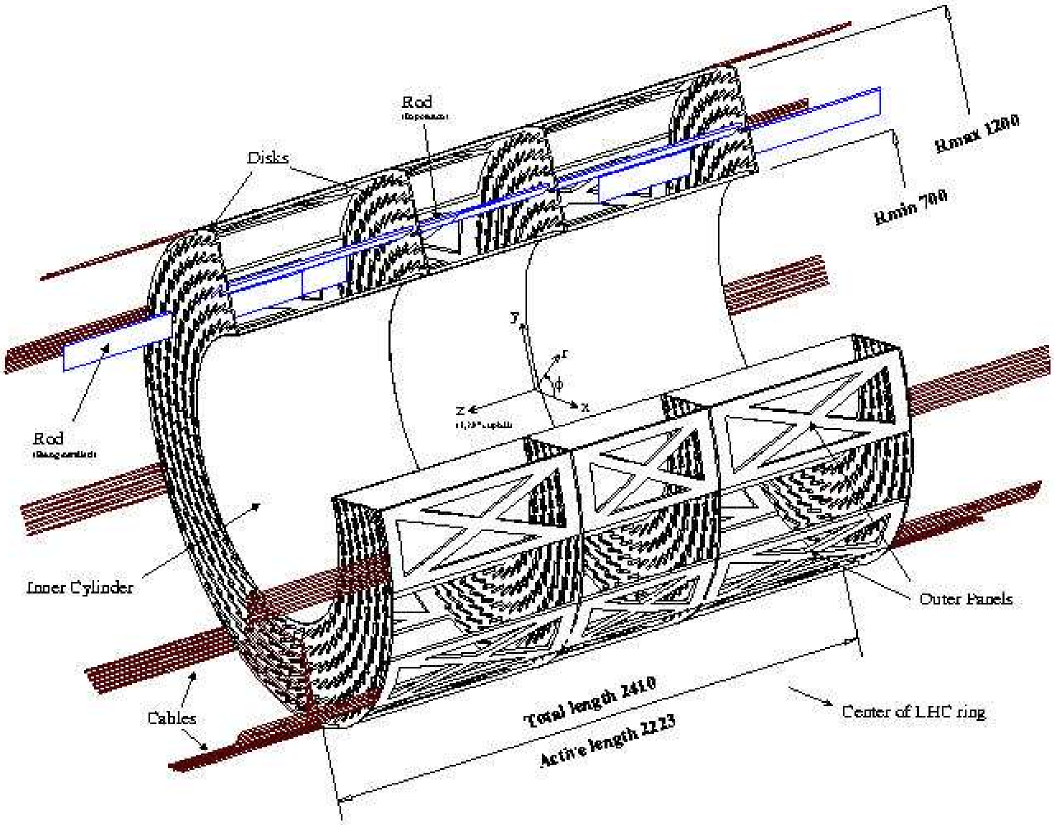

Figure 10: *The CMS outer barrel support structure is made up of four carbon fiber planes with carefully aligned slots. The rods slide into the slots. Rods are installed from each end of the detector in* z *and overlap slightly at* $z = 0$*. The installation of the rods is extremely simple and the overall alignments achieved are much better than what we will need in Run 2b. In addition, every rod is accessible at all times and can be easily removed and repaired.*

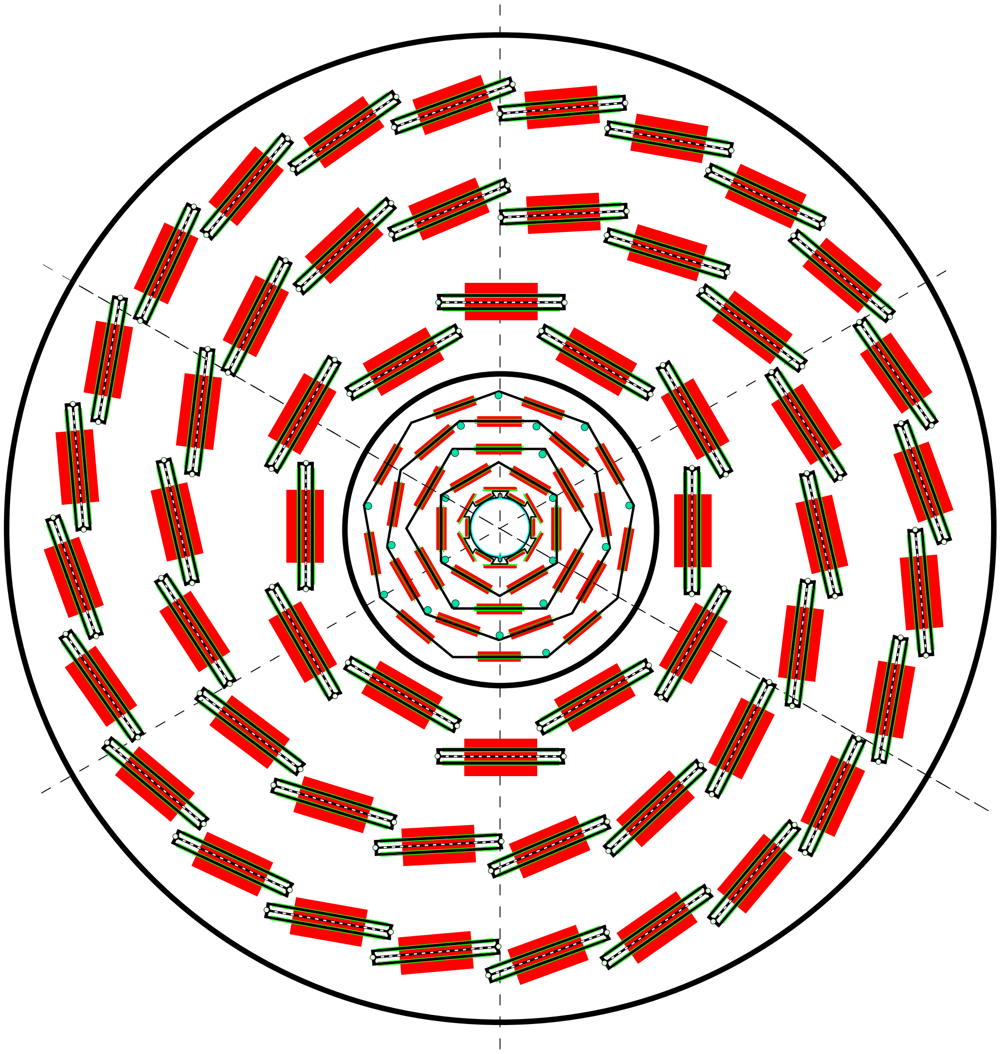

Figure 11: *A schematic end view of a full replacement detector for Run 2b. The new outer detector section for Run 2b is shown with 3 layers uniformly distributed in radius. In the schematic diagram shown we obtain a 60 degree symmetry in ϕ and all modules have the same size in the 3 outer layers.*

to retain the Run 2a coverage to increase our overall acceptance with a shorter luminous region unless we determine that there are serious pattern recognition or occupancy problems at higher luminosity.

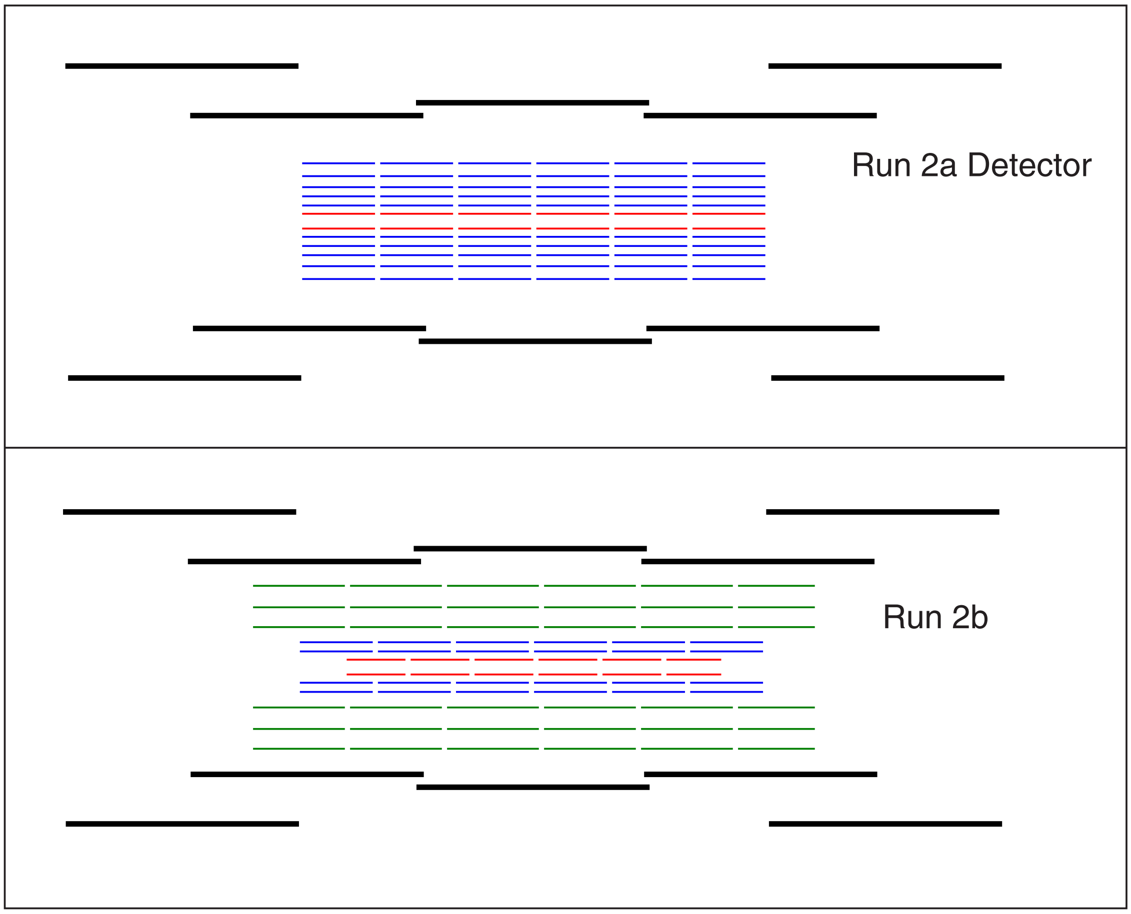

Figure 12: *In this figure we compare the longitudinal cross sectional view of the Run 2a silicon detector to a potential replacement system with longer layers at larger radii.*

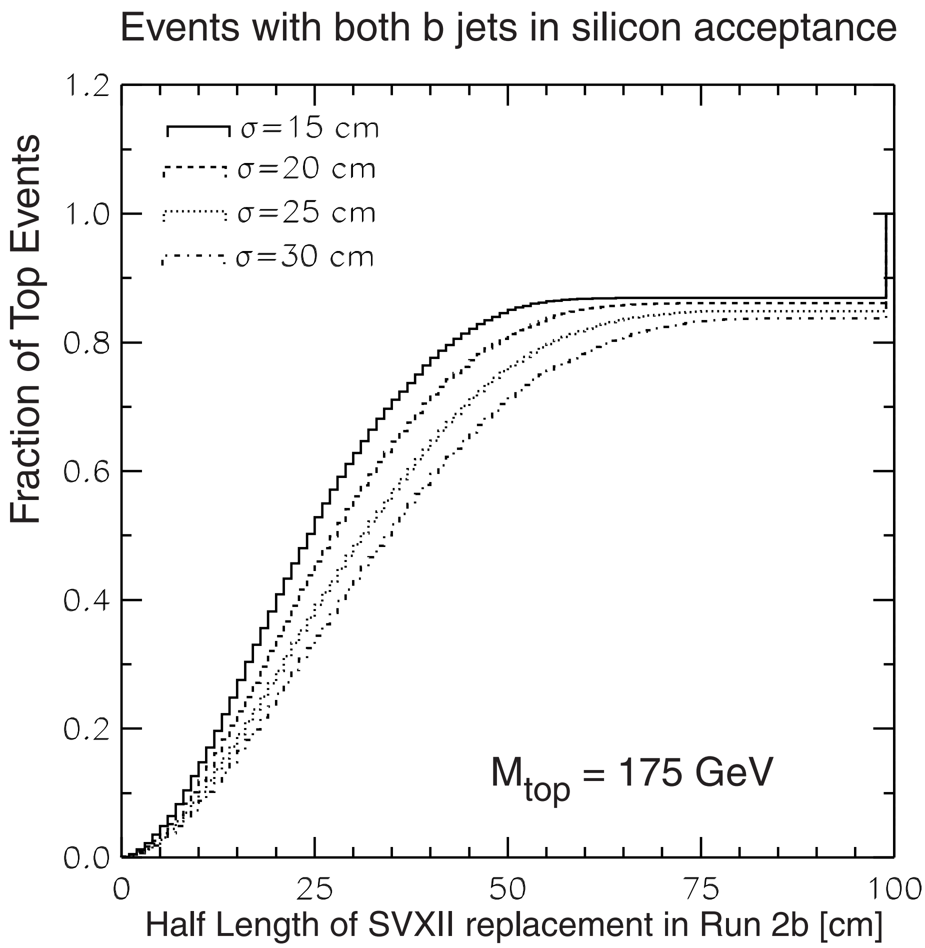

Figure 13: *This plot shows the fraction of top events in which both b jets are contained in the SVX-II acceptance as a function of the half-length of SVX-II. The 4 curves correspond to different luminous region lengths as shown.*

4 Material in the tracking volume

CDF's Run 2 silicon system contains an average of more than 10% of a radiation length (X_0) at normal incidence. The effect of this material on impact parameter is mostly compensated by the low mass and small radius of L00. However, it still degrades the momentum and ϕ_0 resolution particularly for tracks which happen to traverse regions of concentrated material. The dominant sources of this problem are the readout hybrids which are mounted on top of the silicon in SVX-II, and the port-cards which are mounted in a shell between SVX-II and ISL. The cables servicing power to the port-cards are a large part of this material. The ISL hybrids are mounted off the end of the silicon so about half of that material is outside the tracking volume. The ISL port-cards are mounted outside of the tracking volume, off the end in $|z|$.

In a Run 2b replacement, we have an opportunity to reduce the material by moving the SVX-II port-cards outside the tracking volume and/or replacing the DOIMs with lower power devices to minimize the amount of copper needed for power distribution. We can also move some of the readout hybrids outside the tracking volume by either mounting them off the silicon as in ISL, or by using L00 style cables.

We have briefly studied the effect of these potential material reductions by tracing Monte-Carlo tracks through a detailed simulation of the Run 2a geometry. The intersected measurement and scattering planes are used to calculate the covariance matrix for the $r-\phi$ track parameters. We approximate the effect of potential Run 2b material reductions by "turning off" the SVX-II port-cards and/or hybrids in the simulation.

Removing the portcard material decreases the average material encountered by tracks in $|\eta| < 2$ from $0.18X_0$ to $0.15X_0$. Also moving the inner three layers of SVX-II hybrids out of the tracking volume reduces the material encountered to $0.12X_0$. Finally, removing the outer two layers of SVX-II hybrids reduces the material to $0.10X_0$. In the scenarios discussed in the preceding section, we have considered the use of single-sided, cooled sensors and no hybrids in the tracking region for the innermost layers. In the outer layers of an SVX-II replacement we discussed also using single-sided sensors and low mass, double sided, short hybrids. Adjusting for the additional silicon everywhere, the lower mass hybrids at large radius, and the addition of cooling to the inner layers we estimate that the full SVX-II replacement would have an average of $0.14X_0$ as compared to the $0.18X_0$ for the Run 2a detector. This could be reduced to roughly $0.12X_0$ by using low mass cables to also push the hybrids for the outermost layers out of the tracking volume.

The effect on momentum resolution is shown in Fig. 14 where 1 GeV tracks reconstructed using only silicon hits are used as a benchmark. If COT hits can be used as well, the momentum resolution improves substantially, but tracks with $|\eta| > 1$ may only be reconstructible in the silicon system. Taking advantage of potential material reductions improves the mean momentum resolution by about 20%, for tracks formed with silicon data alone.

In addition to the impact of material on track parameter resolutions, it is also important to consider the production of secondary particles and their effect on occupancy. Run 2a simulation studies have shown that the number of tracks produced by secondaries (including secondaries from conversions and nuclear interactions) is roughly equal to the number of tracks from primaries. In the previous section we considered a full replacement option in

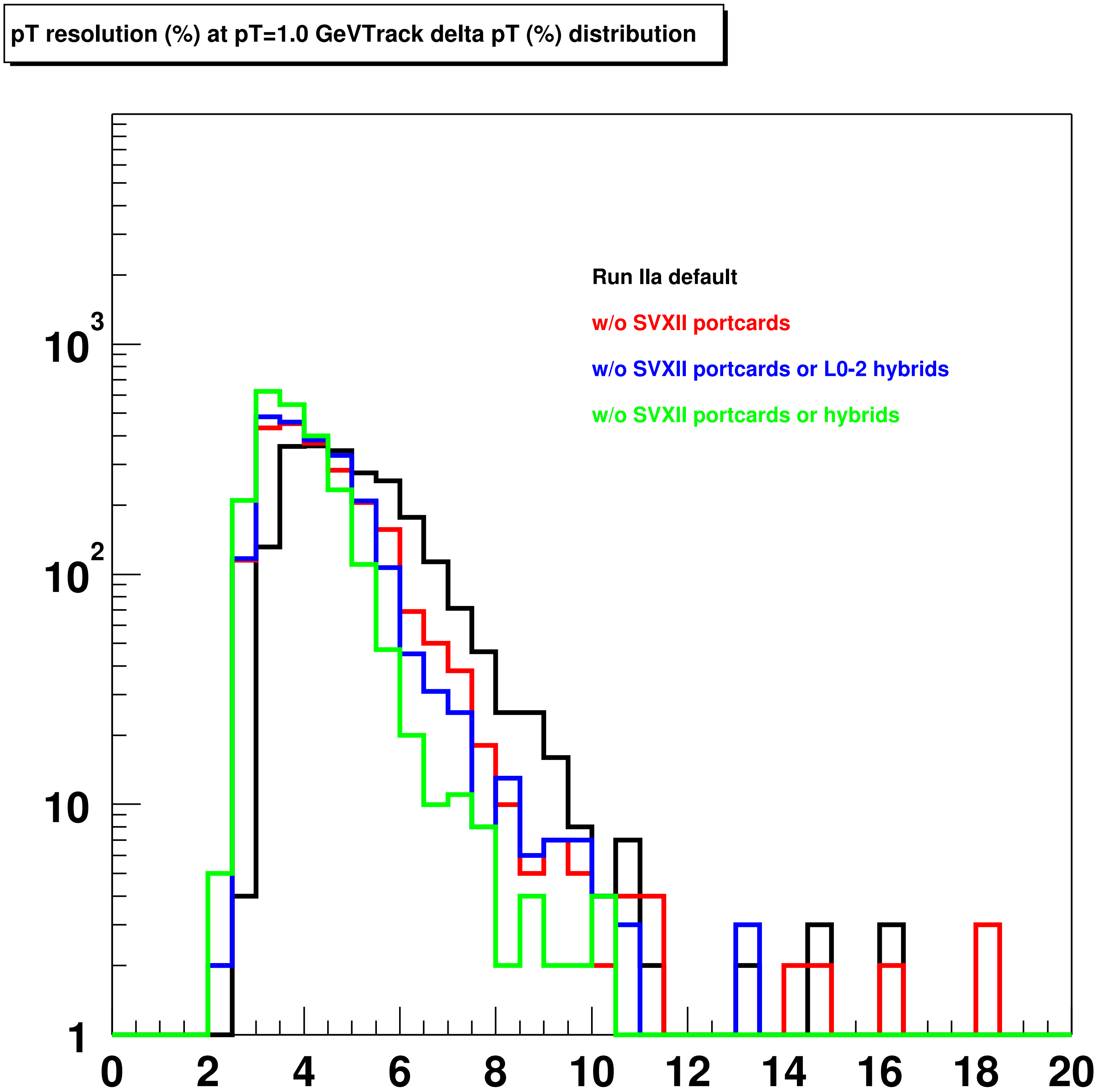

Figure 14: Momentum resolution (in %) for 1 GeV tracks reconstructed with only silicon hits is compared for several configurations: Run 2a default configuration (black = 0.18 X_0 average), without SVX-II port-cards (red = 0.15 X_0 average), without SVX-II port-cards and L0 - L2 hybrids (blue = 0.12 X_0 average), and with SVX-II port-cards and all hybrids removed (green = 0.10 X_0 average).

which we would move the port-cards and hybrids from the innermost layers out of the tracking volume corresponding to a material budget which is scaled down from that of Run 2a by a factor of $\sim 3/4$. If we can drop the material by this factor, then we reduce the overall occupancy by about a third. In complex events like top or Higgs, the occupancy from the hard scattering event dominates over the occupancy from multiple interactions, and this secondary occupancy is correlated in location with the tracks of interest. Reducing this correlated, material-induced occupancy will help to improve pattern recognition capabilities in dense tracking environments. For instance, it will allow us to better cope with the added random occupancy from multiple interactions at high luminosity.

5 Partial Replacement Issues

The assumptions we make are as follows. The silicon returns to Lab C to have L3 and L4 removed for installation into new bulkheads. At least 6 new bulkheads are purchased at a cost of 40k$ each [40]. One pair of bulkheads will be used with the ladders from Barrel 4 for practicing the removal and reuse of SVX-II ladders. The new bulkheads would maintain current SVX-II barrel geometry for the outer two layers. Each of the three pairs of bulkheads would be mounted on their barrel assembly supports (wagon wheels) before the CDF Silicon detector comes over from the collision hall (B0). The port cards could be moved outside of the central part of the detector via extension cables and low mass repeater cards.

The inner layers of the new CDF Run 2b silicon detector would be inserted into the middle of the rebuilt SVX-II layers (*a la* what is being done for L00 in Run 2a). This would occur after the SVX-II ladders have been placed into barrels and the barrels have been placed inside a newly designed and built space tube.

This schedule also assumes that the two barrel assembly stations are in working order. New installation fixturing which is long enough to allow the cables to be dressed to the installation arms outside of the barrel would make the process easier and quicker.

We are also assuming that we have 3 L3 and 3 L4 spare ladders that could be used if we have troubles with any of the ladders removed and reused. This is probably not sufficient. Any loss of ladders beyond these spares would require that the damaged part be repaired. We cannot get any more L3 silicon from Hamamatsu. We can get more L4 silicon from Micron. As mentioned in section 3, it is likely that we would order new double sided silicon for L3 from Micron. This would require new masks. We do not have spare hybrids and would need to order materials and components and restart hybrid production at LBNL and surrounding commercial sites.

Schedule and steps[23]

1. Disconnect cables, cooling, and junction-card supports — 2 days
2. Remove ISL extension cylinder. — 1 day
3. Extract SVX-II from ISL — 2 days
4. Remove top of SVX-II space tube — 1 day
5. Disconnect cables from top port-cards — 1 day
6. Remove L00 hybrid supports and dress cables — 1 days
7. Extract beam-pipe (assuming we're allowed to trash L00) — 2 days

We have 2 barrel assembly stations. With the existing fixtures, we can remove the ladders from one barrel and then insert them into a new two layer barrel. This involves the following steps:

[23] Note that steps 1 - 3 are common to both the partial and full replacement scenarios.

1. Extract an end barrel — 1 day
2. Install the wagon wheels (WW) — 2 days
3. Remove PC rings and screen — 2 days
4. Install on Coordinate Measuring Machine (CMM) — 2 days
5. Align — 3 days
6. Start extraction at a rate of 1 layer/week — 2 weeks
7. Start installation at a rate 1 layer/week — 2 weeks
8. CMM measurements, install port-cards, remove WW — 1 week
9. Testing — 1 week
10. Install in space tube, dress cables and cooling — 1 week

Thus, we estimate it will take nine weeks per barrel. Steps 1-3, 9 and 10 are done off of the CMM's. This will allow some operations to occur in parallel saving 3 weeks from a purely sequential schedule (3 barrels * 9 weeks/barrel = 27 weeks). Total time for all three barrels without contingency is 24 weeks. We will need to purchase additional fixturing at a very rough estimated cost of 50k$.

To get the final sum we add the 2 weeks it took to get at the barrels in the first place and then add to this the amount of time it takes to put it all back together. The final assembly includes the following steps and associated durations in what we believe would be an aggressive schedule:

1. Alignment of the 3 barrels to each other and to the rails. — 1 week
2. Installation of beam-pipe (includes fixtures setup) — 1 week
3. Dressing cables and testing. — 1 week
4. Installation inside ISL — 1 week
5. Installation of extension cylinders and port cards — 1 week

The resulting grand total is of order 33 weeks. This is not a pessimistic estimate. It is based on how long it is taking to do things now and does not include contingency. A reasonable estimate for the latter is 6-8 weeks. Finally, the schedule above does not include the time required to get CDF out of and back into the collision hall. We are told that this is 17 weeks [41]. Add in another week to transport the silicon to and from B0 and SiDet and you get 57-59 weeks total.

In summary, the shutdown required for the partial replacement option is of order 14 months. We conclude that this option does not meet the laboratory constraint of a 6 month total shutdown period. More importantly, it is too costly in terms lost running and data-taking prior to the turn-on of the LHC experiments.

There may be ways of reducing the shutdown time. An obvious possibility would be to go to multiple shifts. It is however likely that it will be necessary to already work long days in order to maintain the schedule presented above. Another potential way of reducing the shutdown time substantially while reusing portions of Run 2a SVX-II would be to disassemble and reassemble the SVX-II barrels in parallel. Let us now consider this possibility.

For disassembly and reassembly of all three barrels in parallel, we would need 6 sets of barrel fixtures. The 3 fixtures used for assembling the new barrels must be installed on CMM's. It may be possible, but not preferable, to get by without CMM's for the fixtures used for disassembly.of the old barrels. Clean room space and granite tables would however still be necessary. Altogether this means 4 new setups and associated clean room space. The assembly setups would need to be fully prepared, with bulkheads and fixtures ready to go, so that we would only need to remove ladders from old barrels and install them in new barrels. The cost of new fixtures is about 100k$ for 4 setups. We could use the 2m B&S CMM, but this would mean that several species of fixtures would be needed. In order to have uniform procedures. programs and fixturing we could purchase at least one additional B&S CMM to replace the G&L CMM's. (The latter are getting old and have become somewhat unreliable in any case.) The existing fixtures would be adapted for use on the B&S machines.

We also need 3 extremely experienced technicians for barrel assembly and 3 other technicians, possibly with CMM operating experience, for disassembly. We currently have only one technician capable of performing all aspects of SVX-II barrel assembly. We would therefore need to spend a significant amount of time and effort to train at least two more technicians in this work. With this scenario it would take as little as 4 weeks to un-stack 3 old barrels and stack 3 new barrels. It would however be a significant feat to have 6 working fixtures with 6 extremely skilled, well-trained technicians all ready to proceed simultaneously at top speed in the shutdown. We therefore assign 100% contingency to the barrel disassembly and assembly.

The schedule can be reduced to roughly 14 weeks at SiDet before considering this contingency. With contingency the sum is 25 weeks. Altogether, with the edge effects discussed earlier, the shutdown period would thus be 42 weeks or 9.5 months.

In all cases, there are a number of risks inherent in a partial replacement plan. Most disconcerting is the fact that any problem that causes a delay in this period adds to the shutdown time.

6 Integrated Circuit Needs for Run 2b Silicon Upgrade

We consider two options for supplying production readout chips for a Run 2b upgrade: purchasing more SVX3D wafers from Honeywell or designing a replacement chip in a different technology. We compare these two options in each of the following categories: cost, schedule, risk, performance, and impact on upgrade design and effort. For the replacement chip option we specifically consider a 0.25 μm feature size chip based on the SVX3D design, fabricated by Taiwan Semiconductor Manufacturing Company (TSMC). There have been two proposals for developing a new chip. The FNAL IC design group has proposed designing a new device (referred to as SVX4), while the LBNL IC design group has proposed a conversion of the SVX3D chip layout to 0.25 μm feature size (referred to as SVX3E). We focus on the latter because it is faster and results of preliminary work are already available.

6.1 Cost

The remaining stock of good and fair SVX3D chips is approximately 200. The number of chips needed for a Run 2b upgrade depends on the upgrade path chosen, but in all cases significantly exceeds 200. While the number of chips in the SVX-II detector is 3,168, the number of good and fair die used for construction was approximately 5,000, due to assembly yields, prototyping and spares. Based on the 5,000 quantity, the number of good and fair chips required to replace only the inner 3 layers would be 2,300. An additional 200 chips would be needed for a L00 replacement. Clearly, a large re-order of SVX3D chips would be necessary for any Run 2b upgrade. Using an average yield of good and fair die of 50%, and the quoted Honeywell wafer cost[42] of $20,000, 2,500 good and fair chips would cost $720,000. This does not include any IC designer time, although some IC designer involvement may be desirable (see below). On the other hand, the cost of an equal number of chips (same size and same assumed yield) from TSMC would cost $192,000. This also does not include design labor, which would be the dominant cost of production for a new chip. As detailed in the next section (see Table 13), the development cost for an SVX3E chip would range between $0.5M and $0.65M (including an SVX2F chip for D0), while the FNAL IC design group has estimated that the development of an SVX4 chip would cost 0.8 - 1.0 M$.

6.2 Schedule

The lead time for Honeywell fabrications has been approximately 5 months. Given that the Honeywell process has had problems with via metalization in previous runs, it would be desirable to add process control modules to a new production run, and perhaps run pilot wafers ahead of the main batch that could be tested after critical steps. These measures would mitigate some financial risk (see below) but add lead time (some IC designer time would also be required). A conservative assumption would probably be 10 months from the time a purchase order is placed until a re-order of Honeywell SVX3D wafers is available for production use.

The FNAL IC design group has estimated that the SVX4 design process could be completed in 2 calendar years.

A considerable amount of work has already been done towards the LBNL SVX3E proposal, which is described in more detail in the next section. Also included is the estimate for a parallel SVX2F chip version for D0. The grand total labor required is 18.5 FTE-months of IC designers plus 7 FTE-months of physicists, students, or IC designers. We assume 1.5 FTE IC designers at each LBNL and Padova, and 1.0 FTE physicist/student. With this level of effort a prototype SVX3E + SVX2F wafer run could be submitted after 6.5 months of design work. The typical fabrication lead time for 0.25 μm foundries is 2 months. Given that mature test setups and procedures already exist, the functionality of the prototype SVX3E chip could be validated in 2 months, if the chip works as expected. After this a full production run could be ordered. However, a conservative view is that the SVX3E prototype will not work as expected, in which case additional test time and minor layout changes would be needed. Allowing 2.5 more months for testing and 2 months for layout changes, an SVX3F production run could be submitted after 15 months, making the total development plus fabrication lead time for a new chip version 17 months. An advantage of 0.25 μm technology is the low fabrication cost, which allows making full quantity prototype runs as an option for buying time. Note that this time estimate includes development of an SVX2F chip for D0, and assumes that the first prototype run will not work as expected.

6.3 Risk

The risk in re-ordering Honeywell SVX3D chips is non-zero, but relatively low. The main component of the risk is financial, since the wafer yields obtained for the Run 1a production of SVX3D chips were erratic, and the causes for the yield fluctuations not well understood.

There is also a risk in the decision itself to lock in the use of Honeywell SVX3D chips for a Run 2b upgrade, because the long term reliability of the SVX3D chip is still unknown. Whether a real threat exists will only be known as Run 2a progresses, at which point it may be too late to begin development of a new chip version. While in general this risk is inherent in using any ASIC, the SVX3D chip does have a history of reliability problems that may warrant giving this more serious consideration.

Present data on long term SVX3D operation are from hybrid and ladder burn-in, which was equivalent to roughly one week of full detector operation. At least 13 chips developed failures during the burn-in process that could not be attributed to scratches or any other known external damage (there may be additional failures that were not well documented). A few of these 13 failures were explicitly identified as an open connection in one via (a different via in each case) that appeared during normal operation. Figure 15 shows the time distribution of the documented burn-in failures.

A new chip would also carry a risk of unknown long term reliability, but this does not preclude its use in mitigating the SVX3D reliability risk. A new chip does additionally involve the usual IC development risks, which are predominantly schedules risks. However, in the particular case of SVX3E there are circumstances that reduce the risk. The SVX3E would be a new version of the SVX3 chip, rather than an entirely new device. This means that most circuit schematics will be recycled, reducing the risk of problems due to unproven circuit designs. Because the SVX3D has been extensively tested, the desired performance tests for the new version are mature, making it straightforward to evaluate the new chip. Finally, the constant improvement of simulation tools reduces risk in new development. "Full

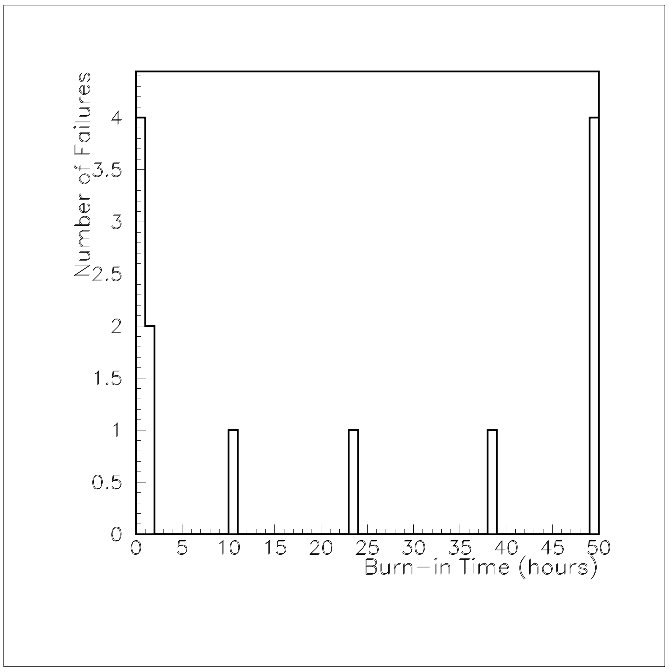

Figure 15: *SVX3D chip failures observed during hybrid and ladder burn-in. Ladder burn-in failures have all been placed at 50hrs, which is roughly the total hybrid burn in time. Three hybrid burn-in failures were placed at zero hours due to lack of failure time data.*

Chip" simulations greatly reduce the risk of mistakes in the integration of sub-circuits that have been individually simulated.

6.4 Performance and impact on upgrade design

The SVX3D chip has marginal noise performance and radiation tolerance for the Run 2b upgrade needs. This limits options for detector design. One could not place SVX3D chips very close to the beam pipe in Run 2b due to noise performance degradation with accumulated dose. Figure 16 shows a summary of noise measurements from high rate radiation tests of SVX3D chips. Even at zero dose the SVX3D chip equivalent noise charge (ENC) is 2,100 e^- for a 30 pF load, which means a relatively low S/N for the use of long L00-style fine pitch cables.

Integrated Circuits fabricated in 0.25 μm technology have been tested by the RD-49 collaboration and seen to tolerate doses of order 30 MRad with little degradation. Additionally, the development of a new chip presents an opportunity to improve noise performance, which would allow more flexibility in the use of fine pitch cables. An abbreviated performance comparison between the present SVX3D chip and an already designed SVX3E 0.25 μm replacement amplifier is given in the next section (Table 10).

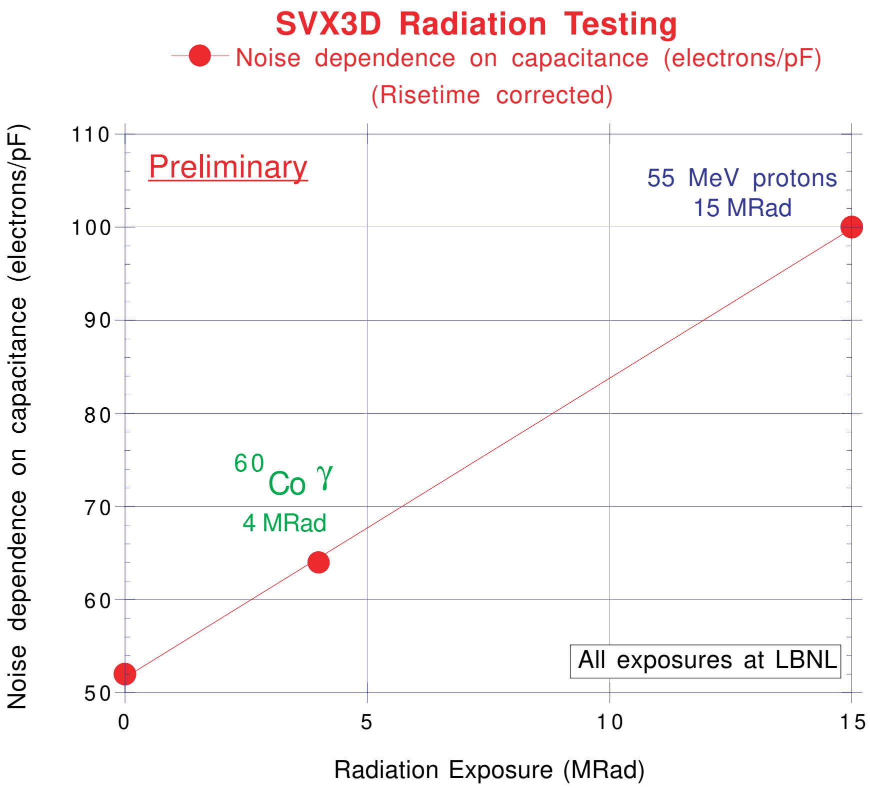

Figure 16: *SVX3D chip combined noise measurements from high rate test irradiations. The figure shows the slope a in the linear expression* $Noise = a \times (Capacitance) + b$. *The intercept b in this expression also approximately doubles from a value of 650 electrons to 1100 electrons over the range of these tests.*

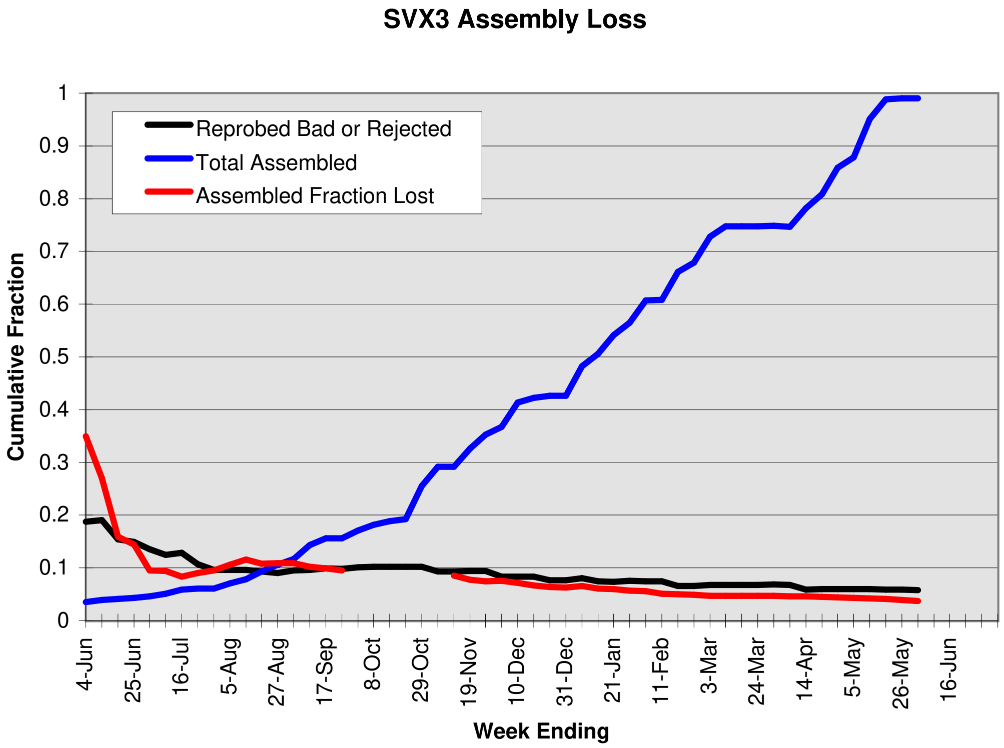

Figure 17: *Time evolution of fraction of SVX3D chips lost post-dicing and post-assembly for Run 2a.*

6.5 Impact on upgrade effort

The level of effort that was required to assemble and test the front end electronics for the Run 2a silicon system was significantly greater than originally expected due to the extreme sensitivity to handling of the SVX3D chip. A similar extra level of effort would be required for a Run 2b upgrade that relied on the SVX3D chip. Electrical testing of individual chips just prior to use in assembly was implemented for Run 2a, but even this did not completely eliminate defective chips on newly assembled hybrids, as handling is an inevitable part of assembly. With individual chip testing a failure rate of newly assembled chips of 4% was achieved, while the total post-dicing failure rate was 11%. In all, 279 chips were removed from hybrids and replaced for Run 2a (not all hybrids with defective chips were repaired). Figure 17 shows the time evolution of the fraction of chips rejected post-dicing (number of chips that failed post-dicing test over number of chips that were good before dicing and tested after dicing) and the fraction of defective chips found after assembly ("Assembled Fraction Lost"). Having to replace chips as part of the normal assembly chain puts significant constraints on hybrid design, and requires additional labor and time for debugging and repairing a large fraction of the production components.

While there is no guarantee that a similar level of effort would not be required with a new chip, it is true that the SVX3D situation was anomalous both in terms of industrial practice and the experience of other silicon construction projects. The expectation is therefore that an SVX3E or SVX4 chip would significantly reduce the assembly effort relative to Run 2a.

6.6 Conclusion

There appears to be no cost disadvantage to developing a new chip version for Run 2b, and depending on the upgrade path chosen there may be a cost advantage. Radiation tolerance and noise performance both favor developing a new chip, and it is likely that the Run 2b construction effort will be lower with an SVX3E or SVX4 chip than with the existing SVX3D. The main drawback and risk of basing the Run 2b upgrade design on a new chip is the longer and more uncertain lead time before production chips are available. However, proceeding with the development of a new chip would serve as risk mitigation even without a decision on whether to use the existing SVX3D for a Run 2b upgrade.

7 SVX3 Conversion to 0.25 μm

This section summarizes a proposal from the LBNL IC design group and the LBNL CDF group to continue an on-going effort to convert the SVX3 integrated circuit to a 0.25 μm layout (referred to as SVX3E). The continuation of this work would involve the University of Padova as well as LBNL, and possibly extend to the SVX2 chip used by D0.

7.1 Introduction

In recent years commercial foundries have been offering 0.25 μm feature size CMOS processes. It was widely expected that the thinner gate oxide inherent in the 0.25 μm feature size would allow for quantum tunneling of electrons, which would prevent build-up of trapped oxide charge- the main mechanism of radiation damage for larger feature CMOS devices. This opened the possibility to produce radiation tolerant devices at high volume, low cost foundries, without having to depend on a very few specialized Defense vendors. Much work has been done, in particular by the CERN RD-49 collaboration, to develop non-proprietary design rules and to test the performance of devices made in commercial 0.25 μm foundries. Test after test has consistently shown the radiation tolerance of these devices to be significantly higher than for any larger feature size process, including those offered by the Defense-related foundries used up to this point. The results are not specific to a particular vendor, and are so encouraging that it is practically certain that an integrated circuit fabricated in an 0.25μm line, using well-known design rules, will exhibit a high degree of radiation tolerance. On the other hand, the results are recent enough that no 0.25 μm device has yet been used in a particle physics detector.

It has rapidly become clear that 0.25 μm technology shows the best promise for future IC design work. However, the change has been so sudden that the generation of particle physics experiments presently under construction has not been designed with this technology in mind. A rapid conversion method, on the other hand, could allow many projects that are still in a chip design stage to capitalize on the new technology. With this in mind a proposal was made by the LBNL IC design group in April, 2000 to pursue a "direct conversion" of the SVX3 chip to 0.25 μm. The idea for this conversion is to recycle the SVX3D circuit schematics and layout geometry, relying heavily on simulation to verify adequate performance of such circuits when implemented in a 0.25 μm process and operated with 2.5V power supplies. This approach minimizes design work by using existing elements and capitalizes on the greatly improved accuracy of present-day simulations. Only when simulations show the performance of a particular circuit to be inadequate will a replacement circuit be designed. Because most circuits will not be designed from scratch to meet given specifications with 0.25 μm technology constraints, the specifications of the 0.25 μm version of the SVX3 chip will be determined after the fact, and will likely differ from those of the SVX3D chip. Physicist input is therefore very important to this conversion process, in order to assure that the end product meets Run 2b needs.

Between May and August, 2000, approximately 2 months FTE work has been carried out, without dedicated funds, in order to explore the feasibility of converting the existing SVX3 circuit to a 0.25 μm layout. From the work done so far the conclusion is that this approach is feasible and reasonable. The effort has centered on (1) simulation to understand the behavior of the SVX3 pre-amp, pipeline analog section and readout FIFO when using Taiwan Semiconductor Manufacturing Company (TSMC) 0.25 μm models at 2.5V operating voltage, and (2) design of an alternate pre-amp circuit to improve noise performance and dynamic range with 2.5V operating voltage.

7.2 Simulation Results

Simulations of the SVX3D preamplifier circuit in the TSMC process at 2.5V showed a performance that was not well suited for the needs of a Run 2b upgrade. A new preamplifier circuit was therefore designed to better match the Run 2b needs. Table 10 shows an abbreviated performance comparison between the new preamplifier design and the existing SVX3D chip circuit. The right two columns are from circuit simulation using the TSMC 0.25 μm transistor models. Effects of enclosed geometry for N-MOS transistors were included in an approximate way in the "New Circuit" simulation by using results measured for an IBM quarter micron process. In general it is possible to have better noise performance when going to smaller feature size because one can have a larger transconductance input transistor. The more impressive improvements in noise and dynamic range for the "New Circuit" have been achieved by using passive cascodes for both the load and input stages of the pre-amp (whereas the SVX3D circuit has active cascodes in both cases). The price for the improvement is lower charge collection efficiency, which is nevertheless adequate for the capacitive loads in question. Note that the new pre-amp circuit is "new" in the sense that it is different from the SVX3D circuit, but it is in fact a more standard circuit than the SVX3D pre-amp. The new pre-amp circuit uses the same configuration as the original SVX chip, the AToM chip used by BaBar, the APV25 0.25 μm chip, the front end chip for GLAST, and many others.

The SVX3D circuits for the pipeline analog sections were also simulated in TSMC at 2.5V. Unlike in the case of the pre-amp, the performance was more than adequate for a Run 2b chip. It was therefore decided to adopt the SVX3D pipeline analog circuits with no change. Figure 18 (top) shows the output of the SVX3 pipeline write amplifier circuit at 2.5V for different simulated input pulses (middle). The bottom plot shows the write amplifier reset waveform used (equivalent to the front end clock). This circuit performs well in the 0.25 μm simulation.

The simulation of the readout data FIFO is in progress. Preliminary results indicate that this circuit will perform properly and will not have to be re-designed.

7.3 Schedule and Cost

Table 11 is an estimate of the work that remains to be done for a full SVX3 conversion, in FTE. There is a significant amount of simulation work that can be carried out by physicists and students, and this has been broken out in the third column. Table 12 is an estimate of the extra work that would be needed in order to convert the SVX2 chip as well as the SVX3 chip, which is relatively small because many of the circuits in the SVX3 and SVX2 chips are the same.

There is some uncertainty in the time estimate due to lack of information about certain

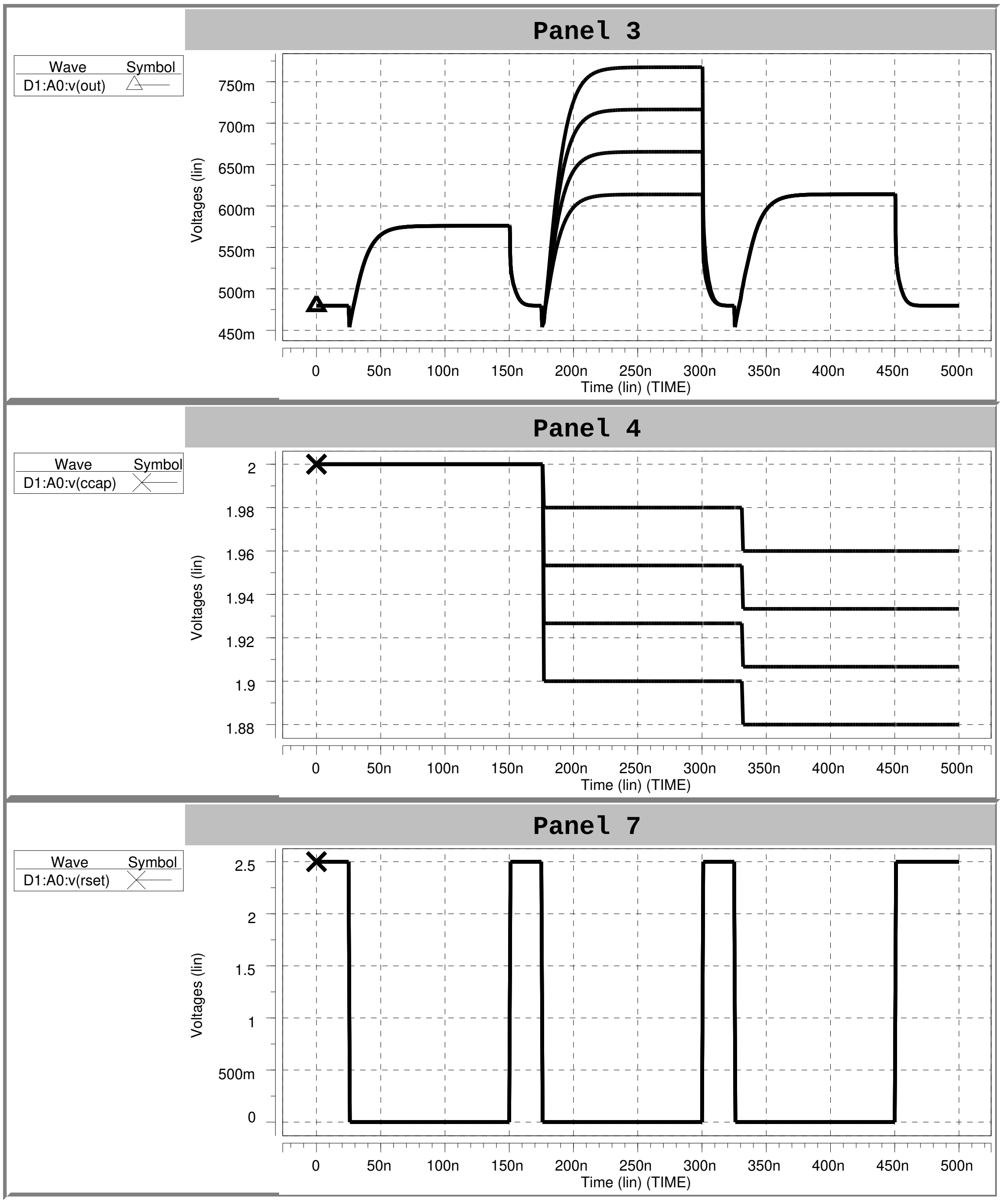

Figure 18: *Simulated waveforms for SVX3D pipeline write amplifier in TSMC at 2.5V.*

	SVX3D Chip	SVX3D circuit at 2.5V	New Circuit at 2.5V
Input Trans. Power	0.95 mW	1.5 mW	0.87 mW
Min. Rise-time (30pF)	75 ns	40 ns	30 ns
Dynamic Range	100 MIPs	30 MIPs	50-60 MIPs
ENC (30pF load)	2170 e^- (75ns rise-time)	1800 e^- (65ns rise-time)	1200 e^- (65ns rise-time)
Charge Collected at full rise-time (30pF load)	100%	(99 ± 1)%	(97 ± 1)%
Charge Collected at full rise-time (50pF load)	100%	(99 ± 1)%	(95 ± 1)%

Table 10: Abbreviated performance comparison between existing SVX3D chip (bench measurements), and 0.25 μm TSMC simulation of (center) the SVX3D pre-amp schematic, and (right) new pre-amp schematic. Rise-times are 0-90%. The "min. rise-time" is the fastest amplifier setting with the given power and load. For the equivalent noise charge measurement the rise-time is deliberately slowed: ideally all ENC values should be reported with the same rise-time, but for historical reasons exact matching data were not available. ENC typically decreases like the square root of the rise-time.

aspects of the conversion process. The vehicle to obtain this information would be a test chip MOSIS submission at the next available date, which is November 25, 2000. This is discussed in the next section.

The cost of labor will vary depending on how much simulation work is done by physicists and students. Taking $100/h for IC designer time (based on FY2001 LBNL labor on a reduced overhead account) the total labor cost (including SVX2) is given in table 13. The table has a high cost column (all work done by IC designers) and a low cost column, where some simulation work is done by physicists and students. Also shown in the table is a prototype wafer run of SVX3E and SVX2F chips. The combined cost for the run from TSMC would be $161,000. Finally, an additional 5 FTE months has been included under the assumption that the prototype run will not yield production quality chips, and further testing and layout modifications will be required. The grand total development cost, including an SVX2F chip for D0, but excluding fabrication of production chips, is between $0.5M and $0.65M.

7.4 Analog Test Chip

As mentioned in the introduction approximately 2 months FTE work has been carried out in order to explore the feasibility of converting the existing SVX3 circuit to a 0.25 μm layout. The culmination of this exploratory phase would be submission, through MOSIS, of a 0.25 μm analog test chip.

Task	Designer FTE	Physicist or Designer FTE
1.0 Preamp		
1.1 Simulation	0.25 months	0.25 months
1.2 Layout	1.0 months	
2.0 Pipeline - Analog		
2.1 Simulation	0.5 months	1.0 months
2.2 Layout	1.0 months	
3.0 Pipeline - Digital		
3.1 Simulation	1.0 months	1.0 months
3.2 Layout	1.0 months	
4.0 ADC - Analog		
4.1 Simulation	0.5 months	0.5 months
4.2 Layout	1.0 months	
5.0 ADC - Digital		
5.1 Simulation	0.75 months	1.25 months
5.2 Layout	1.0 months	
6.0 Interface		
6.1 Simulation	1.0 months	1.0 months
6.2 Layout	1.0 months	
7.0 Full Chip		
7.1 Layout V Schematic	1.0 months	
7.2 Design Rule Check	1.0 months	
7.3 Documentation	0.5 months	0.5 months
Total Labor	12.5 months	4.5 months

Table 11: Estimate of work remaining for full conversion of SVX3 chip to TSMC 0.25 μm

The issues to explore in a November 25 test chip submission would be:

1. Effect of enclosed geometry on input NMOS transistor characteristics- especially noise.
2. Level of flicker noise in NMOS devices for the TSMC process.
3. Reproducibility of metal-metal capacitors.
4. Viability of returning analog ground currents through the substrate.
5. Test of 5V-capable receivers for single ended signals (this would allow one to make a drop-in replacement for the SVX3 chip).

A preliminary footprint and pin-out for such a test chip is shown in Figure 19. It contains:

- 8 preamplifiers.
- 4 truncated pipeline analog sections.

Task	Designer FTE	Physicist or Designer FTE
1.0 Pipeline - Analog		
1.1 Simulation	0.25 months	
1.2 Layout	0.25 months	
2.0 Pipeline - Digital		
2.1 Simulation	0.5 months	1.0 months
2.2 Layout	1.0 months	
3.0 Interface		
3.1 Simulation	0.5 months	1.0 months
3.2 Layout	1.0 months	
4.0 Full Chip		
4.1 Layout V Schematic	1.0 months	
4.2 Design Rule Check	1.0 months	
4.3 Documentation	0.5 months	0.5 months
Total Labor	6.0 months	2.5 months

Table 12: Estimate of additional work for full conversion of SVX2 chip to TSMC 0.25 μm, assuming SVX3 conversion.

- 5 individual NMOS transistors.
- A shift register.
- 5V-capable receivers.

The MOSIS cost of this submission will be approximately $4,400 for 25 chips. About 2 Weeks FTE of designer time will be required for the layout, making the total cost of the analog test chip submission approximately $12,000.

Task	Cost Low	Cost High
Full Chip Layout	200,000	272,000
Extra Layout for Joint SVX3E+SVX2F Submission	96,000	136,000
Prototype Submission	161,000	161,000
Debug Prototype and Layout Changes	64,000	80,000
Total	521,000	649,000

Table 13: Breakdown of SVX3E development cost. Includes SVX2F 0.25 μm prototype for D0. Excludes cost of production run.

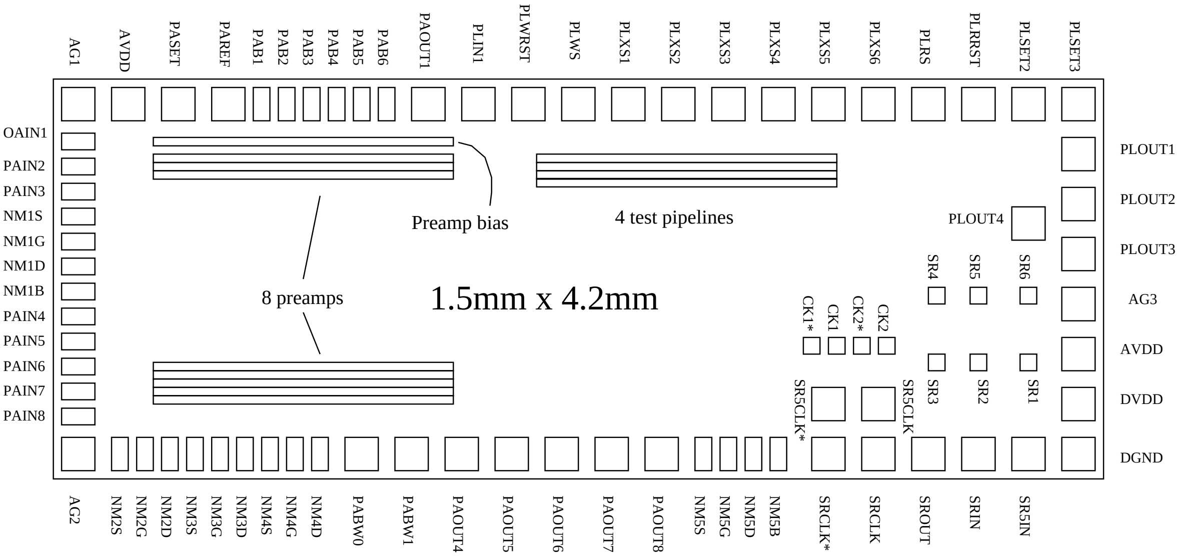

Figure 19: *Preliminary footprint and pin-out of 0.25 μm analog test chip.*

8 Hybrid concepts for the Run 2b Silicon Upgrade

The Run 2b upgrade may require a hybrid count which is as large as the present system. It is crucial that any new construction effort benefit substantially from recent large-scale production experience in order to be as efficient and rapid as possible. The main lessons/issues of the Run 2a project for hybrids were as follows:

1. There were 13 different hybrid designs each with its own flex cable. Assembly and test procedures, fixtures, and documentation had to be developed for each design.

2. The Honeywell SVX3D chips were not robust through assembly and a considerable amount of rework was required. The probability of a chip failing increased in proportion to the number of chips on the hybrid.

3. The SVX-II and ISL hybrids utilized a screen printed fine pitch conductor (4 mil line and 4 mil space) while for L00, the traces were finer (2 mil line and space) but were etched. Open lines were a problem for ISL and SVX-II and required rework while for L00 they were nearly non-existent.

4. For SVX-II, achieving the phi to z side contact was a big effort. The jumper structure required a lot of development and testing and also led to rework in a number of cases. In addition, placing the hybrid on the silicon necessitates two substrates, increases material, and complicates ladder assembly.

5. The ISL hybrid was double sided. Robust assembly methods which allow soldering and surface mounting on both sides were perfected and can be applied to a new Run 2b design.

6. In the course of the Run 2a construction a number of capabilities were acquired by CDF institutions including full test and burn-in setups, probing, and automatic gold ball bonding. These are being retained for use in a Run 2b project.

We propose to simplify any future construction in a number of ways.

1. Keep the number of hybrid designs to a minimum. a) Recycle the L00 design if possible. b) One double sided or perhaps a pair of single sided designs for the inner layers of an SVX-II replacement.. c) One universal double sided design for the outer layers ("Rod" modules).

2. Design the hybrids to hold a practical minimum number of chips. More hybrids with fewer chips is less work to build than having to rework units with too many chips.

3. Utilize the L00 etched conductor technology on all hybrids. This will also save material and money since the hybrids can be made considerably smaller. This technology is available for use on both Alumina and Beryllia. This gives us the option of lower material and high thermal conductivity if required.

4. With the hybrids off the silicon, front to back connections can be made either with double sided hybrids or with cabling.

5. Any Run 2b hybrid would be designed to be compatible with existing test and assembly capabilities.

A rough conceptual layout for a Run 2b hybrid is shown in Figure 20.

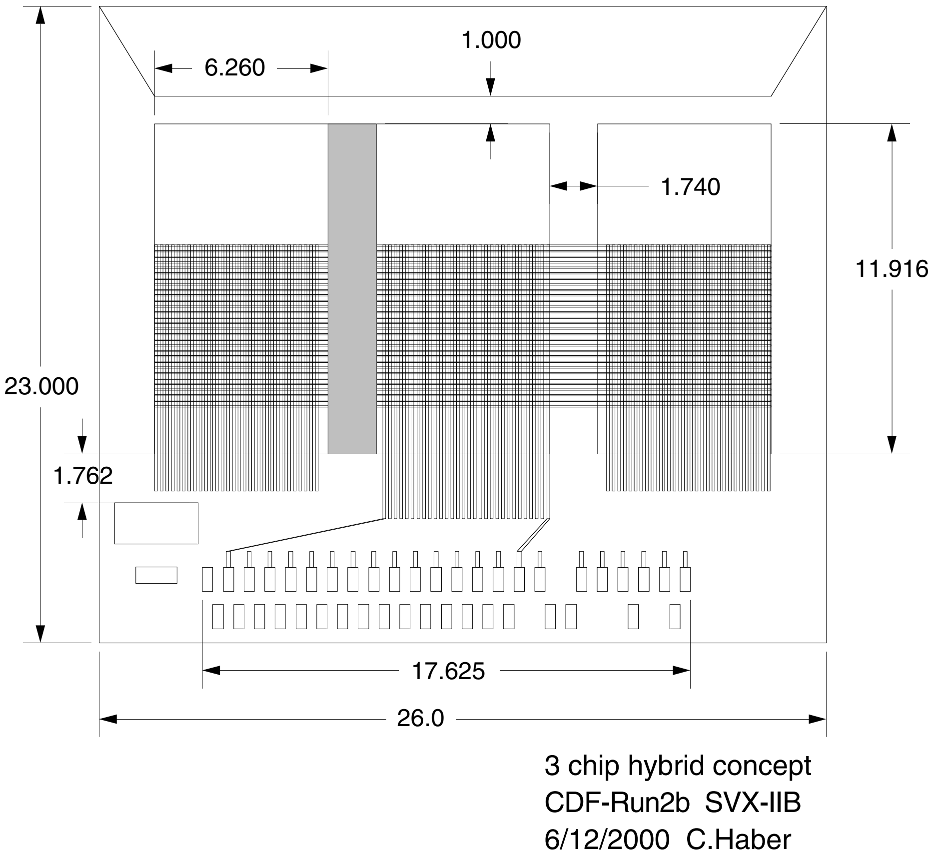

Figure 20: *SVX-II Inner layer replacement hybrid schematic (units are mm).*

9 Port Cards and on-Detector DAQ

9.1 Introduction

A strategy to upgrade and/or replace the port cards (PC) and other portions of Data Acquisition System (DAQ) between the hybrids and the crates outside the detector volume was developed by considering two Run 2b upgrade possibilities: recycle layers 3 and 4 of SVX-II, or replace all silicon inside ISL. As it turns out, the same scheme is preferred in both cases. We refer to it as the mini port card scheme (mini-PC for short). The following subsections first discuss the reasons for abandoning the idea of recycling the existing SVX-II port cards, and then describe the mini-PC scheme.

9.2 Recycling Existing Port Cards

We considered the possibility of recycling the port cards (PC) currently used on SVX-II. In the case that a quarter micron version of the SVX3 chip (SVX3E) is used for a Run 2b upgrade there would be compatibility problems, even though the controls, clocks and data of the SVX3E chip should match quite well the present SVX3D chip. These compatibility problems are:

- The single ended inputs to SVX3E would use 2.5V CMOS levels, whereas the single ended PC outputs and inputs use 5V CMOS. This problem may be partly addressed if an SVX3E chip can be made with 5V capable inputs (the Bottom Neighbor output would still be 2.5V CMOS), but this concept is not demonstrated at this time.
- The PC is designed to operate with 5.0V power. The SVX3E chip would require 2.5V power and a new scheme would need to be implemented to supply digital power to the SVX3E chips.
- The voltage regulators used for chip analog power were designed to regulate the voltage around 5.0V and 3.5V. They will not operate satisfactorily at 2.5V.

In the case that SVX-II layers 3 and 4 are recycled for Run 2b, trying to recycle the port cards as they are used on SVX-II would also present serious problems. The SVX-II PC controls five layers of silicon detectors and, hence, three of the connector sets would be left unused. This would leave an unnecessary amount of material in the detector volume, but would additionally force the use of a large number of off-detector DAQ modules to read out relatively few channels.

Radiation damage of the PC during Run 2a would also need to be addressed. While the Transceiver and Digital-to-analog-converter Decoder and Regulater (DDR) IC's are manufactured using Honeywell technology and should have negligible degradation, the transistors for the voltage regulators would be substantially damaged after Run 2a. Even if the transistors were replaced on every PC, the replacements would not survive the higher dose predicted for Run 2b. The DOIMs will also be substantially damaged. The DOIMs are employed to transmit the hit data optically from the PC to the DAQ system. They would have to be replaced by pin-compatible boards with Transceiver ICs, known as "copper DOIMS" (which would transmit data to the DAQ over copper lines rather than optically). Copper DOIMS have already been used for test purposes but would have to be made in production quantities.

9.3 The Mini-PC Scheme

The implementation of this scheme is very similar whether used to control recycled L3 and L4 ladders or an entirely new device based on an SVX3E quarter micron chip. The basic block diagram of the mini-PC scheme is depicted in Figure 21. It uses the approach already tested by the Intermediate Silicon Layer (ISL) detector to control the hybrids, where the PC is relatively far from the ladders and the communication between the PC and the hybrids is done using differential signals. In the mini-PC scheme a board known as the "junction-PC" is placed at the location presently used by the junction cards, and each junction-PC communicates differentially with several "mini-PC" boards either close to or integral with the hybrids.

The main advantages of this scheme are twofold: the junction-PC location is outside the tracking volume and hopefully in a place where the radiation dose is small. The junction-PC will encompass the functions of the present PC and Junction Card and could be manufactured using either a printed circuit board or thick film on alumina. The components can be mounted in chip size packages and commercial voltage regulators may be used. A cooling channel would pass under the junction-PC to remove the heat from the voltage regulators and the components. All high mass cables for power, control and data will arrive directly to the junction-PC and a low mass set of cables will interconnect the junction-PC with the mini-PC. The data will be transmitted from the junction-PC to the DAQ using copper ribbon cables and Transceiver chips. On the DAQ side the receiver DOIMs will be replaced by Transceivers.

Transceiver chips and copper lines are already used to transmit control signals from the FIB crates to the port cards, and there is confidence that the same scheme can be used to transmit data from the junction-PC to the FIB crates. TX chips transmitting data at 53 MWords/sec over 100 feet of copper ribbon cable have been tested for several months. A bit error rate of 4.3×10^{-16} was measured, which would translate to one error every 3.8 hours if all SVX-II ladders were transmitting data 100% of the time. Even with intentionally added environment noise the error rate was 3.4×10^{-15}, which is acceptable.

The mini-PC itself is a concept that could be implemented either as an independent board or as an integral part of hybrids, as in ISL. A mini-PC has just one Transceiver chip to adapt the differential signals to the single ended signals needed to control an SVX3D or SVX3E chip. A independent board would be preferable if a mini-PC is used to control more than one hybrid, and/or to simplify hybrid production in the case of multiple hybrid types.

A major objective of the mini-PC scheme is to avoid designing new DAQ chips. In this vein, the junction-PC will use existing designs: the Transceiver and the DDR. There are 403 DDR chips left over from Run 2a construction, whereas the number needed to reproduce the digital functionality of the SVX-II port cards would be 432 (including 20% spares). It is therefore very likely that a new DDR production will have to be purchased from Honeywell. We have observed an average yield better than 55% in two different DDR production runs, which gives us enough confidence that a new batch should not have the yield problems observed by the present SVX3D chip. Alternatively, if the radiation dose is small enough, we can explore solutions that avoid the use of rad-hard components. In this case the DDR could be replaced by a field programmable gate array and a digital to analog converter. In contrast to DDR chips, there are 4,300 tested Transceiver chips left over from Run 2a construction. Based on an estimated need of 72 junction-PCs (this is the number of port cards in SVX-II) serving 5 mini-PCs each, 1,600 Transceivers plus spares would be needed for Run 2b.

The mini-PC would also use the existing Transceiver chip, even in order to generate the 2.5V CMOS signals needed to control an SVX3E chip. The non-inverting half of each differential output of the Transceiver chip can be converted to a single ended 2.5V CMOS output by supplying 2.5V power to a dedicated driver current pin, and appropriately connecting ground or power to special pins that control the behavior of the differential outputs. Simulation of this Transceiver configuration shows a 7 ns 0-90% rise-time and 4 ns fall-time for single ended signals driving a 50pF load. This is fast enough for the single ended control signals, which for the most part have wide timing margins.

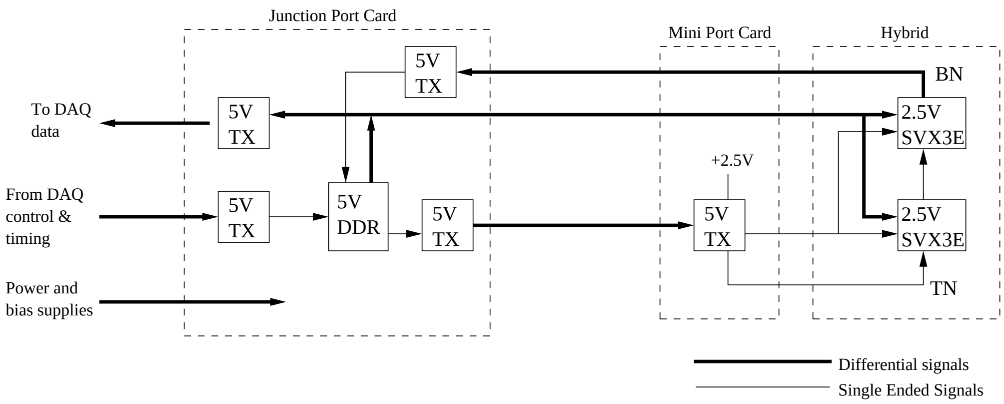

Figure 21: *Proposed "mini-PC" scheme for control and readout of Run 2b hybrids.*

There are several alternatives to using existing Transceivers on the mini-PC in case that capacitive loads are significantly larger than expected, or if there is some other unforeseen obstacle:

- Modify the Transceiver chip layout by increasing the current capability of the differential drivers and/or by adding a dedicated current supply pin to the single-ended drivers (so they too can be turned into 2.5V CMOS) and include this new Transceiver chip in a combined DDR-Transceiver Honeywell run. This would be the default action if a new DDR run is purchased and it requires a mask change. In this case one would get the new Transceiver version "for free".

- Use the 5V CMOS outputs of the Transceiver chip and add voltage dividers using printed resistors on the hybrid to divide the voltage before it connects to the SVX3E chip. The problem with this option is the added complexity of the hybrid with the associated penalty on yield.

- Add the voltage dividers directly into SVX3E chip such that the single-ended inputs are 5.0V compatible. The robustness of this option needs to be demonstrated and it may be challenging to prove that it will be reliable for the duration of Run 2b.

- Design and fabricate a quarter micron version of the Transceiver chip. This fall-back clearly involves the most work, but it may be desirable in the event that Transceiver chips need to be placed in the highest radiation areas. Even though Transceiver chips have not been tested to doses larger than about 1 MRad, based on the performance of digital circuits in the SVX3D chip they are expected to tolerate doses in excess of 10 MRads.

9.4 Cost

In the mini-PC scheme the total cost will be dominated by the required number of junction-PCs and mini-PCs, and hence can not be reliably estimated before a Run 2b detector design is established in some detail. Therefore, Table 9.4 gives a breakdown of cost for individual components, rather than totals. To estimate a range for the total cost we assume that the number of junction-PCs needed will be somewhere between half and twice the number of port cards used in SVX-II (72), with 5 mini-PCs per junction-PC, plus 20% spares. This places the total cost estimate between $325,000 and $830,000 (includes a DDR chip re-run with no mask changes in the higher number only). Note that the assumed number of junction-PCs and mini-PCs varies by a factor of four between these two limits. Depending on the upgrade design, the number actually required may turn out to be near the lower limit, for example if multiple hybrids are served by a single mini-PC, or near the upper limit, for example if occupancy and readout time simulations call for very fine segmentation.

In the case that L3 and L4 of SVX-II are recycled one can consider also recycling some SVX-II port cards, for use as junction-PCs, by adding ISL mezzanine cards (assuming enough DOIMs still operate well). The number of recycled port cards used as junction-PCs for L3 and L4 readout would be 36, which could potentially save $43,000 (including 20% spare factor). However, there would be some added cost for replacing damaged regulator transistors as well as surface mount components to meet the L3 and L4 current needs. Finally, this would place constraints of the mini-PC design that may make a universal mini-PC impractical.

Component	Fabrication and Assembly Unit Cost	Design and Prototyping Total Cost
Junction-PC	\$1,000	\$100,000
mini-PC	\$150	\$40,000
Cable j-PC to m-PC	\$150	\$20,000
Transceiver chip	\$0	\$0
DDR chip	(re-run cost) \$69,000	(if masks change) \$55,000
High M. PWR Cables	\$50	\$3,000
High M. Data Cables	\$140	\$10,000
FIB RX Card	\$30	\$3,000

Table 14: Estimated cost for on-detector DAQ components of the mini-PC scheme for Run 2b. The high mass power cable cost is for adaptor boards to re-use the existing cables.

10 Pixel Option for L00

10.1 Overview

An option exists to replace the CDF L00 silicon micro-strip detector with a pixel detector. This option makes use of advanced R&D by the LHC experiments and the BTeV experiment. The proposal is to form a single layer of pixels around the beam pipe using ATLAS-style sensors. The sensors will be bump-bonded to FPIX readout chips. ATLAS sensors are in production and the FPIX readout chip, developed at Fermilab, exists in an advanced third generation prototype. In fact, a prototype system (ATLAS-style sensors + FPIX chips) was successfully tested in a December 1999 test beam run at Fermilab using CDF SVX readout electronics (STAR+VRB). Position resolution better than 10 μm was demonstrated. The fact that R&D is far advanced makes the order of production chips and sensors in early FY2002 realistic and is a key to the feasibility that this project can be completed by 2004.

The proposed geometry includes 12 staves each 75 cm long and about 1 cm wide. The staves are arranged 12-fold in ϕ to form a long single barrel layer. A stave consists of 12 sensors laid end-to-end with each sensor read out by 8 FPIX chips. The detector comprises 144 sensors and 1152 readout chips. An individual pixel is small: 50 μm $\times$ 400 μm. In total, the detector contains 3.3 M channels.

The FPIX readout chip has an architecture that is different than the SVX3 silicon strip readout chip. The chip is organized into 18 columns of 160 rows. The FPIX chip makes use of the fact that multiple hits on the same pixel are exceedingly rare. Hence, hits are stored within each cell and logic controls the readout column-by-column. Each cell digitizes the charge collected (3-bit ADC) and holds onto a beam crossing number (BCO) that is associated with each hit. Every hit is read out. For the CDF pixel system, a new DAQ module, the pixel-FIB, would need to be designed to receive all the hit information into a deep memory. The module would then time order all the hits, associate the BCO with a Level 1 accept trigger signal, and provide the pixel information to a VRB for readout. A concept also exists that this module would combine pixel hits into effective strips and send this information to the SVT trigger module.

10.2 Physics Motivation and Tracking Performance

For a Standard Model Higgs discovery and for discovery of several types of SUSY signatures, b-tagging efficiency is very important. Pixels provide excellent position resolution (5-9 μm depending upon the incident track angle) in $r-\phi$. Fig. 22 shows the achieved resolution in the December 1999 test beam run. In addition, pixels provide several other attractive features. First, pixels provide fine segmentation in z that can be used to enhance pattern recognition. Second, pixels provide a precision z measurement that could have a resolution better than 400 μm$/\sqrt{12}$. Third, pixels are more tolerant to radiation ($\sim$ 30 Mrad $\equiv$ 30 fb^{-1}) and would require only the single installation even if the accelerator delivers luminosity exceeding current expectations of 15 fb^{-1}. Fourth, pixels have a signal-to-noise that is approximately a factor of 5 larger than with strips.

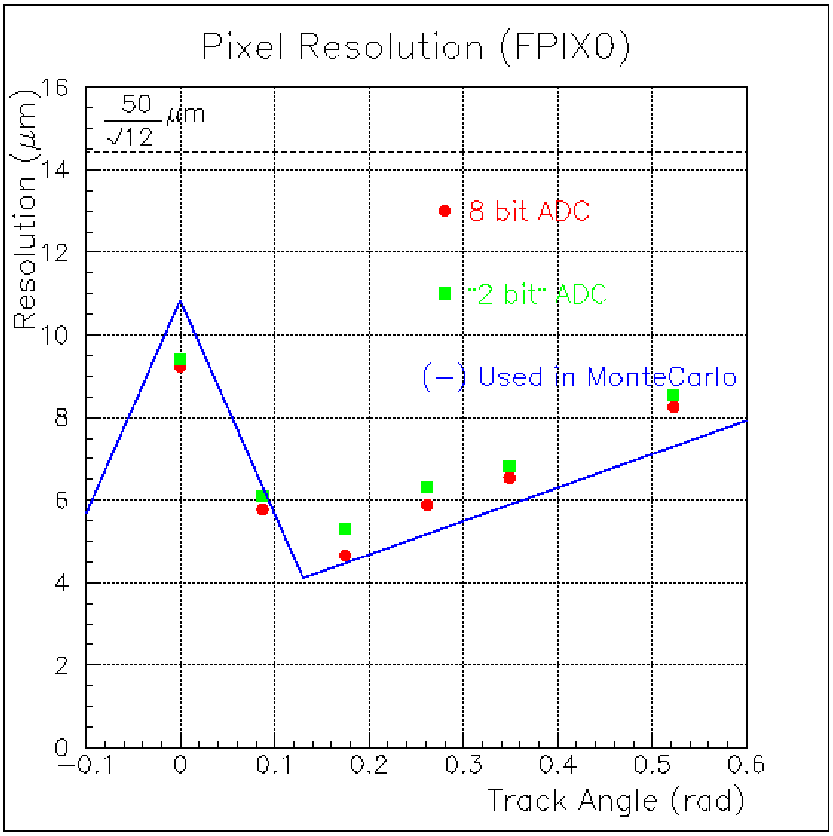

Figure 22: Position resolution of a prototype pixel system versus track angle. These results were obtained from data collected in a December 1999 test beam at Fermilab using prototype ATLAS-style pixel sensors and prototype FPIX readout chips.

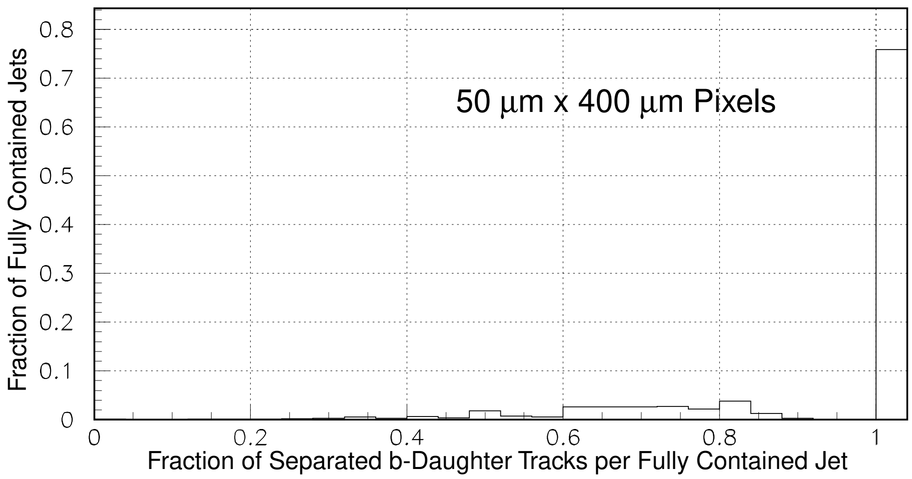

Figure 23: Normalized histogram of the fraction of tracks in fully contained b jets which are separated by a 15 mm radius cylinder of thin 50 μm $\times$ 400 μm pixels.

10.2.1 Track Separation and Pattern Recognition

In the dense cores of jets, the SVX detector and reconstruction algorithms are unable to resolve all tracks. This imposes a limitation on track reconstruction and the identification of secondary vertices in b jets, particularly in high p_T jets from top decay. The charge distributions from tracks in adjacent strips in $r - \phi$ will not be resolved even though the tracks may have z separations of the order of millimeters. The displacement of the charge centroid due to the second track causes measurement degradation in 20-30% of tracks in such jets and leads to spurious impact parameter measurements [43].

We have made a preliminary estimate of the potential for pixels in the innermost layer to cope with the density of tracks in high p_T b jets. PYTHIA [44] was used to simulate b jets from $t\bar{t}$ production at the Tevatron. Tracks from an average of three additional minimum bias interactions were also included with each event. Charged b daughters were selected in a cone of R < 0.4 about the direction of the b jet. The generated tracks were extrapolated through a thin cylindrical surface of 15 mm radius and 75 cm length which was either divided into $50 \times 400 \mu\text{m}^2$ pixels or $50\mu\text{m} \times 15\text{cm}$ strips. For pixels, a b daughter track was considered to have an overlap if another track passed through the same pixel or any of its eight neighbors. For strips, only the same or adjacent strips in $r - \phi$ were considered to be overlapping. Note that many of the b daughters we consider in this track density study would not fall within the η or p_T acceptance of the rest of CDF tracker. Also, the overlaps were purely geometric. Charge sharing with adjacent pixels or strips was not taken into account, nor was an attempt made to resolve overlapping tracks on the basis of deposited charge distributions.

Normalized histograms of the fraction of separated b daughters (those without overlaps) for jets fully contained in the cylinder are shown in Fig. 23 for the pixels and in Fig. 24 for the strips. All the tracks were separated by the pixel array in 76% of the jets, whereas for the strips, 32% of the jets had all tracks separated.

As a further comparison, Fig. 25 shows the fraction of fully contained b jets accepted in the pixels and in the strips for various cuts on the maximum fraction of tracks with overlaps.

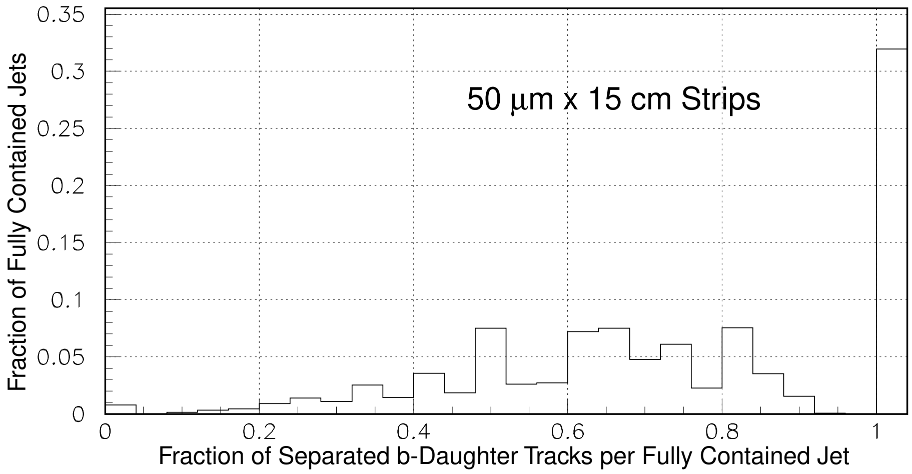

Figure 24: Normalized histogram of the fraction of tracks in fully contained b jets which are separated by a 15 mm radius cylinder of thin 50 μm $\times$ 15 cm strips.

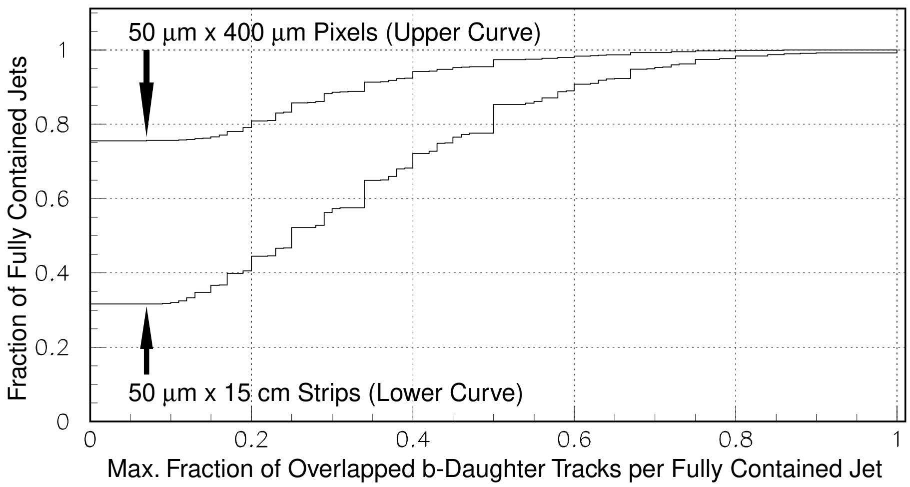

Figure 25: Fraction of jets accepted *vs.* the cut on the maximum fraction of overlapped tracks in fully contained b jets for a thin, 15 mm radius cylindrical surface of pixels (upper curve) or strips (lower curve).

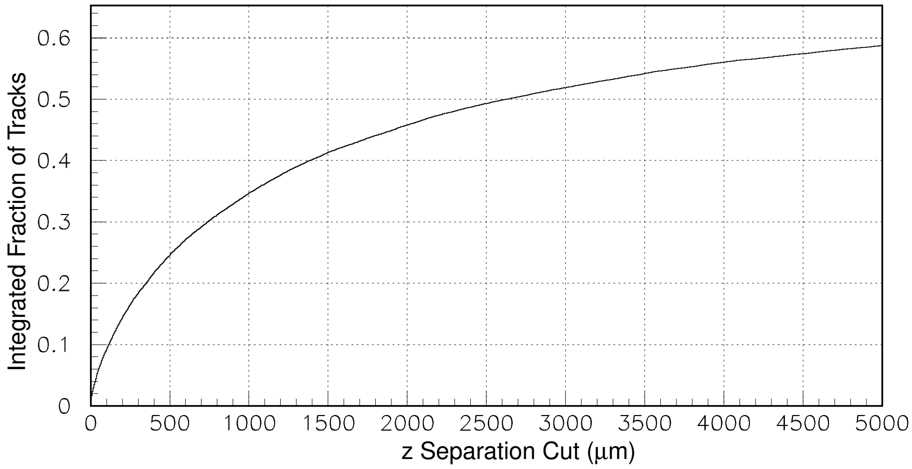

Figure 26: Integral distribution of b jet tracks with nearest overlapping track within the specified z separation cut.

A distribution was made of the distance in z to the closest potentially overlapping track (*i.e.,* within 100 μm in $r - \phi$) for charged b daughters. The integral of this distribution, Fig. 26, provides a measure of the effectiveness of the pixels to separate tracks in b jets as a function of pixel length.

This preliminary simulation shows the potential for pixels at the innermost radius to resolve a substantial number of b daughters in high p_T b jets which would overlap in a strip detector. Of course, the finite sensor thickness and proximity of the planar sensors to the beam will result in tracks depositing charge in some of the adjacent pixels. A more realistic simulation is being developed, taking into account the details of the charge deposition in the sensors and incorporating the pixels into the rest of the CDF tracking simulation. A clustering algorithm must also be developed to resolve nearby tracks and find the best estimate for the hit positions. Here, we can make use of similar work being done by the CMS and BTeV pixel groups who have succeeded in modeling test beam data in terms of cluster distributions.

10.2.2 Precision resolution in z

Pixels also provide a precision measurement in z that is not present with a single layer of L00 strips. The approximate resolution (no charge sharing in z) would be $400\ \mu\text{m}/\sqrt{12} = 115\ \mu$m. It is also possible to arrange the pixels in a “bricked” pattern such that those hits that are shared would have an approximate resolution that is better by a factor of two or 58 μm. The improvements in tracking with this added capability have not yet been fully quantified.

10.2.3 Radiation tolerance

There are large uncertainties in the actual dose expected at the L00 radius in Run 2a. An approximation is that 1 fb$^{-1} \equiv$ 1 Mrad. CMS style strips at L00 in Run 2a are expected to last for 10 fb^{-1} whereas ATLAS-style pixels are expected to last to 30 fb^{-1}. Both the design of the pixel sensor and the FPIX readout chip have been tested satisfactorily at radiation doses equivalent to 30 fb^{-1}. In short, at the L00 radius, the radiation environment is very similar to the LHC environment. Pixels are the best technology choice at this time for providing high precision tracking in such a high radiation environment.

10.2.4 Signal-to-noise

The signal due to the passage of an ionizing charged particle through either a strip or pixel sensor is approximately the same (20,000 e^-) and is proportional to the thickness of the sensor. Noise is usually dominated and proportional to the capacitance of the strip or the pixel. For a strip detector, a typical S:N $\sim$ 10:1 while a pixel detector has a typical S:N $\sim$ 50:1. Among other advantages, a large S:N aids in the precision of the $r - \phi$ measurement since better cluster centroid finding can be achieved. The limit of the $r - \phi$ resolution in pixels is dominated by the fluctuations in the Landau charge distributions rather than by noise or other factors.

10.3 Sensors

ATLAS has chosen pixel sensor technology that has achieved high performance out to about 30 Mrad of radiation dose. The 50 μm $\times$ 400 μm pixels are composed of n^+-type implants on n-type bulk with a p-spray isolation. A series of guard rings is also employed. The end result is a sensor that after type inversion and 30 Mrad of dose can use a 600 V bias to collect approximately 2/3 of the charge that is collected by an un-irradiated sensor.

The ATLAS experiment has selected two vendors (CiS and Tesla) to produce their needs of about 1000 wafers of sensors. Each ATLAS wafer contains three sensor tiles that are meant to be bump bonded to two rows of eight readout chips (16 chips total). The CDF pixel system would require about 50 wafers assuming a yield of 50% or 100-150 total wafers if sensors are shared between D0 and/or BTeV. Each wafer would contain six sensor tiles that are meant to be bump bonded to a single row of eight chips. It is reasonable that sensors with the ATLAS-style specifications could be ordered with a CDF-style geometry in the Fall of 2001.

The CDF University of New Mexico group leads the ATLAS pixel sensor development and testing. This group has facilities that will be available (with minimal impact on their ATLAS commitments) for sensor probing and module tests for acceptance and characterization.

10.4 FPIX readout chip and DAQ

The Fermilab rad hard vertex group has worked with the BTeV group and Ray Yarema's ASIC design group to develop a pixel readout chip that is suitable for use by experiments at the Tevatron. It is anticipated that a CDF pixel system could use a readout chip which is either identical to or only slightly different from the one being developed for BTeV. The current prototype version of the chip has a final design core (amplifiers and digitization for each pixel cell) already qualified in a deep submicron process (0.25 μm). Radiation testing at a Co-60 facility to 30 Mrads shows little or no degradation. A next prototype has been submitted at the end of September 2000 and contains a periphery that tests several options for communication between the pixel chip and the DAQ. This prototype also takes a big step towards final design by deriving all internal voltages off of a single supply voltage. The FPIX readout chip development has gone very well. In some sense, by choosing early to use a deep submicron process, the FPIX chip is more advanced than the LHC pixel readout chips. It is reasonable that production chips could also be ordered in the later part of 2001.

The FPIX chip has a different readout scheme compared with the SVX3 chip. In particular, pixel hits are stored within each pixel cell with a beam crossing number, BCO. Every hit gets read out with row and column information, the BCO, and 3 bits of digitized analog information. The concept is that the pixel detector will send all the data to a deep memory module that will sort pixel hits by BCO and will match L1 accepts with the correct BCO. The module will then provide pixel data to a VRB module for readout. A concept also exists for this module to combine pixel hits back into effective strips to provide data to the SVT with no hardware changes to the SVT. This deep memory module will also provide the control signals to the FPIX chip (it is equivalent to the FIB module). The deep memory/pixel-FIB would be a new module that would need to be developed. The control of the FPIX is simpler than SVX3 so the scale of producing this module is estimated to be equal to the scale for FIB development.

Various other aspects of the pixel DAQ including a pixel port card have been under development for BTeV studies within the same Fermilab ESE group that designed the SVX DAQ. The pixel port card would be expected to contain commercial optical drivers and would sit outside the tracking volume in a not-so-intense radiation environment. A HDI cable would connect FPIX chips on the sensors with the port card. Prototype components of this DAQ are currently under test by the ESE group.

A study has begun to examine the maximum pixel chip occupancy in busy top events in order to identify potential problems or DAQ limitations. In particular, the number of hits in a single pixel chip in busy $t\bar{t}$ events for the chip with the maximum number of hits is a figure of merit. Preliminary studies suggest the occupancy of the busiest chip is almost always below 2%. These hits should be able to be clocked out at 25 MHz (conservative estimate) in a total of 2.3 μs which is small compared with the 5.5 μs 42-deep 132 ns pipeline in the SVX3 chip. Our plans are not only to continue the occupancy studies but also to provide the output of the simulation into a Verilog model of the FPIX chip so that detailed timing issues can be predicted.

10.5 Bump Bonding

Hybridization, or flip-chip bump-bonding (the bonding of the sensor chip to the readout chips in a pixel detector), has been studied for some years by the UC Davis group and by ATLAS and BTeV. Three vendors have been qualified, or nearly qualified, to perform the hybridization for ATLAS. They are all in Europe. Their choice of technology is either that which uses indium for the bump material (two vendors) or Pb/Sn solder (one vendor). A fourth vendor, MCNC-Unitev, is in the U.S. and is under investigation by CMS and BTeV. This vendor uses Pb/Sn. In addition, UC Davis has facilities for the complete process of depositing indium bumps and bonding the chips to the sensors. They also are capable of carrying out the process for a single chip, something that is expensive and time-consuming

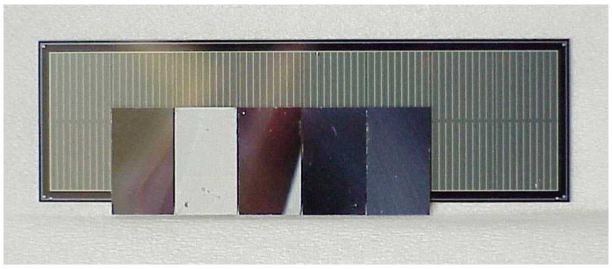

Figure 27: FPIX chips bonded to ATLAS sensor.

when done by commercial vendors, if one can be found that is willing to do it. Prototype chip development typically is done at the chip level, not the wafer level, so one has to be able to bond single die and sensor chips. UCD has done this for several users, most recently for the US CMS beam tests at CERN, as well for their own pixel beam tests at SLAC.

The costs of commercial hybridization are not yet well defined for the size of job represented by a Run 2b pixel upgrade. Cost estimates in 1998 for a set of pixel detectors with about 4,300 chips were roughly $350,000. Linear scaling to a smaller number of chips would not be valid, but sharing with BTeV, for example, could reduce the cost below that of an independent submission. Having UCD do the hybridization would very likely be the least expensive route, but no serious estimates of that cost and schedule have yet been made.

10.6 Mechanical Design, Cooling, and Material Budget

A pixel detector module for CDF would consist of an 8×64 mm^2 silicon sensor with 8 bump-bonded readout chips. A Kapton hybrid circuit would be attached to the top of the sensor to bus signals to and from the readouts via wire bonds. The wire bonds could be encapsulated to prevent damage by interconnecting cables. The pixel size would be 50 $\mu m \times 400$ μm.

Similar modules have been successfully constructed and tested in the Fermilab FPIX program using ATLAS sensors and FPIX readout chips. Fig. 28 shows 5 FPIX chips bump bonded to an ATLAS sensor, which is designed to be read out by 16 chips in two rows. As stated above, the CDF pixel modules would have one row of 8 chips. A test board is shown in Fig. 28. The readout chips are underneath the sensor with their bond pads extending beyond its edge. The Kapton flex circuit is also attached to the board in this prototype. At a later stage, the chips will be connected to a narrower flex circuit mounted on top of the sensor, as in the final design.

The mechanical support and cooling structure is based on the relatively mature ATLAS design. It consists of a barrel made of 12 "staves" holding 12 detector modules each. The active length of each stave is approximately 75 cm, which is shorter than the ATLAS staves (1 m). A cross section of a stave is shown schematically in Fig. 29. The stave includes a long carbon-carbon heat conducting bar to which the detector modules are attached. A thin-walled aluminum cooling pipe runs the length of the bar and is held in place by a carbon fiber-epoxy "omega" channel which provides rigidity. Thermally conductive grease is used to provide thermal contact between the aluminum tube and the carbon-carbon bar. The bar, omega channel and silicon detector module have similar CTEs. The CTE of the aluminum

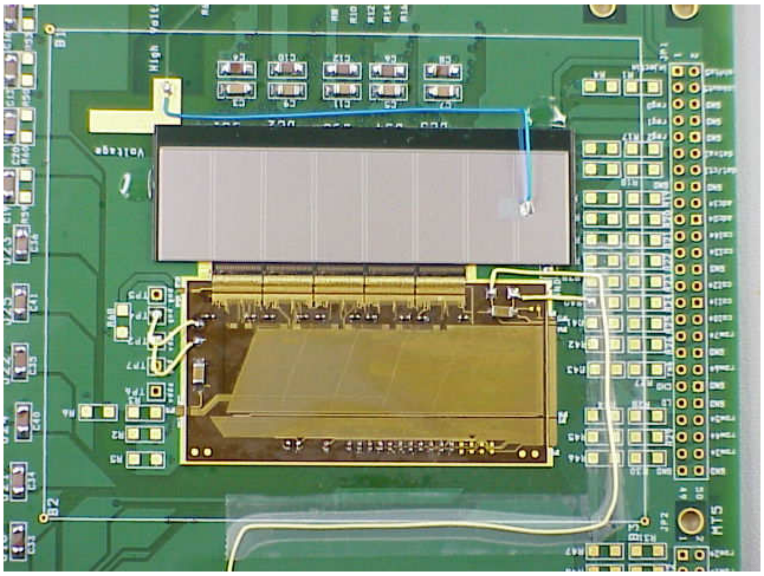

Figure 28: Detector test module with 5 chips wire-bonded to 5-layer flexible circuit.

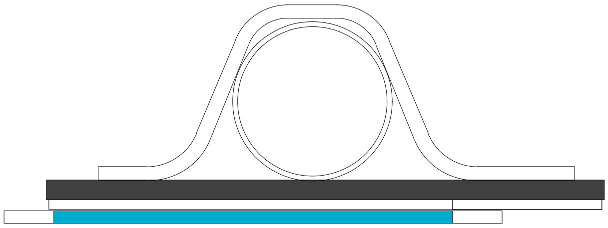

Figure 29: CDF pixel detector stave concept (cross section). The active area of the sensor is shown in color.

tube is sufficiently different that it must not be rigidly attached to the bar.

The ATLAS staves are supported at the ends and center by a carbon composite cylinder at a larger radius. In our case, we envision that the beam pipe would be used for support.

Two possible configurations of the staves to form a barrel layer (tilted or staggered) are shown schematically in Fig. 30 and Fig. 31, respectively. The 10° tilt partially compensates for the Lorentz angle of the charge carriers in the sensors. The tilted design also interposes less material on average between the beam pipe and the first sensor layer. The barrel staves must be positioned to avoid contact with the "flag" on the underside of the beam pipe.

The Kapton cables to connect the detector modules to the outside world are attached to the surface of the hybrid circuit and routed tangentially outward to the region outside the barrel layer where they make a right angle and proceed along the barrel next to the omega channel of the neighboring stave.

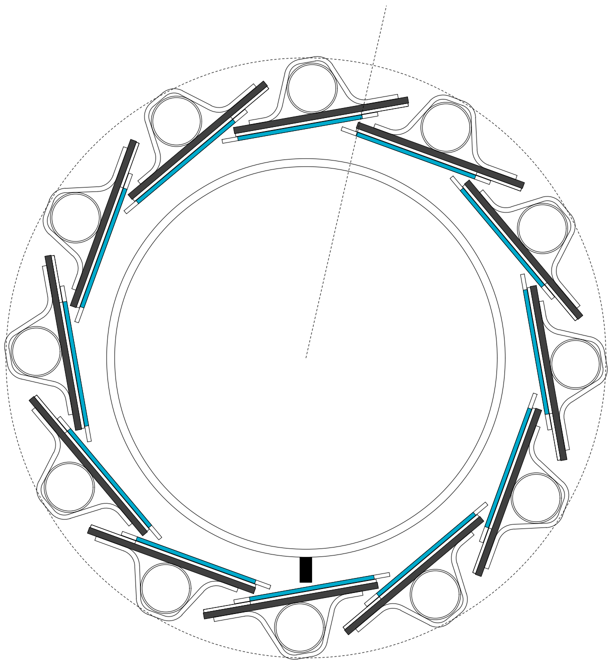

Figure 30: CDF tilted stave configuration (10° tilt).

10.6.1 Cooling

The power dissipation of the FPIX chips is quite high and an adequate cooling system is required to keep most of the pixel system at low temperatures. The core of the pixel chip generates 55 μW with about an additional 20% in the periphery expected. In short, the entire pixel detector is expected to generate 250 W. The ATLAS stave design assumes a somewhat higher power dissipation by area and uses twice as many chips per unit stave length. They found that 2 mm radius cooling tubes were sufficient for their design, which also includes other complexities in terms of the coolant and distribution. We are hopeful that a simpler design using cooling tubes not much larger than 1.5 mm in radius will be more than adequate. We are in the process of simulating our heat generation and cooling scheme to confirm these expectations.

10.6.2 Material Budget

An important design constraint for any precision tracker is to keep the amount of material in the active volume as low as possible. Material estimates for ATLAS and BTeV modules are 0.7% of a radiation length excluding cooling and support. For the ATLAS stave design, the material in a stave is estimated to be 1.59% of a radiation length. In our design, we use similar materials and thicknesses (including 250μm thick sensors and 200μm thick readout chips). However, our geometry has larger overlap between adjacent staves such that we expect the average over ϕ of our detector will be slightly thicker in terms of radiation length. In both the staggered and tilted geometries, you will notice that areas that have four thicknesses of silicon are in regions without cooling. Regions with the additional cooling material generally

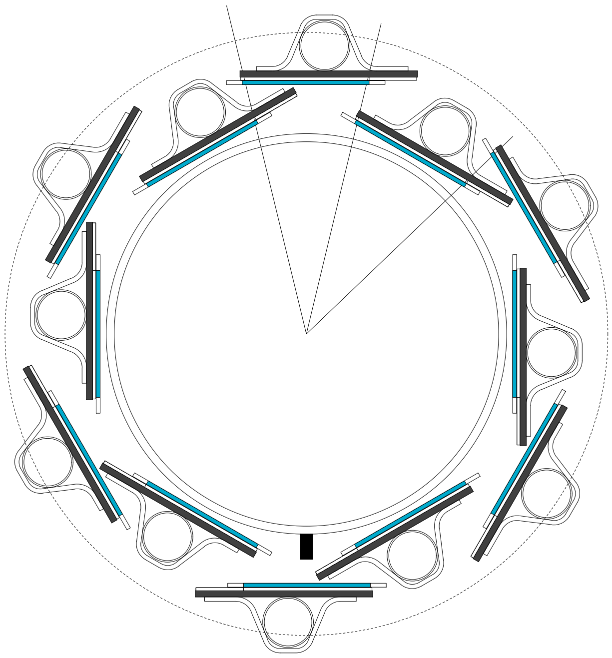

Figure 31: CDF staggered stave configuration.

have fewer layers of silicon. This design helps make the material distribution more uniform in ϕ. Fig. 32 shows a schematic of a quadrant of the pixel detector with eleven regions in ϕ shown. Tab. 15 lists the fractional area of each of the regions and the estimated effective thickness of various materials. The total average radiation length of 1.87% from this study is below an initial goal of keeping the material below 2.5% X_0. Other materials such as bonds, grease, and glue are not expected to contribute substantially. Possible overlapping of HDI cables has not been taken into account. Each HDI cable adds about 0.1% X_0 so that, at most, an additional 0.6% X_0 would be in front of the modules at the ends. An initial study shows that very little degradation in impact parameter occurs even if 2.5% X_0 material is compared with 1.5% X_0 of the current L00 design.

10.7 Resource and Cost Estimates

The resources and costs needed for completing this project are greatly reduced due to the substantial overlap with this project and BTeV's proposed 10% scale test. For this discussion, we assume that both this proposal and a 10% BTeV test are approved (D0 is also considering a pixel option that is nearly identical to this proposal). Table 16 shows our initial cost estimate. The amounts were mostly derived from the BTeV cost proposal and from CDF experience with its Run II silicon system. Contingency of 50% is assumed (30% contingency on sensors, readout chips, and pixel-FIB). In round numbers, the cost to CDF of this project (assume engineering costs are absorbed by FNAL and universities) would be \$1.5M (\$2M if there were no cost sharing with BTeV, and \$1M if CDF, D0, and BTeV all shared costs).

In particular, we make several assumptions. For the sensors, we use costing numbers based upon the ATLAS submission (the actual order costs are not public) of \$25K for setup

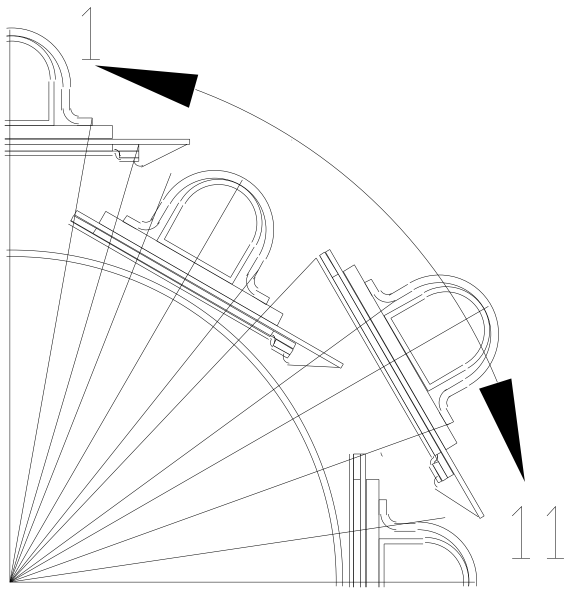

Figure 32: A quadrant of the pixel detector showing eleven regions in ϕ for which the amount of material has been estimated.

Region	%	Si	kapton	Cu	C fiber	Al	H_2O/Glycol	Alumina	X/X_0(%)	Tot.
$X_0(mm)$		93.6	284	14.3	220	89	361	72		
1	11.2	450	200	3	1000	400	2000	0	2.03	0.23
2	7.0	900	400	46	400	0	0	120	1.77	0.12
3	5.6	650	200	43	700	0	0	0	1.38	0.08
4	9.6	450	200	3	1000	400	2000	0	2.03	0.19
5	9.2	450	200	3	1000	400	2000	0	2.03	0.19
6	6.1	450	200	3	700	0	0	0	0.89	0.05
7	10.1	900	400	46	400	0	0	120	1.77	0.18
8	7.9	450	200	3	1000	400	2000	0	2.03	0.16
9	11.3	450	200	3	1000	400	2000	0	2.03	0.23
10	12.6	900	400	46	700	0	0	120	1.91	0.24
11	9.4	450	200	3	1000	400	2000	0	2.03	0.19
Total										1.87

Table 15: Material estimate for a pixel detector for CDF. Shown is the effective thickness of various materials (in μm) in eleven ϕ regions. The percent of a radiation length for each region is tabulated as well as the contribution of each region to the average of the total.

including masks and $1K per wafer in quantities of several 10's (BTeV production costs were $2.5K per wafer). For the FPIX chips, CDF would require about 10 wafers. BTeV would similarly require 10 wafers. These wafers cost $161K for the first ten and only $32K for each additional ten. These examples demonstrate the economy of scale if more than one pixel project overlaps. The bump bonding costs are derived again from BTeV's estimates based upon commercial costs and are substantial. As discussed above, UC Davis has bump bonding capabilities and could perform the production bump bonding. If the bonding is done at UC Davis, there could be cost and schedule savings; however, some funds would be required to provide support for necessary tooling and for technician labor. The construction of modules has been costed assuming that there is no overlap with the BTeV R&D. However, it is possible that for the BTeV 10% tests, these costs could have a high degree of overlap. Test stand and probe station costs are not included since a number of interested institutions already have those capabilities. Most of the other items have costs estimated either by similar items on the BTeV cost estimate or with other expert discussions. For example, the pixel-FIB costs are estimated to be equal to the SVX FIB modules per a discussion with the Fermilab ESE group.

Description	Quantity			Unit	Units	Cost	Cost w/
	Base	Spare	Total	($K)		($K)	contingency
Sensors NRE	0.5		0.5	25	each	12.5	16.3
Sensors	24	26	50	1	wafers	50.0	65.0
FPIX	1152	1700	2852	0.03	chips	96.0	124.8
Bump bonding	24	14	38	2.9	wafers	110.2	165.3
Module R&D	12		12	4	modules	48.0	72.0
Modules	144	84	228	0.58	modules	132.2	198.4
HDI cables	144	84	228	0.50	cable sets	114.0	171.0
Pixel port card	24	6	30	3	boards	90.0	135.0
High voltage	24		24	3	supplies	72.0	108.0
Low voltage	24		24	2	supplies	48.0	72.0
Monitoring	1		1	20	system	20.0	30.0
Interlocks	1		1	20	system	20.0	30.0
Pixel-Fib	24	6	30	5	boards	150.0	195.0
Opto-electronics	1152	348	1500	0.03	each	45.0	67.5
DAQ cables	24	6	30	1	bundles	30.0	45.0
Staves R&D	2		2	20	each	40.0	60.0
Staves	12	3	15	3	each	45.0	67.5
Stave support	1		1	20	system	20.0	30.0
Cooling manifold	1		1	20	system	20.0	30.0
Cooling system	1		1	20	system	20.0	30.0
Total						$1,178	$1,705

Table 16: Preliminary cost estimate for a pixel detector for CDF.

As far as personnel resources, sufficient resources exist with the Fermilab ASIC design and rad hard vertex groups to see that production sensors and readout chips could be ordered in the Fall of 2001. For the bump bonding, we are examining UC Davis' capabilities or we could follow the commercial lead that the BTeV group chooses to employ. For mechanical and cooling, we require the use of engineers and designers currently at SiDet beginning at the earliest possible time (approx. Jan. 2001). We hope university groups will also play a leading role in the mechanical design of this detector. Details on the FY01 needs can be found in a later section of this document.

This project makes use of the expertise of the Fermilab rad hard vertex group and various CDF institutions actively involved in either pixel or diamond work for the LHC experiments. DAQ and other hardware (HDIs and port cards) have also been made by CDF institutions in the past. We expect support from the Fermilab ESE group who has been involved both on the CDF and D0 silicon DAQ and the prototype pixel DAQ for BTeV.

While more complex detectors have been achieved in this short of a time period (SLD CCD detector, for instance), a pixel detector around the beam-pipe at CDF by 2004 requires an aggressive schedule that has little time for R&D. However, as the R&D has been done on many components, we believe the project is feasible. The proposed schedule is that production sensors and chips arrive by the end of 2001. Year 2001 will also be used to complete the mechanical and DAQ design. In 2002, testing sensors/chips followed by bump-bonding will result in the completion of modules by the end of 2002. Also in year 2002, fixturing and other materials will be ordered for the mechanical construction of staves and the detector. Prototype DAQ modules will also be ordered and debugged. Year 2003 will be devoted to constructing staves and assembly of the final detector including DAQ. The detector should be ready for installation in late 2003 or early 2004. A more detailed delineation of a schedule has been tabulated by D0 who arrived at the same conclusions on a detector completion date by 2004.

10.8 Conclusions and Feasibility

The key points of proposing a replacement for L00 micro-strips with a pixel detector are the following. First, pixels provide precision space points that extend our current capabilities by providing advantages in pattern recognition. Second, pixels are radiation hard at a level required for continuous high luminosity running (no second shutdown for another replacement). Third, a pixel detector at CDF makes use of expertise both at Fermilab within the rad hard vertex group, the ESE group, and SiDet; and makes use of expertise among CDF collaborators engaged in silicon and diamond pixel detector development for other projects. Fourth, the cost of this project to the laboratory is reduced due to the overlap with plans for continued pixel development at the Tevatron and the potential for outside groups to raise money for advanced detector development. A pixel detector is the best technology choice at small radius in the collider detectors and is achievable at a reasonable cost to the laboratory.

11 Schedule and Cost

11.1 Schedule for a full SVX-II/L00 replacement

The schedule was formed after considering the following constraints. At the far end we assume that the detector must be complete and ready to install in the ISL by early 2004. At the near end we assume that we need to design and produce readout chips in 0.25 μm technology. We assume that chip development will go into full swing very soon. We then assume that the preliminary chip design can be completed by the end of 2001 or early 2002, followed by an iteration to pre-production by Spring 2002 and a final design iteration to full production by end of 2002. In other words, we are assuming a full production schedule of $\sim$ 2 years. The early design stage assumes 3 submissions prior to the first pre-production ("engineering") run. This is comparable to the schedule we first received from the FNAL integrated circuit (IC) group and longer than the schedule considered by the LBNL IC group.

Not surprisingly, the critical path for the schedule starts with the chips. The chip schedule then puts hybrid fabrication on the critical path which in turn forces the module fabrication and final assembly to be time-critical. Figure 33 shows a first simple example of a full replacement schedule. The tasks which are not on critical path have been rolled up (no sub-tasks shown).[24] Note that for the mechanical components the schedule allots 600 working days. We believe this is adequate for the design and preparation of the support structures, rods, and module frames if we begin initial R&D in FY01. We can benefit from the extensive experience of the CERN and Pisa CMS engineering groups who would provide consultation.

Note also that final module production is scheduled over a period of 150 days. While this seems relatively short by Run 2a standards, it does in fact include a fair amount of contingency. The estimate is based on the ISL for which the assembly and wire-bonding times were each of order 1.5 hours per module. For simple single-sided module designs we expect even shorter fabrication times. In reality we will likely be paced by hybrid deliveries. Silicon deliveries will not be an issue for single sided sensors since there is enormous production capacity for these devices worldwide. We also expect the final assembly period to be short, (e.g. 90 days for rod installation). For the simple structural designs we are considering, this should be adequate.

In summary, we believe that a realistic schedule, for a full Run 2b silicon replacement is possible, provided that development of a new chip proceeds with all necessary support this year and that R&D for the mechanics, hybrids, and port-cards begins very soon, (no later than early 2001).

In addition to the schedule we have begun to analyze the costs of the various scenarios we have considered. While we do not have detailed estimates for all aspects of the various scenarios discussed in this document, we do have reasonably good estimates for many of the most important cost drivers. These include the front-end chips, silicon, port cards, and hybrids. The cost of module assembly is also reasonably well understood. The items which still need a bit more study are the Carbon fiber mechanical supports, Kapton cables, final assembly fixturing, and manpower. For these items we make estimates which we believe are conservative.

[24] The critical path appears in red when the schedule is displayed in color.

ID	WBS	Task Name	Start	Duration
1	**1**	**Run 2b Silicon Project**	**Wed 09/27/0C**	**845 days**
2	**1.1**	**Electronics and DAQ**	**Wed 09/27/0C**	**710 days**
3	**1.1.1**	**Front end Chip**	**Wed 09/27/0C**	**560 days**
4	1.1.1.1	Initial design	Wed 09/27/0C	320 days
5	1.1.1.2	pre-production chips	Wed 12/19/01	90 days
6	1.1.1.3	production chips	Wed 04/24/02	150 days
7	**1.1.2**	**Portcards**	**Wed 09/27/0C**	**450 days**
11	**1.1.3**	**Hybrids**	**Wed 09/27/0C**	**710 days**
12	1.1.3.1	Hybrid Initial design	Wed 09/27/0C	150 days
13	1.1.3.2	Hybrid Prototypes	Wed 04/25/01	150 days
14	1.1.3.3	Hybrid Pre-production	Wed 04/24/02	120 days
15	1.1.3.4	Hybrid Production	Wed 11/20/02	150 days
16	**1.1.4**	**Signal Cables**	**Wed 09/27/0C**	**473 days**
21	**1.2**	**Mechanics**	**Wed 09/27/0C**	**600 days**
22	**1.2.1**	**Support Structures**	**Wed 09/27/0C**	**600 days**
27	**1.2.2**	**Frames**	**Wed 09/27/0C**	**540 days**
32	**1.2.3**	**Rods**	**Wed 09/27/0C**	**600 days**
37	**1.3**	**Cooling and Interlocks**	**Wed 09/27/0C**	**540 days**
48	**1.4**	**Silicon**	**Wed 09/27/0C**	**540 days**
53	**1.5**	**Module Production**	**Wed 08/29/01**	**500 days**
54	1.5.1	Module Prototypes	Wed 08/29/01	120 days
55	1.5.2	Module Pre-production	Wed 04/24/02	120 days
56	1.5.3	Module Production	Wed 01/01/03	150 days
57	**1.6**	**Module Final Asembly**	**Wed 07/31/02**	**365 days**
58	1.6.1	Support Structure Assembly	Wed 07/31/02	140 days
59	1.6.2	Support Alignment	Wed 02/12/03	40 days
60	1.6.3	Installation of Modules on rods/shells	Wed 01/08/03	150 days
61	1.6.4	Installation of rods/shells	Wed 05/14/03	90 days
62	1.6.5	Installation of portcards	Wed 09/17/03	30 days
63	1.6.6	Final system testing	Wed 10/29/03	20 days
64	1.6.5	Install Screen	Wed 11/26/03	20 days

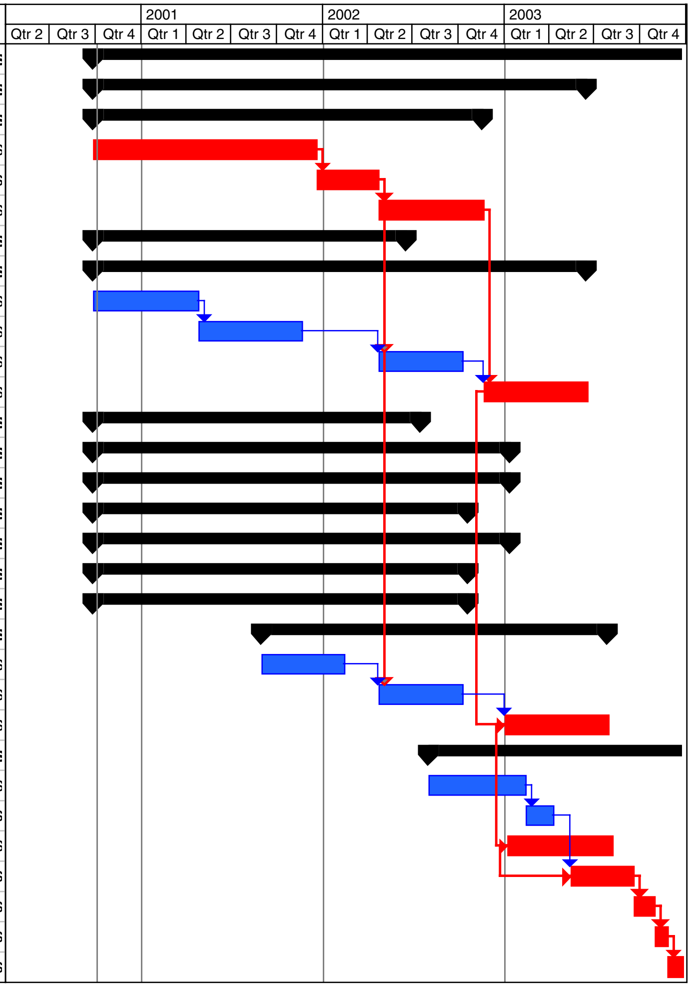

Figure 33: *An example of a Run 2b full replacement project schedule.*

Item	Estimated Cost (k$)	Contingency	Total Costs
SVX3 Chips	-	-	-
Silicon (100+100)	64	12	76
Fine-pitch Cables	50	20	70
Hybrids & Pig-tails	60	15	75
Supports & Cooling	10	5	15
Total M&S	184	52	236
Tech. Labor (FTE-years)	1.5	0.5	2.0

Table 17: Costs involved in making a replica of L00.

The purpose of our R&D program in FY01 would be to refine the technical and cost details of the various scenarios we have presented as well as to start the development of long lead time items. The goal is to be prepared to launch into the right upgrade program for CDF in FY02. This plan allows us to take into account early Run 2 data that will help us to clarify longevity and performance issues of the Run 2a silicon. In the next section of this note we present an estimate of the resources we will need in FY01 for this R&D program to be successful.

11.2 L00 replacement cost

We have discussed replacement of L00 with either a strip system or a pixel layer. The cost for an exact replica of L00 can be estimated reliably based upon our current experience. Some of the most difficult and costly portions of the L00 project were the development of the fixtures and the carbon fiber supports. These costs would be essentially absent for an exact replacement. Similarly there would be no new DAQ or power supply needs. Costs are presented in Table 17. Note that these are likely to be conservative for several reasons. We may have enough remaining narrow silicon to only need to buy wide silicon. This would reduce the sensor cost by 40% relative to that shown. We have assumed that there are enough readout chips remaining from Run 2a. The first batch of fine-pitch cables were made by CERN for a cost of roughly 25 k$ and it may be possible to have CERN make a new set for CDF.[25] Hence the total estimated cost of 296 k$ is conservative and less than 40% of the cost of the original L00.

For a pixel system, the costs are estimated in Table 16. It is of course not possible to estimate these as reliably as for a replica L00 system.

11.3 Full SVX-II replacement cost

The cost estimates for a full SVX-II replacement are presented in Table 18. The estimates for the SVX 0.25 μm chip development assumes 2 FTE engineers for 2 full years. It also assumes

[25] The cost to make these commercially in the US would be $\sim$ 150 k$. We are currently qualifying a Japanese company for new cable production. The cost for this vendor is not yet known but is anticipated to be much lower than the US vendor.

Item	Estimated Cost k$	Contingency	Total Costs
0.25 μm Chip submissions	300	150	450
Silicon	800	300	1,100
Fine-pitch Cables	200	200	400
Hybrids & Pig-tails	600	200	800
Power Supplies	200	100	300
Port cards	500	350	850
Mechanics & Cooling	400	400	800
Be beam pipe	150	50	200
Total M&S	3,150	1,750	4,900
IC Engineers (FTE-years)	2.5	1.5	4.0
Mech. Engineers	6.0	3.0	9.0
Module Labor	8.0	4.0	12.0
Final Assembly Labor	4.0	2.0	6.0

Table 18: Costs involved in making a full SVX-II replacement.

3 test submissions, a large scale engineering submission, and a final production submission. This estimate is reasonable but will soon be superseded by a more refined estimate which we expect to be one of the outcomes of an upcoming meeting of FNAL, LBNL, and Padova engineers to be held at FNAL. The cost for the silicon is based upon budgetary quotations received from Hamamatsu Photonics [39]. The cost of the fine pitch cables is based upon our experience with L00 and takes into account the fact that fine pitch cables on the innermost layers of an SVX-II replacement can have wider pitch and traces which will drive down costs considerably.

For hybrids we are assuming a unit cost of 1k$ including contingency. This is conservative when compared to Run 2a ISL hybrid costs especially upon consideration of the fact that we expect the Run 2b hybrids to be more simple and robust. For power supplies we have assumed that the innermost two layers of the SVX-II replacement will require higher bias voltage supplies similar to those used in L00. The L00 power supply unit cost was assumed. The port-card cost is based upon that presented in the port-card section earlier in this note. Since the exact scheme is unknown we have used the median cost with contingency large enough to cover the uppermost cost estimate. For mechanics and cooling we have assumed a total cost of 400 k$ and 100% contingency for the production of carbon fiber support cylinders, end-caps, rods and frames. This cost is the least well understood at this time and one which we hope to resolve better in our R&D efforts in FY01. Finally, to save shutdown time, we would purchase a new Be beam-pipe. The cost for the Run 2a beam-pipe was roughly 150 k$. We suspect the price could go up for a future order so we add 50 k$ in contingency. Altogether we come up with an M& S cost of 4.9M$ of which 3.15M$ is the base cost with a contingency of 56%.

For labor we have assumed a substantial amount of mechanical engineering. Technical labor is based on the assumption that all modules are assembled manually. For these we base our unit labor estimates on the time required to build ISL modules. The final assembly will be simple as a result of the adoption of the CMS rod and wheel concepts but we have nevertheless assigned substantial technical support to this task.

Combined with the cost of a L00 replica, we thus estimate the total M&S cost to replace all of the CDF silicon except the ISL at 5.1 M$ with contingency. We believe that these cost estimates are conservative and true costs could be significantly lower for several reasons, as mentioned above. In addition such things as automated module assembly systems similar to those used by CMS may be used and would drive down the module assembly labor. The chip development may need fewer submissions and less design effort may be required if a direct translation is feasible. More robust chips would dramatically reduce the rework rate for hybrids. Also, more robust and simple hybrid designs will likely result in significantly lower costs than those presented. Finally, the mechanical support designs may be greatly facilitated by consultation with CMS engineers who have already resolved many of the key issues involved.

A portion of the M&S costs would be funded by CDF collaborators.

11.4 Partial SVX-II replacement cost

For a partial SVX-II replacement there are a number of new items that must be purchased. For instance, spare ladders would have to be made to replace those outer layer ladders that are damaged in disassembly of Run 2a SVX-II barrels. One of the original vendors of our double-sided silicon now only makes single sided silicon. As a result, we would have to remake masks and purchase new double sided silicon at higher cost than single sided silicon. New inner layer ladders would have to be made from either new single sided silicon or new double sided silicon. To minimize the shutdown period additional bulkheads would be needed. Finally, new port-cards, hybrids, and power supplies would also be necessary. Since we need to keep the shutdown time to the absolute minimum, a significant amount of additional fixturing and labor would be required to disassemble and reassemble 3 barrels in parallel. A very preliminary estimate of the cost of this scenario is presented in Table 19. The total M&S cost is seen to be of order 1M$ less than that of the full replacement scenario, which however has one more silicon layer at large radius. The partial replacement cost table also does not include the cost for new CMM's for barrel assembly stations. Also note that the technical labor required for this scenario would very likely be greater than in the complete replacement scenario while the engineering would likely be less.

Item	Estimated Cost k$	Contingency	Total Costs
Chip submissions	300	150	450
Silicon	700	350	1,050
Hybrids & Pig-tails	300	150	450
Fine-pitch Cables	200	200	400
Power Supplies	200	100	300
Port cards	350	175	525
Mechanics & Cooling	350	175	525
Be beam pipe	150	50	200
Assembly fixtures	100	50	150
Total M&S	2650	1,400	4,050
IC Engineers (FTE-years)	2.5	1.5	4.0
Mech. Engineers	4.0	2.0	6.0
Module Labor	11.0	6.0	17.0
Final Assembly Labor	6.0	3.0	9.0

Table 19: Costs involved in making a partial SVX-II replacement.

12 Proposal for a program of R&D in FY01

12.1 Micro-strip detector R&D

As mentioned above, we have identified several items which need to start development work in FY01. The most important of these is the front-end chip. The main costs in FY01 would be for engineering and designer manpower. To obtain a preliminary estimate for these costs we assume a flat manpower profile over the entire two year project duration and also assume that the engineering and production submissions would occur after FY01. The latter are estimated at $\sim$ 160 k$ each, implying an FY01 M&S cost, including contingency of order 90 k$.

The other DAQ related R&D items we need to start in FY01 are prototypes of hybrids and port-cards. Figure 34 details the cost of hybrid prototypes. For port-card work we estimate 20k$ in materials and 0.5 FTE for an engineer and a technician. For the initial design and prototyping of modules, the cost would be fairly modest. We estimate that we would need 0.5 FTE engineer, roughly 0.5 FTE technician and of order 20 k$ for materials and machining of fixtures. For rods, cylinders, end-caps and cooling we would require 1 FTE engineer, 0.5 FTE designer and 1 FTE technician. Material and fixture costs would be higher than for modules. We estimate that we would need of order 100 k$ to produce molds and assembly fixtures for Carbon fiber supports and to have water-jet cutting performed commercially.

The resources required for an effective micro-strip replacement R&D program in FY01 are presented in Table 20.

1	Hybrid Prototypes	num	materials	mat total	labor	labor-cost
1.1	substrate					
1.1.1	BeO blanks	30	$75.00	$2,250		
1.1.2	laser machining	30	$10.00	$300		
1.2	thick film					
1.2.1	CAD	1			200	$9,050.00
1.2.2	NRE	1	$4,500.00	$4,500		
1.2.3	printing	25	$650.00	$16,250		
1.2.4	laser machining	1	$550.00	$550		
1.3	fanouts					
1.3.1	CAD	1			8	$362.00
1.3.2	mask	1	$1,500.00	$1,500		
1.3.3	fabrication	50	$125.00	$6,250		
1.3.4	dicing	75	$5.00	$375		
1.4	cables					
1.4.1	CAD	1			30	$1,357.50
1.4.2	NRE	1	$990.00	$990		
1.4.3	parts	25	$100.00	$2,500		
1.5	components					
1.5.1	discretes	1	$300.00	$300		
1.5.2	connectors	100	$4.00	$400		
1.6	assembly					
1.6.1	surface mount	25	$75.00	$1,875		
1.6.2	fixture	1			35	$1,609.30
1.6.3	bond chips	25	$75.00	$1,875		
1.6.4	fixture	1			35	$1,609.30
1.6.5	misc assy,QC				35	$1,609.30
1.7	test					
1.71	misc fixtures	1			35	$1,609.30
1.72	misc components	1	$1,500.00			
				$39,915		$15,597.40
	CAD rate		$45.25			
	shops rate		$45.98			
	student rate		$13.80			
	Total FY01			$55,512		

Figure 34: *Cost of prototyping Run 2b hybrids in FY01.*

Item	Estimated Cost k$	Contingency	Total Costs
FE Chips submissions	60	30	90
Hybrids (LBNL)	55	25	80
Port cards	20	10	30
Module Mechanics	20	10	30
Support Mechanics & Cooling	100	50	150
Total M&S	255	125	380
IC Engineers (FTE-years)	1.5	0.5	2.0
Port-card Engineering	0.5	0.25	0.75
Technicians	2.0	1.0	3.0
Mech. Engineering	1.5	0.75	2.25

Table 20: Resources required for micro-strip R&D in FY01.

12.2 FY01 R&D needs for pixels

In this section, we spell out R&D needs for FY01 for the option to replace L00 with a pixel detector. These needs reflect a constraint on available financial resources; however, they are sufficient provided that activities lead towards the beginning of fabrication in FY02. We first provide an overview of our requirements for personnel and financial resources. We then provide details of what we wish to accomplish in FY01 for CDF pixel electronics and mechanics. Note that many of the FY01 activities on electronics overlap with planned activities by the Fermilab rad hard vertex, ESE, and ASIC design groups. The costs for a pixel R&D program in FY01 is summarized in Table 21.

12.2.1 Personnel needs

We need two mechanical engineers/senior technicians at a level of 25-50%. Presumably these engineers would be located at SiDet. One engineer would oversee conceptual design and mock-up of the larger scale system (mounting on the beam pipe, cable and cooling routing etc.). The other engineer would help coordinate the design of the carbon fiber supports and cooling structures. Resources equivalent to one FTE technician would be required for making prototypes. Designer/drafter support at the level of one FTE is also required. We assume that periodic support from other personnel at SiDet would be available.

For electronics, we require a small amount of support from the Fermilab ESE and ASIC design groups. We believe that activities during FY01 will overlap substantially with BTeV activities so that no additional personnel will be required. CDF physicist involvement in these activities will allow these groups to increase their current FY01 plans to allow for both BTeV and CDF specific work.

Item	Estimated Cost k$	Contingency	Total Costs
DAQ Test stand	15	7.5	22.5
System Mechanics	20	10	30
Staves prototypes	20	10	30
Cooling	15	7.5	22.5
Total M&S	70	35	105
Mech. Engineering (FTE)	1.0	0.5	1.5
ESE	0.5	0.25	0.75
Design	1.0	0.5	1.5
Technician	1.0	0.5	1.5

Table 21: Resources required for Pixel R&D in FY01.

12.2.2 Financial needs

We would need a total of $70K before contingency for the following purposes. For both the FPIX readout chip and for ATLAS-style sensors, we require no additional funds in FY01 (if CDF cannot use the BTeV chip, a CDF specific FPIX prototype would cost $37.5K – this is not expected to be needed). For a CDF pixel DAQ test stand, we need $15K for modifying a SVX test stand into a pixel test stand. These funds would also be used to purchase prototype electronic components that are CDF specific. For system level mechanical design, we would need $20K for the components necessary for a system mock-up and other R&D needed to qualify certain materials and technology choices. We would need $20K to produce prototypes of carbon support and cooling structures. This includes fixtures and materials for producing the carbon elements. We'd need up to $15K for materials and equipment used in cooling tests.

12.2.3 Electronics

FPIX chip: We require no additional FNAL resources. CDF will benefit from FPIX prototype submissions and studies carried out by the rad-hard vertex, ESE, and the ASIC design groups. Final decisions on the exact nature of the periphery will be made and tested in these prototypes. There will also be radiation testing of prototype devices to check for resistance to single event upset and single event gate rupture effects. These tests will lead to the final specifications of the FPIX chip. The FPIX road-map is such that a full size chip should be ready for submission in early FY02. This chip could be the production chip; but, the schedule allows for a standard sequence of a preproduction run followed by a production run. In addition, planned R&D in FY01 includes establishing wafer scale testing procedures at Fermilab. By the end of FY01, we should have a prototype FPIX chip in hand that would need only minor changes before the production order can be placed.

Sensors: We require no additional FNAL resources. CDF will benefit from resources earmarked for BTeV to produce prototype sensors. Engineering and CAD work will be done either at FNAL or at a university to transform ATLAS GDS files into CDF sensor designs.

The University of New Mexico will provide assistance especially if the "bricked" pixel option is chosen as they have produced prototypes in the past. UNM will also be establishing testing and characterization facilities for the sensors. By the end of FY01, we should have the final design of the sensor ready in appropriate GDS files. The layout of sensors on wafers will be specified if wafers are shared between CDF and BTeV and D0. Early in FY02, production sensors should be able to be ordered.

Bump bonding: We require no additional FNAL resources. UC Davis will be available for prototype bump bonding activities as they have done for other efforts in the past. In FY01, UC Davis will determine whether they wish to be considered for doing the production scale bump bonding for this project. Other FY01 activities include the evaluation and reliability tests of commercial bump bonding with thinned FPIX devices. Prototype modules (discussed below) will also be constructed and will test bump bonding. By the end of FY01, we should have determined the preferred methods for bump bonding readout chips to sensors.

HDI cable: We require no additional FNAL resources. On-going BTeV studies include the evaluation of HDI cables. CDF Run 2b silicon strips also require specialized fine pitch HDI cables. By the end of FY01, preferred vendors should be selected and prototypes evaluated with near final specifications determined.

Modules: We require no additional FNAL resources. BTeV activities include the construction of prototype "stacks," several FPIX1 readout chips bump-bonded to a prototype sensor with a wire-bonded HDI. By the end of FY01, the module concept will have been completely prototyped.

Pixel port card (CDF specific): We require minimal additional FNAL resources. BTeV activities include the evaluation of various options for driving FPIX signals and controls between the DAQ and pixel detector. Specifications of this board will be driven by the final design choices of the periphery of the FPIX chip. It is thought that the same concepts for a similar BTeV component will be shared with the CDF pixel port card, but some tests may be necessary to be carried out for CDF specific issues. By the end of FY01, concepts to be used on the port card should have been tested such that prototypes can follow in FY02.

Pixel-FIB (CDF specific): We require minimal additional FNAL resources. This board is thought to be similar in scope to the Run II FIB module. The Fermilab ESE group who designed the Run 2a FIB module and is working on BTeV DAQ issues believes that it can take a lead role in the design and fabrication of this board. Assistance from universities especially with software and testing is also expected. A great deal of work and effort is required on this board in FY01. Some components may need to be purchased for testing. However, most of the work is in the engineering design that incorporates CDF required specifications. By the end of FY01, progress on the design and specifications of this board will allow for prototypes to be produced in FY02.

SVT Interface (CDF specific): We require minimal additional FNAL resources. We require engineering design to best make pixel information available for the SVT. This interface is likely to be incorporated into the pixel-FIB module. This activity will overlap with the development of specifications of the pixel-FIB. Some components may be purchased for tests. By the end of FY01, we should have the concept firmly defined and prototype circuitry designed.

DAQ test stand: We require minimal additional FNAL resources. BTeV activities include the commissioning of a test stand for reading out the prototype module "stacks." This test stand will test conceptual DAQ features such as differential signal readout followed by optical transmission. A test stand dedicated towards CDF specific activities should also be commissioned. It is expected that there will be some costs associated with this activity. By the end of FY01, a CDF pixel test stand should be commissioned.

12.2.4 Mechanical

The FY01 goals for mechanical issues are to validate the concepts outlined in this document, construct prototypes of the stave elements and a complete system, and begin to produce engineering drawings to be used for the actual construction of the pixel detector.

System mock-up: We do require funds and engineering and technician assistance. This system mock-up will be used to determine outstanding issues associated with the stave concept and other global mechanical issues. Besides a visible mock-up of a pixel detector, by the end of FY01, this activity will lead to concepts and engineering drawings of the support system, cooling manifold, cable routing, etc.

Prototype stave: We do require funds and engineering and technician assistance. The goal is to produce prototype carbon based structures including the C-C plate and the carbon fiber omega-channel. Particular attention will be made to the stave stiffness and environmental effects such as temperature and humidity dependence. By the end of FY01, the construction techniques for staves will be established.

Cooling test: We do require funds and engineering and technician assistance. Cooling the pixel detector both for removing the heat generated by the readout chip and for keeping the sensors cold is critical for the detector. The concept is to use a cooling system based upon ATLAS designs, but simpler. For example, we envision using an aluminum cooling tube within the omega channel instead of relying on a seal between the C-C plate and omega channel. These concepts do require testing and can be done either at SiDet or a university. By the end of FY01, the concept for cooling staves will be finished with calculations of the temperature profile along the stave performed.

13 Conclusions and Recommendations

We have studied the lifetimes of all components of the CDF Run 2a silicon detectors. We have established integrated luminosity levels which we believe can be attained with reasonable detector performance. We cannot guarantee that these safe limits, which are listed in Table 9, can be exceeded. As a result, we have seriously considered the possibility that a substantial portion of the Run 2a detector will not survive Run 2b (15 fb^{-1}). In particular, there is a significant likelihood that L00, the innermost 3 layers of SVX-II, and all SVX-II port-cards will need to be replaced.

In order to minimize lost running time, CDF should be prepared to install new silicon detector components during the shutdown for accelerator luminosity upgrades. This is currently scheduled for late 2003 or early 2004. An alternative later date, while allowing more time for detector design and production, is not in the interest of CDF physics goals and should be avoided.

A major renovation, on such a short time scale, that retains or improves the CDF detector performance, requires the use of simple components, designs, and streamlined construction techniques. To that end, the Run 2b Silicon Working Group has carefully studied the Run 2a detector experience and many new technological developments in the field - such as those now being used for LHC silicon trackers. The Working Group then developed and studied detailed examples for several replacement scenarios.

The conclusion that we draw from our studies is that a full replacement of the L00 and SVX-II detectors would have the greatest likelihood of achieving our schedule, performance, and luminosity goals. There are many reasons why this is true. First of all, a careful analysis of partial SVX-II replacement scenarios indicates that the shutdown period required would be a minimum of 9.5 months and possibly as much as 14 months. This is an unacceptably long time to be off the air. In addition, partial SVX-II replacement scenarios were found to involve more risk and a potential loss of performance. Alternatively, an example of a full replacement scenario was developed by the Working Group that would have lower risk and potentially improved performance over the Run 2a detector. Unfortunately, in either case the replacement project would be of substantial scale. Initial estimates for the resources required for full and partial SVX-II replacement scenarios are presented in Table 18 and Table 19, respectively.

With an accumulation of as little as 0.5 fb^{-1}, (but preferably 1 - 2 fb^{-1}), of data on tape, the Working Group expects that the longevity of Run 2a components will be much better understood. This will occur in the first year of running and will allow us to greatly refine our plans. For example, we may determine with good confidence that only L00 and L0 will not survive to 15 fb^{-1}. In this case, we will only need to replace L00. This could be done with either a replica of the Run 2a device using more rad-hard components, or pixels. The latter have the potential to greatly enhance the overall performance of the tracker. At the other extreme, it is possible that the majority of SVX-II layers need to be replaced. In this case, as mentioned above, we must be prepared to make a timely but major replacement in the shortest possible shutdown period. The Working Group finds that this can only be achieved if all of SVX-II and L00 are replaced by a new system that is constructed, tested, and ready to install in ISL at the start of the shutdown.

To be prepared to start building the right replacement components at the right time, we need R&D to be carried out in FY01. We have prepared a proposal for an R&D program that would focus on the design of a new sub-micron readout chip starting as soon as possible. For either a partial or a full SVX-II replacement, production readout chips will be needed in quantity in just over 2 years. Our FY01 R&D program would also have as its goal the development of robust new hybrids and port-cards, and a well developed and prototyped mechanical design for a new silicon tracker. We would continue our studies of pixels which we believe could provide major benefits to the CDF physics program.

We foresee the following time line for the CDF Run 2b Silicon tracker. In FY01 we would hope to get half way to the completion of a new readout chip to replace the SVX3D. We would also produce prototypes of our new hybrid and port-card concepts as well as prototypes of modules and module support and cooling systems. For pixels we would prototype cooling and mechanics and refine our understanding of new DAQ components. R&D would continue on the chip and sensor within the already existing FNAL pixel development project. By the end of FY01 we would prepare refined designs of potential replacement systems and also refine our cost estimates and schedules. By that time or shortly thereafter, we would expect to have enough collider data to greatly refine our lifetime estimates of the Run 2a system. From these new estimates we would make a decision about the scale of the Run 2b replacements and would choose a system design based upon the knowledge gained in our FY01 R&D program. The design would be adjusted to have a scope that matches the time available before the replacement shutdown. The final system choice and proposal would be presented to the PAC and FNAL directorate as early as possible in FY02.

The Working Group believes that the plan just outlined is the most reasonable one available to us at this time. The FY01 R&D program is the most critical element of this plan. We strongly recommend that the FNAL PAC and Directorate support this effort immediately. The resources we need for FY01 R&D programs for micro-strips and pixels are summarized in Table 20 and Table 21, respectively. While not negligible, the Working Group feels that the M&S costs and manpower needs are not large and represent our only insurance for continued operation in Run 2b. We strongly recommend that there be a decision to support this program at the FNAL PAC meeting held at FNAL in November of 2000.

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[3] J.Goldstein et al. hep-ph/0006311, Fermilab-pub-00-146-T, June 2000

[4] J. Lykken, presentation to the FNAL PAC at Aspen, June 2000

[5] Letter to the CDF Spokespeople from the Fermilab Director, July, 2000.

[6] It has been recently pointed out that the start of the shutdown could be as late as June 2004. Mike Witherell, private communication.

[7] We received the following quotation from Honeywell on October 18, 2000: 60 wafers, $27,980 each for a total of $1,678,800 (no yield guarantee) or $32,500 each, total for a total of $1,950,000 (5% yield guarantee). Prices decline slightly for 90 wafers.

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[9] J. Matthews et al., CDF internal note 3408.

[10] J. Matthews, CDF internal note 3937.

[11] S. Worm et al., CDF internal note 4357.

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[29] CERN/LHCC 98-6, CMS TDR 5 (Tracker), 15 April 1998. See http://cmsdoc.cern.ch/cms/TDR/TRACKER/tracker.html

[30] R. Wunstorf, ATLAS Collaboration, private communication.

[31] Proposal P-909, CDF Collaboration, Submitted to the FNAL directorate and the PAC January 5, 1999

[32] See http://fiore.home.cern.ch/fiore/gantry/gantry.html

[33] See
http://cms-usl-tmb.web.cern.ch/CMS_TMB/barrel_silicon/outer_barrel_silicon.html

[34] P.Azzi-Bacchetta et al. CDF Note 4924, March 1999

[35] http://www-cdf.fnal.gov/internal/upgrades/layer00/layer00.html

[36] A. Gandi, CERN Microcable group.

[37] Max Levy Corp. claimed that they were capable of producing Layer 00 cables but at an average cost of $\sim$ 800$. The cost to make all Layer 00 cables (including 25 % spares) would be $\sim$ 150k$.

[38] Key-com corporation. This company made the Belle SVD cables which have similar pitch and fine traces. The company claims they can do even more stringent specifications on even thinner backing materials. We are currently having them make us a Layer 00 cable to assess cost and quality.

[39] Budgetary quotes were received from Hamamatsu Photonics Corporation. For single-sided, double-metal detectors the sensors would cost roughly 650$. For non-double metal detectors the sensor price is roughly half this amount.

[40] Quotation received August 2000, from Speedring Corp. Note that in Run 2a there were 8 bulkheads purchased. We are assuming that this will not be necessary for Run 2b.

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