Checkout Sheet

Technician Name: ______________________

TRACER # : ______________________

Fermilab

Particle Physics Division/CDF Upgrade Project

Checkout Procedure for **TR**igger **A**nd **C**lock **+** **E**vent **R**eadout Module **(TRACER_V2.1)**

Theresa M. Shaw

Rodney L. Klein

9/28/98

Checkout Sheet
Technician Name: ______________________
TRACER #: _______

Note any test which initially fails and the action taken to repair it:

Name of Failing Test: ____
Repair Steps: ____
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Name of Failing Test: ____
Repair Steps: ____
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Name of Failing Test: ____
Repair Steps: ____
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Name of Failing Test: ______________________________

Repair Steps: ______________________________

Name of Failing Test: ______________________________

Repair Steps: ______________________________

Name of Failing Test: ______________________________

Repair Steps: ______________________________

Name of Failing Test: ______________________________

Repair Steps: ______________________________

Name of Failing Test: ____
Repair Steps: ____

Name of Failing Test: ____
Repair Steps: ____

Name of Failing Test: ____
Repair Steps: ____

Name of Failing Test: ____
Repair Steps: ____

TRACER Pre-Production Module Checkout

______ Visual Board Inspection
Look for rotated ICs, missing components, poor soldering, etc.

______ Check for shorts between power and ground

The **BOLD** Components MUST be Programmed and Inserted into sockets
Do not stuff switch S4

06/22/98 09:40:51 Electronics Design System Page: 0001

Bill of Materials

<<<From Job: J:\TRACER_PROD_V2_1\vbdc\tracer_prod.prj>>>

Fermi National Accelerator

PPD/ET&T/CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF DESG
1	3	AD9501JP	Dig Prog Delay Gen, JP pkg	20.00	U56-U58
2	1	AMP 1-520459-3	AMP Modular Jack Connector 8 Pos	2.25	J1
3	1	AMP 3-520459-3	AMP Modular Jack Connector 8 Pos	2.25	J2
4	1	AMP 226968-1 DIGI A1126-ND	Twinax Bulkhead	24.58	J6
5	1	AMP 269050-1	AMP Optronic Data Link - RCVR 200Mb/s	76.47	U15
6	1	AMP 352009-1 PLUS SHIELDS .	AMP 5x19 Z-PACK 2mm Female Conn w/gnd sh	25.00	P0
7	1	AMP269049-1	200 Mb/s 1300 nm optical transmitter.	20.00	D6
8	**1**	**AM27S19SAPC**	**32x8 PROM**	**1.25**	**U35**
9	1	AM29F010-45JC	No PDB description available	10.45	U11
10	1	AM7968-175JC	Taxi xmtr	20.00	U22
11	1	AM7969-175JC	TAXI RCVR	25.00	U16
12	1	BOT d_strip	Bottom Discharge strip	.01	X2
13	**1**	**C&K P8121 1160-1890**	**Mom. Push button Panel mnt**	**2.48**	**S4 - do not stuff**
14	3	CAP_CER_SMT_SPARE_1206	SMT CAP SPARE	0.168	C147,C149,C151
15	1	CY7B991-7JC	ROBOCLOCK	21.85	U42
16	5	CY7C470-15JC	Cypress 8K x 9 FIFO	22.00	U17,U28,U38,U44
*					U49
17	5	CY74FCT16500TTSSOP	18-bit Registered Transceivers	5.78	U23,U29,U30,U32
*					U39
18	1	CY74FCT16543CTPAC	No PDB description available		U31
19	5	CY74FCT162244TTSSOP	16-Bit Buffers/Line Drivers	3.95	U18,U27,U37,U43
*					U48
20	1	DS26C32ATN RS-422 recvr National	Diff Line RCVR	3.50	U52
21	1	DS90C031 National	Differential Line Driver	2.23	U9
22	1	DS90C032 National	Differential Line Receiver	2.23	U41
23	3	DS1020	Programmable 8-bit Silicon delay line 1n	22.00	U61-U63
24	2	ERIE 8131-100-651-104M 1415-3140	Bypass Cap .1UF	0.05	C17,C25
25	1	ERIE 8131-100-651-153M 1415-3090	Bypass Cap .015UF	0.07	C1
26	4	ERJ-6ENF19.1 Digi P19.1CBK-ND	1/10W 1% 19.1 ohm	0.061	R40,R43,R51,R54
27	8	ERJ-6ENF51.1 Digi P51.1CBK-ND	1/10W 1% 51.1 ohm	0.061	R41,R42,R44,R45
*					R52,R53,R55,R56
28	1	ERJ-8ENF1.00K Digi P1.00KFBK-ND	1/8W 1% 1.0K ohm	0.0542	R37
29	3	ERJ-8ENF8.0K Digi P8.0KFBK	1/8W 1% 8.0K ohm	0.0542	R78-R80
30	7	ERJ-8ENF66.5 Digi P66.5FBK-ND	1/8W 1% 66.5 ohm	0.0542	R26,R32,R35,R39
*					R46,R65,R68
31	2	ERJ-8ENF82.5 Digi P82.5FBK-ND	1/8W 1% 82.5 ohm	0.0542	R70,R71
32	2	ERJ-8ENF100 Digi P100FBK-ND	1/8W 1% 100 ohm	0.0542	R48,R72
33	2	ERJ-8ENF121 Digi P121FBK-ND	1/8W 1% 121 ohm	0.0542	R73,R74
34	2	ERJ-8ENF158 Digi P158FBK-ND	1/8W 1% 158 ohm	0.0542	R29,R30
35	2	ERJ-8ENF169 Digi P169FBK-ND	1/8W 1% 169 ohm	0.0542	R17,R25
36	2	ERJ-8ENF249 Digi P249FBK-ND	1/8W 1% 249 ohm	0.0542	R23,R24
37	2	ERJ-8ENF267 Digi P267FBK-ND	1/8W 1% 267 ohm	0.0542	R28,R34

06/22/98 09:40:51 Electronics Design System Page: 0002
Bill of Materials
<<<From Job: J:\TRACER_PROD_V2_1\vbdc\tracer_prod.prj>>>

Fermi National Accelerator
PPD/ET&T/CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF DESG
38	2	ERJ-8ENF394 Digi P394FBK-ND	1/8W 1% 394 ohm	0.0542	R49,R50
39	80	Ground Via	Ground-Via	.00	VG1-VG7,VG18,VG19
*					VG20-VG85,VG89
*					VG90-VG93
40	3	HARTING-male	VME64 Card Connector	25.00	P1-P3
41	1	HIROSE TM5RJ1-66 DIG H9083-ND	Modular Jack 6pos 6contact	2.30	J3
42	1	HP HFBR-2412	Fiber Optic RCVR	18.15	U26
43	4	HP HLMP-1301 1445-0475	Red LED	0.24	D1,D3-D5
44	1	HP HLMP-1401 1445-0495	Yellow LED	0.24	D2
45	1	IDT 74FCT244DTP	8 bit Tri-state buffer	3.40	U50
46	17	KEMET T340B106K015AS	10UF 15V Bullet	.80	C56,C57,C59,C61
*					C104,C132,C137
*					C157,C161,C167
*					C181-C183,C206
*					C208,C211,C212
47	3	KEMET T354H336K016AS	33UF 16V RADIAL Dip	.85	C18,C26,C53
48	2	LITTLEFUSE 251010 Newark 20F604	10 AMP PCB Fuse	0.74	F1,F2
49	**1**	**MACH 110-12JC**	**AMD PLD 44 Pin PLCC**	**7.00**	**U25**
50	2	MC10E116	QUINT differentail Line Receiver	10.00	U40,U76
51	1	MC10H350	PECL Receiver	10.00	U51
52	2	MOTOROLA 1N5908	Transient Suppressor 6.0V	1.24	D7,D8
53	**3**	**PALCE22V10H-7PC**	**Programmable Logic Device**	**5.00**	**U10,U34,U47**
54	15	PAN ECS-H1CC106R DIG PCT3106	SMT CAP 10.0UF	0.9765	C2,C5,C6,C11,C13
*					C14,C15,C24,C28
*					C30,C31,C36,C37
*					C41,C52
55	1	PAN ECS-H1CY105R DIG PCT3105	SMT CAP 1.0UF	0.3955	C48
56	11	PAN ECU-V1H103KBG DIG PCC103BN	SMT CAP 0.01UF	0.168	C7,C9,C29,C32,C39
*					C46,C90,C101,C102
*					C119,C205
57	5	PAN ECU-V1H103KBM DIG PCC103BCT	SMT CAP 0.01UF	0.168	C19,C50,C51,C92
*					C93
58	152	PAN ECU-V1H104KBW DIG PCC104B	SMT CAP 0.1UF	0.5914	C3,C4,C12,C16,C21
*					C23,C27,C33,C34
*					C35,C38,C42,C43
*					C44,C45,C49,C54
*					C55,C58,C60,C62
*					C63-C89,C91,C94
*					C95-C100,C103
*					C105-C118,C120
*					C121-C131,C133
*					C134-C136,C138

06/22/98 09:40:51 Electronics Design System Page: 0003
Bill of Materials
<<<From Job: J:\TRACER_PROD_V2_1\vbdc\tracer_prod.prj>>>

Fermi National Accelerator
PPD/ET&T/CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF DESG
*					C139-C146,C148
*					C150,C152,C153
*					C154-C156,C158
*					C159,C160,C162
*					C163-C166,C168
*					C169-C180,C184
*					C185-C204,C207
*					C209,C210,C213
*					C214,C215,C245
59	6	PAN ECU-V1H561JCX DIG PCC561CGCT	SMT CAP 560pF	0.125	C8,C10,C20,C22
*					C40,C47
60	40	PN32	test point		GP1-GP18,TP18
*					TP23,TP24,TP31
*					TP32,TP33,TP40
*					TP44-TP58
61	5	RC05-270 1487-0290	270 ohm 1/8W 5%	0.19	R1,R3,R4,R6,R7
62	1	RC05-820K 1487-0497	1/8W 820Kohm 5%	0.18	R5
63	3	RC05-1000 1487-0325	1000 ohm	0.18	R14-R16
64	1	RC07-1.5M 1487-1125	1/4W, 5PCT, THRU	0.14	R76
65	2	RC07-1M 1487-1105	1/4W, 5PCT, THRU	0.19	R2,R77
66	1	RC07-5.6 Digi 5.6QBK-ND	1/4W, 5PCT, THRU	0.06	R75
67	5	RC07-4700 1487-0825	1/4W, 5PCT, THRU	0.08	R10-R13,R36
68	1	RN55C-13K	1/8W 1PCT Thru	0.04	R19
69	3	RN55C-27K	1/8W 1PCT Thru	0.04	R20-R22
70	2	RN55C-84.5	1/8W 1PCT Thru 249 Ohm	.04	R62,R63
71	1	RN55C-100K	1/8W 1PCT Thru	0.04	R18
72	1	RN55C-249 1487-4365	1/8W 1PCT Thru 249 Ohm	.04	R61
73	13	SN74ABTE16245SSOP	16 Bit Incident Transceiver	5.60	U1,U7,U8,U21,U33
*					U45,U46,U54,U59
*					U60,U65,U66,U75
74	1	SN74ABTE16246SSOP	11 Bit Incident Transceiver	7.50	U14
75	3	Samtec TSW-12-07-L-D 2pin sip	2 pin jumper - mates with SNT-100-BK-G $	0.16	S1-S3
76	8	Spare-IC 24DIP3	Spare 24 pin DIP	0.00	U67-U74
77	16	TEST_PIN	.025 x .025 square post.	.01	TP2-TP6,TP14,TP19
*					TP20,TP25,TP30
*					TP34-TP37,TP42
*					TP43
78	**1**	**TIBPAL16L8-5C**	**Programmable Logic Device**	**5.00**	**U13**
79	1	TOP d_strip	Top Discharge strip	.01	X1
80	28	VCC Via	VCC-Via	.00	VP1-VP25,VP59
*					VP60,VP61
81	1	XC3130A-1PQ100C	Xilinx XC3130A Logic Cell Array	35.00	U4

06/22/98 09:40:51 Electronics Design System Page: 0004
Bill of Materials
<<<From Job: J:\TRACER_PROD_V2_1\vbdc\tracer_prod.prj>>>

Fermi National Accelerator
PPD/ET&T/CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF DESG
82	1	XC4005EPQ100-3	Xilinx FPGA	60.00	U19
83	1	XC4013E-3PQ240C	Xilinx FPGA	250.00	U6
84	**1**	**XC17128-PD8C**	**XILINX PROM**	**13.00**	**U20**
85	**2**	**XC17256-PD8C**	**XILINX PROM**	**13.00**	**U3,U12**
86	2	mc10h351l	Quad TTL to PECL translator.	10.00	U36,U55
87	15	res_spare1206	1/8W 1% 1.0K ohm	0.00	R8,R9,R27,R31,R33
*					R38,R47,R57,R58
*					R59,R60,R64,R66
*					R67,R69
88	1	1N5817	Scottky Diode	.80	D9
89	1	3 pin jump 3SIP60 TSW-12-07-L-D	3 pin jumper	0.30	U24
90	1	10x-2-102	10 pin 1K SIP, pin 1 common	1.50	RP1
91	1	74F04N	hex inverter	0.53	U53
92	2	74F38N	Open collector nand	0.53	U5,U64
93	1	74LS14N 1455-8014	schmitt trigger inverter	0.31	U77
94	1	74LS123N 1455-8123	Multivibrator	0.35	U2
95	4	2503-5020-UG 3M 20pin Rt Ang HDR	3M 20 pin right angle header		J7-J10
96	6	2743021446 PSC ELECTRONICS	SMT FERRITE BEAD 10UH	1.30	L1-L6

Total Parts Used: 573
Total Parts Cost: 1313.17

Begin Checkout Procedures

POWER

______ Check that Power LED **D1** (page 1) comes on when board plugged in

______ Check voltage level on both sides of Fuses **F1** and **F2** (page 1). You should see 5 Volts.

RESET

______ Plug in a Reset Cable from the CDF Reset Module to Tracer Front panel Connector J3.
Issue a reset by issuing command by
1) logging into dorothy
2) type "ld <reset.o"
3) type "timer_on"
4) type "menu"
5) Select "Reset one Crate" option and select appropriate cable # (1-96)

When the Reset is sent, you should see the MVME162 re-boot itself.

Verify Download of FPGAs

______ Look at **U12**-4 (page 3A). This pin will have a high logic level if the VME_slave FPGA is properly downloaded.

______ Check for a high logic level at pin **U3**-4 (page 9A). This verifies the download of the TSI Interface FPGA.

______ Check for a high logic level at pin **U20**-4 (page 9B). This verifies the download of the Local Teststand Calibration FPGA.

Begin VMEbus Checkout

______ With only the TRACER module and a VRC (MVME162) in the crate, open the generalized checkout program VASE. Choose the option to MAP the crate.

______ Verify that the result of the crate map is a readout of the TRACER's ID PROM **U35** (page 4)in the correct slot. The ID PROM should be similar to the one below:

0987 001 TRACER_V2
where,
0987 reflects the serial number (changes on board by board basis - **should match engraved serial number**)
001 is the board type (always the same)
TRACER is the user specified text

VMEbus Register Checkout

______ Going back to VASE, select the TRACER submenu, and then choose the **Tracer Checkout Menu** option.

Choose the **Test all Registers** option.

This will allow you to do an initial test of most TRACER registers automatically. If errors are detected, exit menu and select Register Test Menu option to test individual registers.

- ______ Diagnostic Register (inside VMEbus Slave FPGA)
- ______ Control Register (inside VMEbus Slave FPGA)
- ______ Calibration Register (inside local Teststand Calibration FPGA)
- ______ Start Delay Register (inside local Teststand Calibration FPGA)
- ______ Calibration Delay Register (inside local Teststand Calibration FPGA)
- ______ Halt Delay Register (inside local Teststand Calibration FPGA)
- ______ Interrupt Return Vector Register (inside VMEbus Slave FPGA)
- ______ TDC Pulses Enable Register (inside VMEbus Slave FPGA)
- ______ TDC Calibration Course Delay Register (inside VMEbus Slave FPGA)
- ______ TDC Calibration Fine Delay Register (page 3A U23, U39)
- ______ TDC Calibration Pulse Width Register (page 3A U29, U30)
- ______ TBUS Register (page 14)
- ______ Transition Port Read/Write Register (inside VMEbus Slave FPGA)
- ______ Transition Port Address Register (inside VMEbus Slave FPGA)
- ______ Event FIFO Data (U30, U37, U41, U46 page 7)
- ______ Event FIFO Status Check
- ______ Word Count Register (inside VMEbus Slave FPGA)
- ______ Event Header Register (inside VMEbus Slave FPGA)
- ______ A’s Pattern Register (inside VMEbus Slave FPGA)
- ______ 5’s Pattern Register (inside VMEbus Slave FPGA)

______ Run looping test, **Test all Registers in Loop Mode**, for 100 loops.

Verify Flash RAM Registers

A 1 Megabit (131,072 x 8-Bit) AMD AM29F010 Flash Memory has been incorporated on the TRACER (see **page 13**). The purpose of this Flash Memory is to serve as a storage device for any TRACER or crate level constants.

Like all Flash RAM, a specific algorithm must be used when erasing or programming the contents.

Two examples below describe how to set up the erase and the write alogorithms to these devices. For additional information on these devices, please refer to AMD's data sheet.

To erase the Flash RAM

```
write 0xAA 0000   to    addr  0xYY61 5554(YY is Geo. Address)
write 0x55 0000   to          0xYY60 AAA8
write 0x80 0000   to          0xYY61 5554
write 0xAA 0000   to          0xYY61 5554
write 0x55 0000   to          0xYY60 AAA8
write 0x10 0000   to          0xYY61 5554
```

To write the Flash RAM

```
write 0xAA 0000         to    addr  0xYY61 5554
write 0x55 0000         to          0xYY60 AAA8
write 0xA0 0000         to          0xYY61 5554
write desired data      to          desired adrress
```

______ Using the **Test Flash RAM** option in the TRACER Checkout menu within VASE, verify that the FLASH RAM can be loaded with data, verified and erased.

Module Select Light

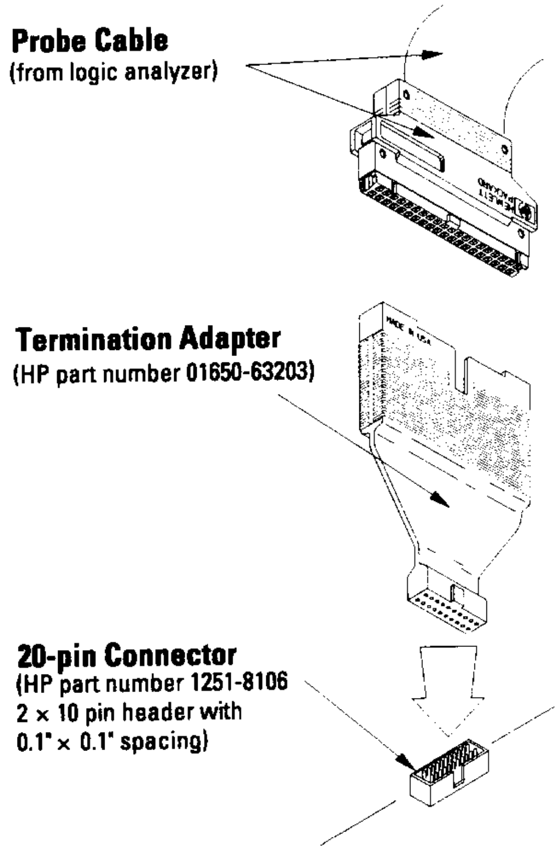
______ As the board is addressed over VMEbus, the yellow Module Select light, **D2** (page 3) should come on. Verify that it does, and that it is off when the module is not addressed.

Externally Applied Pulse

______ Use the PECL pulse generator box to drive a pulse over a Twinax cable to the Twinax Connector on the front panel of the TRACER (**J6** page 5). This pulse should be received by **U76** and is driven off the module with **U40**. Verify this is the case by looking (with o-scope) at front panel connector **J7** pin **13** (page 11). This pin is being driven by a differential receiver which is looking at the backplane.

Logic Analyzer Port - On the TRACER

Tracer Front Panel Ports J will provide ports for easy access to the CDF backplane trigger and clock signals. These ports will bring TTL level signals to four 20 pin right angle box headers on the front panel. The ports can be used by a wide range of oscilloscopes or logic analyzers, but are specifically designed for ease of use with HP logic analyzers and the HP Terminator Adapter.



Hewlett Packard Pinout on Terminator Adapter (HP part number 01650-63203)

Pin	Signal	Pin	Signal
20	GND	19	D0
18	D1	17	D2
16	D3	15	D4
14	D5	13	D6
12	D7	11	D8
10	D9	9	D10
8	D11	7	D12
6	D13	5	D14
4	D15	3	CLK1
2	CLK2	1	+5V

Create a setup disk for the HP Logic Analyzer, so that all the ***BOLD Italicised*** signals are available for viewing when required by the tests which follow.

CDF Signals are connected to the Port as follows:

Port J7 - POD 1

Pin	Signal	Pin	Signal
20	GND	19	***CDF_TDC_CAL0****
18	CDF_RowA1	17	***CDF_TDC_CAL1****
16	CDF_RowA2	15	***CDF_TDC_CAL2****
14	CDF_RowA3	13	***CDF_TDC_CALIB***
12	CDF_RowA4	11	No Connect
10	CDF_RowA5	9	***CDF_TDC_DONE***
8	***CDF_CLOCK***	7	CDF_RowC7
6	No Connect	5	CDF_RowC8
4	CDF_RowA8	3	CDF_CLOCK
2	No Connect	1	No Connect

Port J8 - POD 2

Pin	Signal	Pin	Signal
20	GND	19	CDF_RowC9
18	***CDF_BC****	17	CDF_RowC10
16	***CDF_B0****	15	CDF_RowC11
14	CDF_RowA11	13	***CDF_GLIVE****
12	***CDF_L1A****	11	***CDF_L1_CALIB****
10	***CDF_L1R****	9	***RSVD_L1W2****
8	***CDF_L2B0****	7	***CDF_STOP****
6	***CDF_L2B1****	5	***CDF_TEST****
4	***CDF_HALT****	3	CDF_CLOCK
2	No Connect	1	No Connect

Port J9 - POD 3

Pin	Signal	Pin	Signal
20	GND	19	***CDF_RUN****
18	CDF_RowA17	17	***CDF_RL0****
16	***CDF_RECOVER****	15	***CDF_RL1****
14	CDF_RowA19	13	***CDF_RL2****
12	***CDF_ABORT****	11	***CDF_CALIB3****
10	***CDF_CALIB0****	9	***CDF_CALIB4****
8	CDF_RowA22	7	***CDF_CALIB5****
6	***CDF_CALIB1****	5	***CDF_CALIB6****
4	***CDF_CALIB2****	3	CDF_CLOCK
2	No Connect	1	No Connect

Port J10 - POD 4

Pin	Signal	Pin	Signal
20	GND	19	***CDF_CALEN****
18	CDF_RowA25	17	CDF_RowC26
16	***CDF_ERROR****	15	***CDF_L2R****
14	***CDF_L2A****	13	***CDF_L2A_EN****
12	***CDF_L2BD0****	11	***CDF_EVID0****
10	CDF_RowA29	9	***CDF_EVID1****
8	***CDF_L2BD1****	7	***CDF_EVID2****
6	***CDF_RSVD0****	5	***CDF_EVID3****
4	***CDF_RSVD1****	3	CDF_CLOCK
2	No Connect	1	No Connect

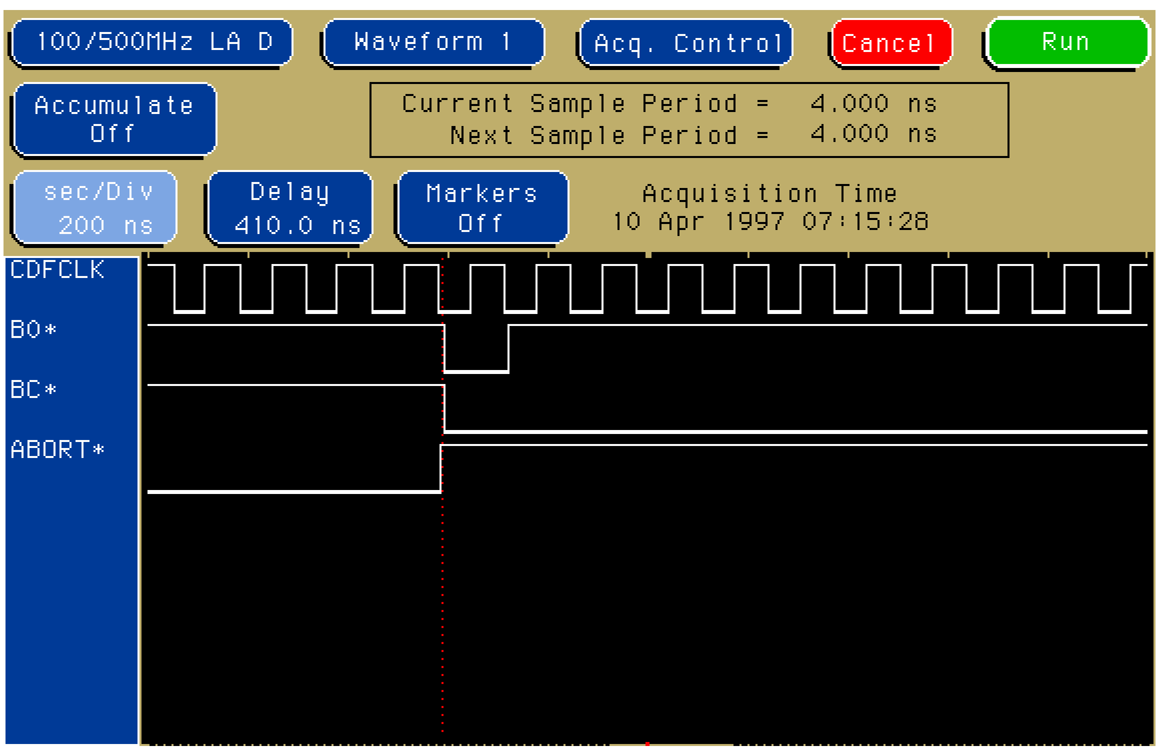
Master Clock Interface

______ For this test, the TESTCLK module must be used.
Prior to inserting the TESTCLK, make sure that the TESTCLK jumpers **S13** and **S14** are **removed**.

______ Now, from VASE, select the TESTCLK submenu. Go to the TSIE submenu and turn on the Cable clock driver.

Now connect the Clock Cable between TESTCLK and TRACER front panel connector **J2** page 5.
With an o-scope or Logic Analyzer, view the four clock signals on the following front panel connector.
CDF_CLOCK
CDF_BC*
CDF_B0*
CDF_ABORT*

Trigger on CDF_B0*, and verify the pattern looks as pictured below.



______ Change the scale of the clock signals and put the Logic Analyzer in "Accumulate On" mode.
Verify that the clock signals are not drifting.

Checking Phase Lock Loop Function

______ Verify the Phase Lock Loop **U42** (page 8) is functioning properly. Do this by verifying that U42 pins 1 and 17 have a 132 ns clock running in phase (rising edges are aligned). The duty cycle at pin 17 should be 50%.

______ Next check U42 pins 10 and 11. These are all x2 versions of the clock. They should have a period of 66 ns, a 50% duty cycle, and will be in phase with each other but 180 degrees out of with the reference clock signal on pin 1.

______ Next check U42 pin 20. This is a x4 version of the clock. It should have a period of 33 ns, a 50% duty cycle, and be in phase with each other as well as with the reference clock signal on pin 1.

TSI Interface

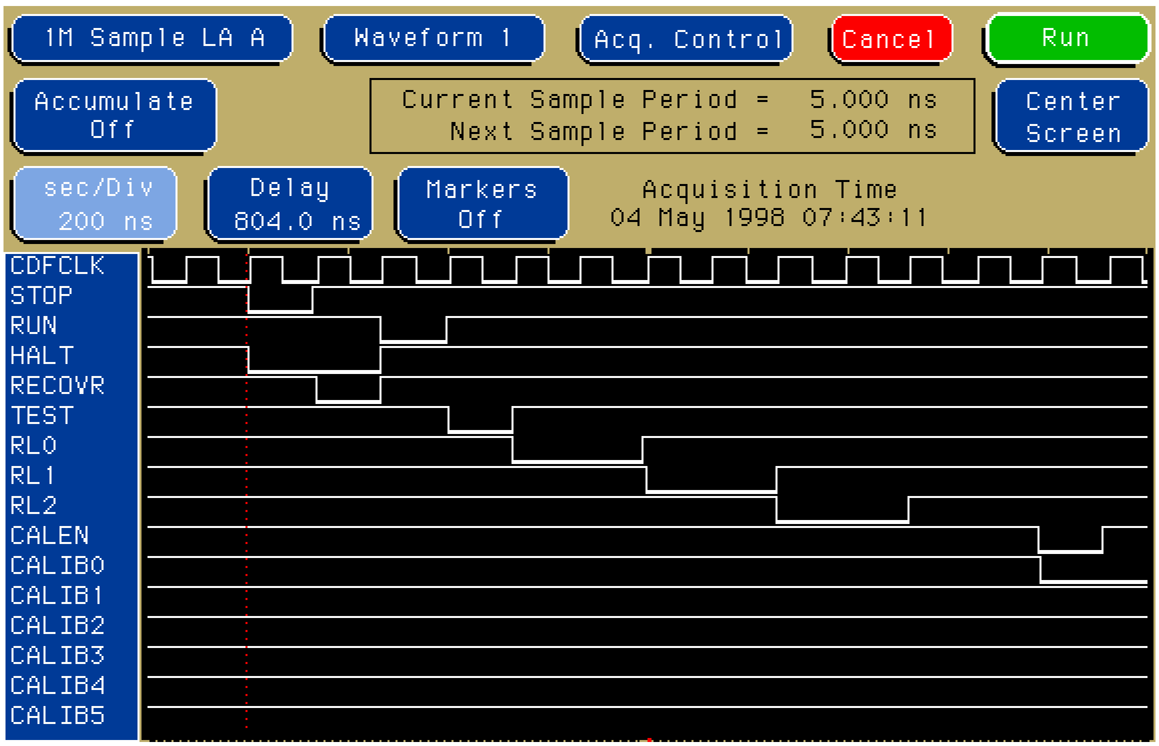
______ The TSI (Trigger System Interface) interface will now be tested. To do this, the TESTCLK will again be used. The Clock cable (**J2** page5) must be connected between the TESTCLK and TRACER as well as the Fiber Optic Cable (**U15** page 9). Within VASE: Tracer Checkout Menu, select the **TSI Interface Test** option. The program enables the Cable Clock, and sets TSIE start wait condition on the Testclk.

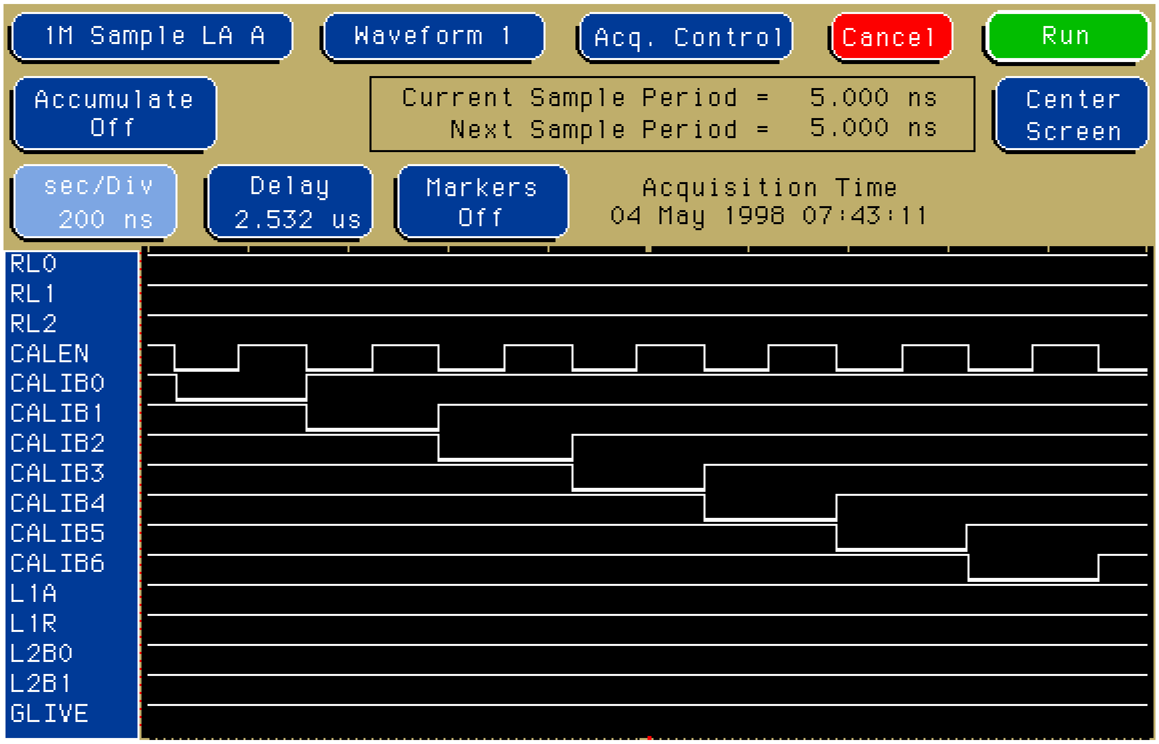
______ Prior to starting test, set the Logic Analyzer to trigger off STOP* going low.

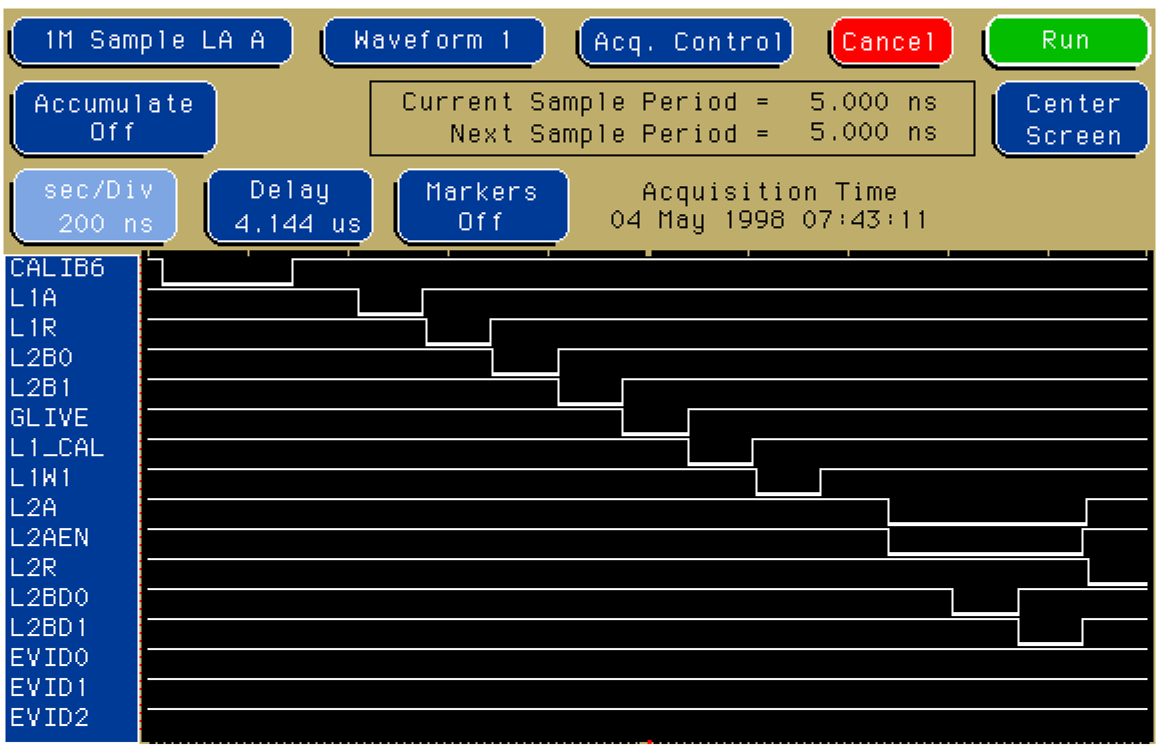
The **TSI Interface Test** software will:

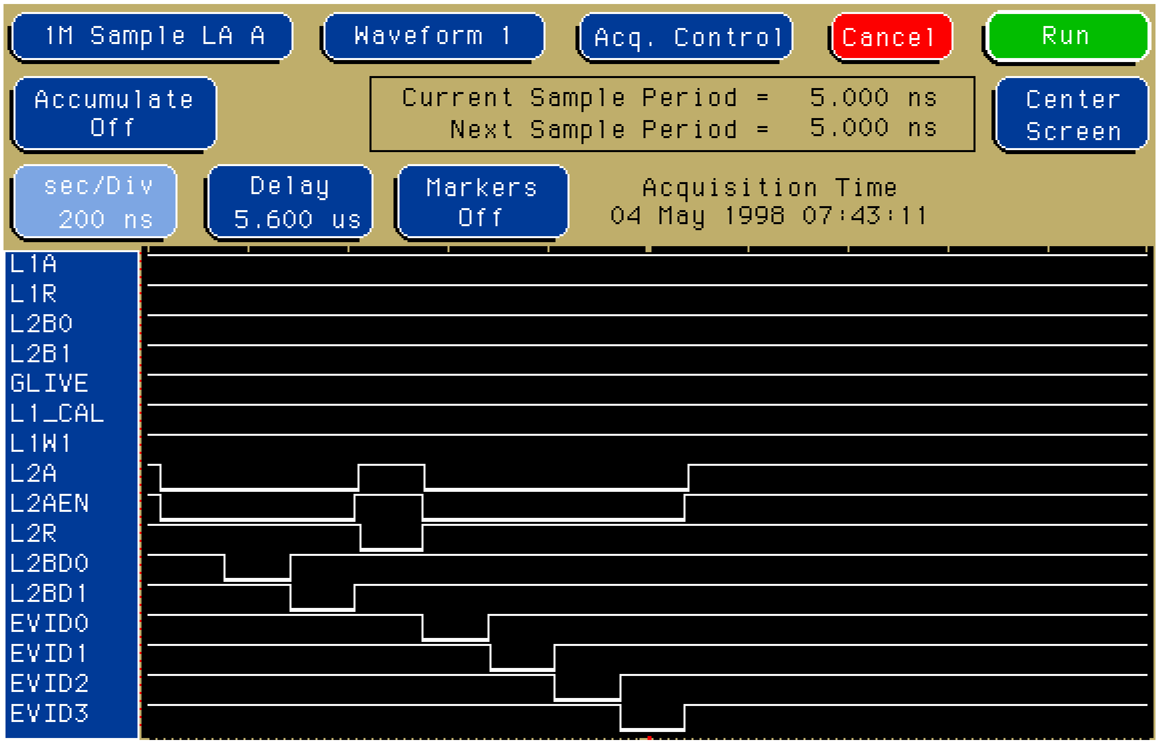
- Enable the Cable Clock at the TESTCLK.
- Set the "Enable CDF Trigger Signals to backplane" bit in the Tracer's Control Register
- Load the TESTCLK TSIE FIFO and Enables the transmission of the tsi trigger file "toggle_all.tsi".

______ Trigger on STOP going low, and you should see the following patterns:




1M Sample LA A
Waveform 1
Acq. Control
Cancel
Run
Accumulate Off
Current Sample Period = 5.000 ns
Next Sample Period = 5.000 ns
Center Screen
sec/Div 200 ns
Delay 2.532 us
Markers Off
Acquisition Time
04 May 1998 07:43:11
RL0
RL1
RL2
CALEN
CALIB0
CALIB1
CALIB2
CALIB3
CALIB4
CALIB5
CALIB6
L1A
L1R
L2B0
L2B1
GLIVE


1M Sample LA A
Waveform 1
Acq. Control
Cancel
Run
Accumulate Off
Current Sample Period = 5.000 ns
Next Sample Period = 5.000 ns
Center Screen
sec/Div 200 ns
Delay 4.144 us
Markers Off
Acquisition Time
04 May 1998 07:43:11
CALIB6
L1A
L1R
L2B0
L2B1
GLIVE
L1_CAL
L1W1
L2A
L2AEN
L2R
L2BD0
L2BD1
EVID0
EVID1
EVID2


1M Sample LA A
Waveform 1
Acq. Control
Cancel
Run
Accumulate Off
Current Sample Period = 5.000 ns
Next Sample Period = 5.000 ns
Center Screen
sec/Div 200 ns
Delay 5.600 us
Markers Off
Acquisition Time
04 May 1998 07:43:11
L1A
L1R
L2B0
L2B1
GLIVE
L1_CAL
L1W1
L2A
L2AEN
L2R
L2BD0
L2BD1
EVID0
EVID1
EVID2
EVID3

Automatic Testing of Trigger Sum bits Using CBSS Module

This test will use the CBSS module to verify what you have visually observed above.
This test requires that you have a TESTCLK, CBSS and the TRACER under test installed in the crate.

______ Assert CDF_ERROR* on the backplane by using special Error generator module.

______ Now within Vase and the TRACER Checkout Menu, select the **TRACER -> CBSS Trigger Test**

The test will:

- Setup the TESTCLK so that the cable clock is on and the clock cable is installed between the TESTCLK and the TRACER.
- Set the Wait for B0 bit on the TESTCLK.
- On the CBBS board, clear the FIFOs and make sure the Enable VME access bit is low.
- Have the TESTCLK send the file “CBSS_test.tsi” in looping mode.
- Check to verify that the FIFOs on the CBSS have filled
- Enable VME access in the CBSS Control Register
- Verify that the contents of the FIFO matches a known comparison file

_____ Next, run the **Tracer -> CBSS Trigger Test in Loop Mode** for at least 100 loops.

Test of the Start Scan Register

The Start Scan Register receives its information from the Level 2 word sent from the TSI. To perform the next level of testing, you will send TSI patterns from the TESTCLK to set Start Scan Register bits.

______Within VASE: Tracer Checkout Menu, select the **TSI - Start Scan Test**. The Clock cable **J2** page5) must be connected between the TESTCLK and TRACER as well as the Fiber Optic Cable (**U15** page 9).

The test program performs the following tests:

- Check that the test enables Testclk Cable Clock. And sets the TSIE Start Wait condition.
- Set the DONE bit in the DONE register.
- Load the TSIE file START_SCAN.tsi
  Read the Start Scan Register and verify that the Start Scan bit is set. All other bits (besides the CDF_TDC_DONE) should be low.
- Set the DONE bit in the DONE register.
- Load the TSIE file EVID0.tsi
  Read the Start Scan Register and verify that the Event ID 0 bit is set. All other bits (besides the CDF_TDC_DONE) should be low.
- Load the TSIE file EVID1.tsi
  Read the Start Scan Register and verify that the Event ID 1 bit is set. All other bits (besides the CDF_TDC_DONE) should be low.
- Load the TSIE file EVID2.tsi
  Read the Start Scan Register and verify that the Event ID 2 bit is set. All other bits (besides the CDF_TDC_DONE) should be low.
- Load the TSIE file EVID3.tsi
  Read the Start Scan Register and verify that the Event ID 3 bit is set. All other bits (besides the CDF_TDC_DONE) should be low.
- Load the TSIE file L2B0.tsi
  Read the Start Scan Register and verify that the L2 Decision Buffer Address 0 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.
- Load the TSIE file L2B1.tsi
  Read the Start Scan Register and verify that the L2 Decision Buffer Address 1 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.
- Load the TSIE file RL0.tsi
  Read the Start Scan Register and verify that the Readout List 0 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.
- Load the TSIE file RL1.tsi
  Read the Start Scan Register and verify that the Readout List 1 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.

- Load the TSIE file RL2.tsi
  Read the Start Scan Register and verify that the Readout List 2 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.

- Load the TSIE file CAL0.tsi
  Read the Start Scan Register and verify that the Calibration bit 0 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.

- Load the TSIE file CAL1.tsi
  Read the Start Scan Register and verify that the Calibration bit 1 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.

- Load the TSIE file CAL2.tsi
  Read the Start Scan Register and verify that the Calibration bit 2 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.

- Load the TSIE file CAL3.tsi
  Read the Start Scan Register and verify that the Calibration bit 3 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.

- Load the TSIE file CAL4.tsi
  Read the Start Scan Register and verify that the Calibration bit 4 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.

- Load the TSIE file CAL5.tsi
  Read the Start Scan Register and verify that the Calibration bit 5 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.

- Load the TSIE file CAL6.tsi
  Read the Start Scan Register and verify that the Calibration bit 6 bit is set. All other bits (besides the CDF_TDC_DONE and Start Scan) should be low.

_____ Next, run the **TSI - Start Scan Test Loop** for at least 100 loops.

Test of the Done bit in the DONE Register

The Done bit is set over VMEbus and reset whenever a Start Scan is received from the TSI.

______ From the VASE: Tracer Checkout Menu, select the **TSI - Done Test** option and verify the following:

- Test will verify that it can set the DONE bit.

______ Verify the DONE LED (**D3** on page **10**)turns on.

- Test loads the TSIE file START_SCAN.tsi.
- Test verifies that the DONE bit in the Done Register has been reset.

______ Verify the DONE LED (**D3** on page **10**)turns off.

- Test verifies that the Start Scan bit in the Start Scan Register has been set.
- Test will now again write the DONE bit and verify it has been set.
- Verify that the above step has reset the Start Scan bit in the Start Scan Register.

______ Next, run the **TSI - Done Test Loop Mode** for at least 100 loops.

TSI Diagnostic FIFO

It is possible for the TSI to turn on the input to the TSI Diagnostic FIFO by sending the "TEST" bit in the TSI Control Word. When "TEST" is sent, the FIFO is flushed and the next 8K data words received from the TSI to be clocked into a FIFO. In its this operating mode, once the FIFO is full, no further data recording will be done. In order to repeat the test, the original "TEST" state must be cleared by toggling the "reset tsi test" bit in the Control Register.

______ From the VASE: Tracer Checkout Menu, select **Testclk - Tracer TSI Diagnostic FIFO TEST Mode Test** option.

The test will perform the following:

- Turns on the Cable Clock at the TESTCLK.
- Clears any possible ERROR state by toggling the "Reset TSI Taxi Error" bit (high then low) in the Control Register.
- Sets the "Enable CDF Trigger Signals to backplane" bit in the Control Register
- Sets the TSI "TEST" bit low by downloading the following tsie pattern to TESTCLK and sending it across the optical link.

  H000 "L1 word - nothing active
  H003 "Control word - clear TEST
  H000 "L1 word - nothing active

- Begins by toggling (high and then low) the "Reset TSI Diagnostic FIFO TEST mode" bit.
- Resets the TSI Diagnostic FIFO by toggling the "Reset TSI Diagnostic FIFO" bit.
- Verifies the TSI Diagnostic FIFO is empty by checking the FIFO status in the Control register.
- Downloads a tsie pattern to the TESTCLK which will turn on the "TEST" mode and then send across random data.

  The first active lines of this file should be

  H000 "L1 word - nothing active
  H013 "Control word - set TEST
  H000 "L1 word - nothing active
  H003 "Control word - clear TEST
  H000 "L1 word - nothing active
  …. To be followed by 8K of random data in the range of H000 to H1FF.

- The TSI Diagnostic FIFO should fill up. Verifies this by checking the FIFO status in the Control register.
- Resets the TEST mode state by toggling (high and then low) the "Reset TSI Diagnostic FIFO TEST mode" bit. This will prevent the FIFO from continuing to fill as we read it out.

- Reads out the FIFO information and compare it to what was downloaded.

_____ Next, run the **Loop Mode - Testclk -> Tracer TSI Diagnostic FIFO TEST Mode Test** at least 100 loops.

A second diagnostic mode possible - it will, however, be overridden by any "TEST" message written from the TSI. In the second mode, it is possible to save the last ~8K of TSI commands by setting the "tsi_save_mode" bit of the Control Register. When this bit is set the TSI Diagnostic FIFO will be filled by incoming TSI commands. As the FIFO limit is approached, automatic readout is begun to clear space for new commands. If at any time a CDF_ERROR* condition occurs, the state of the FIFO will be frozen. Hopefully, this will aid in determining what was going on in the crate at the time of the error.

______ From the VASE: Tracer Checkout Menu, select **Testclk - Tracer TSI Diagnostic FIFO SAVE Mode Test** option.

The first part of this test is done automatically for you, the second part is user interactive.

- Test turns on the Cable Clock at the TESTCLK.

- Test clears any possible ERROR state by toggling the "Reset TSI Taxi Error" bit (high then low) in the Control Register.

- Test sets the "Enable CDF Trigger Signals to backplane" bit in the Control Register

- Test sets the TSI "TEST" bit low by downloading the following tsie pattern to TESTCLK and sending it across the optical link.

  H000 "L1 word - nothing active
  H003 "Control word - clear TEST
  H000 "L1 word - nothing active

- Test now toggles (high and then low) the "Reset TSI Diagnostic FIFO TEST mode" bit.

- Test resets the TSI Diagnostic FIFO by toggling the "Reset TSI Diagnostic FIFO" bit.

- Test verifies the TSI Diagnostic FIFO is empty by checking the FIFO status in the Control register.

- Test sets the "Enable TSI Diagnostic FIFO Save Mode" bit in the control register.

- Test downloads a tsi pattern to the TESTCLK, and in a looping mode send across **somewhat** sequential data in the range of H000 to H1FF. The data never set bits 4, 1, and 0 all at once or the TSI "TEST" mode may be set. Therefore there will be skips of H013, H017, H01B, H01F, H033, ….

User Interactive part.

______ The TSI Diagnostic FIFO should never fill up. Verify this by checking the FIFO status in the Control register.

______ Simultaneous reads and writes should be occurring. Observe the activity on the READ* pin (**U17-18** on page **10**) and WRITE* pin (**U17-2**). Both should contain a train of pulses.

______ Generate a CDF_ERROR* signal on the backplane through the use of a small circuit card designed for the purpose.

______ Now, with CDF_ERROR* still asserted readout the TSI Diagnostic FIFO. It should contain evidence of our "somewhat" sequential data.

______ Also, while CDF_ERROR* is asserted, observe the ERROR Front Panel LED (**D4** on page 10). The LED should be on.

______ Check the ERROR mask by setting the “Mask CDF_ERROR” bit in the Control register. The ERROR LED should go off.

______ Now reset the “Mask CDF_ERROR” bit in the Control register. The ERROR LED should come on again.

______ Now clear the CDF_ERROR* signal being asserted by the small circuit card.

______ Clear the ERROR state by toggling the “Reset TSI Taxi Error” bit (high then low) in the Control Register.

______ The ERROR LED (D4) should turn off.

______ Now TSI Diagnostic FIFO read and write activity should begin again. Observe the activity on the READ* pin (**U17-18** on page **10**) and WRITE* pin (**U17-2**). Both should contain a train of pulses.

TSI Return Cable

The TSI Return Cable is a copper link which returns the signals DONE, ERROR, and BUSY to the TSI. The state of these signals is also visible by looking at the Front Panel LEDs (page **10**).

DONE
Previously observed and checked.

ERROR
Previously observed and checked.

BUSY

BUSY will be set to a logic high state in two possible ways.

The default TSI Busy uses the status of the EVENT FIFO Flags. Bit 0 of the Control Register should be low. The Event Status Level that the busy operates off can be programmed with bits (3:1) of the Control Register. By default, TSI BUSY will turn on when the Event FIFO becomes greater than half full.

______ From VASE: Tracer Checkout Menu, select **Busy Test.**

The test will perform the following:

- Set bit 0 of the Control Register low.
- Set Control Register bits (1) low
  (2) high
  (3) high
- Reset the Event FIFO

_____ Verify the BUSY LED is OFF

- Partially fill the EVENT FIFO to more than half full by writing 4,100 words into it.

_____ Verify the BUSY LED is ON

- Reset the Event FIFO.

_____ Verify the BUSY LED is OFF.

- Set Control Register bits (1) high
  (2) low
  (3) low

______ Verify the BUSY LED is ON.

Secondly, Busy can be set when the VME buffer space in the VME Readout Buffer (VRB) is approaching full.

- To do this, set the Select the TAXI-Test Busy as the source for the TSI Busy. Do this by setting bit 0 of the Control Register high.

You can simulate this state with the Taxi Test module. Transmit a Busy condition over a Fiber Optic Cable plugged into **U26** (page 8) on the front panel. In the Taxi-Test Menu select the RX # Control Menu and enable the BUSY SET bit.

_______ The BUSY LED should turn on, and

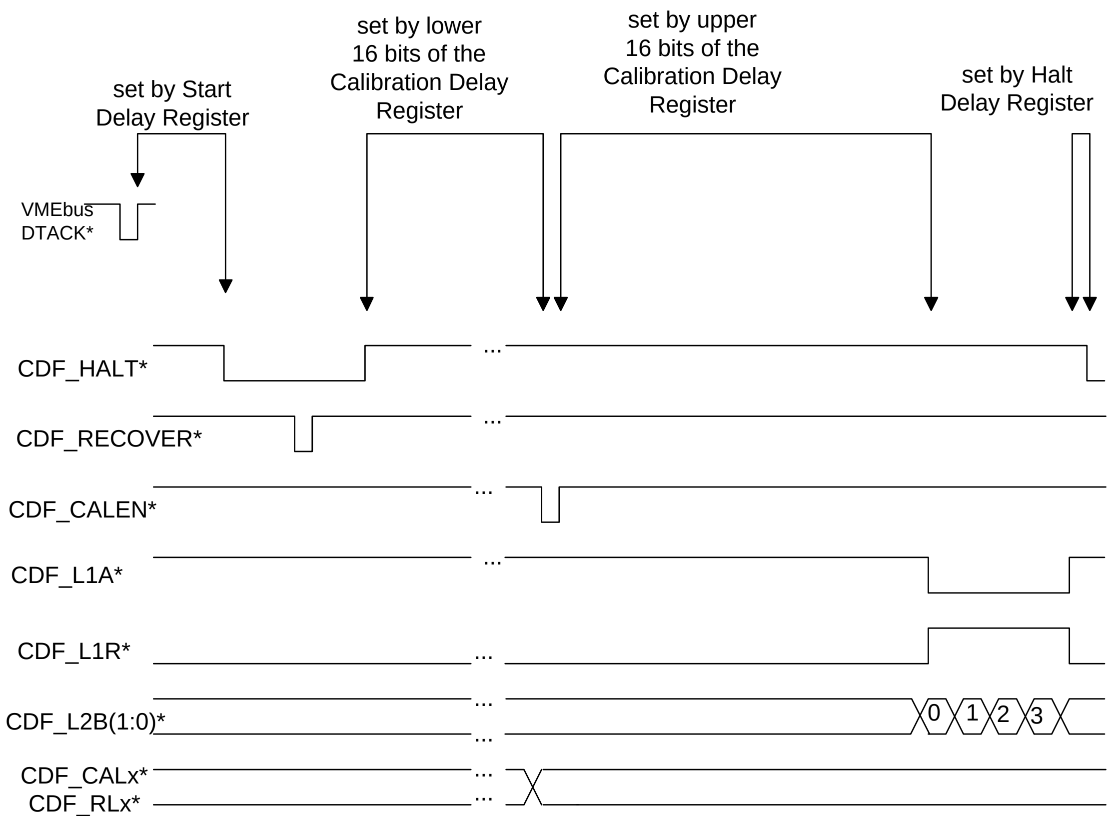
- VRB Busy bit in the Control Register should be set.

Local Teststand Calibration

Calorimetry

The Tracer has the capability of driving the following lines for doing a teststand calibration:
VME_DTACK*
CDF_L1A*
CDF_L1R*
CDF_L2B0*
CDF_L2B1*
CDF_HALT*
CDF_RECOVER*
CDF_CALEN*
CDF_CALIB0*
CDF_CALIB1*
CDF_CALIB2*
CDF_CALIB3*
CDF_CALIB4*
CDF_CALIB5*
CDF_CALIB6*
CDF_RL0*
CDF_RL1*
CDF_RL2*
CDF_TDC_CAL0*
CDF_TDC_CAL1*
CDF_TDC_CAL2*
CDF_CLOCK

A typical Calibration sequence will look as follows:
(Make sure that the rising edge of CDF_CLOCK validates all the gated trigger signals shown below.)


set by Start
Delay Register
set by lower
16 bits of the
Calibration Delay
Register
set by upper
16 bits of the
Calibration Delay
Register
set by Halt
Delay Register
VMEbus
DTACK*
CDF_HALT*
CDF_RECOVER*
CDF_CALEN*
CDF_L1A*
CDF_L1R*
CDF_L2B(1:0)*
0
1
2
3
CDF_CALx*
CDF_RLx*

The following sequence is involved in the Local Teststand Calorimetry Calibration:

- Issue a Calibration command by writing to the TRACER Calibration Register.
- Tracer will wait programmed time, determined by the TRACER Start Delay Register.
- Tracer will issue Halt - Reset - Run sequence.
- Tracer will wait programmed time, determined by the TRACER Calibration Enable Delay Register.
- Tracer will issue Calibration Enable.
- Tracer will issue four successive L1 Accepts at a programmed number of crossings (set in the Calibration Delay Register) after calibration enable. These L1 Accepts will occur a programmed number of CDF_CLOCK cycles after the CDF_CALEN* pulse. The successive L1 Accepts will fill buffers 0, 1, 2 and 3 in that order.
- Tracer will wait a programmed delay, determined by the TRACER Halt Delay Register.
- Tracer will issue Halt (if halt mode enabled).
- Tracer will set a bit in a register to indicate process is done.

______ From VASE: Tracer Checkout Menu, select **Teststand Calibration Test.** Verify the following pictures with a Logic Analyzer.

The test performs the following:
(NOTE: timing mentioned in each step is not observable until you get to the step which writes to the Calibration Register.)

- Turns on the Cable Clock at the TESTCLK.
- Sets the "Enable CDF Trigger Signals to backplane" bit in the Control Register
- Sets the "CDF Trigger Signal Source" to "1" to select the Local Calibration Sequencer. This is set in the Tracer's Control Register.
- Writes to the Start Delay Register. Each count equals 132ns, and a typical value to be set is 1ms, for a count of **1D97(hex)**. This value controls how long the Tracer waits to begin the Calibration sequence following a write to the Calibration Register. You can measure this with the Logic analyzer by looking at the time difference between the VME DTACK* line from the write to the Calibration Register to the assertion of CDF_HALT*
- Writes two values to the Calibration Delay Register. The lower 16 bits (example 1 sets this to **4 hex,** example 2 sets this to **13 hex**) represents how many clock cycles to wait before issuing CDF_CALEN* following the Halt-Recover-Run sequence. You can measure this with the Logic analyzer by looking at the time difference between the signal CDF_HALT* to the assertion of CDF_CALEN*

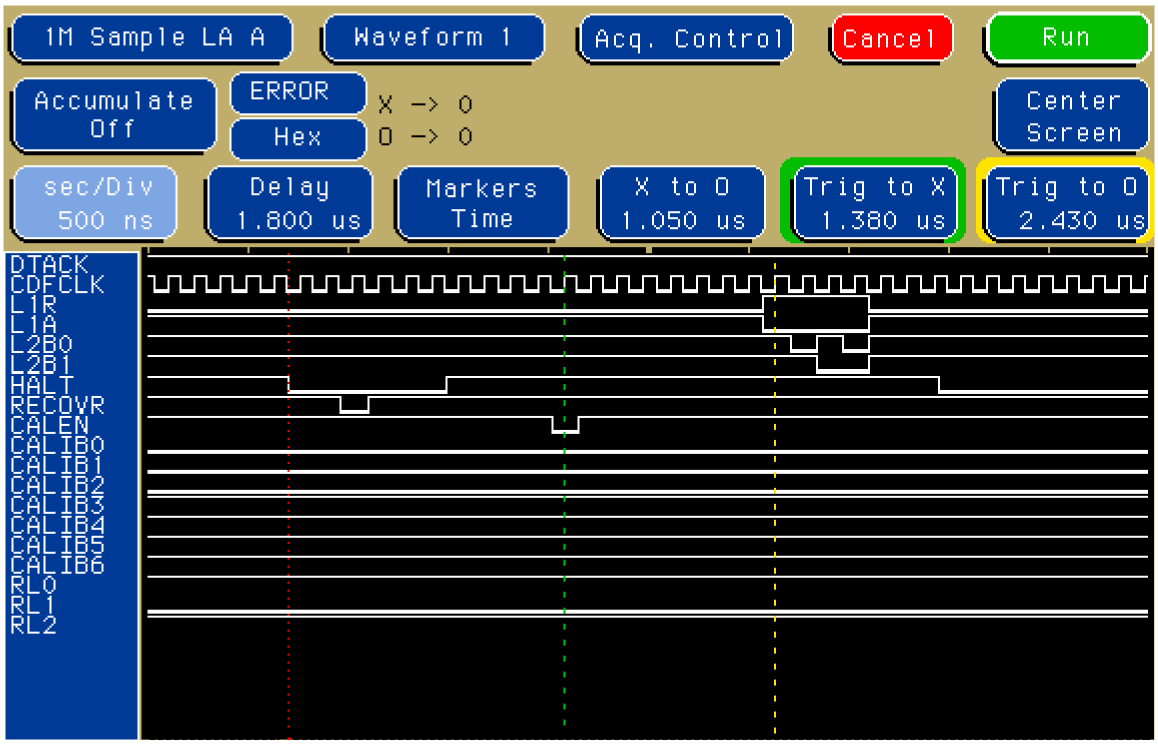
  The upper 16 bits (example 1 sets this to **8 hex,** example 2 sets this to **29 hex**) control the number of CDF_CLOCK cycles after CDF_CALEN* until the sequence of four

CDF_L1As occur. Typically, this value will be set to 29(hex). You can measure this with the Logic analyzer by looking at the time difference between the signal CDF_CALEN* to the assertion of CDF_L1A*

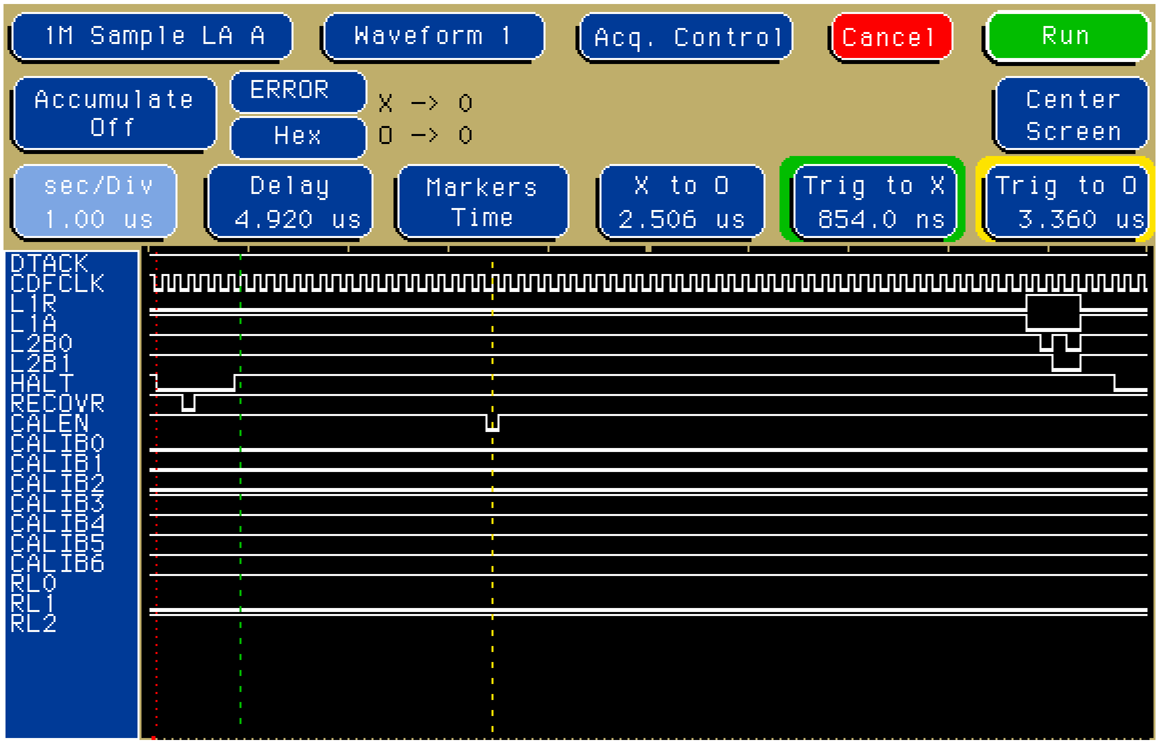
- Writes to the Halt Delay Register. This is an eight bit register which controls the number of CDF_CLOCK cycles (examples set this to **03 hex)** following the L1As until CDF_HALT* is issued (assuming the "Enable Halt Mode" bit is set in the Calibration Register). You can measure this with the Logic analyzer by looking at the time difference between the signal CDF_L1A* to the assertion of CDF_HALT*

- Writes to the Calibration Register. Writing to this register will begin the sequence. The "Local Calibration Enable" bit must be set, along with a value for Calibration Enables (6:0). You should observe CDF_CAL(6:0)* backplane lines which match the value you gave it. (Example enables CDF_CAL0*, CDF_CAL1* and Halt Mode).

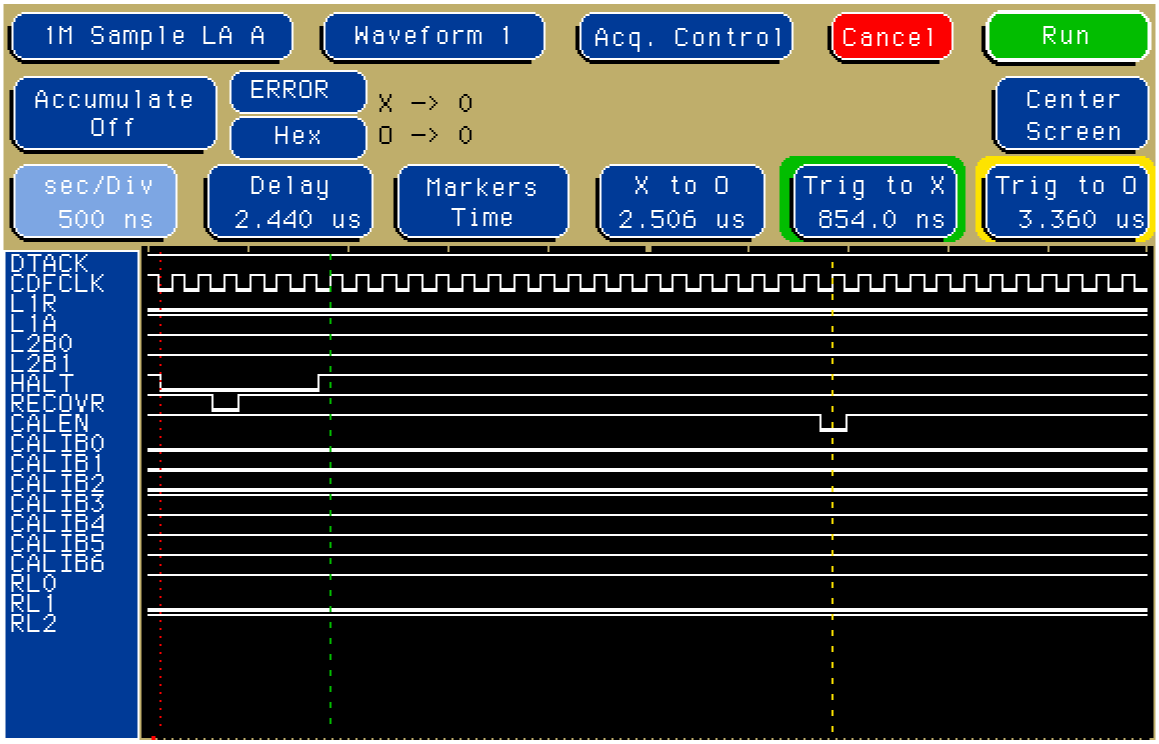
- When the sequence is done, reads the Calibration Done Register and verifies that the "Teststand Calibration Done" bit has been set. (This bit is cleared at the beginning of each Local Teststand Calibration sequence.)



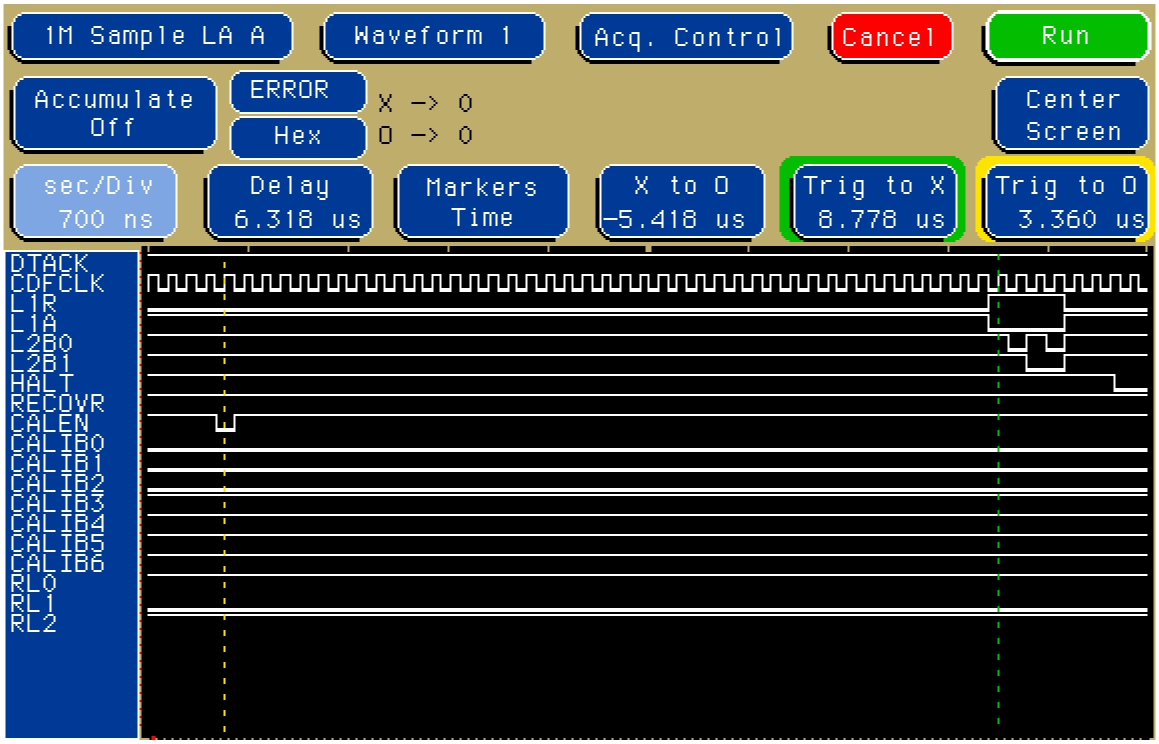
Example 1)
start delay = 1D97 (~1ms)
calen delay = 4 (note CALEN* occurs 4+1 cycles after HALT*)
l1 delay = 8 (note L1A* occurs 8 cycles after CALEN*)
halt delay = 3 (note HALT* occurs 3+1 cycles after last L1A*)



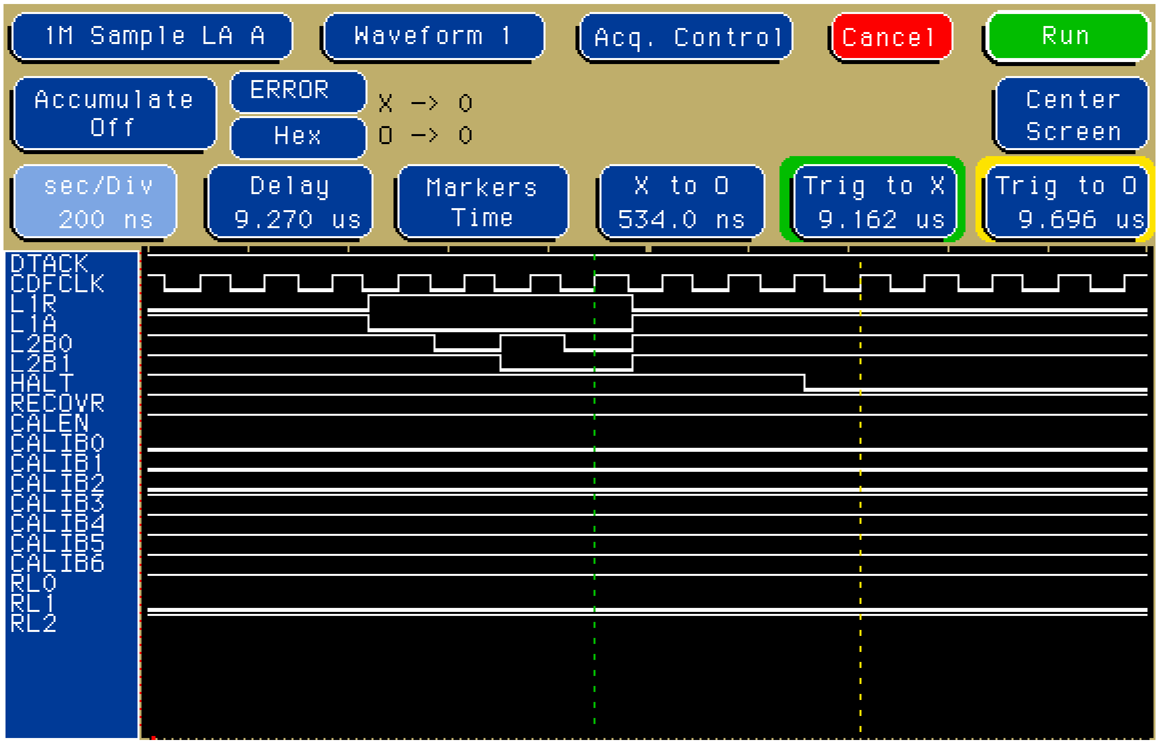
Example 2)
start delay = 1D97 (~1ms)
calen delay = 13 hex (note CALEN* occurs 13+1 hex cycles after HALT*)
l1 delay = 29 hex (note L1A* occurs 29+1 hex cycles after CALEN*)
halt delay = 3 (note HALT* occurs 3+1 cycles after last L1A*)



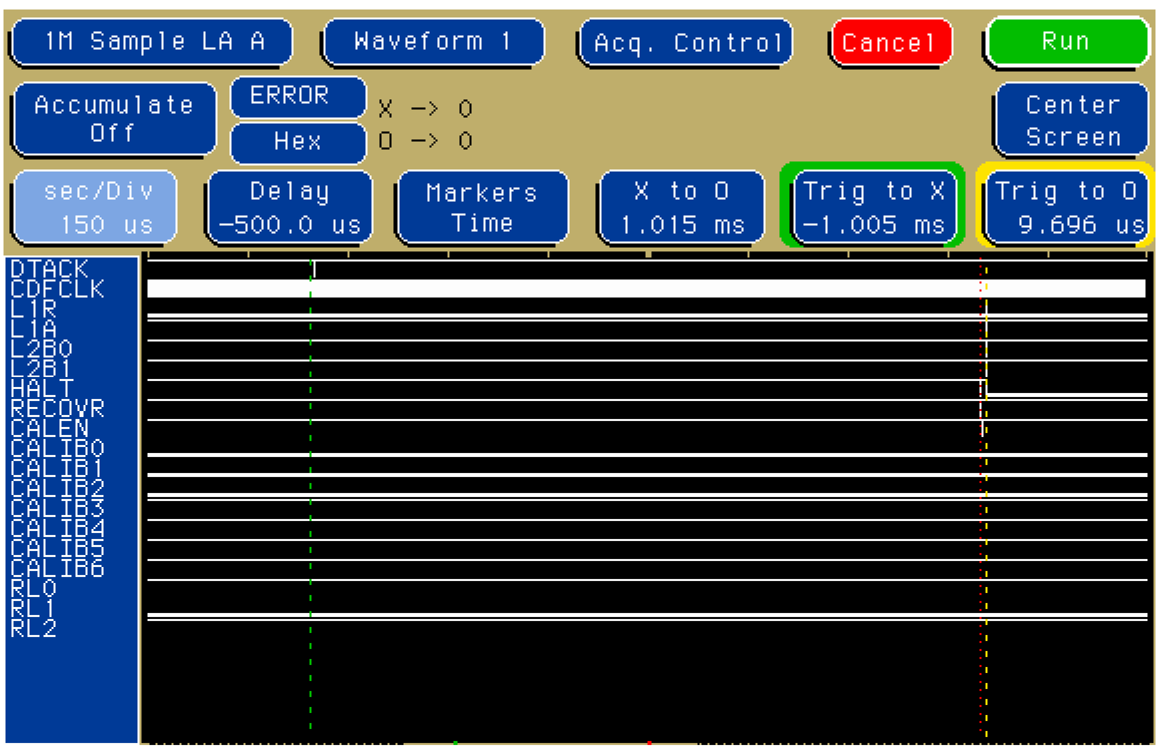
Zoom in on timing between HALT* and CALEN*. Note timing matches predicted delay of 2.5us.



Zoom in on timing between CALEN* and L1A*. Note number of crossings and timing matches predicted delay of 5.4us.



Zoom in on timing between last L1A* and HALT*. Note HALT* occurs (3+1) crossings after L1A*.



Zoom in on timing between VMEbus DTACK* which begins Local Calibration and beginning of cycle (HALT* going low). Note timing matches predicted delay of 1ms.

TDC Calibration Pulses

It is also possible to trigger the TDC Calibration pulses

trig(0)
trig(1)
trig(2)
CDF_TDC_CAL0*
CDF_TDC_CAL1*
CDF_TDC_CAL2*

from control of the local teststand calibration used for the calorimetry.

______ In order to trigger the CDF_TDC_CAL(2:0)* pulses it is necessary to select from the VASE: Tracer checkout Menu, **TDC Calibration Test.** Verify the following pictures with a Logic analyzer.

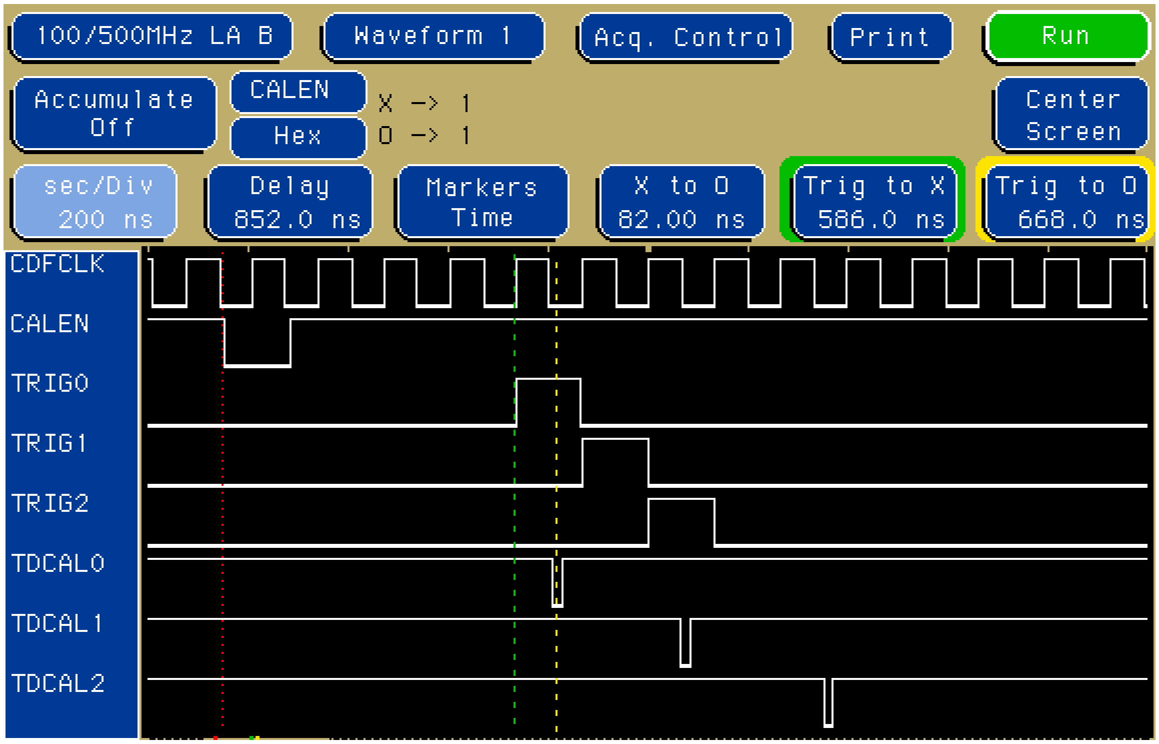
The test will perform the following:

- Writes to the TDC Calibration Pulses Enable Register and enable the pulse or pulses which you want to test. **Example enables all three pulses.**

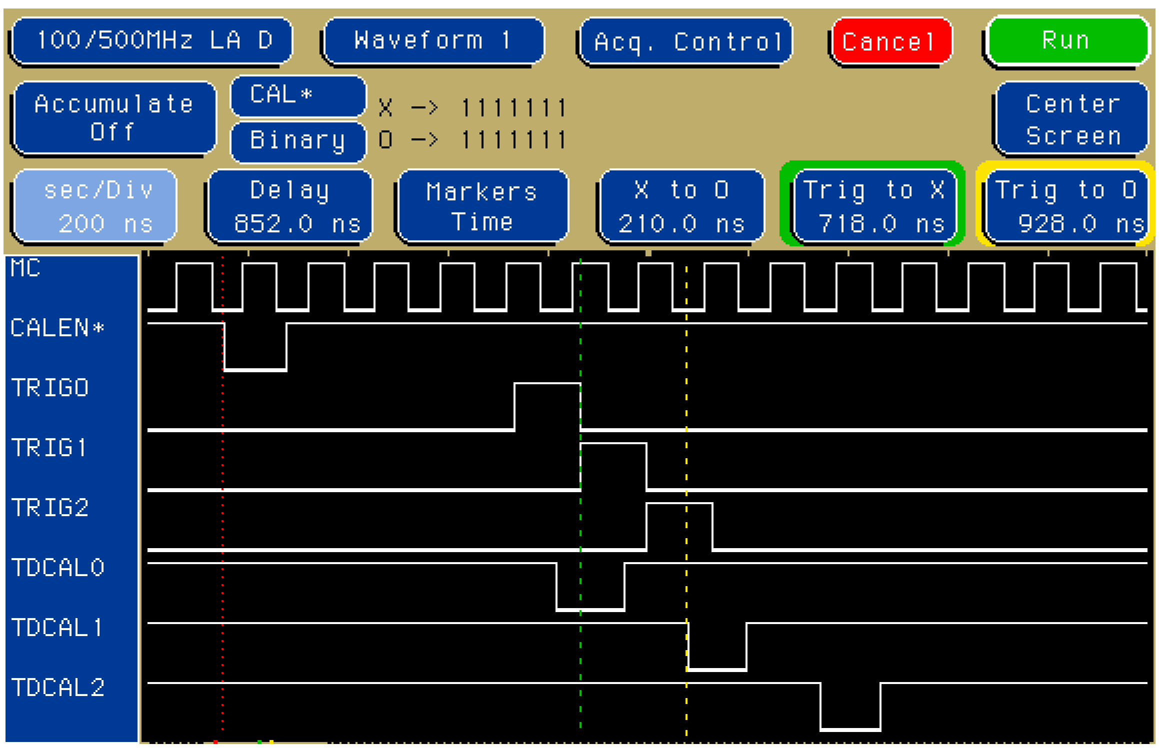
- Writes to the TDC Calibration Course Delay Register. This register will allow you to set the number of CDF_CLOCK cycles which occur prior to firing the TDC trigger pulses trig(2:0) (page 9). **Example sets course delays of 3, 4 and 5 for CDF_TDC_CAL0*, CDF_TDC_CAL1*, and CDF_TDC_CAL2*.** Note that the true delay is always the programmed number plus one.

- These trigger pulses, trig(2:0), now go to rest of the TDC calibration pulse logic. It is necessary to write to the TDC Calibration Fine Delay register **(Example sets all Fine Delay values to 0 , 80 and FF hex).**

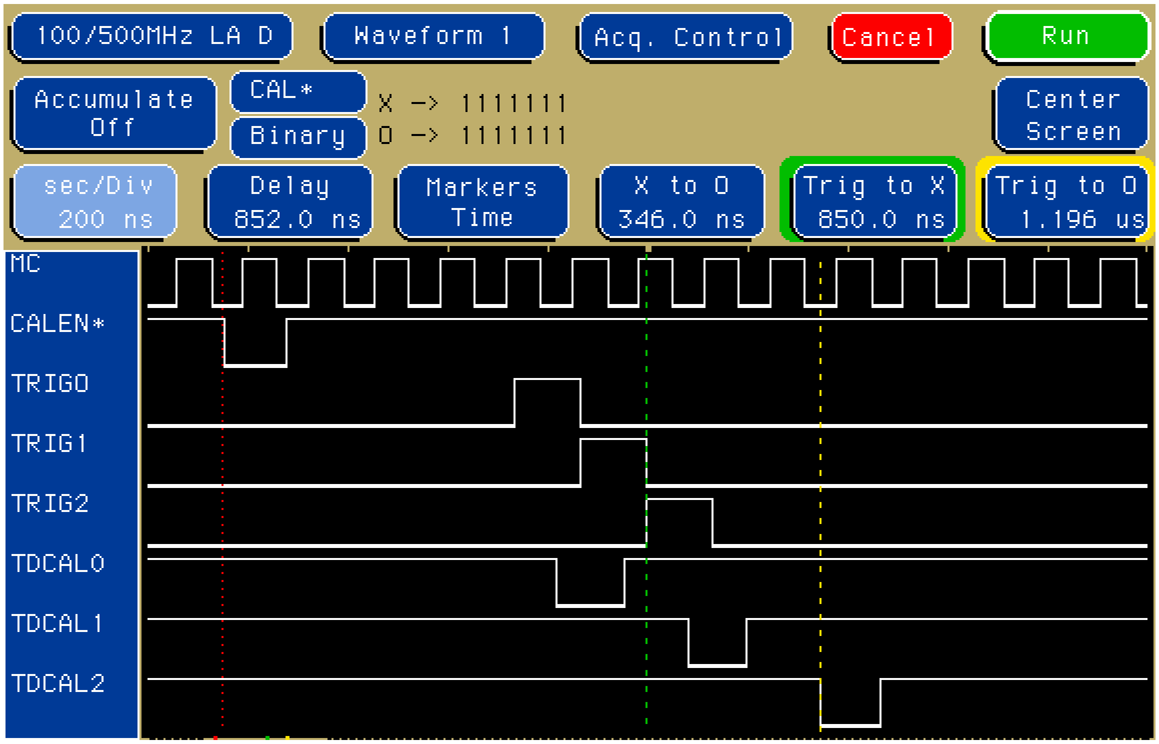
- Sets the TDC Calibration Width Delay Register **(Example sets all values to 7 hex)** to have further control over the pulse width and timing.



Note the delay of 82 ns between TRIG0 and TDC_CAL0*. This is the inherent delay of the programmable pulse generator.



Note the delay of 210 ns between TRIG1 and TDC_CAL1*. This is the sum of the inherent delay (~82ns) plus half scale of the full range (~265ns).



Note the delay of 346 ns between TRIG2 and TDC_CAL2*. This is the sum of the inherent delay (~82ns) plus full scale of the full range (~256ns).

Event Data FIFO

The TRACER has an optical data link to the VRB. This link uses the TAXIchip (AM7968-175JC) protocol and AMP optical driver (AMP 269049-1). It operates at two times the CDF_CLK.

An 8K by 32 bit Event FIFO feeds this data link. It is possible to fill this Event FIFO in two ways. One way is to simply do a VMEbus write into the FIFO. If the VRC is used to do zero suppression and data formatting, this method would be used. The VRC would first read in raw event data, do the formatting and then write the formatted data to the Event FIFO.

A sequencer on the TRACER detects when data is present in the FIFO, serialize the data through the use of a TAXIchip, and transmit it upstairs to the Readout Memory (VRB) module via an optical link. The data can be transmitted to the VRB at a rate of up to one byte every 66 ns (twice the CDF clock). A Taxi Sync signal is sent up at least every 5 bytes; thus, a data rate of 4 Bytes/(5 x66ns), or 12.1 MB/s is achievable out of the crate.

______ Connect dual optical cable between Tracer's Event data and Busy Ports to the Taxi-Tester Data and Busy Ports.

______ From VASE: Tracer Checkout Menu, select **Tracer -> Taxi-Test Test**.
The test will perform the following:

- Make sure the Testclk is driving the Cable Clock to the TRACER.
- Make sure that the "Event Data Taxi Enable" in the Tracer's Control Register is set low.
- Load the Tracer's Event Data FIFO with Sequential Data. The FIFO flags should indicate a high state.
- Enable the Taxi-Tester Module so that it is ready to accept data. (Enable receive mode, clear the FIFO, reset the flags, wordcount, and enable BUSY).
- Now, set the "Event Data Taxi Enable" in the Tracer's Control Register.
- Data will flow from Tracer to Taxi-Tester until the FIFO on Taxi-Tester becomes almost full.
- At this point the Taxi-Tester will send BUSY. Verify that you see the Front Panel WAIT LED turn on.
- In order to clear the WAIT state, read out the FIF0 on the Taxi-Tester until its status is empty - you should observe the sequential data.
- You should see the Event FIFO status flags indicate Empty as well when you read them.
- Now (leaving the "Event Data Taxi Enable" bit set in the Tracer's Control Register), fill the Event FIFO with random data.
- Data will flow from Tracer to Taxi-Tester. Repeat the readout of the Taxi-Tester FIFO until it is empty.
- You should also see the Event FIFO status flags indicate Empty when you read them.
- Now look at the data in the Taxi-Tester FIFO. It should be identical to what was sent.

Spy Mode Test of VMEbus Reads

A second method for getting event data to the VRB would involve using the TRACER's Spy capability. The TRACER will have the capability to spy on the data as the VMEbus Readout Controller (VRC) reads it out. During event readout, the TRACER has the ability to clock data into the Event FIFO. The data which gets clocked into the event FIFO includes any VMEbus reads of data in the L2 Buffer Space (specified in CDF/DOC/TRIGGER/CDFR/2288), and any write to the Done Register which sets the EOB marker. This Spy mode would be used only if there is no need for the VRC to do data formatting.

______ Connect dual optical cable between Tracer's Event data and Busy Ports to the Taxi-Tester Data and Busy Ports

______ From VASE: Tracer Checkout menu, select **Tracer -> Taxi-Test in Spy Mode** and verify the following:

The test will perform the following**:**

- Make sure the Testclk is driving the Cable Clock to the TRACER.
- Make sure that the "Event Data Taxi Enable" in the Tracer's Control Register is set low.
- Set the "Spy Mode Enable" bit in the Tracer's Control Register.
- Now fill the Event FIFO with sequential data read from some other memory module on the VMEbus - a possible source is the ADMEM's Diagnostic FIFO.
- Readout the Tracer's Event FIFO and verify the match between it and the source.
- Now repeat the fill of the Event FIFO with sequential data read from the other memory module on the VMEbus.
- This time transmit the data to the Taxi-Tester by:
- Enable the Taxi-Tester Module so that it is ready to accept data. (Enable receive mode, clear the FIFO, reset the flags, wordcount, and enable BUSY).
- Now, set the "Event Data Taxi Enable" in the Tracer's Control Register.
- Data will flow from Tracer to Taxi-Tester until the FIFO on Taxi-Tester becomes almost full.
- At this point the Taxi-Tester will send BUSY. Verify that you see the Front Panel WAIT LED turn on.
- In order to clear the WAIT state, read out the FIF0 on the Taxi-Tester until its status is empty - you should observe the sequential data.
- You should see the Event FIFO status flags indicate Empty as well when you read them.
- Make sure that the Violation Flag on the Taxi-Tester remains low.

Spy Mode Test of VMEbus Reads of Tracer's Event Space Registers

- Make sure the Event FIFO is empty - this can be done by toggling software reset or toggling the "Event Data Taxi Enable" bit.

  Reads of the Tracer's "Event Space" registers should be captured by the Event FIFO in Spy mode. These registers include:
  - Word Count Register
  - Event Header Register
  - TSI TAXI Violation Counter Register
  - A's Pattern Register
  - 5's Pattern Register

- With "Spy Mode" enabled and the "Event Data Taxi Enable" bit set low, readout the above registers.

- Now readout the Event FIFO. The contents of the Event FIFO should match exactly with the contents of the registers just read out. Verify this.

Spy Mode Test of VMEbus write to the Tracer's Done Register and setting of EOB (End of Block)

It is possible to append set an End of Block (EOB) marker on the transmitted data stream. This is done by writing to the EOB bit in the Done register. Whenever a logic high is written to this bit, the equivalent of a 33 bit word will be clocked into the Event FIFO. The MSB will be set high and will indicate the EOB. This EOB bit will be passed to the TaxiChip as the 9th data bit, which can then be decoded as EOB by the VRB.

______ Connect dual optical cable between Tracer's Event data and Busy Ports to the Taxi-Tester Data and Busy Ports.

______ From VASE: Tracer Checkout menu, select **Tracer -> Taxi-Test Spy - EOB Test**.

The test will perform the following:

- Make sure the Testclk is driving the Cable Clock to the TRACER.
- Make sure that the "Event Data Taxi Enable" in the Tracer's Control Register is set low.
- Make sure the Event FIFO is empty - this can be done by toggling software reset or toggling the "Event Data Taxi Enable" bit.
- Set the "Spy Mode Enable" bit in the Tracer's Control Register.
- Write to the Tracer's DONE register. Bit 31 must be set in order to cause an EOB.
  The EOB marker cannot be read on the Tracer - it is set only as the data goes to the TAXI link.
- Enable the Taxi-Tester Module so that it is ready to accept data. (Enable receive mode, clear the FIFO, reset the flags, wordcount, and enable BUSY).
- Now, set the "Event Data Taxi Enable" in the Tracer's Control Register.
- One word of data will flow from Tracer to Taxi-Tester.
- Readout the contents of the Taxi-Tester FIFO. There should be on word (four bytes).
- On the fourth byte which is read out, you should see that the ninth bit has been set. This is the EOB marker which we wrote to the Tracer's Done Register.

______ Run the **Tracer -> Taxi-Test Loop Mode Test Sequential Data** for at least 100 loops.

______ Run the **Tracer -> Taxi-Test Loop Mode Test Random Data** for at least 100 loops.

______ Run the **Loop Mode Test of Tracer -> Taxi-Test in Spy Mode** for at least 100 loops.

______ Run the **Tracer -> Taxi-Test in Spy EOB Loop Test** for at least 100 loops.

Test Interrupt functionality

The Clock cable must be connected between the TESTCLK and TRACER as well as the Fiber Optic Cable (**U15** page 9).

______ Within VASE: Tracer Checkout Menu, select **Interrupt Test.**

The test performs the following:

- Enables the Cable Clock and TSIE Start Wait condition on Testclk.
- Enables the Interrupt mode on the TRACER by setting the “Interrupt Mode Enable” bit in the Tracer’s Control Register.
- Sets the “Enable CDF Trigger Signals to backplane” bit in the Control Register
- Connect the Interrupt Handler by doing an RLOGIN to the MVME162 and executing the “inter” routine. This routine will generate an interrupt return vector which must be loaded into the lower 8 bits of the Tracer’s Interrupt return vector.
- Load the Tracer’s Interrupt return Vector at the prompt.
- The test loads the TSIE file START_SCAN.tsi
  Reads the Start Scan Register and verifies that the Start Scan bit is set. All other bits (besides the CDF_TDC_DONE) should be low.
- The setting of the Start Scan bit should generate an interrupt which prints a message to the screen the Interrupt Handler is running on.

Tracer Transition Module Port

The Tracer has a Transition Module Port on it. In order to use this port, one must first write a address to the Transition Port Address Register. The transition module register is then accessible by reading or writing to the Transition Port Read/Write Register.

______ From VASE: Tracer Checkout Menu, select **Transition Card Test**

The test will perform the following:

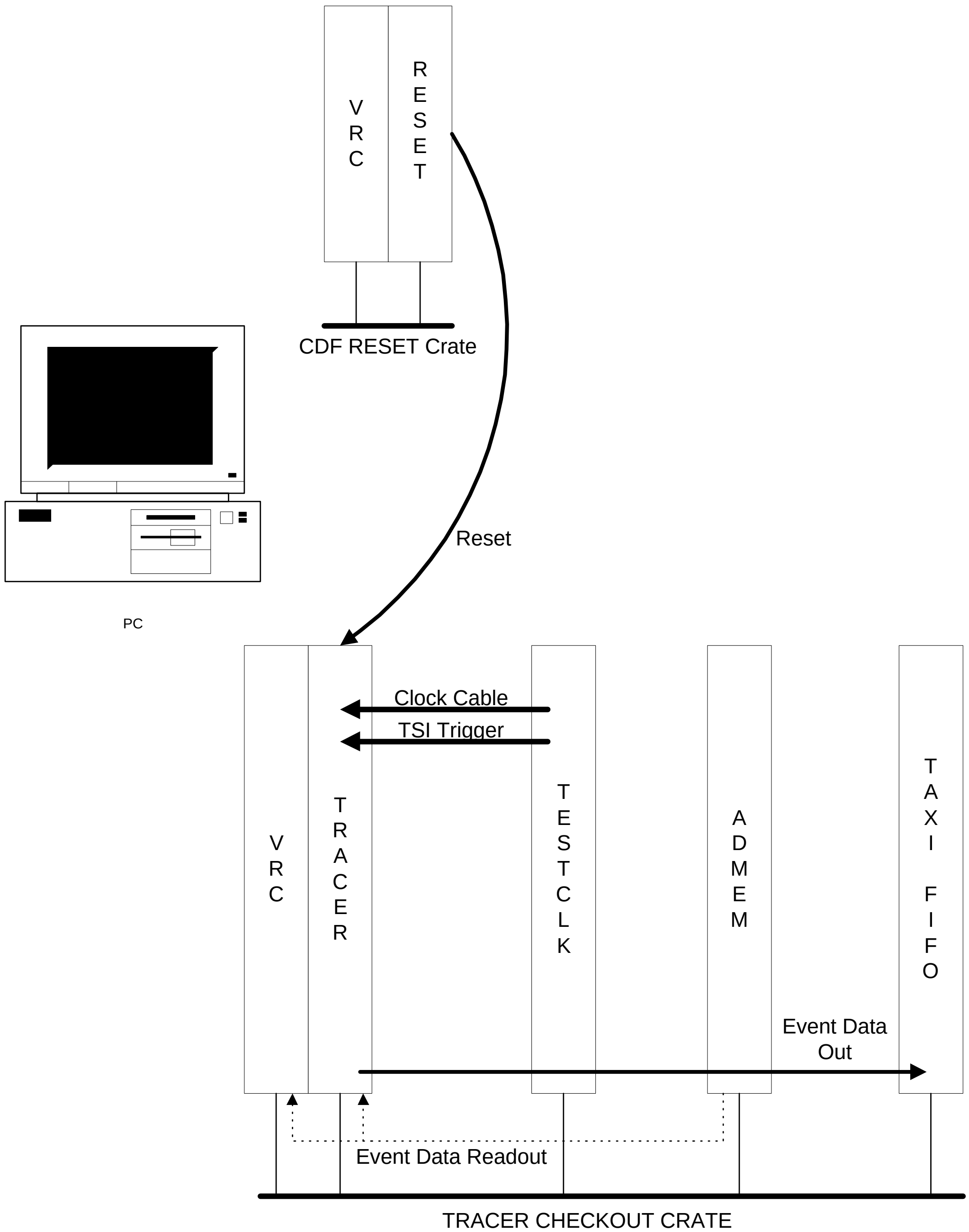
- Writes a unique pattern to each register.
- Reads out each register and compares data.
- Rotates a 1 through a field of 0's in each register.
- Rotates a 0 through a field of 1's in each register.

System Testing with the VRB

The final testing will take place at the System Testing checkout stand. Connect the TRACER to the Testclk module and the VRB.

______ From VASE: Tracer Checkout Menu, select **Tracer Data Loop Test 1.**

______ From VASE: Tracer Checkout Menu, select **Tracer Data Loop Test 2.**


VRC
RESET
CDF RESET Crate
Reset
PC
VRC
TRACER
Clock Cable
TSI Trigger
TESTCLK
ADMEM
TAXI FIFO
Event Data Out
Event Data Readout
TRACER CHECKOUT CRATE