A CMOS Delay Locked Loop and Sub-Nanosecond Time-to-Digital Converter Chip

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Abstract

Phase-locked loops have been employed in the past to obtain sub-nanosecond time resolution in high energy physics and nuclear science applications. An alternative solution based on a delay-locked loop (DLL) is described. This solution allows for a very high level of integration yet still offers resolution in the sub-nanosecond regime. Two variations on this solution are outlined. A novel phase detector, based on the Müller C-element, is used to implement a charge pump where the injected charge approaches zero as the loop approaches lock on the leading edge of an input clock reference. This greatly reduces timing jitter. In the second variation the loop locks to both the leading and trailing clock edges. In this second implementation, software coded layout generators are used to automatically layout a highly integrated, multichannel, time-to-digital converter (TDC) targeted for one specific frequency. The two circuits, DLL and TDC, are implemented in CMOS 1.2μm and 0.8μm technologies, respectively. Test results show a timing jitter of less than 30 ps for the DLL circuit and less than 190 ps integral and differential non-linearity for the TDC circuit.

I. INTRODUCTION

The generation of precise delays with very low jitter is useful for time measurement in particle detector systems. While many solutions use phase-locked loops (PLL's), delay-locked loops offer a straightforward implementation of time-to-digital converters. In designing DLL's, one of the main problems is the phase detector. Unlike the situation in synchronization circuits for telecommunications, the phase detector must distinguish a positive (leading) from a negative (lagging) delay between the relevant features of the two waveforms to be compared. Several solutions have been proposed for this problem [1,2]. This design is proposed as a robust alternative when only one frequency of operation is of interest.

The DLL lends itself for use as a kernel in a number of applications, such as clock pulse alignment and de-skewing, time interval generation for serialization and de-serialization schemes in telecommunications, and time-to-digital conversion. Direct time-to-digital conversion, as opposed to time-to-amplitude conversion followed by a multichannel analyzer, requires excessive clock speed if sub-nanosecond time resolution is to be achieved. An improvement can be made if the clock period is finely divided into smaller intervals; then time intervals, not pulses, are counted. In this work a tapped, electrically controllable delay line is used to obtain edges delayed by 1/32 of the clock period. Precise spacing of the successive pulse edges is achieved by using CMOS delay elements in conjunction with a feedback scheme forming a delay-locked loop.

II. DELAY LOCKED LOOP

An overall block diagram of the DLL circuit is shown in Fig. 1. The tapped delay chain is controlled by a DC voltage generated by the phase detector, the operating principle of which ensures that feedback is always negative. The multiplexer is built along conventional lines, and will not be discussed here. The critical components of the diagram in Fig. 1 are the delay chain and the phase detector.

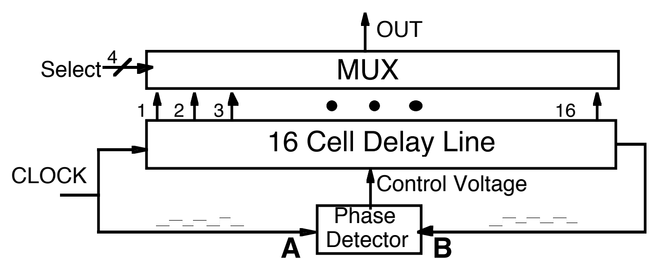

Fig. 1 Block diagram of the DLL chip

A. Delay Chain

The delay chain is a modified version of the one used by Arai *et al* [3]. One cell is depicted in Fig. 2.

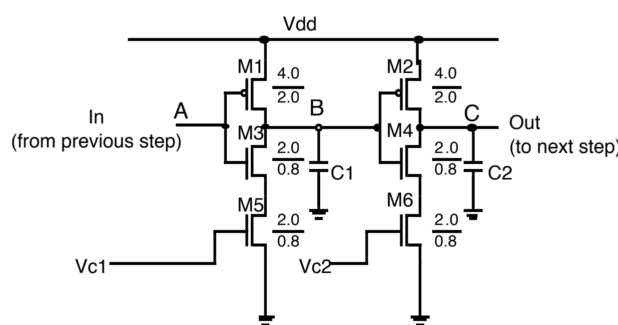

Fig. 2 Delay element unit cell.

During the time when the input of the circuit in Fig. 2 is high, the current available to discharge the parasitic capacitance C1 seen from point B to ground is the current through M5. This current determines the delay between turning on M2 and turning off M4. It can be readily observed that this variable delay acts on the leading edge of the waveform at the output of the inverter M2-M4. A similar line of thought applies to M6 with respect to the rate of discharge of the parasitic capacitance

C2, with the difference that now the current through M6 controls the delay of the trailing edge of the waveform at the output of the circuit. If this cell is part of a chain of *n* similar cells, a pulse delayed by *nt* with respect to the input appears at the output, where *t* is the delay of the cell represented in Fig. 2. This delay is controlled by the gate voltages of M5 and M6. The range of delay can be controlled by appropriately sizing the transistors in the circuit.

B. Phase Detector

The causal relationship between the two waveforms to be compared (A and B in Fig. 1) makes it necessary for the phase detector to distinguish between a phase lag of *a* and a phase lead of $2n\pi$-a. This is distinct from the situation in a PLL, as in PLL's the two waveforms whose phase is to be compared are uncorrelated. The P and N pulses needed to drive the charge pump of Fig. 3 are generated by a phase detector based on the Müller C-element [4].

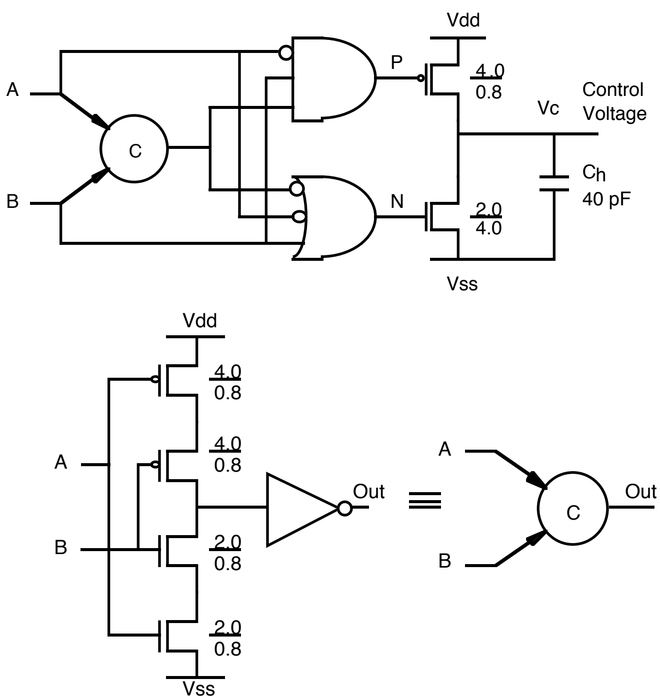

Fig. 3 Complete phase detector

Fig. 4 shows the relevant idealized waveforms for the complete phase detector circuit. It is readily observed in Fig. 4 that the output of the C-element follows whichever of the inputs, A or B, lags the other. The only condition for this behavior is that the two inputs must overlap.

The addition of some simple logic permits the generation of the P and N signals to control the pump that supplies the control voltage V_C for the delay chain.

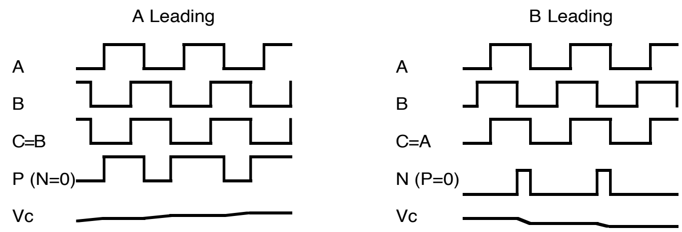

Fig. 4 Idealized waveforms of the phase detector circuit showing the proportional control.

As implemented, the circuit operates on the falling edge of waveforms A and B. Feedback is negative; a positive change in V_C decreases the delay. Under lock, P stays at logic level 1 and N at 0, and V_C only has to change to compensate for charge lost through leakage on the holding capacitor C_h. Very low jitter is thus to be expected.

The DLL uses a 16-element delay line. Care was taken to ensure that the load presented at each tap of the line is identical. This is accomplished with a multiplexer featuring buffered inputs sized to match the delay elements. In addition, the last element in the delay chain is loaded by a dummy cell. A reset-on-power-up circuit is included to provide for proper initialization. This circuit ensures that the chain starts at minimum delay (approximately 18 ns), so that the A and B waveforms in Fig. 4 are certain to overlap.

III. TDC CIRCUIT

A. Dual Edge Phase Detector

For the TDC circuit a pair of the Müller C-element based phase detectors is used. Each phase detector separately locks to the leading and falling edges of the reference clock. The dual edge control allows very long delay chains to be constructed without concern for signal dispersion or extinction due to potentially different propagation speeds of the two clock edges. With additional logic and two charge pumps, this circuit generates two control voltages (Vc1 and Vc2) needed to control the delay chain. The two resulting feedback loops, being of first order, are inherently stable. Similar TDC circuits have been reported previously, but these are based on single-edge control [3,5,6].

B. TDC Implementation

The simplified block diagram of the TDC circuit is shown in Fig. 5. The delay line shown is a 32-element chain of double inverters with a dual phase detector for separately controlling the delay on the leading and falling clock edges. In this variation the control voltages Vc1 and Vc2 separately connect to the control points on M4 and M5 in the delay element.

Simulation results for the propagation delay through the delay element unit cell are shown in Fig. 6. The results are given for Vc1=Vc2.

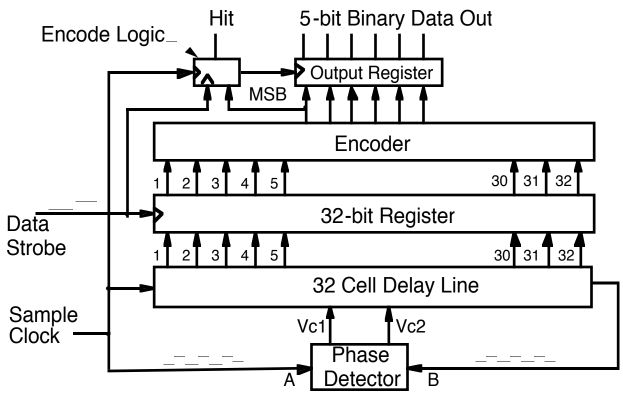

Fig. 5 Block diagram of the TDC chip

C. *Latching Scheme*

Operation of the TDC circuit is shown in Fig. 5. When an asynchronous Data Strobe edge is received, the 32-bit register stores the state of the delay line along the 32 time intervals into which the clock period is divided. This information is encoded and latched one cycle later. The encoded output represents the time-of-arrival of the Data Strobe edge with respect to the clock edge.

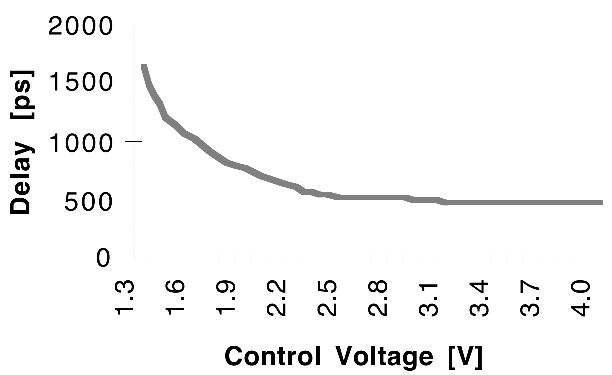

Fig. 6 Simulation of the delay through a unit cell as a function of the control voltage for Vc1=Vc2.

IV. Test Results for the DLL Circuit

The DLL circuit is implemented in a 1.2µm, double-metal, single-poly CMOS technology. Tests were carried out using a fast pulse generator and a high resolution time interval counter. The loop locks for clock periods between 17.97 ns (55.6 MHz) and 30.08 ns (33.2 MHz). In this frequency range, the standard deviation of the delay through a single element is less than four tenths of the unit delay. Delay lock time is 2.5 µs and time jitter is 50 ps. Because the measured jitter of the pulse generator is 37 ps, a reasonable value for the jitter of the DLL circuit should be below 30 ps.

V. Test Results for the TDC Circuit

A TDC chip was built using a standard 0.8µm CMOS process with a single poly-silicon layer and three metal layers. The chip was tested using a fast pulse generator, a high resolution time interval counter, and a logic analyzer. The loop is stable for clock periods, T , between 16.89 ns and 25.15 ns, giving least significant bits (T/32 = 1 LSB) between 0.53 ns and 0.79 ns. A plot of differential (DNL) and integral non-linearity (INL) versus clock period is shown in Fig. 7. The DNL, measured as the deviation in code width from one LSB, is corrected for gain error [7]. The INL is defined as the deviation of the center-of-code from the best-fit straight line [7]. Both DNL and INL are less than 190 ps throughout the frequency range.

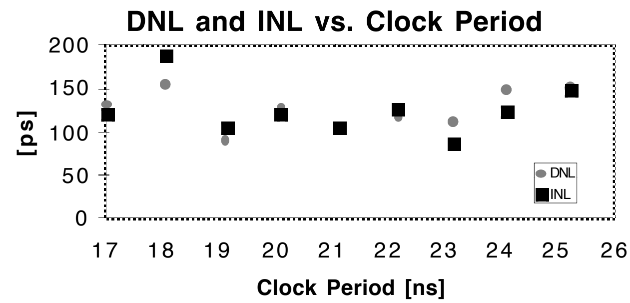

Fig. 7 Plot of TDC Integral and Differential Non-Linearity.

VI. Conclusions

Loop performance is limited at the high end of the frequency range by the minimum delay achievable within the available technology, and at the low end by the degree to which control transistors M4 and M5 can be current-starved.

If a very long chain is desired, the inevitable asymmetries in the delay times for the leading and the falling edge of the clock pulse (assumed above to be a symmetrical square wave) will eventually lead to pulse extinction. This difficulty can be circumvented by using a double loop configuration, where one loop controls the leading edge of the delayed pulse and the other the falling edge.

References

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