MIL-STD-1553B DOD Interface Standard Protocol

Hardware and Software Support in D0 VME Local Stations

Protocol Standard

Hardware

- D0 1553 Rack Monitor RT
- VME 1553 Controller Board
- VME Local Station

Software Support

- Command blocks
- Command queue
- Data Access Table
- Settings: Analog, digital
- 1553 Test Page

CDAQ direct access

D0 Downloading

Protocol Standard

Defined by DOD

Used in aircraft

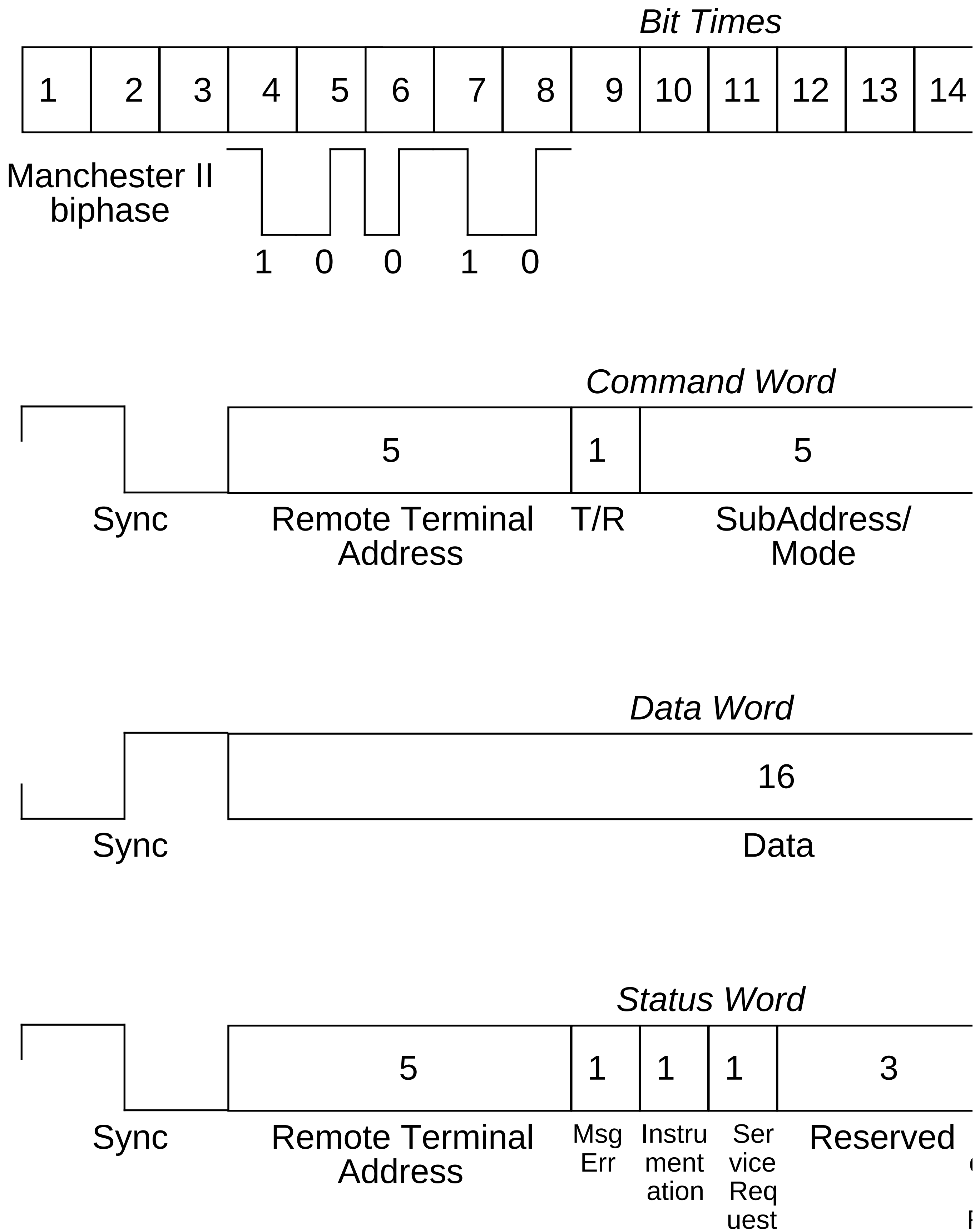
Single shielded twisted pair cable

Transformer-coupled: Manchester II biphase

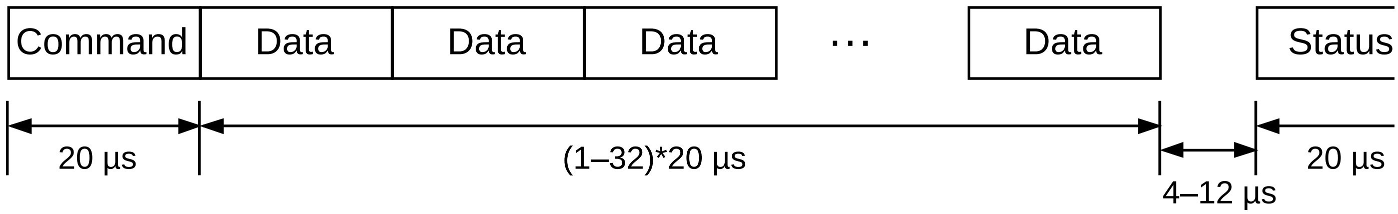
Master-slave protocol: commercial chip support

- Bus Controller
- Remote Terminal (up to 30)

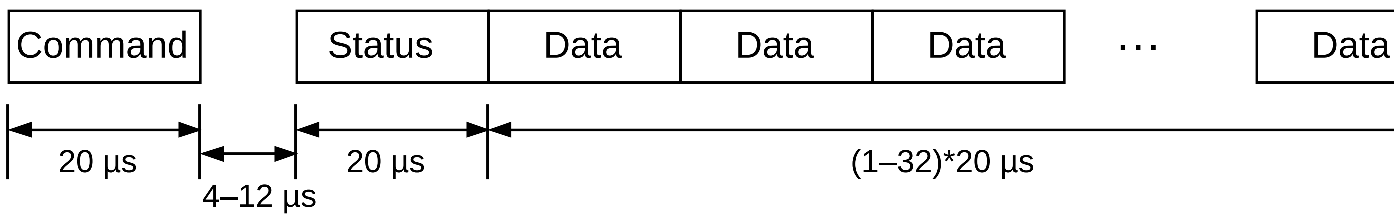
1 MHz serial: 20 μs per 16-bit data word


Bit Times
1
2
3
4
5
6
7
8
9
10
11
12
13
14
Manchester II biphase
1 0 0 1 0
Command Word
5
1
5
Sync
Remote Terminal Address
T/R
SubAddress/ Mode
Data Word
16
Sync
Data
Status Word
5
1
1
1
3
Sync
Remote Terminal Address
Msg Err
Instru ment ation
Ser vice Req uest
Reserved

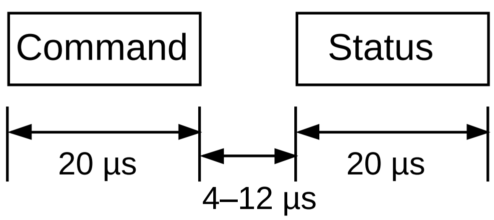
Controller to RT Transfer (T/R=0)



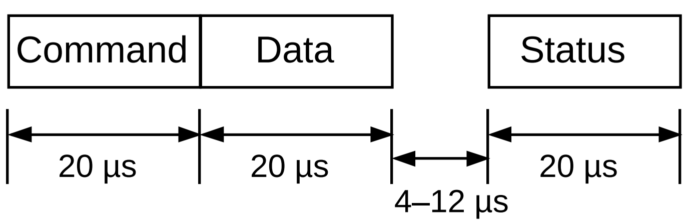
RT to Controller Transfer (T/R=1)



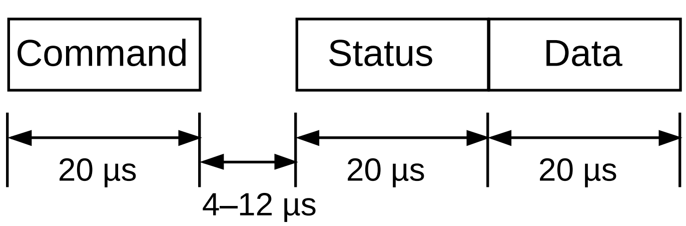
Mode w/o Data



Mode w/ Data (T/R=0)



Mode w/ Data (T/R=1)



D0 1553 Rack Monitor

Remote Terminal

SubAddress	*T/R*	*SubSystem*
1–8	0/1	Analog 8-channel 12-bit D/A
16–19	0/1	Digital 4-words I/O
20	1	Analog 64-channel 12-bit A/D
30	1	Status/ID word
31	0	(mode=17) Initial A/D channel#

VME 1553 Controller Board

Stereo controller

Each controller chip uses DMA to
access its own 64K-byte non-volatile memory

Executes one command, interrupts CPU

Error status word returned from RT

Controller error status word

VME Local Station

Hardware complement

- VME 68020 CPU board
- 1 MB non-volatile memory
- Token ring interface
- Crate utility board
- 1553 Controller board

Operates synchronously at 15 Hz

- Update data pool (24 ms for 1200 words)
- Reply to active requests that are due
- Scan for alarms (10 ms for 370 channels + 200 bits)
- Run current Page application

1553 I/O hidden from users, historically

- Analog channels—A/D and D/A
- Digital bits, bytes

Software Support

Command Blocks in controller memory

Pre-defined structures DMA-accessed by controller

Command queue in controller memory

Command Blocks in Controller Memory

```
N MEMORY DUMP     02/05/98 0709
0752:200500 78A2 13F1 0000 1000
0752:200508 0000 0000 0000 0000
0752:200510 0000 0000 0000 0000
0752:200518 0000 0000 0000 0000
0752:200520 0000 0000 0000 0000
0752:200528 0000 0000 0000 0000
0752:200530 0000 0000 0000 0000
0752:200538 0000 0000 0000 0000
0752:200540 0000 0000 0000 0000
0752:200548 0000 0000 0000 0000
0752:200550 0000 0000 0000 0000
0752:200558 0000 0000 0000 0000
0752:200560 0000 0000 0000 0000
0752:200568 0000 0000 0000 0000
0752:200570 0000 0000 0000 0000
0752:200578 0753 C88F BEA4 9005

0752:200580 78A2 1680 1000 51F1
0752:200588 C252 52F3 3F34 BE25
0752:200590 B346 1A97 1C58 1A29
0752:200598 1A7A 1B4B 1BAC 1B0D
0752:2005A0 206E 214F 1B60 1531
0752:2005A8 1482 13D3 1304 1295
0752:2005B0 11D6 1177 10E8 0B59
0752:2005B8 0ABA 0A6B 09EC 098D
0752:2005C0 090E 08EF 08D0 0000
0752:2005C8 0000 0000 0000 0000
0752:2005D0 0000 0000 0000 0000
0752:2005D8 0000 0000 0000 0000
0752:2005E0 0000 0000 0000 0000
0752:2005E8 0000 0000 0000 0000
0752:2005F0 0000 0000 0000 0000
0752:2005F8 06D3 C88A BEA4 80F3

N MEMORY DUMP     02/05/98 0711
0752:201680 38A2 2641 2000 FFFE
0752:201688 0000 0000 0000 0000
0752:201690 00A2 2241 FFFE 2000
0752:201698 0000 0000 0000 0000
0752:2016A0 0000 0000 0000 0000
0752:2016A8 0000 0000 0000 0000
0752:2016B0 0000 0000 0000 0000
0752:2016B8 06D3 9FB8 CE2F 8EE8
```

Command Queue in Controller Memory

4K-bytes

Accessed by software task/interrupt code

```
N MEMORY DUMP      02/05/98 0916
0752:20F000 00F0 00F0 00F0 0F00
0752:20F008 0010 1553 0001 5400
0752:20F010 1880 1001 0019 383C
0752:20F018 18C0 1001 0019 383E
0752:20F020 1901 1001 0019 3840
0752:20F028 1941 1001 0019 3842
0752:20F030 1981 1001 0019 3844
0752:20F038 19C1 1001 0019 3846
0752:20F040 1A01 1001 0019 3848
0752:20F048 1A41 1001 0019 384A
0752:20F050 1A81 1001 0019 384C
0752:20F058 1AC1 1001 0019 384E
0752:20F060 1B01 1001 0019 3850
0752:20F068 1B41 1001 0019 3852
0752:20F070 1B81 1001 0019 3854
0752:20F078 1BC1 1001 0019 3856
0752:20F080 1C01 1001 0019 3858
0752:20F088 1C41 1001 0019 385A
0752:20F090 1C81 1001 0019 385C
0752:20F098 1CC1 1001 0019 385E
0752:20F0A0 1D00 1001 0019 38A0
0752:20F0A8 1D41 1001 0019 38D0
0752:20F0B0 1E00 1010 0014 7000
0752:20F0B8 1E10 1010 0014 7010
0752:20F0C0 1E20 1010 0014 7020
0752:20F0C8 1E30 1010 0014 7030
0752:20F0D0 1E41 1010 0014 7040
0752:20F0D8 1E51 1010 0014 7050
0752:20F0E0 1E61 1010 0014 7060
0752:20F0E8 1E71 1010 0014 7070
0752:20F0F0 1700 1001 0019 3830
0752:20F0F8 1740 1001 0019 3832
0752:20F100 1780 1001 0019 3834
0752:20F108 17C0 1001 0019 3836
```

```
0752:20F110 1800 1001 0019 3838
0752:20F118 1840 1001 0019 383A
0752:20F120 1880 1001 0019 383C
0752:20F128 18C0 1001 0019 383E
0752:20F130 1901 1001 0019 3840
0752:20F138 1941 1001 0019 3842
0752:20F140 1981 1001 0019 3844
0752:20F148 19C1 1001 0019 3846
0752:20F150 1A01 1001 0019 3848
0752:20F158 1A41 1001 0019 384A
0752:20F160 1A81 1001 0019 384C
0752:20F168 1AC1 1001 0019 384E
0752:20F170 1B01 1001 0019 3850
0752:20F178 1B41 1001 0019 3852
0752:20F180 1B81 1001 0019 3854
0752:20F188 1BC1 1001 0019 3856
0752:20F190 1C01 1001 0019 3858
0752:20F198 1C41 1001 0019 385A
0752:20F1A0 1C81 1001 0019 385C
0752:20F1A8 1CC1 1001 0019 385E
0752:20F1B0 1D00 1001 0019 38A0
0752:20F1B8 1D41 1001 0019 38D0
0752:20F1C0 1E00 1010 0014 7000
0752:20F1C8 1E10 1010 0014 7010
0752:20F1D0 1E20 1010 0014 7020
0752:20F1D8 1E30 1010 0014 7030
0752:20F1E0 1E41 1010 0014 7040
0752:20F1E8 1E51 1010 0014 7050
0752:20F1F0 1E61 1010 0014 7060
0752:20F1F8 1E71 1010 0014 7070
```

Data Access Table

List of instructions

Directs updating of data pool

```
N MEMORY DUMP     02/05/98 0926
0752:101000 7F00 0001 0000 0000
0752:101008 0000 0000 0000 0000
0752:101010 0C00 0000 0020 0500  Queue 2 commands,
controller #0
0752:101018 0000 0000 0080 0002
0752:101020 0C00 0200 0021 0500  Queue 2 commands,
controller #1
0752:101028 0000 0000 0080 0002
0752:101030 0C00 0020 0020 0600  Queue 30 commands, #0
0752:101038 0000 0000 0080 001E
0752:101040 0C00 0220 0021 0600  Queue 30 commands, #1
0752:101048 0000 0000 0080 001E
0752:101050 0C05 0020 0020 1500  Queue 32 commands, #0
0752:101058 0000 0000 0040 0020
0752:101060 0C05 0060 0021 1500  Queue 32 commands, #1
0752:101068 0000 0000 0040 0020
0752:101070 0C05 00A0 0020 1D00  Queue 2 commands, #0
0752:101078 0000 0000 0040 0002
0752:101080 0C05 0100 0021 1D00  Queue 2 commands, #1
0752:101088 0000 0000 0040 0002
0752:101090 0C00 0700 0020 1E00  Queue 8 commands, #0
0752:101098 0000 0000 0010 0008
0752:1010A0 0C00 0708 0021 1E00  Queue 8 commands, #1
0752:1010A8 0000 0000 0010 0008
0752:1010B0 0E11 0000 0000 0000  Await completion,
post-process
0752:1010B8 0000 0000 0028 0002
0752:1010C0 0405 0000 0019 3000  Copy digital into data
pool
0752:1010C8 0000 0000 0000 0180
0752:1010D0 1D00 0000 0000 0000  Execute local
applications
0752:1010D8 0024 0004 00E5 0000
0752:1010E0 0300 07FF 0014 7FF2  Memory word
0752:1010E8 0000 0000 0002 0001
0752:1010F0 1A00 07C0 0000 0F35  Memory byte
```

```
0752:1010F8 0000 0000 0002 0001
```

Settings

Analog

Digital bits, bytes, words

All settings one-word data transfers

Performed with wait, check error status

1553 Test Page

Page application runs in local station

Accessible via little console or via “Page G”

User prepares list of commands to be executed at 15 Hz

Counts and displays errors

Software builds entire command block

Queues pointer to command block to command queue

Awaits completion

Collects error status

CDAQ listype access recently added: 1553 *not* hidden

Ident includes controller memory address, command

D0 Downloading

CDAQ protocol

Supported via Local application

Special listype setting for 1553 block transfer

Setting acknowledgment delayed

Block transfer queue

LA returns ack upon completion of transfer

Host downloading should use multiple active settings to achieve maximum efficiency of downloading transfers