4 Preshower Front End Electronics and Trigger System

The Preshower Front End Electronics, PS FE, and Trigger system includes all of the Forward Preshower channels and the Central Preshower stereo channels. Some of the main features of the system are as follows.

The Preshower System

1 Includes all of the Forward Preshower channels.
2 Includes Central Preshower stereo channels.
3 The CPS Stereo has no L1 trigger capabilities.

L3 Readout

1 The analog signal from each strip is split and input into a HIGH and a LOW gain channel. Digitized values are available to L3 only. Discriminator outputs are used for L1 and L2.
2 The HIGH and LOW gain channels for a given strip are input into two different MCM's. (Note for the CPS Axial in the CFT FE both are input into one.) Thus the HIGH gain channels can have different SIFT thresholds and gains and SVX range than the LOW.
3 Each channel has several gain switches that are set dynamically and are independent for HIGH and LOW gain channels.
    A The SIFT threshold gain
    B The SIFT analog gain
    C The fC/count setting of the SVX2.
4 The HIGH and LOW gain channels each have one discriminator output.

PS Trigger System

1 Provides the means for triggering at level 1 on the information from the FPS detectors. (Central L1 is part of the CFT system.)
2 FPS North is isolated from FPS South at the L1FPSTM.
3 Supplies information for the level 2 Preshower Trigger Preprocessor, PSpp, from FPS & CPS Stereo. (CPS Axial comes from CFT system.)

For the L1 FPS Trigger

1 Clusters are tagged with the absence or presence of a MIP in the upstream layers to distinguish between electrons and photons.
2 A loose match is required between clusters found in the U and the V layers.
3 Counts the number of clusters found independently in N/S.
4 The numbers of clusters found is forwarded to the FPS Trigger Manager, FPSTM, for the global L1 decision.

For the L2 PS preprocessor

1 Pipelines cluster information indexed by edge strip and width in the forward and central. FPS & CPS Stereo.
2 Upon the receipt of a L1 accept, bit extends strip address and forwards information to the PSpp. FPS & CPS Stereo.

A block diagram of the components of the system is shown in Figure 1. There are two sets of front-end electronics boards, FE, in several crates located above the VLPX cryostat in the detector platform. These boards receive the analog signals from the VLPC's and process them for the L3 readout, shown as the Sequencer and VRB crates, and for the L1 and L2 triggers. In the center of figure 1 is the Concentrator system. This receives the L1 and L2 information from each of the FE boards, concentrates it and sends it on to the L1 and the L2 triggers.

The location of the VLPC cassettes for the FS system is shown in Figure 2. The FPS FE boards are located in two crates at each end of the row of cassettes on the platform. The CPS Stereo FE Boards are located in two smaller crates located just inboard of the FPS crates.

The FPS FE and Trigger systems are discussed in section 4.1, and the CPS Stereo FE and Trigger systems are discussed in section 4.2.

4.1 FPS FE Electronics and Trigger System

The Forward PreShower FE Electronics, FPS FE, provides the L3 read-out and the Trigger System provides the means for triggering at level 1 on the information from the FPS detector and supplies information for the level 2 Preshower Trigger Preprocessor, L2PSpp.

For the L1 FPS Trigger the system forms a count of the number of clusters found. These clusters are tagged with the absence or presence of a MIP in the upstream layers to distinguish between electrons and photons and with a loose match between clusters found in the U and the V layers. The numbers of clusters found is forwarded to the FPS Trigger Manager, FPSTM, for the global L1 decision. [xxx trigger ref]

For the L2 preprocessor the system pipelines cluster information indexed by strip number and width, and upon the receipt of an L1-accept compresses, sorts and forwards this information to the L2PSpp.

4.1.1 Functional Description

During L1 live running the operation of the system can be separated into four function blocks as shown in figure 3. In each of the FE boards clusters are found Independently for each of the u and v back layers. Both the location and width of each cluster is found. See figures 5 and 6. For each cluster found a mask whose position and size are dependent on the cluster position and width, is placed over the forward layer. See figure 7. If any strip within that mask has a MIP the cluster is tagged as an e-type cluster, else it is tagged as a gamma type cluster. Then a loose u/v layer match is made. See figure 8. If the u-layer has at least 1 e-cluster and the v-layer has at least 1 e-cluster the number of clusters for both u and v layers are recorded and the cluster indexes stored. The same matching is done for the gamma-clusters. The numbers of clusters in 4 categories (u/v and e/gamma) are then sent to the preshower receiver, PSRC, board. The list of clusters indexed by edge strip and width is placed in a pipeline at the FE for use by the L2. The maximum number of clusters that are stored at each FE is 32 total, which can be any mixture of u- and v-layer clusters.

The set of 4 sums from each FE board are sent over fast serial links to the Concentrator system. There the sets of 4 sums from 32 FE boards are summed into a single set of 32 sums, which in turn are sent over 4 fast serial links to the Forward Preshower Trigger Manager, FPSTM. The 32 sums represent the number of clusters per quadrant (4) for e/gamma (x2) for u/v-layer (x2) and for North or South end (x2).

Whenever an L1-accept is received the system stops normal processing and shifts to L2 and L3 readout modes. The functional description for this can be divided into three blocks as shown in figure 2. In each FE the data for the correct crossing is pulled out of the L2 pipeline and sent to the FPS RC boards. Because it is important for monitoring the operations of the trigger, this data is also placed into the virtual SVX, VSVX, for inclusion in the L3 readout stream. Information from the L1 for this crossing is also in the VSVX. Independently at each FE the analog values are pulled out of each SVX pipeline, digitized and read out for the L3. The L3 readout system (with the exception of the VSVX) is shared with the silicon system and is not detailed in this document.

The arrival from the FE of L2 type data switches the Concentrator system over to L2 mode. In this mode it takes the lists of found clusters from each FE, and combines and truncates them, and sends them on to the Preshower preprocessor, PSpp.

4.1.2 System Architecture

4.1.2.1 Geometry and Definitions

The mechanical properties of the FPS system are:

1. The FPS is divided into two parts, North and South,
2. The FPS North(South) is divided into 16 sectors which are separate physical modules that overlap slightly and each contain four layers of scintillating strips,
3. Layers 1 & 3 (counting from interaction point) are u stereo, 2 & 4 are v,
4. Layers 1 & 2 are the forward layers and detect single charged particle deposition, Layers 3 & 4 are the backward layers and detect showers,
5. Layers 1 & 2 have 101 strips each, Layers 3 & 4 have 135 strips each.

Electronic and Trigger properties are **defined** as:

1 The FPS L1 Trigger is divided into two parts, North and South, each with 1(2) TM(s) and 16(32) AND/OR Terms;
2 Each detector sector is a stand-alone trigger sector, Therefore there are 16 + 16 trigger sectors;
3 Each trigger sector is contained on one FE board;
4 The FE boards are arranged in 2 FE crates, there is no data sharing between FE boards;
5 The Concentrator and L1 TM are the same hardware as for the CFT.

4.1.2.2 Trigger Sectors

For a high speed trigger such as that needed for level 1 it is necessary to have all the data needed to make a trigger decision concentrated at one location. The FPS trigger achieves this by dividing the global trigger into a series of local triggers each of which is independent of one another and located on a single FE board. Since each FE board is self contained no data sharing across the back plane is required.

The exact details of the L1 algorithm and results on the MC studies which stimulated and verified the design are given elsewhere.[xxx MC ref, algorithm ref.]

4.1.2.3 Hardware Inventory

<u>The FPS/CPS Trigger system has;</u>

1 GS with SCL
1 VRB Crate
1/2 Sequencer Crate
2 FPS Front End Crates, 8-cassette crates
2 CPS Front End Crates, 3-cassette crates
32 FPS FE Boards, 16 RHB & 16 LHB
10 CPS FE Boards, 5 RHB & 5 LHB
1 Concentrator Crate
1(2) TM Crate - 16(32) AND/OR trigger terms

<u>Each VRB crates has;</u>

1 VRB Controller board with SCL receiver
11 VRB Boards
11 VEPA Boards
44 Optical link receivers (from Seq)

<u>Each ½ Sequencer crates has;</u>

½ Sequencer Controller Board with SCL receiver
11 Sequencer boards
44 Optical link transmitters (to VRB), 4 per board

44 50-Conductor Cables, 4 per board

Each FPS FE crate has;
8 Right Hand FPS FE Trigger Boards
8 Left Hand FPS FE Trigger Boards
16 BP Connectors for 50-Conductor Sequencer Cables
1 BP Connectors for Cryo I/O

Each CPS FE crate has;
3(2) Right Hand FE CPS Trigger Boards
3(2) Left Hand FE CPS Trigger Boards
6 BP Connectors for 50-Conductor Sequencer Cables
1 BP Connectors for Cryo I/O

Each FE board has;
1 Serial link to Concentrator crate
1 1553 Node to receive down load
2 SVX Strings
1 Interface for 50-Conductor Cable from Sequencer
2 Analog and Serial Clock generator
16 MCM, each with 1 SVX and 4 SIFT chips

Each Concentrator crate has;
1 CC, Controller board
4 L1CN, L1 Concentrator Boards - for FPS
4 L2CN, L2 Concentrator Boards - for FPS
2 L2CN - for CPS Stereo
4 RC, Receiver Boards - for FPS
2 RC - for CPS
4 Cu links to L1PSTM
6 Glass links to L2PSpp

4.1.2.4 Hardware description

Figure 1 shows the overall data flow of the system. It could also be considered a crate level diagram of the system since each box corresponds to one or more crates.

The data starts in each of the 32 FE boards located on the VLPC cryostat in the center platform. See figure 2. To be a deadtimeless trigger the FE board must accumulate all the data for one crossing within that crossing and it must transmit the results of its calculation off the board within one crossing's time. Within the FE board the data for several crossings in different states of processing is stored in a large pipeline. The resultant data is transmitted off the FE board on a fast serial link. This link, which serves a dual function, goes to one crate on the west platform. During L1 live time this second link carries cluster counts from the FPS FE, and during L2 readout carries the list of found clusters.

4.1.2.4.1 FE Boards

4.1.2.4.1.1 Analog Design

Each FE board receives the VLPC output from one physical sector of the detector. Each of these wedges has two forward layers with 101 strips each and two backward layers with 135 strips each. Figure 9 shows the routing of the signals on the FE board. On the right hand side of the drawing are depicted the 16 MCMs that receive the analog signals. The signals into the MCMs are arranged by layer and gain. The 135 L4 channels for example are split into HIGH and LOW gain channels. The LOW gain channels are routed to MCMs 7 and 8, while the HIGH gain channels are routed to MCMs 15 and 16. This layer separation works in the MCMs because they have 72 available channels each. The VLPC Cassette Modules, however, only have 64 channels each. Therefore the mapping into the cassettes is not as simple. The numbers of each layer in each Module can be seen in the figure.

The forward strips are used to detect single particles before the lead converter and the backward strips are used to detect showers originating in the lead converter. The showers in the backward strips produce a large dynamic range of signals from the VLPC. To cover that range for the digitization of the signals and for the triggers, the charge from each strip is split into a HIGH gain and LOW gain channel on the FE board. This charge division is accomplished by putting a capacitive charge division circuit on each channel as shown in figure 11. The signal from the VLPC in carried on the Bias return, which is at analog ground and the Bias supply is at a DC potential of about -6.5V. The bias is generated on the FE board independently for each cassette module. If a VLPC pixel fails by going to small resistance that pixel will warm up and radiate infrared light. This light will be seen in neighboring pixels and be output as noise. The current limiting resistor, which completes the DC circuit, prevents this. The AC circuit is completed by capacitively coupling the two SIFT chips to the bias return line. The value of that capacitor will determine how much of the total available charge is seen by each SIFT chip. Since the SIFT chip has a virtual impedance a large drain capacitance is required to balance the circuit. The drain capacitance is about 100 fC, while C1 and C2 are smaller and are about the ration of C1:C2::1:8. See table xxx for the values of the charge division. If you neglect the stray capacitance on the circuit board and the input impedance of the SIFT chip the gain of input channel 1 is;

$$G1 = C1 / (C1 + C2 + Cdrain)$$

The high gain channels are sent to the high gain set of MCM's and the low gain to a separate set of low gain MCM's. Inside each MCM are four SIFT chips and a single SVX-2e chip. All four SIFT chips share common clock lines and most voltage lines. The SIFTs are divided into two sets of two for the discriminator threshold and gain settings and the analog output gain setting.

Each MCM
72 Channels
4 SIFT chips
1 SVX-2e chip

36 channels with a common >>
SIFT Discriminator Threshold
SIFT Discriminator gain setting - x1 or x2
SIFT Analog Gain setting - x0.2 or x0.4

Figure 14 shows a cartoon of the interior of an MCM. Each SIFT chip has 18 active channels. The analog outputs of the four SIFT chips are sent to a single SVX chip which has 72 of its 128 channels bonded. Two sets of control lines enter the MCM, which allows for differing operation for the two groups of 36 channels. Figure 12 shows a simplified diagram for a single channel in the MCM. The signal enters the SIFT chip, is amplified and buffered before being shared by the analog and digital arms of the chip. In the digital arm the voltage from the preamp is compared to an externally applied threshold voltage. When the input voltage exceeds this threshold the output of the discriminator goes high. The discriminator output is latched with the rising edge of the HOLD signal onto an output driver. The output of the discriminator returns to zero when the preamp is next reset while the latch remains high until the next HOLD. The latch is present because If the input signal is near threshold or arrives near the end of the crossing cycle the discriminator will not go high until just before the reset and thus remain high for a short time. The latch and driver guarantee that the SIFT chip output to the logic remains stable for and entire cycle. The gain switch on the discriminator adds or subtracts a second bypass capacitor to the discriminator amplifier. This switch is not shown in the figure.

In the analog arm the output of the preamp is stored on one or two capacitors in parallel. The voltage is moved onto the capacitor(s) with the closure of the first switch, the HOLD switch, and transferred out to the SVX with the closure of the second, the READ switch. The HOLD switch is closed for a short time at the end of the crossing cycle when the preamp has integrated the maximum charge from the input. It is then opened and the READ switch is closed. The HOLD and READ switches are not both closed at the same time. Since the HOLD is open when the READ is closed the SVX preamp is isolated from the SIFT preamp and the READ can take place under the SIFT preamp reset. This overlapping operation results in about 30ns extra integration time per cycle. The phase between the SVX and SIFT clocks must be maintained so that the SIFT READ occurs during the active integration time of the SVX chip. This is done by taking the 53/7 MHz SVX clock which originates in the Sequencer and using it to generate all of the SIFT clocks on the FE board.

4.1.2.4.1.2 Charge Pileup

The preamplifier in the SVX chip is not reset every crossing since it needs a large fraction of a microsecond to settle. Therefore it is only reset during a time when beam crossings are not seen by the detector. Initially there will be three super-bunches in the Tevatron and eventually there may be only one. Between preamplifier resets the SVX sees all of the charge from all particles traversing a given scintillation stip. The average amount of charge into the SVX per turn can be calculated from M.C. data. This value is important because the digitized output of the SVX is the difference of the integrated charge after a pipeline stage minus the integrated charge before that stage. The SVX preamplifier saturates at about 450 fC and once it has reached saturation all subsequent pipeline stages will digitize to zero, the pedestal value. Also as the preamplifier approaches saturation a single hit may push the preamplifier into saturation resulting in a truncated digitized value.

From D0-note/PHYS-3493 figures 5.32(5.33) the occupancy in upstream (downstream) strips for an event plus 2 minimum bias events is about 7%(1.2%). However, the occupancy of the backward layer is given for a threshold cut of 5 MIPS well above the single-particle-track energy deposit. The forward threshold is at about the single-particle energy deposit level so therefore the backward occupancy should be about the same as the forward. One particle deposits a minimum of 30 fC in the forward and 96 fC in the backward. (0.3MIP/1MIP – 15pe/MIP – 40K VLPC Gain) For the backward layers this is a low estimate because the tails of a shower are 1-3 MIPs and several strips wide while the peak is from 10 to 35 MIPS. Putting these numbers together we get:

	Forward Layers			**Backward Layers**		
Occupancy	7%			7%		
MIPs	0.3	30	fC	1	96	fC
average charge		2.1	fC		6.7	fC
charge div	100%	2.1	fC	30%	2.0	fC
SIFT gain	0.4	0.84	fC	0.4	0.8	fC
Crossings	40	34	fC		32.3	fC
	120	101	fC		97	fC

In the forward all of the charge is input into a single SIFT channel and transferred to the SVX with a gain of 0.4, which results in 101 fC into the SVX per turn. In the backward the HIGH gain channel has a charge split of 30% and a gain of 0.4 into the SVX which results in 97 fC into the SVX per turn. This is a crude estimate and needs MC results, but indicates that a once a turn reset for the SVX is probably sufficient.

From the M.C. data the amount of energy per strip per crossing was histogrammed and the probability density for a given energy per strip per crossing was found. This plot for the forward or MIP layers is seen in figure xxx and for the backward or shower layer in figure xxx. For both of these plots there are two minimum bias events per crossing, each of which is a dijet of 2 – 5 GeV.

The average was also looked at where one of the two dijets was a high energy dijet of 50 – 400 GeV. The increase in the average energy was not significant.

	Forward Layers		Backward Layers	
Average MeV		0.05		0.11
MIPs	0.8	0.07		0.14
average charge		6.5 fC		13.2 fC
charge div	100%	6.5 fC	30%	4.0 fC
SIFT gain	0.4	2.60 fC	0.4	1.6 fC
Crossings	40	104 fC		63.4 fC
	120	311 fC		190 fC

Table xxx – Calculation of charge pileup in the SVX for 1/3 and 1 turn, when the average charge is taken as the amount from TWO minimum bias interactions.

The above table calculates the total charge pileup from the M.C. inputs. The top row has the found average energy per strip per crossing in MeV. From the test beam and M.C. work it was determined that 1 MeV = 0.8 MIPs in the FPS strips. The second row shows the averge in MIPs. Using a VLPC gain of 40K and a value of 15 p.e. per MIP the average charge is calculated in line 3. In the forward layer all the charge is sent to the MCM, in the back the charge is divided with the larger channel getting 30%. In the SIFT the charge is de-amplified finally gets to the SVX. Then the average per crossing is multiplied by 40 crossing for one third of a turn and 120 crossings for a complete turn.

As an estimate of the uncertainty the p.e. per MIP may range from 15 up to 20 and the M.C. results could have an equally large uncertainty. Therefore the total charge per turn could be 75 to 100 fC larger or smaller.

It is seen in the table that when running with an average of TWO interactions per crossing that the SVX will need to be reset THREE times each turn. At a lower luminosity the resets may be made once each turn. Note that only the luminosity matters and not the number of crossings, 36 versus 118, since we are calculating on a per turn basis.

4.1.2.4.1.3 L3 Readout

The SVX2e chips in the 16 MCMs are connected together into two strings of 8. See figure 13. The two strings are read out by one channel of a sequencer board. The L3 readout for these SVX chips is identical as for those in the silicon detector. Please see reference [xxx] for more details on the Silicon L3 readout system. For the FPS the Sequencer and VRB are in their own crates and form a single and independent geographic sector, GS.

4.1.2.4.1.4 Trigger Logic

While the trigger outputs of the MCM are latched they are read into the trigger logic. Within this logic the clusters are formed and the forward match is made to distinguish between electron and photon candidate clusters. See figure 10. After the clusters are found in the u and v layers a loose match is made. For the L1 trigger the number of matches is recorded, for the L2 the ID of the clusters is stored. The cluster counts are immediately passed to the serial link transmitter and sent the concentrator system. The cluster IDs are stored in a pipeline for retrieval after a L1 accept. When a L1 accept is received the inputs from the MCMs are ignored and the list of cluster IDs is sent over the serial link to the Concentrator system.

The details of the coding within the trigger logic to find clusters and determine their width and produce an ID are given elsewhere.[4][?]

4.1.2.4.2 Data Transfer

4.1.2.4.2.1 L1 Transfer

Each FPS FE board as discussed above forms clusters in each of the backward u and v strips. During L1 live time the number of matched clusters made in each of e/gamma by U/V is sent to the Concentrator.

From FE to Concentrator – 4 Numbers - 8 bits per number
Each link - (e/gamma) by (U/V)

This set of four counts is sent from each FE board every crossing to the Concentrator system.

Frame #	*Marker*	*Word 1*	*Word 2*	*Word 3*	*Word 4*	*Word 5*	*Word 6*
1	L1-counts	e-u / e-v	g-u / g-v	spare	spare	spare	spare

Table xxx - L1 event package from each FE to the Concentrator. The package consists of 1 frame containing 4 counts.

The L1 FPS Trigger looks at counts of the number of matched clusters in 32 categories,

(North/South[2]) by (quadrant[4]) by (e/gamma[2]) by (U/V[2]),

within a pair of Trigger Manager boards. The four links from the Concentrator are split at the TM crate and each of the four links has an input into both TM boards. Each of the TM boards can form up to 16 AND/OR terms so 32 terms are available. The 32 numbers can be used in either of the two TM boards with suitable firmware changes to trigger on the number of counts in any single quadrant or matches between quadrants on one end or even matches between quadrants of opposite ends. The details of the TM capabilities are given elsewhere.[??]

From Concentrator to Trigger Manager, FPSTM, - 32 (8-bit) numbers
Link 1 - (quadrant [1,2]) by (e/gamma) by (U/V) for North
Link 2 - (quadrant [3,4]) by (e/gamma) by (U/V) for North
Link 3 - (quadrant [1,2]) by (e/gamma) by (U/V) for South

Link 4 - (quadrant [3,4]) by (e/gamma) by (U/V) for South

The Trigger Manager boards are the MUON designed boards. Therefore the link to them from the Concentrator must follow their protocol exactly. The data frame is somewhat different with a marker word at the end of 6 data words.[??] Also this link must continue during L2 readout times. Therefore the Concentrator will send NULL characters whenever its L1 input is missing.

Word 1	*Word 2*	*Word 3*	*Word 4*	*Word 5*	*Word 6*	*Marker*
q1>e-u/e-v	q2>e-u/e-v	q1>g-u/g-v	q2>g-u/g-v	spare	spare	parity

Table xxx - L1 event package from the Concentrator to the FPSTM. The package consists of 1 frame containing 8 counts.

The L1 Framework must receive its AND/OR inputs in time to issue a L1 accept to the FE's before they reach the end of their pipelines. For this the Framework should receive its inputs by 2.5 us after a crossing. The expected time for the FPS L1 Trigger is:

400ns	latency in FE
132ns	data transfer duration from FE to Concentrator
100ns	signal propagation time from FE to Concentrator
200ns	computation time in Concentrator
132ns	data transfer duration from Concentrator to TM
100ns	signal propagation time from Concentrator TM
500ns	decision time in TM
500ns	signal propagation time from TM to Framework
2064ns	Total L1 time to Framework**

** Very preliminary values

4.1.2.4.2.2 L2 Transfer

When a FE board shifts to L2 mode it begins transferring the L2 information to the Concentrator which in turn passes it on to the L2FPSpp. The data from each FE is a list of 32 clusters. The clusters from FE to Concentrator and to Preprocessors each consist of two words of 16 bits. The meaning of the bits for the cluster words are:

Bit #'s	size in bits	Objects
Cluster m-0		
15	1	word marker – always off
14-3	12	Upstream bit mask / Spare
2	1	North / South
1	1	Type of cluster
		for FPS -> 1=e / 0=gamma
		for CPS Stereo -> not used

		for CPS Axial -> 1= CFT Track match / 0=no match
0	1	Orientations of cluster (U/V)
Cluster m-1		
15	1	word marker – always on
14-12	3	width of cluster
11-8	4	Sector number
7-0	8	address of lowest strip in cluster

Notice that the sector ID or number is inserted at the FE. The four bit sector ID plus the single bit N/S identification gives each cluster a unique global ID for use in the preprocessor.

The data for an event is arranged into 11 frames, which contain diagnostic information and the 32 clusters. The event package is shown in table xxxx. The 11 frames are always sent, which means that 32 cluster words are always sent. When there are less than 32 clusters in a FE, the m clusters that were found are put into the first m cluster words of the package and the remainder are maked as NULL clusters. They are marked by inserting FF as the 'address of lowest strip in cluster'.

Frame #	*Marker*	*Word 1*	*Word 2*	*Word 3*	*Word 4*	*Word 5*	*Word 6*
1	L2-cluster	ID/cross#	turn #	cluster 1-0	cluster 1-1	cluster 2-0	cluster 2-1
2	L2-cluster	cluster 3-0	cluster 3-1	cluster 4-0	cluster 4-1	cluster 5-0	cluster 5-1
11	L2-cluster	cluster30-0	cluster30-1	cluster31-0	cluster31-1	cluster32-0	cluster32-1

Table xxx - L2 event package from each FE to the Concentrator. The package consists of 11 frames which contain 32 clusters, an 8 bit FE ID, an 8 bit crossing number, and a 16 bit turn number.

The data transfer from the L2PSCN to L2PSpp follows the same protocol as for the L2CFTpp. Also the Data format is the same as for CFT except for the content of the data frames and the maximum number of data frames sent. For the FPS case a maximum of 64 clusters are sent. Please see section 2 of this TDR and the L2 CFTpp TDR.[xxx]

The time for the transfer from the FE is fixed at 11 x 132ns = 1.45us. The latency within the Concentrator system is about 0.5us and the time needed to transmit a full count of 64 clusters (plus16 bytes of header/control) is 2.72us. All of this totals about 4.7us.

4.1.2.4.3 Concentrator Crate

4.1.2.4.4 L1 Trigger Manager

The Forward Preshower Trigger Manager, FPSTM, uses the Muon Trigger Manager, as is done for the CFTTM. Please see section 2 for the description of the CFTTM. Either one or two TM boards can be used giving 16 or 32 AND/OR terms for the L1FPS Trigger. The four links from the concentrator are passively split and all four sent to the two TM boards when both are in use.

4.2 CPS Stereo FE Electronics and Trigger System

4.2.1 Functional Description

During L1 live running the operation of the system can be separated into four function blocks as shown in figure 16. In each of the FE boards clusters are found Independently for each of the u and v stereo layers. Both the location and width of each cluster is found using the same algorithm as for the FPS. The found clusters in 2 categories (u/v) are pipelined for later readout. The maximum number of clusters that are stored at each FE is 32 total, which can be any mixture of u- and v-layer clusters.

Whenever an L1-accept is received the system stops normal processing and shifts to L2 and L3 readout modes. In each FE the data for the correct crossing is pulled out of the L2 pipeline and sent to the FPS RC boards. Because it is important for monitoring the operations of the trigger, this data is also placed into the virtual SVX, VSVX, for inclusion in the L3 readout stream. Information from the L1 for this crossing is also in the VSVX. Independently at each FE the analog values are pulled out of each SVX pipeline, digitized and read out for the L3. The L3 readout system (with the exception of the VSVX) is shared with the silicon system and is not detailed in this document.

The arrival from the FE of L2 type data switches the Concentrator system over to L2 mode. In this mode it takes the lists of found clusters from each FE, and combines and truncates them, and sends them on to the Preshower preprocessor, PSpp.

4.2.2 System Architecture

4.2.2.1 Geometry and Definitions

Given mechanical properties are.

1 Each CPS strip is divided into two parts, North and South.
3 Stereo Layers u & v go to CPS FE boards, 512 channels per board.
4 The axial layer goes to the CFT FE, 16 north and 16 south per board.
5 Each Stereo FE board has 256 contiguous u-strips and 256 v-strips from one end (N/S).

Electronic and Trigger properties are **<u>defined</u>** as.

1 There is no L1 trigger for the stereo strips.
2 The axial strips are combined with the CFT trigger at their FE board, clusters are flagged if they have a track match.
3 Each CFT FE board outputs clusters for L2 - 2 per sector per end

4 Each Stereo FE board forms clusters and outputs them for L2 - 16 per 256 strips.
5 Clusters are **not** formed across Stereo FE board boundaries.
6 The Stereo FE boards are arranged in 2 FE crates.
7 The L2 Concentrator is the L2PSCN.

The cassette assignment for the CPS detectors is as shown in figure 2. The CPS FE boards are located in two special smaller crates located just inboard of the FPS crates. These 3-cassette wide crates have the identical backplanes as the FPS crates but contain only 6 slots.

The CPS detector is constructed of three layers of scintillator, u, v and axial. The axial is part of the CFT trigger system and is discussed there.

4.2.2.2 Trigger Sectors

The CPS Stereo is read out only for the L2 trigger. Each FE board receives the input from 256 contiguous strips. Clusters are found for these strips using the exact same algorithm as in the FPS. Clusters are not formed across the FE board boundaries. Since they are grouped into 256 wide groups there are only 5 'cracks'.

4.2.2.3 Hardware Description

4.2.2.3.1 FE Boards

The CPS Stereo FE boards share their design with the FPS FE boards. The values of the capacitors on the charge dividers are different because of the different amount of light from this detector. The number of channels in each module and MCM are different because of the number of strips per cassette. See figure xxx. And the L1 trigger logic is omitted.

4.2.2.3.2 Data Transfer

The CPS Stereo does not transfer data in L1 mode. When it receives a L1 accept it switchers to L2 mode and operates exactly as the FPS FE boards described above. The only difference is the type bit is not used.

Tables

		15 p.e. per MIP													
		40 K VLPC Gain													
VLPC Output															
	15pe/MIP	40K Gain	Drain	**HIGH Gain**		SIFT Output		SVX		**LOW Gain**		SIFT Output		SVX	
MIP	pe	fC		%	fC	gain	fC	scale	counts	%	fC	gain	fC	scale	counts
1	15	96	60%	30%	29	0.4	12	150	20	10%	10	0.2	2	150	3
2	30	192	60%	30%	58	0.4	23	150	39	10%	19	0.2	4	150	7
5	75	481	60%	30%	144	0.4	58	150	98	10%	48	0.2	10	150	16
10	150	961	60%	30%	288	0.4	115	150	197	10%	96	0.2	19	150	33
20	300	1,922	60%	30%	577	0.4	231	150	256	10%	192	0.2	38	150	66
40	600	3,845	60%	30%	1,153	0.4	461	150	256	10%	384	0.2	77	150	131
80	1,200	7,690	60%	30%	2,307	0.4	923	150	256	10%	769	0.2	154	150	256
0.5	7.5	48.1	60%	30%	14.4	0.4	5.8	150	9.8	10%	4.8	0.2	1.0	150	1.6
0.067	1.0	6.4	60%	30%	1.9	0.4	0.8	25	7.9	10%	0.6	0.4	0.3	25	2.6
0.067	1.0	6.4	0%	100%	6.4	0.4	2.6	25	26.4						
1	15	96	76%	20%	19	0.4	8	150	13	4%	4	0.4	2	150	2.6
2	30	192	76%	20%	38	0.4	15	150	26	4%	8	0.4	3	150	5.2
5	75	481	76%	20%	96	0.4	38	150	66	4%	19	0.4	8	150	13
10	150	961	76%	20%	192	0.4	77	150	131	4%	38	0.4	15	150	26
20	300	1,922	76%	20%	384	0.4	154	150	256	4%	77	0.4	31	150	52
40	600	3,845	76%	20%	769	0.4	308	150	256	4%	154	0.4	62	150	105
80	1,200	7,690	76%	20%	1,538	0.4	615	150	256	4%	308	0.4	123	150	210
100	1,500	9,612	76%	20%	1,922	0.4	769	150	256	4%	384	0.4	154	150	256
0.5	7.5	48.1	76%	20%	9.6	0.4	3.8	150	6.56	4%	1.9	0.2	0.4	150	0.66
0.05	0.8	4.8	76%	20%	1.0	0.4	0.4	150	0.66	4%	0.2	0.2	0.0	150	0.07

Table 1 This table lists the analog values for the shower layers. For the FPS these are the backward layers and for the CPS these are all three layers. The top half of the table shows the preferred charge division of 60:30:10. The bottom half an alternative division. One MIP produces from 15 to 20 pe's, 15 is used here. The gain of the VLPC's vary between 30 and 50k, 40k is used here. The internal gain of the SIFT chip can be switched between 0.2 and 0.4, and the full scale counts of the SVX can be varied from 25 to 150 fC full scale (256 counts).

15 p.e. per MIP
40 K VLPC Gain

VLPC Output																	
	15pe/M	40K Gain	Drain	**HIGH Gain**		SIFT Output		SVX		**LOW Gain**		SIFT Output		SVX	
MIP	pe	fC		%	fC	gain	fC	scale	counts	%	fC	gain	fC	scale	counts
0.1	1.5	9.6	0%	80%	7.69	0.4	3.08	150	5.2	20%	1.9	0.2	0.4	150	0.7
0.3	4.5	28.8	0%	80%	23.1	0.4	9.23	150	16	20%	5.8	0.2	1.2	150	2.0
0.5	7.5	48.1	0%	80%	38.4	0.4	15.4	150	26	20%	9.6	0.2	1.9	150	3.3
1	15.0	96.1	0%	80%	76.9	0.4	30.8	150	52	20%	19.2	0.2	3.8	150	6.6
2	30.0	192	0%	80%	153.8	0.4	61.5	150	105	20%	38.4	0.2	7.7	150	13.1
5	75.0	481	0%	80%	384.5	0.4	153.8	150	256	20%	96.1	0.2	19.2	150	32.8
40	600.0	3,845	0%	80%	3,075.8	0.4	#####	150	256	20%	769.0	0.2	154	150	256.0
0.3	4.5	28.84	0%	100%	28.84	0.4	11.53	150	20	0%	-	0.2	-	150	-
0.5	7.5	48.06	0%	100%	48.06	0.4	19.22	25	197	0%	-	0.4	-	25	-
0.067	1.0	6.44	0%	100%	6.44	0.4	2.58	25	26						

Table 2 This table lists the analog values for the forward layer of the FPS. The top half of the table shows a proposed charge division of 0:80:20. The bottom half an alternative division.

VLPC Output

MIP	97	15	pe per MIP
pe	1455	40	K VLPC Gain
fC	9323.6		

Charge Splitter

	Drain	High Gain	Low Gain
%	76%	20%	4%
fC	7086	1864.728	372.9456

SIFT Disc

gain
5% delta Vth

SIFT Ouput

Gain	0.40	0.40
fC	745.89	149.18

SVX

scale	90.00	150.00
counts	2,121.65	254.60

Table xxx An input of 97 MIPs then saturates the low gain channel.

4.3 *Figures*

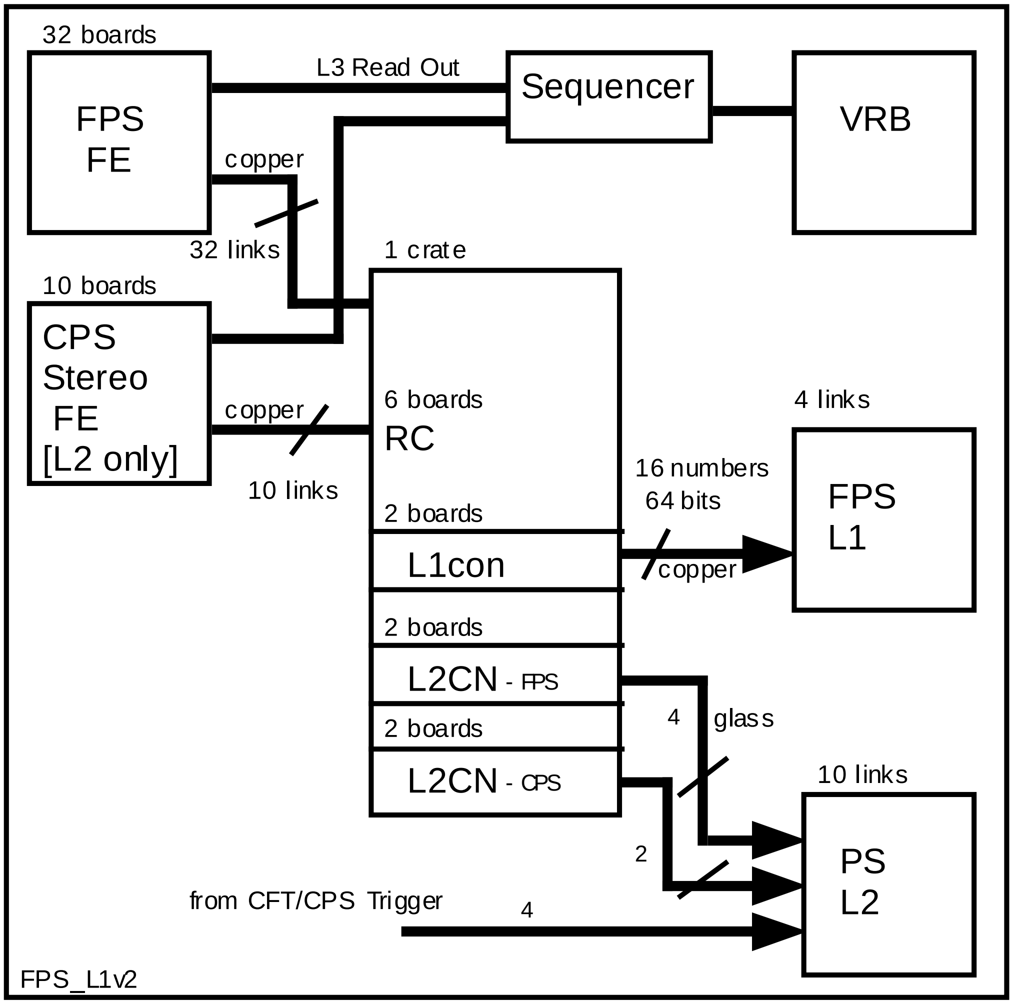


Figure 1. Block diagram of the Preshower Trigger system. The data orginates in the FPS and CPS FE boards, is passed to the Concentrator System and from there to the L1FPSTM for a L1 trigger decision and to the L2PSpp.

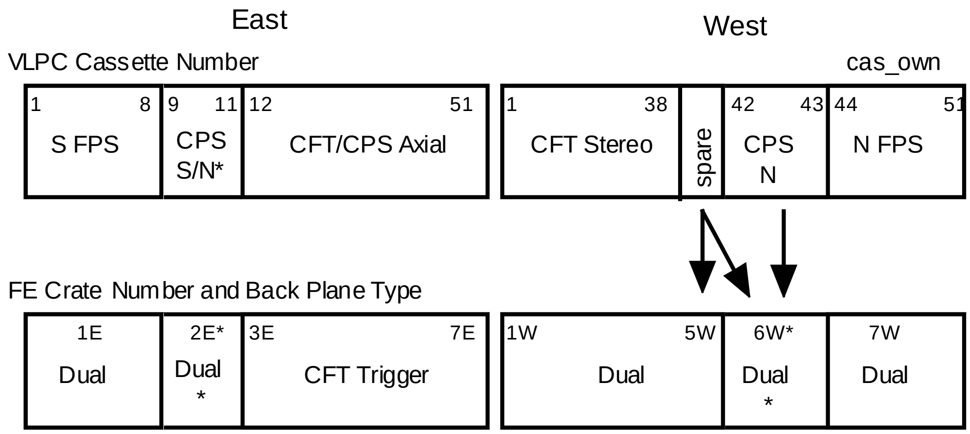


Figure 2 - shows the cassette assignment for the PS detectors. The FPS is housed at either end of the cassette cryostat in 8 cassette wide crates. The CPS Stereo is housed just inboard of these in special 3-cassette crates. The CPS Axial is mixed in with the CFT Axial.

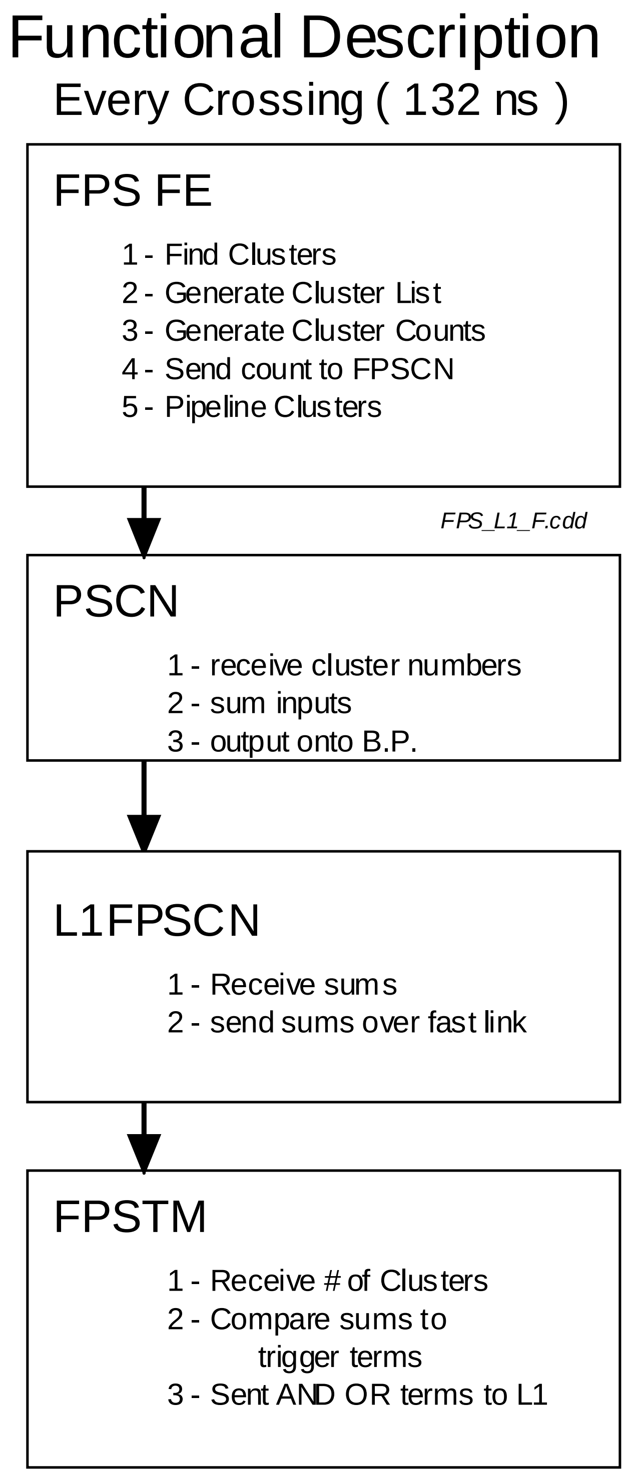


Figure 3. Functional description of the main blocks of the FPS L1 Trigger system. This figure shows the functions carried out for each crossing cycle during L1 live time.

Functional Description

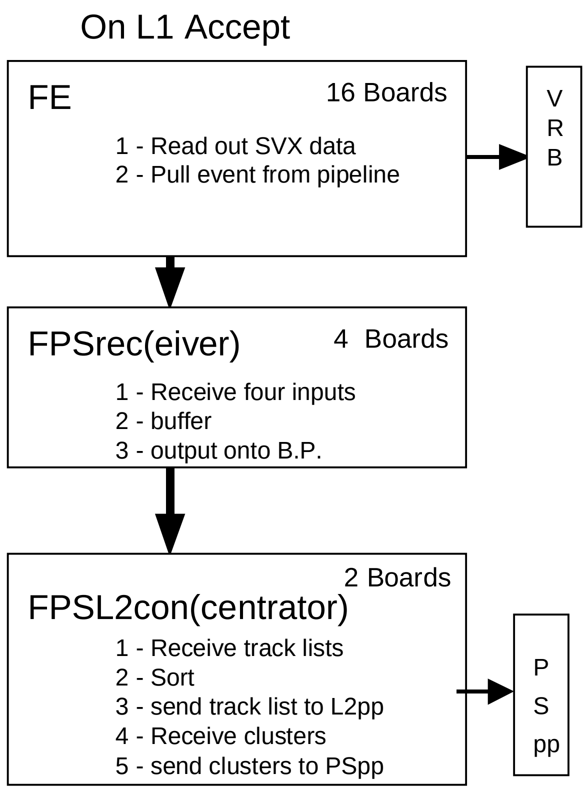


Figure 4. Functional description of the main blocks of the FPS Trigger system. This figure shows the functions carried out after a L1 accept is received.

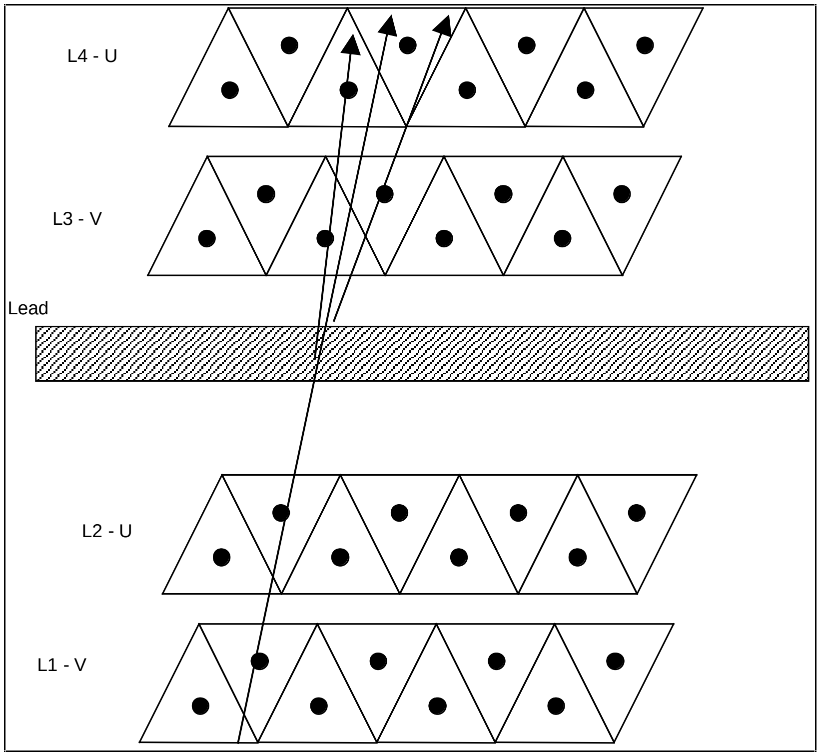


Figure 5 - The FPS detector consists of two layers of triangular strips in front of a lead radiator and two behind. Each pair of layers has a U layer and a V layer. There are 101 strips in the forward layers (L1 & L2) and 135 in the back layers (L3 & L4).

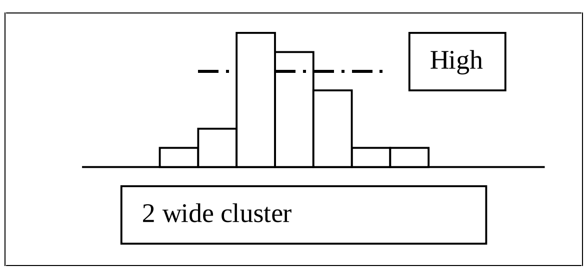


Figure 6 - Definition of a Cluster is the same in either of the two back layers of the FPS and in any of the three layers of the CPS. A cluster is defined as one-or-more strips above the HIGH threshold. Found are cluster edge and width.

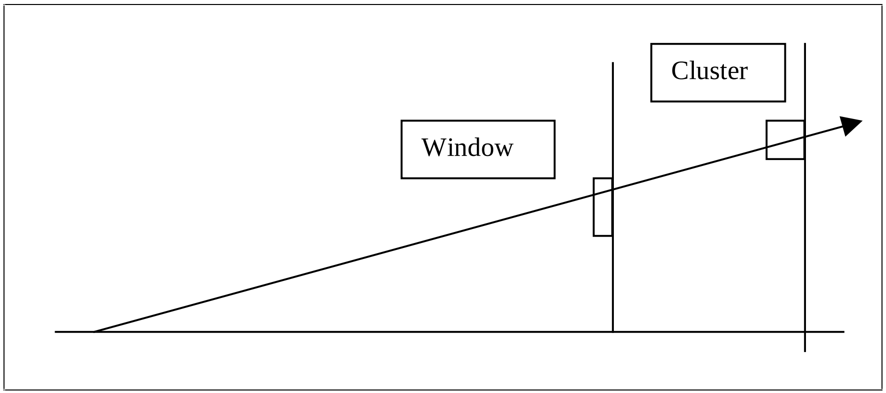


Figure 7 - A U(V) electron candidate consists of a cluster in a back U(V) layer in coincidence with a MIP in the WINDOW in the Forward U(V) layer. A photon candidate is similar but with a VETO from the WINDOW in the Forward layer.

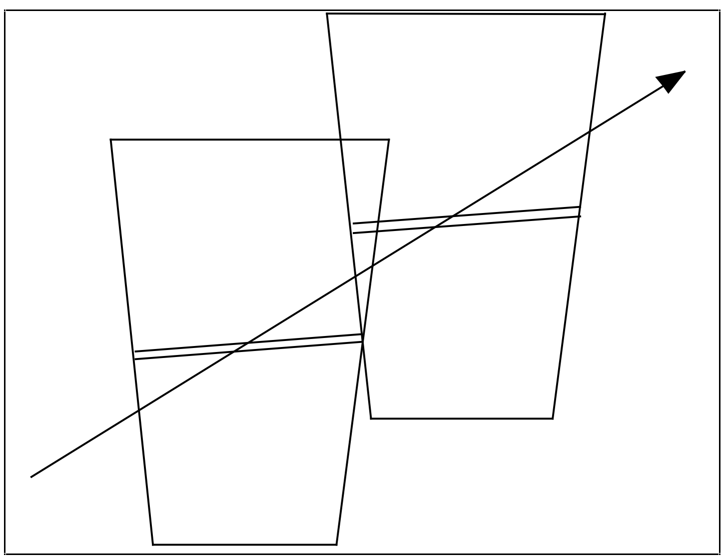


Figure 8 - Cluster matching - All U e-candidate clusters are kept if there are one-or-more V e-candidates. All V e-candidate clusters are kept if there are one-or-more U e-candidates. The same for gama-candidates.

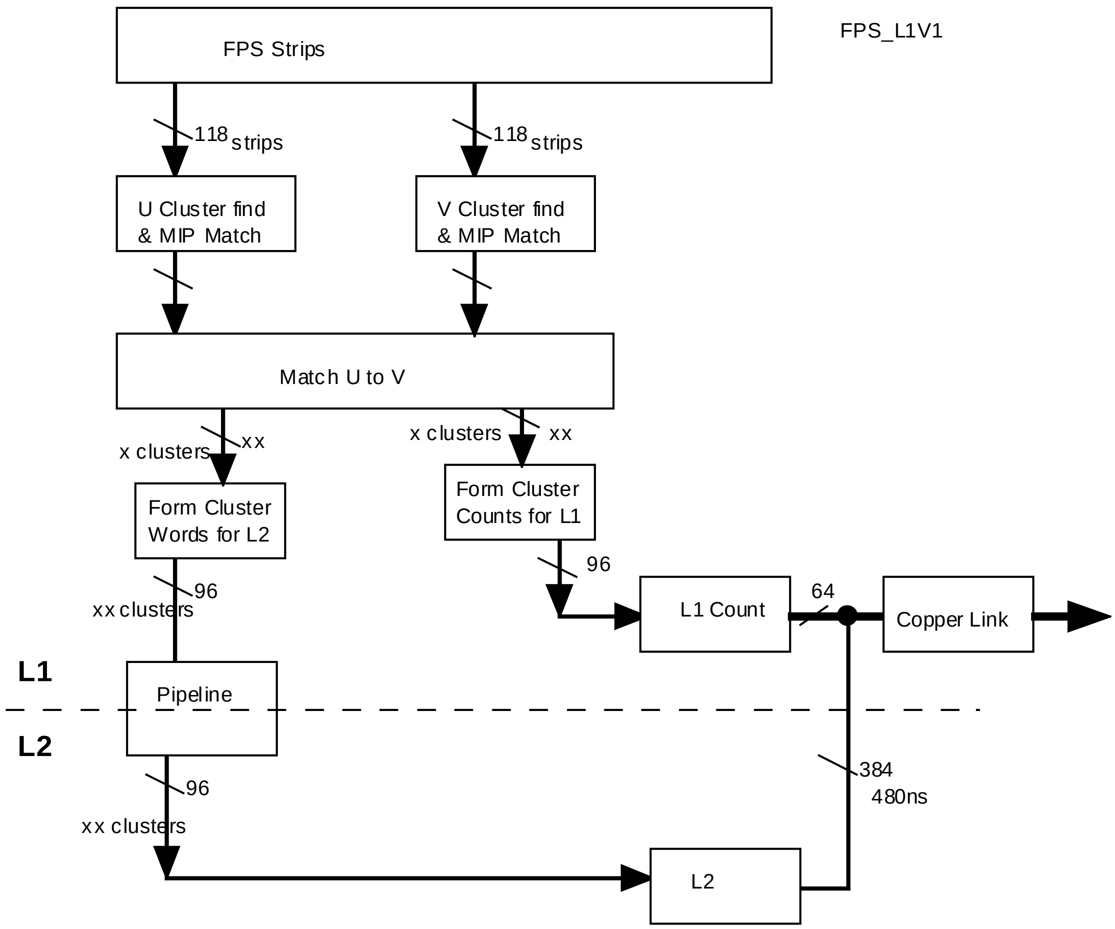


Figure 10 - Block diagram of the trigger logic on the FPS FE board. The clusters are found, then tagged as electron or gamma with a forward MIP match, and finally matched in the u and v layers. The counts of clusters are then sent on for the L1 and the clusters themselves are pipelined for readout to L2. The CPS Stereo is a subset of the FPS. No MIP match is performed and no L1 processing occures.

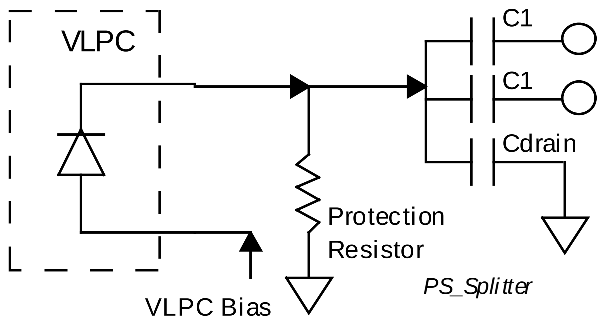


Figure 11 Simplifiied schematic of the charge splitting on the FE board for the PS channles. The charge from the VLPC is split 3 ways with most of the charge dumped through the drain capacitor. Since C1 and C2 are much smaller the charge division is proportional to C1(2) / SUM.

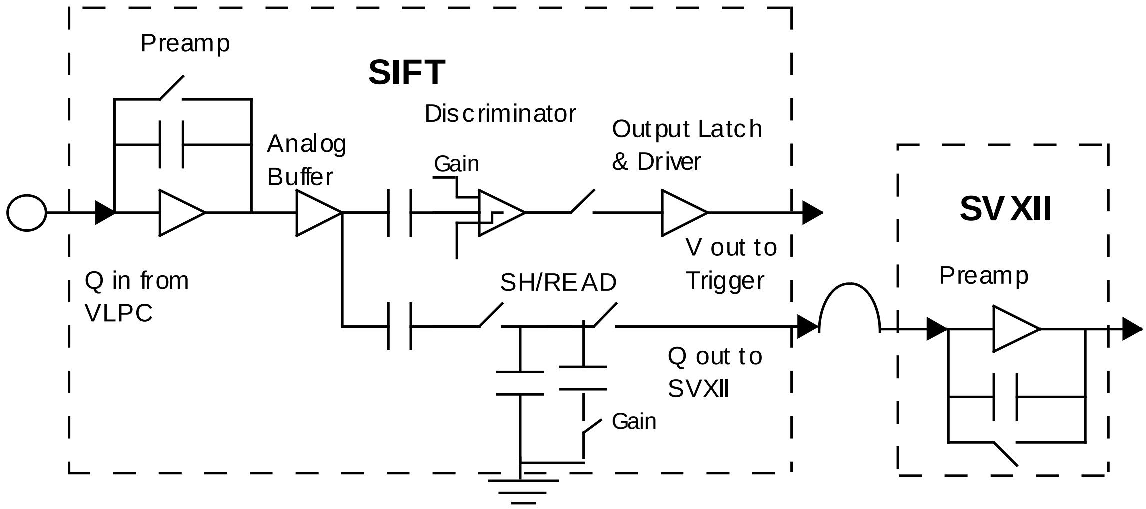


Figure 12 - Simplified schematic of a single channel of the MCM. Each analog input is routed to a SIFT channel where it is discriminated for a Voltage output and integrated and passed onto an SVX2e chip input channel. The output of the SVX2e is a digitized amplitude.

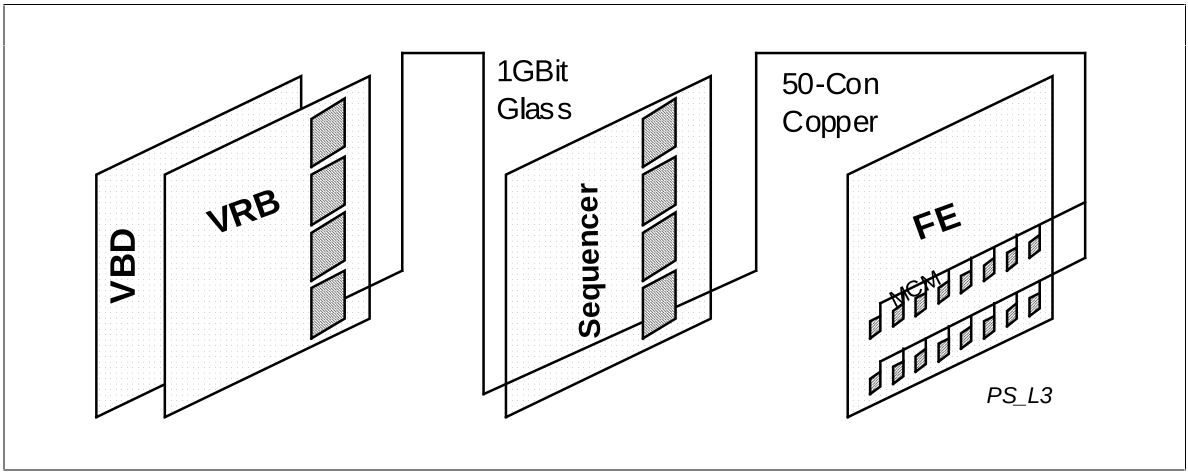


Figure 13 - Cartoon of the L3 Read Out. The MCM's on each FE board are linked into two, eight SVX chips long, read out strings. Each two strings are linked via a 50 conductor copper cable to a Sequencer board located in a crate nearby on the Platform. The sequencer takes the data from two strings and puts it onto a single glass link and sends it to the VRB. The VRB is read out by the VBD and into the DAQ system.

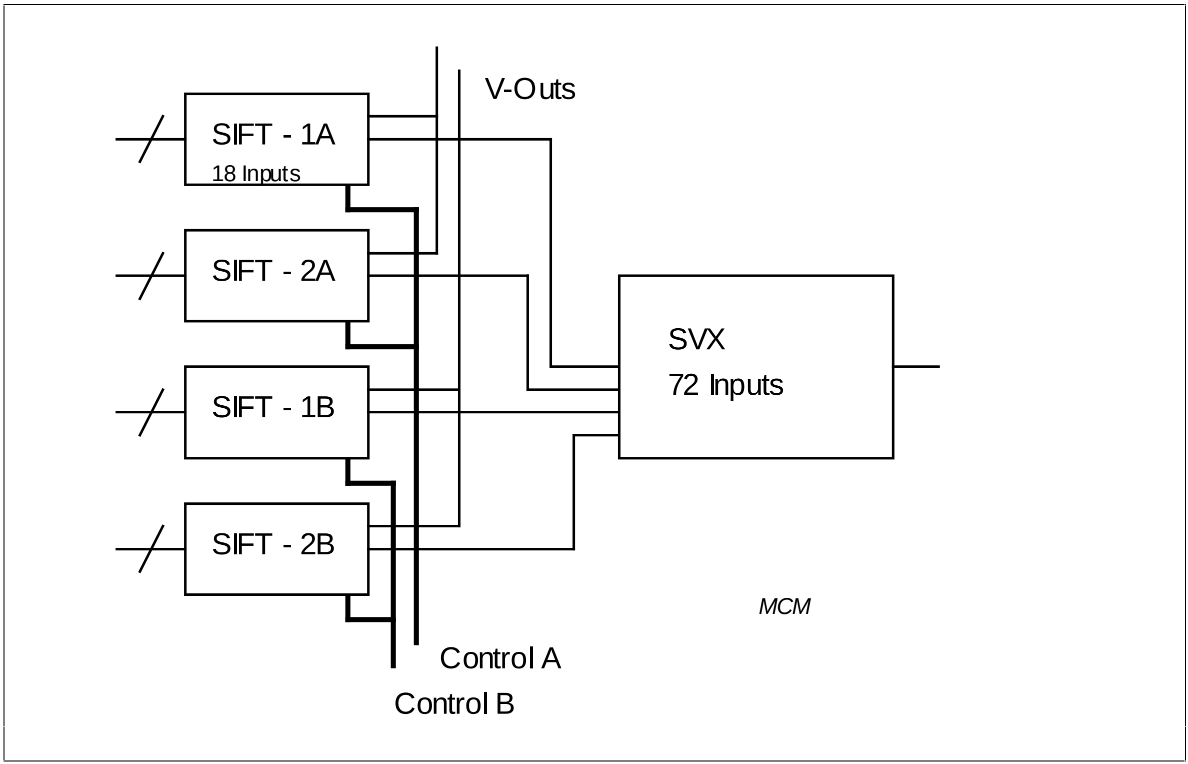


Figure 14 - Simplified schematic of the multi-chip module, MCM. Each MCM has 72 analog inputs that are divided into two groups of 36. There are separate controls for the A and the B groups on the SIFT preamp dynamic range, the discriminator threshold and gain, and the SIFT analog gain.

marker 1	word 1	word 2	word 3	word 4	word 5	word 6

Figure 15 - Frame of data over the link from the FE boards to the concentrator. Each frame consists of a leading marker word and 6 data words. One frame is sent every crossing. The marker contains synchronization information and marker information as to whether the frame contains data for L1, or L2.

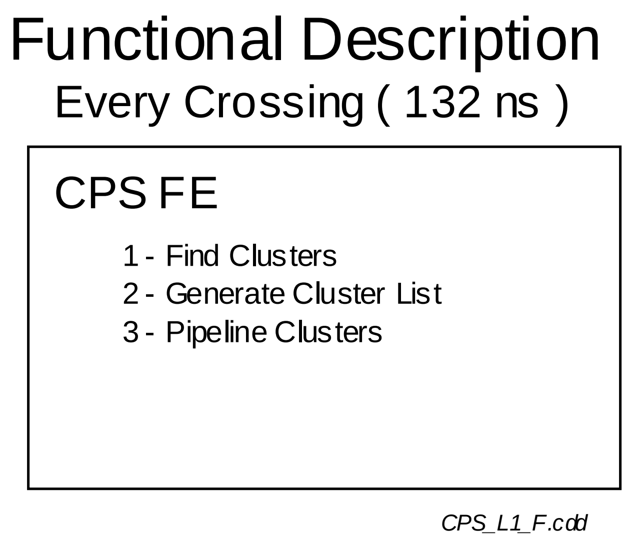
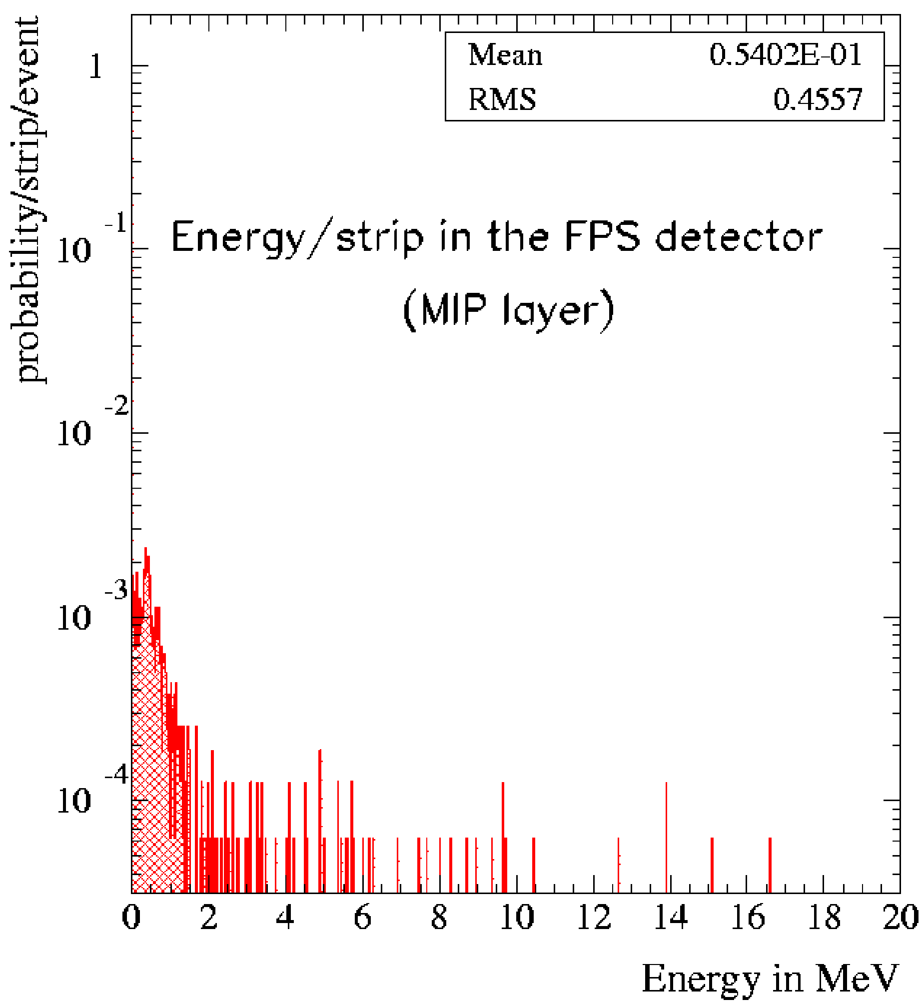
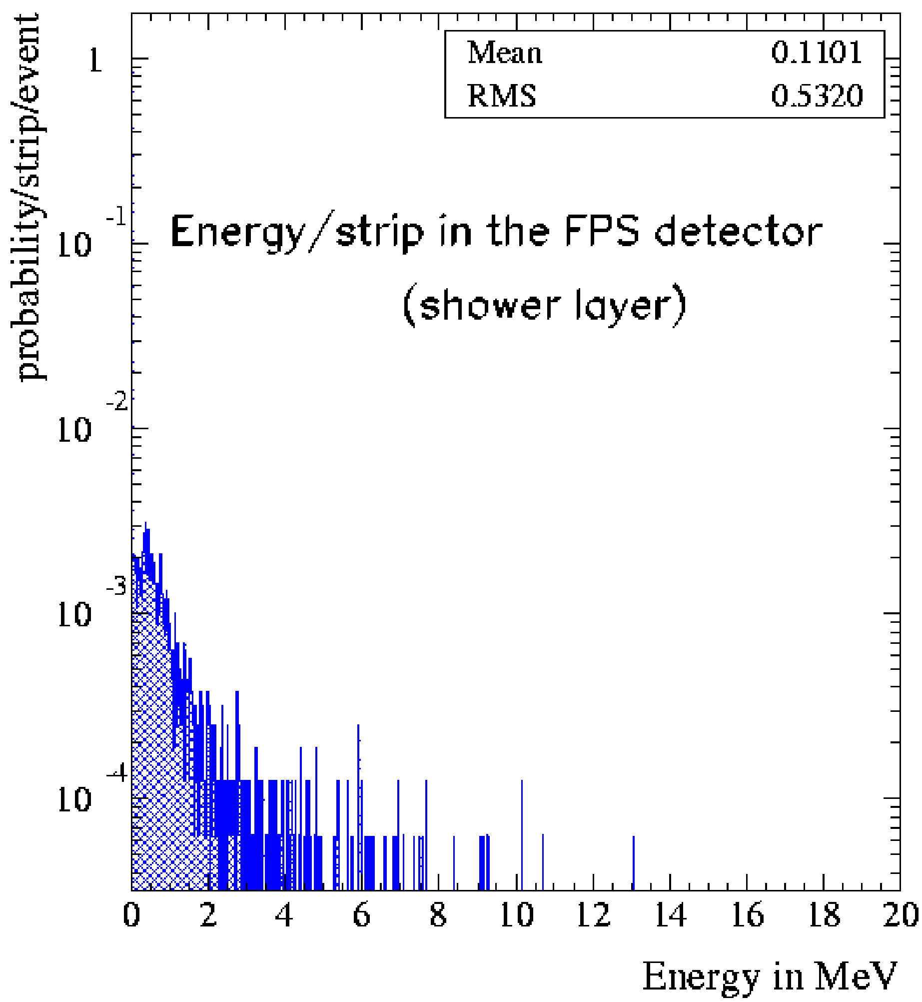
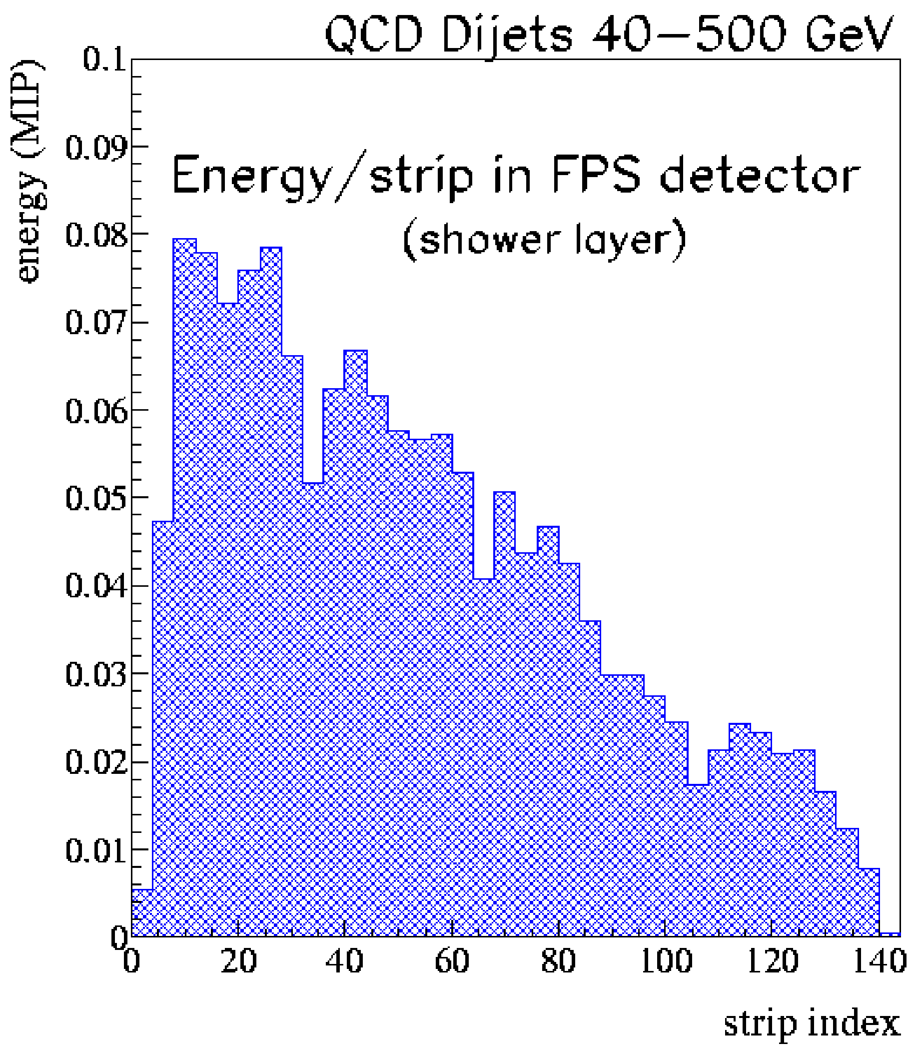
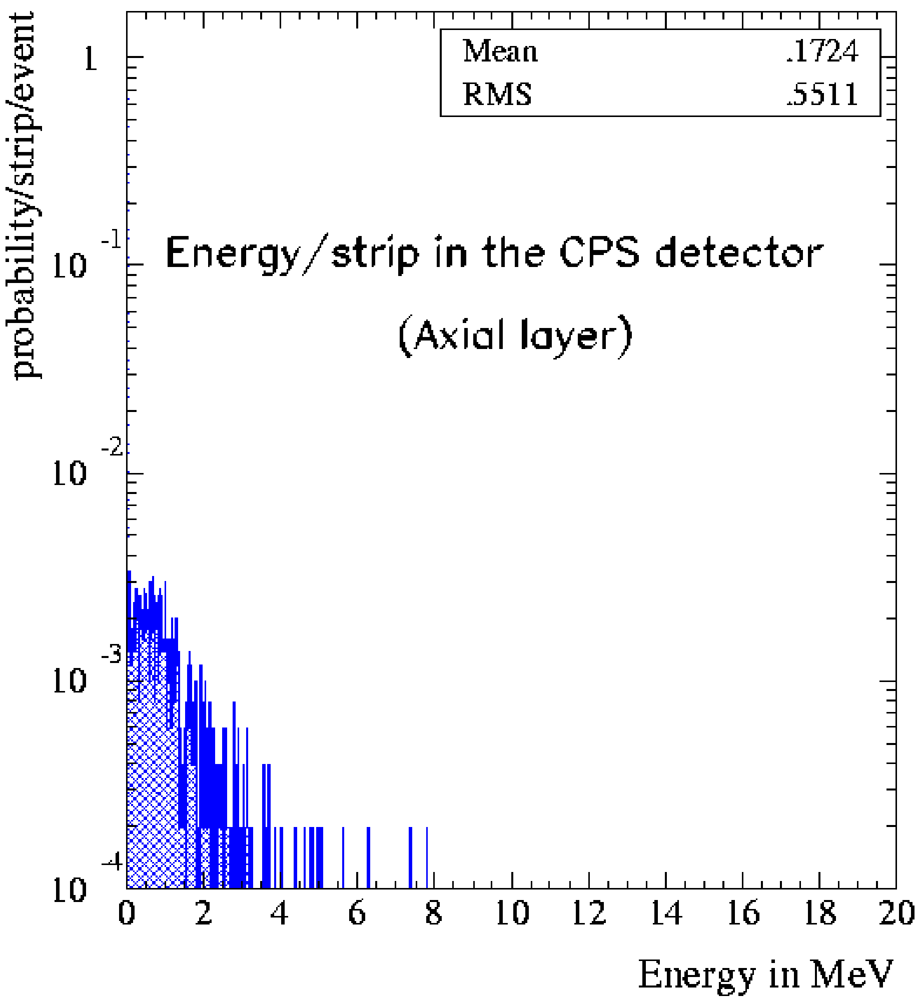


Figure 16 - Functional diagram of the CPS system during L1 live time.


Mean 0.5402E-01
RMS 0.4557
Energy/strip in the FPS detector
(MIP layer)
probability/strip/event
1
10^-1
10^-2
10^-3
10^-4
0
2
4
6
8
10
12
14
16
18
20
Energy in MeV


Mean 0.1101
RMS 0.5320
Energy/strip in the FPS detector
(shower layer)
probability/strip/event
Energy in MeV
1
10^-1
10^-2
10^-3
10^-4
0
2
4
6
8
10
12
14
16
18
20


QCD Dijets 40−500 GeV
Energy/strip in FPS detector
(shower layer)
energy (MIP)
0.1
0.09
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
0
20
40
60
80
100
120
140
strip index


probability/strip/event
1
10^{-1}
10^{-2}
10^{-3}
10^{-4}
Mean .1724
RMS .5511
Energy/strip in the CPS detector
(Axial layer)
0 2 4 6 8 10 12 14 16 18 20
Energy in MeV

References:

[1] The D0upgrade for the FPS, Muon and L2 trigger, FERMILAB-FN-641, D0note 2894.

[2] "TDR of the Forward Preshower detector for the D0 Upgrade", J. Kotcher et al.

[3] "The Central PreShower in the Axial CFT Trigger", Fred Borcherding, D0Note 3514, November 25, 1997.

[4] "A L1 FE Trigger for the Forward Preshower Detector, Design Version 1", Fred Borcherding, private communication.

[5] http://d0server1.fnal.gov/Projects/TriggerElectronics/WebDocs/Trigger_index.htm, Home page for the CTT FE Electronics and Trigger Project, contains an index of technical drawings and documents.

[6] "Definition of a L1 e- and photon trigger with the FPS", bbbbb et al., D0Note 3493, July 1998.