Electro-Thermal Simulation of a 100 A, 10 kV Half-Bridge SiC MOSFET/JBS Power Module [†]

T. H. Duong[1], J. M. Ortiz-Rodríguez[1], R. N. Raju[2], and A. R. Hefner[1]

[1] National Institute of Standards and Technology, Semiconductor Electronics Division
Gaithersburg, MD 20899, USA

[2] General Electric Global Research Center
Niskayuna, NY 12309, USA

Abstract— **This paper presents the results from a parametric simulation study that was conducted to optimize the performance of 100 A, 10 kV, 20 kHz half-bridge SiC MOSFET/JBS power modules. The power modules are being developed by the DARPA WBGS-HPE Phase II program and will be used in the 13.8 kV, 2.75 MVA SSPS developed in the HPE Phase III program. The simulations are performed using recently developed and validated physics-based electrical and thermal models. The total device active areas and the various gate resistances and inductances are optimized in order to minimize overall power dissipation. A detailed description of the loss mechanisms and the simulation results for a representative SSPS topology is also presented.**

Keywords: Silicon Carbide; high-voltage; high-frequency; MOSFET; Junction Barrier Schottky (JBS); half-bridge power module; Solid State Power Substation.

I. INTRODUCTION

Recent breakthroughs in Silicon Carbide (SiC) material and fabrication technology have led to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 20 kHz power switching capability [1]. The goal of the Defense Advanced Research Projects Agency (DARPA) Wide Bandgap Semiconductor - High Power Electronics (WBGS-HPE) Phase II program is to develop 100 A, 10 kV SiC half-bridge power modules required to demonstrate the 13.8 kV, 2.75 MVA Solid State Power Substation (SSPS) in the DARPA WBGS-HPE Phase III program [2].

The purpose of this parametric simulation study is to optimize Phase II module parameters in order to minimize power losses and amplitude of the temperature cycles, and thus achieve the best possible performance for the circuit conditions required for the Phase III SSPS. The simulations are performed using experimentally validated electrical physics-based models for 10 kV SiC semiconductor devices (MOSFETs and JBS diodes) developed in [3, 4, 5] and the experimentally validated thermal model for the module package developed in [6].

The simulations emulate the hard switching conditions similar to the ones present during operation of a SSPS full

wave inverter with a quarter sine-wave current cycle, while requiring the use of only one 10 kV MOSFET switch and one 10 kV JBS diode [7, 8]. This is accomplished using a 5 kV boost converter circuit as described in [9] with a 50 % duty cycle and a current ramp time of approximately 4.167 ms. Using the circuit in [9] and the models in [3, 4, 5, 6], the performance of the 100 A, 10 kV half-bridge SiC MOSFET/JBS power module is optimized by varying power module parameters such as the number of SiC MOSFET and SiC JBS diode chips and the various gate resistances and inductances. The optimized module model is then used to perform simulations using a more realistic SSPS circuit.

II. ELECTRO-THERMAL SIMULATION METHODOLOGY

The optimization makes use of a simulation of both the electrical and thermal behavior of the power module using a basic 5 kV boost converter as shown in Fig. 1. Fig. 2 circuit topology of the 100 A, 10 kV half-bridge SiC MOSFET/JBS power module model [5] and the thermal component models [6]. The junction temperature node (T_J) of each SiC device in the half-bridge power module is connected to the surface-temperature node of the SiC chip thermal network component model. The chip thermal model is also connected to the package header node (T_H) of the package heat conduction model. The package heat conduction model is connected to the package integrated-cooling heat-transfer model at the package fluid channel interface T_C. Finally, the package integrated-cooling heat-transfer model calculates the heat transfer across the fluid to case interface for a fluid temperature of T_A.
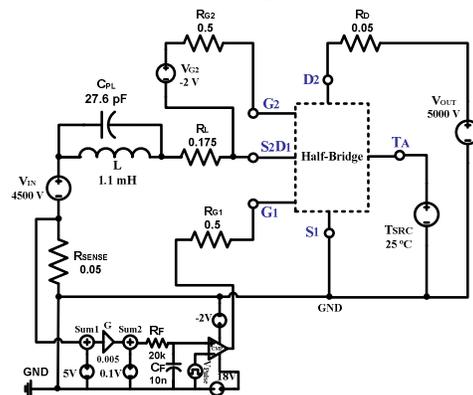
Fig. 1: The basic 5 kV boost converter used for the 100 A, 10 kV half-bridge SiC MOSFET/JBS power module simulation.
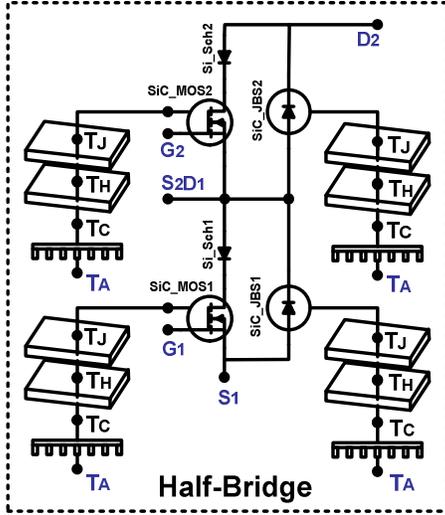
Fig. 2: Circuit topology of the 100 A, 10 kV half-bridge SiC MOSFET/JBS power module with series silicon Schottky power diodes to prevent reverse conduction in the SiC MOSFETs.

III.   ELECTRO-THERMAL ANALYSIS OF THE HALF-BRIDGE SiC MOSFET/JBS POWER MODULE

The high-voltage boost converter test circuit shown in Fig. 1 shows the connection of the 100 A, 10 kV half-bridge SiC MOSFET/JBS power module. The high-voltage boost converter is designed to operate a single power switch (lower MOSFET in the module) and a single power diode (upper diode in the module) for continuous 20 kHz hard switching conditions at 5 kV, 100 A with a 50 % duty cycle. The circuit is repetitively gated on for one-quarter 60 Hz sine-wave and off for the next one-quarter cycle to mimic the device current and heating stress conditions of a full-wave PWM inverter. The upper MOSFET gate (G_2) is connected to a negative gate voltage supply ($V_{G2} = -2$ V) through the gate resistor. The negative gate voltage supply is referenced to the source of the upper MOSFET at S_2D_1.

A.   Electrical Operation and Thermal Response

Fig. 3 shows the temperature waveforms at T_J and T_H for (a) the lower SiC MOSFET (SiC_MOS1) and (b) the upper SiC JBS diode (SiC_JBS2) as shown in Fig. 2. Notice that the T_J waveform of SiC_MOS1 spikes at a 20 kHz rate during the 60 Hz quarter sine-wave phase when the device is switching (e.g., the time interval between 0 ms to 4.167 ms) due to the switching energy losses in the SiC_MOS1 that results from charging the capacitances of the upper SiC MOSFET (SiC_MOS2) and the lower SiC JBS diode (SiC_JBS1) in the module. Also, notice that T_J cools during the phase in which the device is off (i.e., the time interval beginning at $t = 4.167$ ms at the peak of the inductor current and ending at $t = 8.334$ ms).

Fig. 3(a) shows the thermal response of the lower SiC MOSFET. The parameters used in the thermal model of the SiC-chip determine the SiC MOSFET temperature variations during the device 20 kHz switching cycle (e.g., T_J varies approximately from 67 °C to 71 °C as indicated by $\Delta T_{20\,kHz}$ because the temperature at the T_H node does not change during the 20 kHz cycles). The thermal response of the SiC-chip and module package determines the device temperature variations during the 60 Hz sinusoidal

current variations, e.g., T_J varies approximately from 61 °C to 67 °C as indicated by ΔT_{60Hz}. This occurs because electrical network 20 kHz time constant is faster than the time required for heat to diffuse into the package.

For the boost converter simulation of Fig. 1 requires approximately 45 minutes of real time for the temperature to reach a steady-state condition. Thus, a simulation of the complete thermal startup condition would take an excessive amount of simulation time for the 20 kHz boost converter operation. To avoid running the simulation for the many 60 Hz cycles required to reach steady-state, a temperature initial condition iterations strategy similar to the strategy derived in [10] is used.

To implement this iterations strategy, a power source equal to the average power in each of the SiC MOSFET/JBS devices in the power module is connected to each device in thermal network arrangement in Fig. 2 and the electrical network turned off to set the initial temperature. The electrical network is turned back on soon after the transient is initiated. Note that the average power can be calculated using the waveform calculator in Saber to integrate the power dissipation in the SiC MOSFET/JBS over a single switching cycle of the boost converter and then to divide it by half of the time interval of the switching cycle, assuming that each device is on for two quarters of the 60 Hz switching cycle. This initial power is iterated until the power obtained at the end of several cycles matches the initial condition.

(a)

(b)
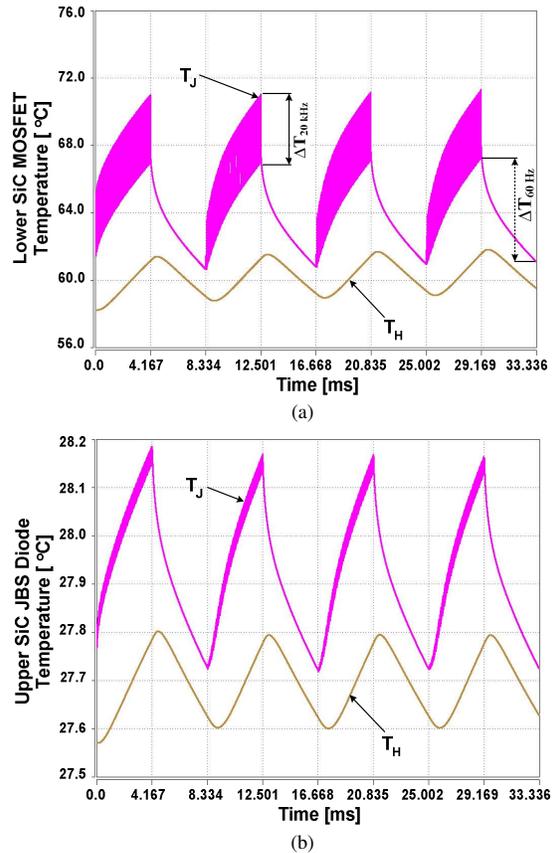
Fig. 3: Temperature waveforms at the SiC-chip surface (T_J) and chip-package interface (T_H) for the lower SiC MOSFET (SiC_MOS1) and the upper SiC JBS diode (SiC_JBS2) in the 100 A, 10 kV half-bridge SiC MOSFET/JBS power module shown in Fig. 2.

Fig. 4 shows the simulated thermal response for the low-frequency components of the temperature waveforms at T_J and T_H for SiC_MOS1 and SiC_JBS2 during the start-up of the boost converter shown in Fig. 1. For the start-up simulation, the initial condition for the temperature throughout the thermal network is 25 °C, and the average power dissipation level steps from 0 W to 721 W for SiC_MOS1 and 0 W to 80 W for SiC_JBS2 at $t = 0$ s. The SiC-chip and module package temperature waveforms asymptotically approach the steady state values after about 366.74 ms.

(a)

(b)
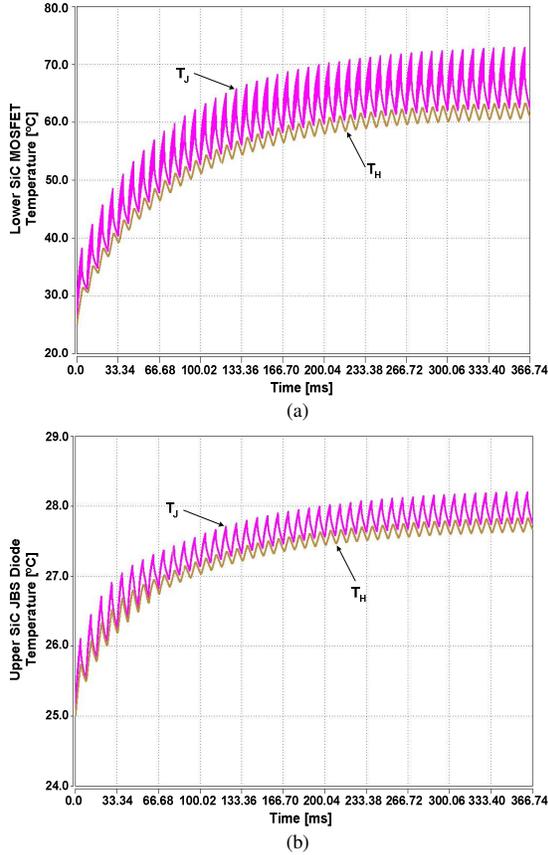
Fig. 4: Simulated thermal response at startup for the average power dissipated in the SiC_MOS1 (a) and SiC_JBS2 (b) indicating the temperature at the junction (T_J) and chip-package interface (T_H).

B. Power Dissipation and Switching Energy of SiC MOSFETs and JBS Diodes

Fig. 5 shows the (a) drain-source voltage (V_{DS}), (b) drain current (I_{DS}), (c) instantaneous power dissipated as heat (P_{INS}), and (d) cumulative dissipated energy (E_{CUM}) for the lower SiC MOSFET during one 20 kHz switching cycle of the simulation in Fig. 3 (i.e., the time interval between 29.145 ms to 29.175 ms). The instantaneous power dissipated as heat (provided at the thermal node) is not equal to the product of terminal current and voltage waveforms because the internal capacitance currents do not produce heat [5]. Fig. 5 was chosen so that the details of both the turn-on and turn-off waveforms are viewed on the same graph.

Before SiC_MOS1 is turned on, the inductor current is flowing through SiC_JBS2. When SiC_MOS1 is switched

on ($t = 29.150$ ms shown in Fig. 5), the inductor current is transferred from SiC_JBS2 to SiC_MOS1.

(a)

(b)

(c)

(d)
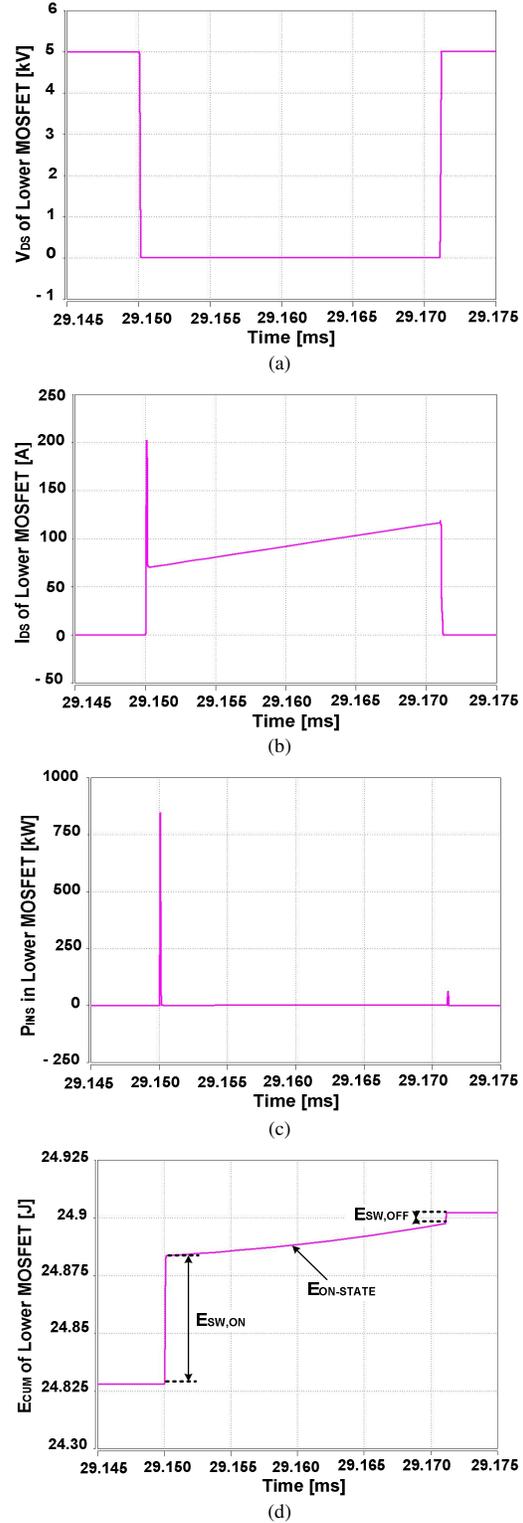
Fig. 5: One switching cycle from the 20 kHz simulation of the (a) drain-to-source voltage (V_{DS}), (b) drain current (I_{DS}), (c) instantaneous dissipated power (P_{INS}), and (d) cumulative dissipated energy (E_{CUM}) for the active lower SiC MOSFET (SiC_MOS1) in the 100 A, 10 kV half-bridge SiC MOSFET/JBS power module previously shown in Fig. 2.

In addition to the inductor current, SiC_MOS1 also conducts capacitive currents resulting from charging the output capacitances of the other SiC MOSFETs and JBS diodes within the module. This results in a drain current spike at turn-on (see Fig. 5(b)) that is larger than the on-state current and results in a turn-on switching energy indicated in Fig. 5(d) of $E_{SW,ON}$ = 56 mJ/cycle.

During the reverse recovery of diode SiC_JBS2, the drain-source voltage of SiC_MOS1 drops and approaches the SiC MOSFET on-state voltage. Once the MOSFET is fully on, the instantaneous power dissipation is determined by the product of the on-state voltage and drain current. During this on-state phase of the switching cycle (e.g., the time interval between 29.150 ms to 29.172 ms), the instantaneous power dissipation is small compared to the value of the power spikes during switching events, but the time duration of the on-state phase of the switching cycle is much longer than the switching times. Therefore, the energy-loss waveform rises with a constant slope (determined by the inductor current and the SiC MOSFET on-state voltage) during the on-state phase of the switching cycle.

When the gate of SiC_MOS1 is turned off (t = 29.172 ms in Fig. 5), V_{DS} rises to maintain the constant current in the load inductor. During the voltage rise the load current charges the output capacitances of all of the devices within the module. Once V_{DS} reaches the supply voltage of 5000 V, the drain voltage is clamped at the supply voltage by the anti-parallel diode on SiC_MOS2. Because the MOSFET channel is turned off rapidly before the voltage begins to rise, the turn-off switching energy indicated in Fig. 5(d) ($E_{SW,OFF}$ = 5 mJ) is less by more than an order of magnitude than the turn-on switching energy.

IV. RESULTS OF MODULE OPTIMIZATION PARAMETRIC STUDY

Table 1 summarizes the results of a parametric module simulation study performed to optimize the 100 A, 10 kV half-bridge module and circuit parameters for the circuit conditions similar to a 13.8 kV, 2.75 MVA SSPS. The results are obtained using the circuit shown in Fig. 1 that emulates the conditions of a hard-switched boost converter with a 5 kV bus and a continuous current of 100 A [9]. These simulations assume that the coolant flow rate is sufficient to keep the baseplate bottom temperature at 25 ºC.

Table 1 lists the total dissipated power (P), and the individual SiC MOSFET and SiC JBS diode dissipated powers (P_{MOS} and P_{JBS}). The components of loss are also indicated for each device; that is, on-state loss ($E_{ON-STATE}$ for SiC MOSFET and E_{COND} for SiC JBS diode), turn-on loss ($E_{SW,ON}$), and turn-off loss ($E_{SW,OFF}$). Also, the peak temperatures ($T_{PEAK, MOS}$ for SiC MOSFET and $T_{PEAK,JBS}$ for SiC JBS diode) are given for each device. Each case in the table is for a different set of module parameters; i.e., total MOSFET and diode chip areas (A_{MOSFET} for SiC MOSFET and A_{JBS} for SiC JBS diode), and gate resistance (R_G).

As a baseline, Case 1 uses A_{MOSFET} = 3.09 cm^2 and A_{JBS} = 5.0 cm^2 as validated in Figs. 2 through 5 as in [5] with R_G = 0.5 Ω. Making the SiC MOSFET larger than the baseline reduces the losses slightly and reduces the

MOSFET temperatures but requires the gate resistance to be scaled inversely proportional to the MOSFET area (see Cases 2 and 3). Making the SiC JBS diode smaller than the baseline reduces the losses and decreases the MOSFET temperature (see Cases 4 and 5). Further reduction of diode area does not reduce loss substantially and increases the maximum on-state voltage of the SiC JBS diode, thus increasing the voltage blocking requirement of the series blocking diode.

In addition to the optimal SiC MOSFET and JBS diode die area and gate resistance requirements for the 100 A, 10 kV half-bridge SiC MOSFET/JBS power module, the SiC MOSFET also requires sufficiently low gate inductance to enable fast (20 kHz capable) turn-on and turn-off. Fig. 6 shows the effect of the gate inductance on the drain-source voltage, drain current, gate-source voltage, and gate current waveforms for five different values of the gate inductance (L_G = 0 H, 10 nH, 20 nH, 30 nH, 40 nH) for the lower SiC MOSFET in the half-bridge power module. A gate voltage overshoot and switching delay due to increasing gate inductance can be clearly seen. Thus, it is necessary to keep the gate inductance value below 20 nH to prevent a gate voltage spike exceeding the maximum reliable gate voltage (20 V).
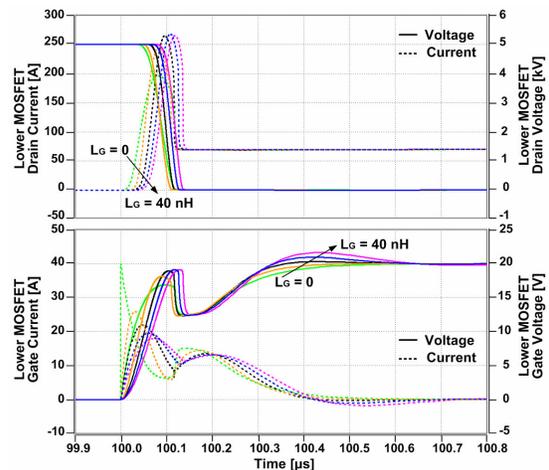
Fig. 6: The effect of the gate inductance on the drain-source voltage, drain current, gate-source voltage, and gate current waveforms for five different values of the gate inductance L_G (0 H, 10 nH, 20 nH, 30 nH, 40 nH) for the lower SiC MOSFET in the 100 A, 10 kV half-bridge power module.

V. SSPS SIMULATION RESULTS

Fig. 7 shows an example circuit that can be used as a building block to implement a SSPS [8]. To handle a 13.8 kV-rms AC primary voltage, four of these blocks can be connected in series at the primary for each phase. This would result in each block handling a nominal 5 kV operating peak 60 Hz bus voltage with the 10 kV SiC bridges. The outputs of the four blocks can be connected in parallel to provide the low voltage SSPS output. This configuration would require twelve blocks to implement a three-phase 2.75 MVA, 13.8 kV to 465 V SSPS.

The SSPS building block of Fig. 7 consists of several stages: 1) a front-end rectifier which converts the input

60 Hz AC into a nominally 5 kV MV-DC bus, 2) a high frequency link (using 10 kV SiC half-bridge modules, a nanocrystalline core HF transformer, and a low-voltage rectifier bridge) that steps down the voltage, and 3) a low-voltage inverter bridge that creates the 60 Hz AC output.

Fig. 8 shows the electro-thermal simulations for the circuit shown in Fig. 7 and a module configuration similar to Case 5 of Table 1. The simulations are for the worst case coolant temperature of 80 °C. In this case, the MOSFET junction temperature reaches about 100 °C at the rated load and 0.8 power factor lagging. This represents enough margin in the SiC modules to handle transient overloads or fault conditions and represents an acceptable temperature cycle for step load changes.

Fig. 8: Simulated waveforms for the circuit shown in Fig. 7 with an optimized module configuration similar to Case 5 of Table 1.

Fig. 7: Example of a building block circuit for an SSPS. This building block converts medium voltage AC (MV-AC) at the primary (PRI) to low voltage AC (LV-AC) at the secondary (SEC).

Table 1: Power and Energy Calculations for 10 kV SiC MOSFET/JBS Module

Case #	Total	SiC MOSFET					SiC JBS Diode				
	P [W]	P_{MOS} [W]	$E_{ON\text{-}STATE}$ [J]	$E_{SW,ON}$ [J]	$E_{SW,OFF}$ [J]	$T_{PEAK,MOS}$ [° C]	P_{JBS} [W]	E_{COND} [J]	$E_{SW,ON}$ [J]	$E_{SW,OFF}$ [J]	$T_{PEAK,JBS}$ [° C]
1	801	721	0.019	0.056	0.005	71.15	80	0.0094	0.0077	0.0077	28.17
2	859	773	0.011	0.065	0.007	55.41	86	0.0101	0.0077	0.0077	28.25
3	780	695	0.011	0.057	0.007	54.87	85	0.0099	0.0077	0.0077	28.23
4	713	600	0.018	0.044	0.005	67.47	113	0.0133	0.0046	0.0048	32.51
5	694	533	0.018	0.037	0.005	61.30	161	0.0188	0.0030	0.0031	39.52
6	1055	933	0.021	0.072	0.010	77.31	122	0.0142	0.0047	0.0047	32.60

Case 1: A_{JBS} = 5.00 cm^2, A_{MOSFET} = 3.09 cm^2, R_G = 0.5 Ω. (baseline)
Case 2: A_{JBS} = 5.00 cm^2, A_{MOSFET} = 5.00 cm^2, R_G = 0.5 Ω.
Case 3: A_{JBS} = 5.00 cm^2, A_{MOSFET} = 5.00 cm^2, R_G = 0.309 Ω
Case 4: A_{JBS} = 3.09 cm^2, A_{MOSFET} = 3.09 cm^2, R_G = 0.5 Ω.
Case 5: A_{JBS} = 2.00 cm^2, A_{MOSFET} = 3.09 cm^2, R_G = 0.5 Ω. (Optimized)
Case 6: A_{JBS} = 3.09 cm^2, A_{MOSFET} = 3.09 cm^2, R_G = 2.0 Ω.

VI.   SUMMARY OF RESULTS AND CONCLUSIONS

A parametric simulation study is presented to optimize Phase II 100 A, 10 kV, 20 kHz half-bridge SiC MOSFET/JBS for circuit conditions similar to those required for the Phase III SSPS. The simulations are performed using the experimentally validated electrical model for the 10 kV SiC MOSFET and SiC JBS diode, and the recently developed and validated thermal model for the module package. The simulations are performed for a circuit that emulates hard switch conditions similar to the SSPS full wave inverter with a quarter sine-wave current cycle, while only requiring the use of one 10 kV MOSFET switch and one 10 kV JBS diode. The results indicate that the performance of the module can be optimized by varying power module parameters such as the number of SiC MOSFET and SiC JBS diode chips, gate resistance, and gate inductance. The detailed description of the loss mechanism and the simulation results for a representative SSPS is also presented.

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