4. Power Electronics Research and Technology Development

4.1 Wide Bandgap Materials

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Objectives

- Assess the impact of replacing silicon (Si) power devices in transportation applications with devices based on wide-bandgap (WBG) semiconductors.
- Develop device models for system level simulation studies and analyze the impact of silicon carbide (SiC) devices on the system performance.
- Build high-temperature packages for SiC power devices to operate at 200°C.
- Study the feasibility of building a 55-kW all-SiC inverter.

Approach

- Develop models of WBG semiconductor devices, especially SiC diodes, junction field-effect transistors (JFETs), and metal oxide semiconductor field-effect transistors (MOSFETs).
- Model a 55-kW all-SiC inverter and compare it with similarly rated all-Si and Si-SiC hybrid inverters.
- Build high-temperature packages for SiC power devices to operate at 200°C.
- Survey possible device packaging techniques.

Major Accomplishments

- Acquired several SiC Schottky diodes, JFETs, and GaN Schottky diodes.
- Tested, characterized, and modeled SiC Schottky diodes, JFETs, and GaN Schottky diodes.
- Modeled a 55-kW all-SiC inverter and compared its performance with that of similarly rated all-Si and Si-SiC hybrid inverters.
- Built high-temperature packages for SiC power devices to operate at 200°C.
- Built and tested all-Si and Si-SiC hybrid inverters [Si insulated gate bipolar transistors (IGBTs) and SiC Schottky diodes] and compared the results.

Technical Discussion

A. Device Modeling

Several new WBG devices were acquired this year and were tested, characterized, and modeled. The list of devices includes SiC JFETs, Schottky diodes, and GaN Schottky diodes. All the devices obtained

were experimental samples. A data record of devices tested to date is located in the appendix to this section.

A.1 SiC Schottky Diode

SiC Schottky diodes are majority carrier devices and are attractive for high-frequency switching because they have lower switching losses than pn diodes. However, they have higher leakage currents, which affect the breakdown voltage rating of the devices. Tests were conducted of 600-V/75-A SiC Schottky diodes, and the results are presented in the following subsections.

Static characteristics

I-V characteristics of the 600-V/75-A SiC Schottky diode were obtained at different temperatures in the –50°C to 175°C temperature range (Figure 1). Considering the piece-wise linear (PWL) model of a diode—which includes a dc voltage drop, V_D, and a series resistor, R_D— the diode I-V curves can be approximated with the following equation:

$$V_d = V_D + R_D \cdot I_d \tag{1}$$

where V_d and I_d are the diode forward voltage and current, and V_D and R_D are the diode PWL model parameters.

Figure 2 shows R_D and V_D values of the 600-V /75-A SiC Schottky diodes with respect to temperature. As seen in the figure, V_D decreases with temperature and R_D increases with temperature. The increase in R_D is an effect of the positive temperature coefficient of the SiC Schottky diodes, which enables these devices to be paralleled easily. Equations (2) and (3) show the temperature dependence of the SiC Schottky diode PWL model parameters.

$$V_D = -0.001 \cdot T + 0.94 \text{ (Volts)} \tag{2}$$

$$R_D = 8.9 \times 10^{-5} \cdot T + 0.013 \text{ (Ohms)} \tag{3}$$

where T is the temperature in degrees C.

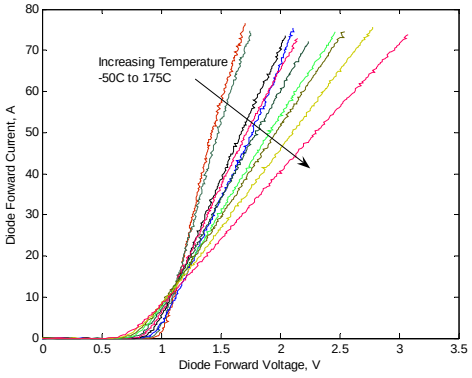


Figure 1. Experimental I-V curves of the 75-A SiC Schottky diode.

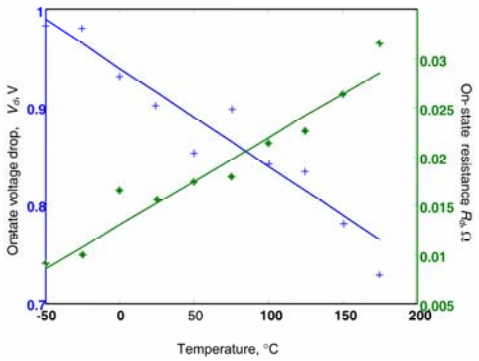


Figure 2. R_D and V_D obtained from the experimental data in Figure 1.

Dynamic characteristics

The SiC Schottky diode was also tested in a chopper circuit (Figure 3) to observe its dynamic characteristics. The IGBT in the circuit was switched at a low switching frequency of 1 Hz to prevent self-heating effects on the diode. The double pulse circuit enables the use of an inductive load instead of the resistive and inductive load together. The current through the inductor builds up during the first pulse and peak forward current is adjusted by changing the width of the first pulse. The switch is turned off and turned on for short periods after the first pulse. The turn-on and turn-off energy losses can be obtained during the short pulse intervals. The double pulse waveforms are shown in Figure 4.

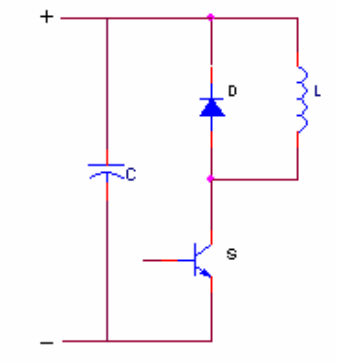


Figure 3. Test circuit for dynamic characterization.

To obtain the switching characteristics at high temperatures, a test set-up was built as shown in Figure 5. The device under test was placed inside the box on a heat sink, and the temperature was controlled using a resistive load paced in the box on the heat sink. The temperature of the heat sink was monitored using a thermistor.

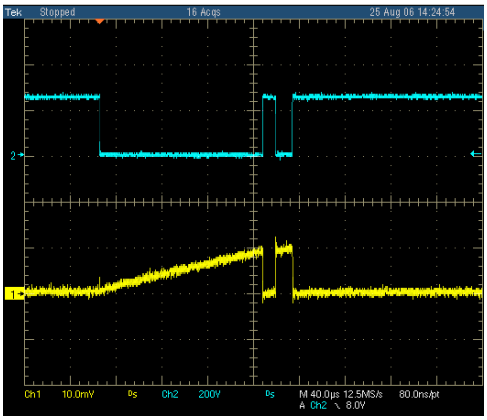


Figure 4. Current and voltage waveforms of SiC JFET S3—double pulse test.

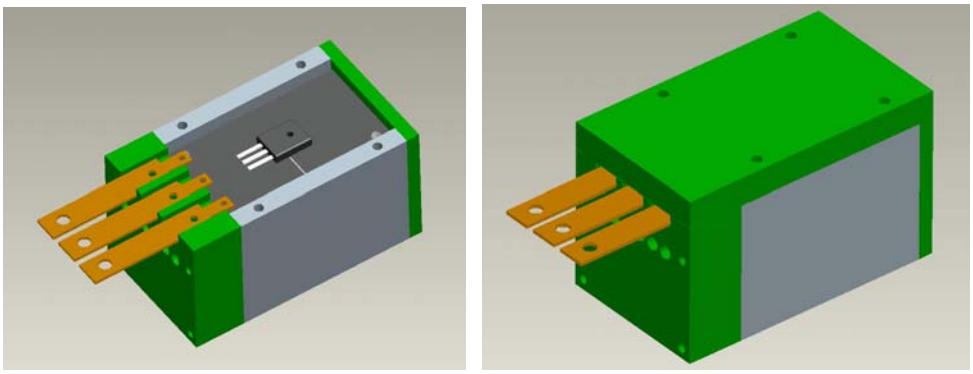


Figure 5. Temperature-controlled box used for high-temperature testing.

The reverse recovery current waveforms obtained for different forward currents at room temperature are shown in Figure 6. The reverse recovery current did not change with forward current. Note that, theoretically, Schottky diodes do not display reverse recovery phenomenon because they are majority carrier devices and do not have a stored charge. The switching losses obtained at different temperatures are shown in Figure 7. The switching loss equation is given below in Equation (4).

$$E_{sw} = -6.5\times10^{-9}\cdot I + 3.2\times10^{-7} \quad \text{(Joules)} \tag{4}$$

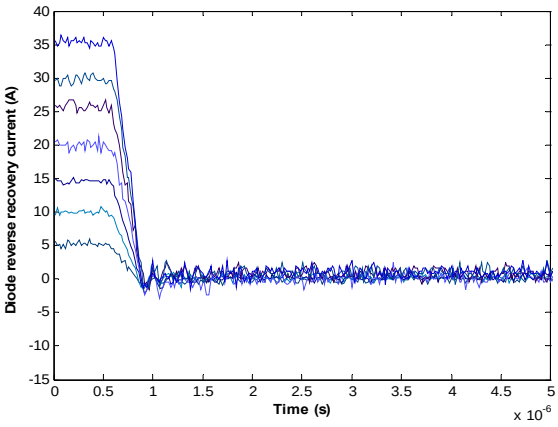


Figure 6. Reverse recovery current waveforms of the SiC Schottky diode for different forward current values.

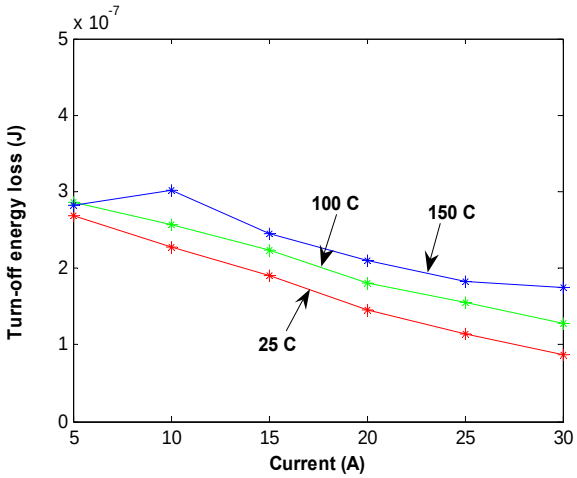


Figure 7. Switching energy losses of SiC diode at different temperatures.

A.2 GaN Schottky Diodes

Static characteristics

The static characteristics of a 600-V/4-A GaN diode in a temperature range of 25 to 175°C are shown in Figure 8. The PWL model parameters were extracted from the static curves (as discussed in the previous section) and plotted in Figures 9 and 10. V_d decreases and R_d increased with an increase in temperature, as expected. The static characteristics of a similarly rated SiC diode are better compared with the GaN diode, as shown in Figure 11. It should be noted that the GaN device is still an experimental sample and SiC Schottky diode technology is more mature.

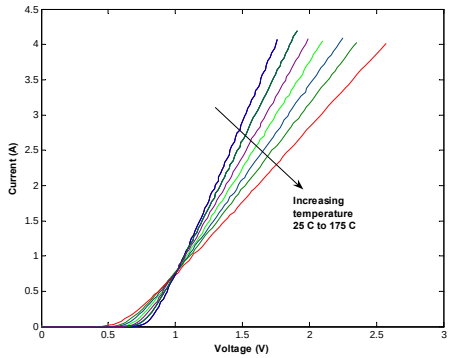


Figure 8. Static characteristics of GaN Schottky diode.

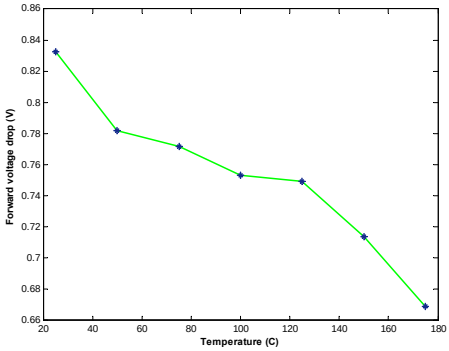


Figure 9. V_d forward voltage drop of GaN Schottky diode.

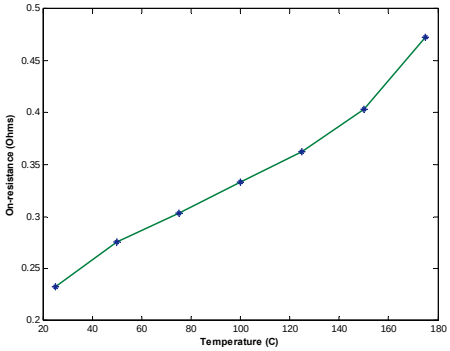


Figure 10. R_d on-state resistance of GaN Schottky diode.

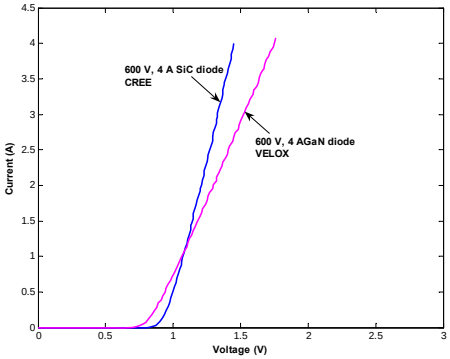


Figure 11. Comparison of i-v curves of SiC and GaN Schottky diodes.

Dynamic characteristics

The dynamic characteristics of the GaN Schottky diode were obtained using the same chopper circuit and high-temperature test set-up as the SiC Schottky diode. Results show that the GaN Schottky diode also has almost zero recovery losses, as expected, similar to the SiC diode (Figure 12). The corresponding turn-off energy losses are shown in Figure 13 for three different temperature conditions. The switching

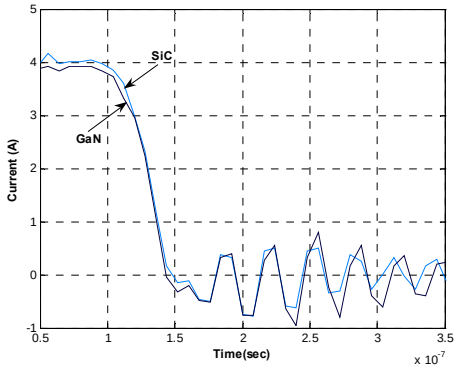


Figure 12. Comparison of reverse recovery currents between SiC and GaN at 25°C.

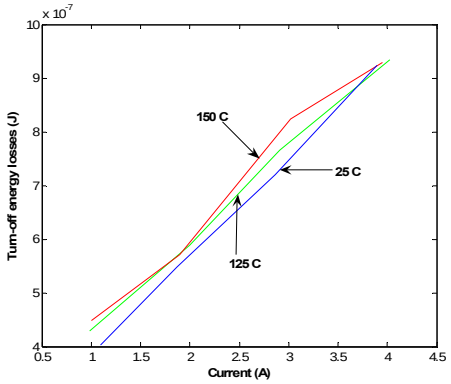


Figure 13. Turn-off energy losses of GaN diode at different temperatures.

losses of the GaN diode were compared with those of a similarly rated 600-V, 4-A SiC Schottky diode, shown in Figure 14, for 125°C operation. The losses of the SiC Schottky diode are slightly less than those of the GaN Schottky diode for this operational condition.

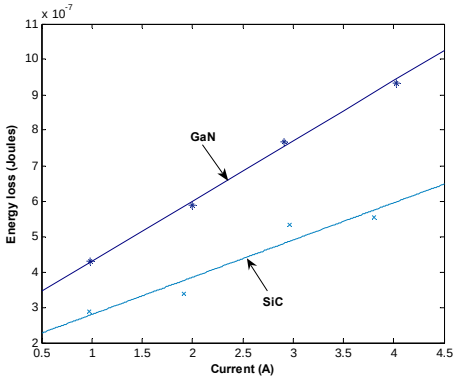


Figure 14. Energy losses comparison between Si and GaN diodes at 125°C.

A.3 JFETs

Static characteristics

Several experimental JFET samples were obtained from different manufacturers. Static characteristics of three different JFETs—S1 (600-V, 5-A), S2 (1200-V, 15-A), and S3 (1200-V, 10-A)—at different temperatures are shown in Figures 15–17, respectively. SiC JFETs have a positive temperature coefficient, which means that like SiC Schottky diodes, their conduction losses will be higher at higher temperatures. However, positive temperature coefficient makes it easier to parallel these devices and reduce the overall on-resistance.

The on-resistance of the switch S3 increases from 0.25 Ω at −50°C to 0.58 Ω at 175°C, as shown in Figure 18. The on-state resistance can be expressed as a function of temperature as shown in Equation (5).

$$R_D = 7.6\times10^{-5}\cdot T^2 + 0.00068\cdot T + 0.26 \ \text{(Ohms)} \qquad (5)$$

The transfer characteristics of an SiC JFET are shown in Figure 19. The negative gate pinch-off voltage required to turn off the device is higher than that required for Si devices. The earlier-generation devices had pinch-off voltages that varied between samples, as shown in Figure 20. The pinch-off voltages of the newer-generation devices obtained this year do not vary as much. The transfer characteristics obtained for ten different samples are shown in Figure 20. This is a significant improvement that indicates that SiC JFET technology is maturing.

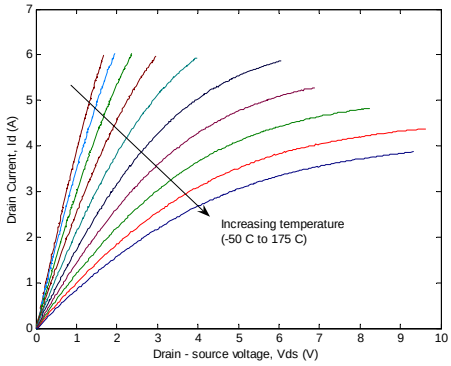


Figure 15. i-v curves of JFET S1.

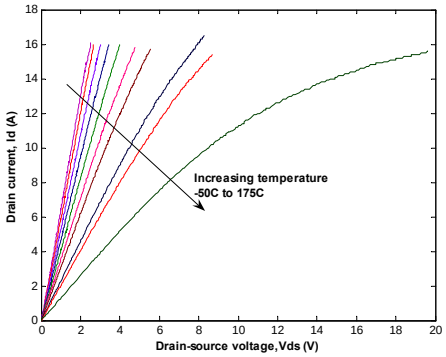


Figure 16. i-v curves of JFET S2.

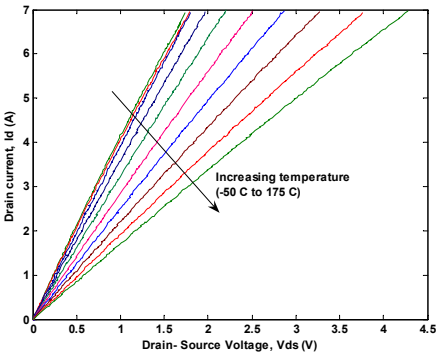


Figure 17. i-v curves of JFET S3.

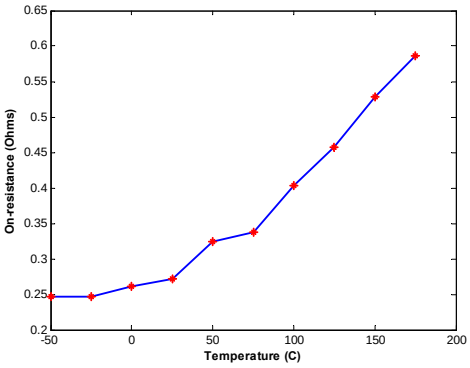


Figure 18. On-resistance of S3.

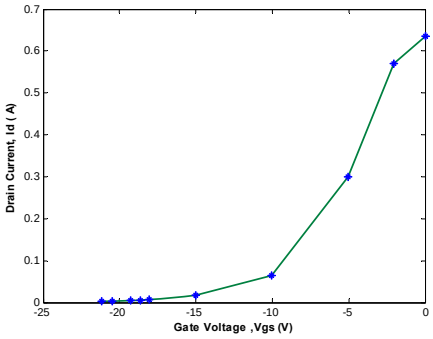


Figure 19. Transfer characteristics of JFET S3.

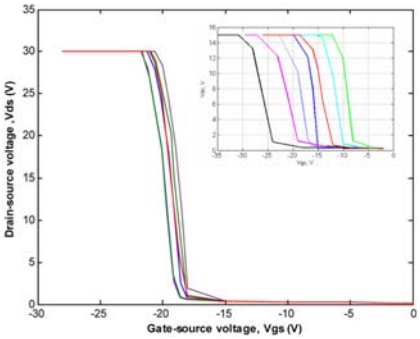


Figure 20. Transfer characteristics of several SiC JFET samples.

Dynamic characteristics

SiC JFETs are normally-on devices, and they can be turned off only by applying a negative voltage. Based on the transfer characteristics (Figure 20), a gate voltage of –22 V has been selected, as that would be enough to turn off most of the samples tested. The dynamic characteristics of the JFET S3 at several temperatures and currents were obtained using the high-temperature set-up and the double pulse circuit test. The total energy losses of the JFET during switching are shown in Figure 21. The losses do not change much with temperature The switching loss equation is given below in Equation (6).

$$E_{swtotal} = 12.2 \times 10^{-5} \cdot I + 1.7 \times 10^{-5} \text{ (Joules)} \quad (6)$$

B. 55-kW Inverter Modeling

Three different inverters were modeled in Simulink to compare and study the system-level benefits of replacing SiC devices with Si devices. The total system-level model with a control system block, device loss model blocks, and a heat sink model block is shown in Figure 22. The power losses of the switches are calculated and fed to the heat sink model, which calculates the junction temperatures of the devices. These temperatures are fed back to the device loss models so that the temperature-dependent device parameters are updated. The blocks in the model will be explained in detail in the next few subsections.

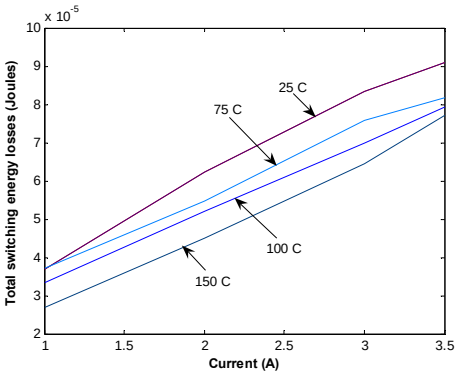


Figure 21. Total switching energy losses of JFET S3 at different currents and temperatures.

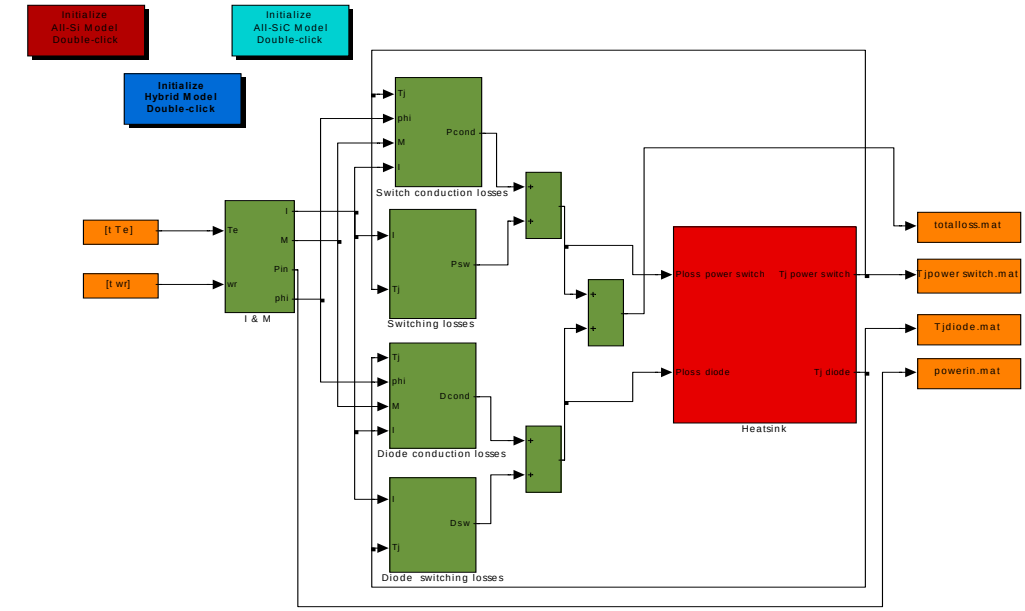


Figure 22. Block diagram of the system level model.

B.1 Control Block Model

The speed and torque profiles for a Federal Urban Driving Schedule (FUDS) cycle were obtained from the power train system analysis toolkit (PSAT), a drive train simulation software developed by Argonne National Laboratory. The speed and torque profiles were fed to the control block, which calculates the peak current, modulation index, input power, and power factor for the average loss model. The control block is explained in detail by Ozpineci.[1]

B.2 Device Models

The devices used in three different inverters are listed in Table 1.

Table 1. Ratings of the devices used in the inverters

	Switch	Diode
All-SiC inverter	1200-V/10-A SiC JFET	600-V/75-A SiC Schottky diode
Hybrid inverter	600-V/50-A Si IGBT	600-V/75-A SiC Schottky diode
All-Si inverter	600-V/50-A Si IGBT	600-V/80-A Si pn diode

The devices listed in Table 1 were scaled to a rating of 600 V and 600 A for the power switches and 600 V and 450 A for the diodes to be able to simulate a 55-kW inverter. The device loss models were developed from the static and dynamic characteristics of the devices. The conduction losses were calculated using an average modeling technique that is explained in detail in Ozpineci.[1] The conduction loss parameters derived from the test data were used in the modeling equations. The switching loss models were calculated from total energy losses during switching. The SiC JFET and SiC diode modeling was discussed in earlier sections of this report. Si IGBT and Si pn diode modeling will be presented in the following sections.

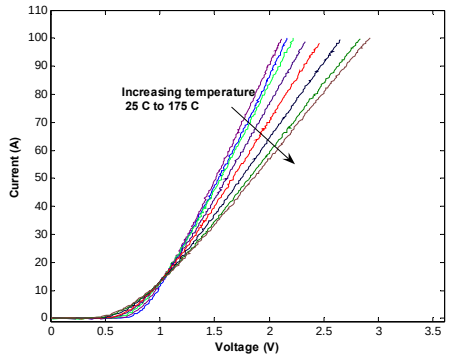


Figure 23. i-v characteristics of IGBT at different temperatures.

Si IGBT model

A 600-V, 50-A trench-stop technology–based IGBT with a maximum junction temperature specification of 175°C was chosen for the all-Si and hybrid inverter simulations. This IGBT is a commercial device from Infineon, part number IGP60N50T.

Static characteristics

The static characteristics of the IGBT at different temperatures are shown in Figure 23. The IGBT has a positive temperature coefficient similar to that of an SiC diode. The static characteristics of the IGBT are very similar to those of the diode and can be modeled using the PWL model. The PWL model parameters were extracted from the static curves and are derived as a function of temperature as shown in Equations (7) and (8).

$$V_D = 1.7\times10^{-7}\cdot T^3 + 4.3\times10^{-5}\cdot T^2 - 0.0032\cdot T + 0.91 \text{ (Volts)} \quad (7)$$

$$R_D = 1.9\times10^{-7}\cdot T^2 + 2.5\times10^{-5}\cdot T + 0.012 \text{ (Ohms)} \quad (8)$$

Dynamic characteristics

The dynamic characteristics of the IGBT were obtained using the double pulse circuit and the high-temperature setup described earlier with both an SiC Schottky diode and a Si pn diode to model the effects of the reverse recovery on the turn-on current of the IGBT. Figure 24 shows the difference in turn-on losses of the IGBT. The better reverse-recovery characteristics of the SiC diode help in reducing the losses of the IGBT. This is because when a diode in an inverter is turning off, the diode-reverse-recovery current passes through the other IGBT in the same phase leg, causing additional losses. The IGBT turn-off losses do not change much with Si or SiC diodes because the diode affects only the turn-on losses of the IGBT, as shown in Figure 25.

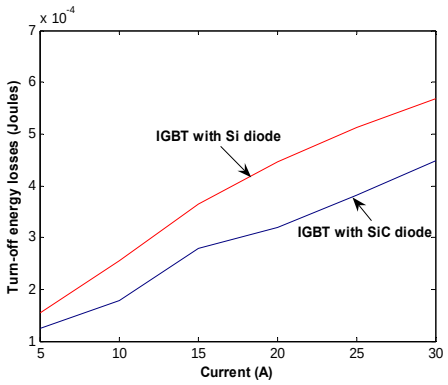


Figure 24. Turn-on switching energy losses of IGBT with Si and SiC diodes at 25°C.

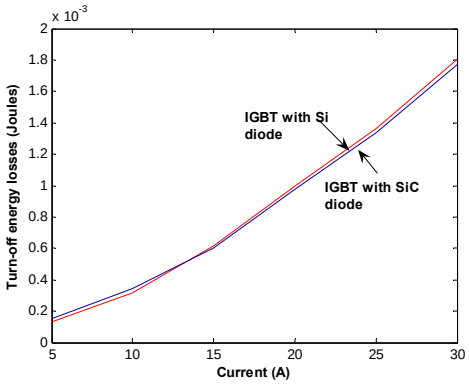


Figure 25. Turn-off switching energy losses of IGBT with Si and SiC diodes at 25°C.

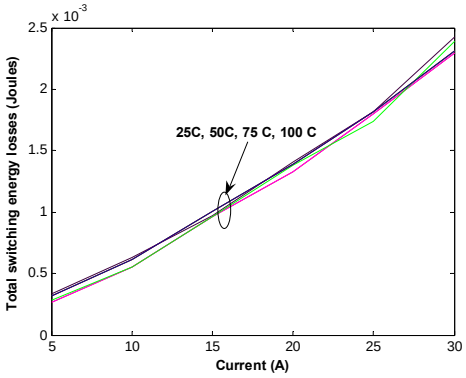


Figure 26. Total switching energy losses of IGBT at different currents and temperatures

The diodes in the test were kept outside the temperature-controlled box and hence did not affect the IGBT losses at different temperatures. The turn-off losses of the IGBT dominated the turn-on losses. Since the turn-off losses did not change much with temperature, the total switching losses of the IGBT did not change much with temperature (Figure 26). The variation in switching losses of the IGBT at different temperatures obtained from tests matched the data presented in the data sheet. The switching loss equation is given below in Equation (9).

$$E_{swtotal} = 1.2\times10^{-6}\cdot I^2 + 3.8\times10^{-5} \cdot I + 3.2\times10^{-5} \text{ (Joules)} \quad (9)$$

Si diode model

A 600-V/ 80-A Si pn diode with a maximum junction temperature specification of 175°C was chosen for the all-Si and hybrid inverter simulations. The diode is a commercial device from Infineon and the part number is RURG8060.

Static characteristics

The static characteristics of the diode at different temperatures are shown in Figure 27. The Si diode has a negative temperature coefficient, as expected, unlike the SiC Schottky diode. The static characteristics of the diode can be modeled using the PWL model. The PWL model parameters were extracted from the static curves and are derived as a function of temperature as shown in Equations (10) and (11).

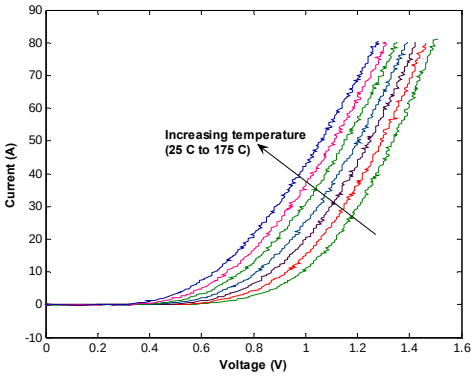


Figure 27. i-v characteristics of Si pn diode at different temperatures.

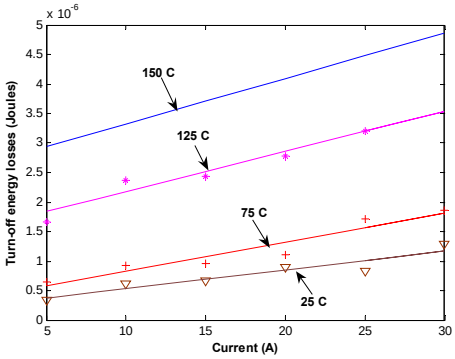


Figure 28. Turn-off energy losses of Si pn diode at different currents and temperatures.

$$V_D = -0.0012 \cdot T + 0.59 \,(\text{Volts}) \qquad (10)$$

$$R_D = 1.5\times10^{-7} \cdot T^2 + 1.5\times10^{-5} \cdot T + 0.0078 \,(\text{Ohms}) \qquad (11)$$

Dynamic characteristics

The dynamic characteristics of the Si pn diode were obtained using the same chopper circuit and high-temperature set-up as used for the SiC Schottky diode. The switching energy losses due to the reverse recovery current are shown in Figure 28. The reverse recovery losses of the Si pn diode increase with an increase in current and temperature, as seen in Equations (12) and (13)

$$E_{swoff} = \mathrm{a} \cdot I + b \ \text{(Joules)} \qquad (12)$$

$$a = 3.6\times10^{-10} \cdot T + 2.3\times10^{-8} \qquad (13)$$

$$b = 2.1\times10^{-10} \cdot T^2 - 1.8\times10^{-8} \cdot T + 5.3\times10^{-7} \qquad (14)$$

where T is in °C.

B.3 Thermal Model

The thermal model developed is a 1-dimensional thermal resistance model with 2-dimensional heat spreading effects modeled using finite element analysis. The thermal resistance calculated is a sum of 1-dimensional cross section resistance and the resistance due to heat spreading through the cross section area. A side view of the cross section is shown in Figure 29. The structure, thicknesses, and materials of the layers used in the model were taken from Semikron's SKAI module. The heat sink model was based on the commercially available air-cooled inverter. Note, however, that the heat sink used in the calculation is a model with adjustable fin length and thickness and is designed for natural convection. The equivalent circuit is shown in Figure 30. The model assumes that the temperature along the top of the base plate is uniform. This is a valid assumption because the thermal resistance in the entire cross section is high, from the base plate to the tip of the fins

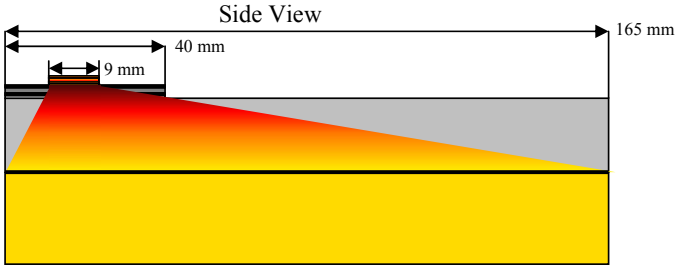


Figure 29. Side view of the cross section of the inverter.

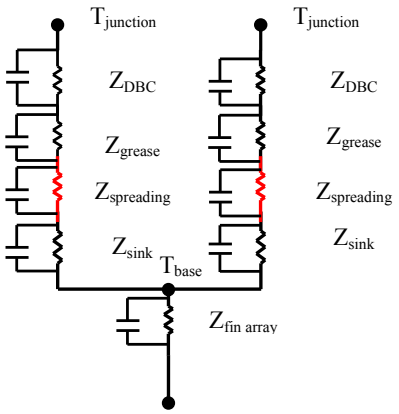


Figure 30. The equivalent circuit of the thermal model.

on the heat sink. The spacing between devices on top of the direct bonded copper is based on the number of devices and the length of the DBC sled and is the same as in the Semikron SKAI unit. The dimensions of each device on top of the DBC can be changed. However, the diodes and the main power switches are assumed to be the same dimensions so that there is a line of symmetry along the cross section.

B.4 Simulation Results

The three different inverter models were simulated for several operating conditions, and some of the results are discussed below. Efficiency vs output power plots for several operating conditions comparing the inverters are shown in Figures 31 and 32. The hybrid inverter and all-SiC efficiencies are higher than those of the all-Si inverter for all operating conditions. The percentage loss reduction was calculated comparing the power loss differences between the hybrid inverter and the all-SiC inverter with respect to the all-Si inverter, as shown in Equation (15).

$$\%\,loss\ reduction = \frac{P_{loss}^{All-Si} - P_{loss}^{All-SiC}}{P_{loss}^{All-Si}} \times 100 \qquad (15)$$

The temperature profiles of the JFETs and Schottky diodes in the all-SiC inverter over a FUDS cycle are shown in Figure 33.

The heat sink used in the simulations was designed for 30-kW continuous power. Using the inverter loss model and the thermal model, the junction temperatures calculated for 30-kW operation of the all-Si and all-SiC inverters at different ambient temperatures are shown in Figure 34. The figure also shows the volume of the heat sink required, corresponding to the junction temperature of the device. Figure 34 shows that with natural convection, the all-Si inverter can operate only at 25°C ambient conditions because of the junction temperature limitations. At 105°C ambient, the junction temperatures are beyond the theoretical limits of the Si devices, and even increasing the heat sink volume does not reduce the junction temperatures because the heat sink is saturated. The temperatures of the SiC devices are much lower because of the reduced losses compared with the Si devices. Hence, for the same junction temperature of 150°C, the heat sink volume needed is two-thirds less for an all-SiC inverter than for an all-Si inverter.

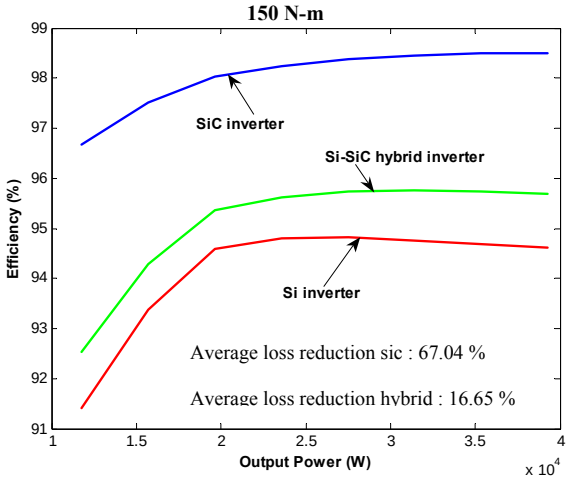


Figure 31. Efficiency vs output power of three different inverters at 150 N-m load.

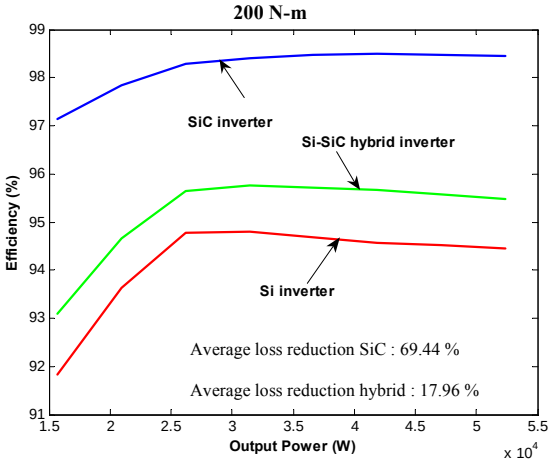


Figure 32. Efficiency versus output power of three different inverters at 200 N-m load.

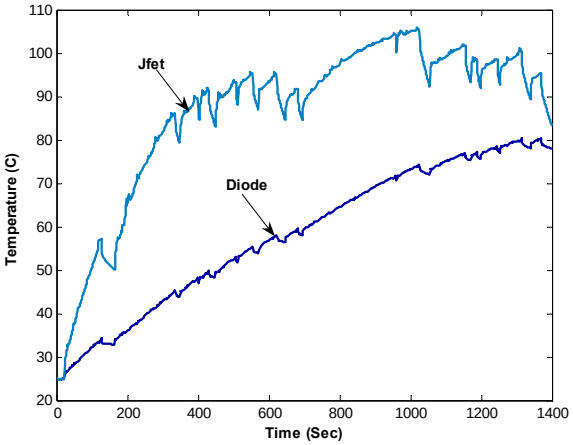


Figure 33. Temperature profile of devices over FUDS cycle.

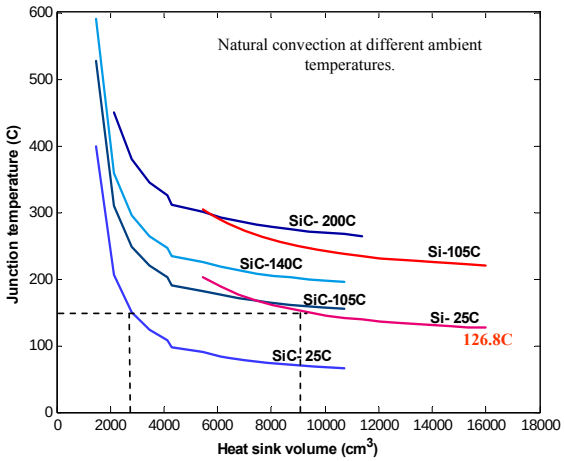


Figure 34. Heat sink volume vs device junction temperatures for all-Si and all-SiC inverters.

C. High-Temperature Packaging Tests

One of the most important characteristics of SiC power devices is that they can operate at much higher temperatures (>300°C) than do Si power devices. Presently, SiC devices use Si device packages that limit the operation temperature (~125°C). Tests at Oak Ridge National Laboratory (ORNL) have shown that at high temperatures, these packages break open and leave the devices inoperable. This year, ORNL collaborated with the University of Arkansas to build several high-temperature packages to demonstrate packages that can operate at 200°C ambient. Two different packages with SiC Schottky diodes were delivered and tested at ORNL.

- TO-220 package

A single-die 600-V/75-A SiC Schottky diode was packaged in a TO-220 through-hole style package (Figure 35). The package was tested at different current levels at 200°C ambient temperature without a heat sink. The case temperature of the diode was measured using a thermocouple. The diode forward voltage drop was measured at different current levels using a Keithley data acquisition system. The voltage drop of the diode and case temperature as measured are shown in Figures 36 and 37. The diode operated at 361°C at 20 A for over an hour without a failure. However, at 25 A, the diode operated for a short time and then failed by shorting across the junction. This is a significant milestone in terms of operating temperature of the device; it clearly demonstrates the high-temperature operation capability of SiC devices.

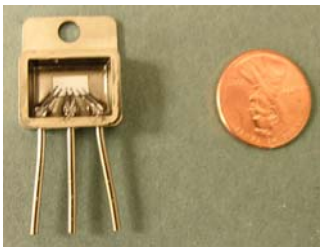


Figure 35. TO-220 through-hole high-temperature package of 75-A SiC Schottky diode.

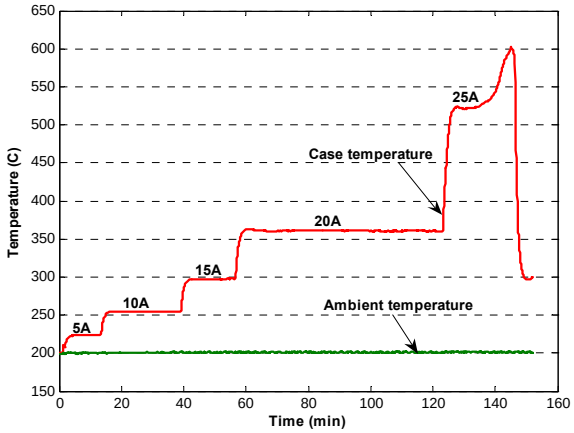


Figure 36. Case temperature of 75-A diode at different current level measured at 200°C ambient.

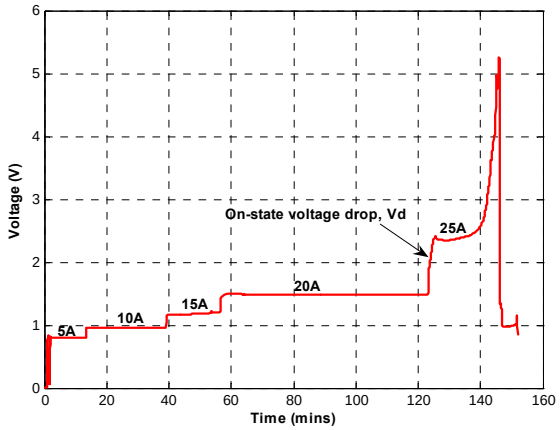


Figure 37. Voltage drop across the diode at different currents.

- 450-A package

Six 600-V/75-A SiC Schottky diodes were packaged in a module yielding a combined rating of 600 V and 450 A, as shown in Figure 38. The static characteristics of the module obtained at different temperatures are shown in Figure 39. The module was also tested at 200°C ambient at different current levels, similar to the testing of the single-die package. The case and ambient temperatures of the diode module were measured using a thermocouple. The forward voltage drop and temperatures are shown in Figures 40 and 41. The module was limited by the contact solder to a maximum operating temperature of 308°C. The upper test temperature limit was set to 282°C so that it would remain below the solder limitation. The operating current corresponding to 282°C was 50 A. The diode operated without any failure for a long duration at this operating point. The effect of the temperature coefficient of the device is evident in the voltage drop plot. The change in current increases the voltage drop, and then the effect of the temperature increase decreases the voltage. Note from Figure 39 that the diode module has a negative temperature coefficient below 120 A and a positive temperature coefficient above that temperature. The maximum current to which the diode module was tested was limited to 50 A.

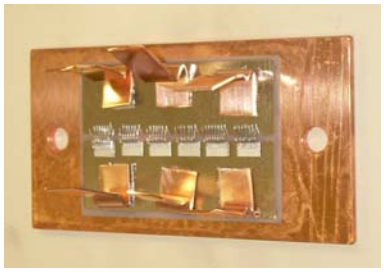


Figure 38. A 450-A high-temperature SiC diode module with six 75-A Schottky diodes in parallel.

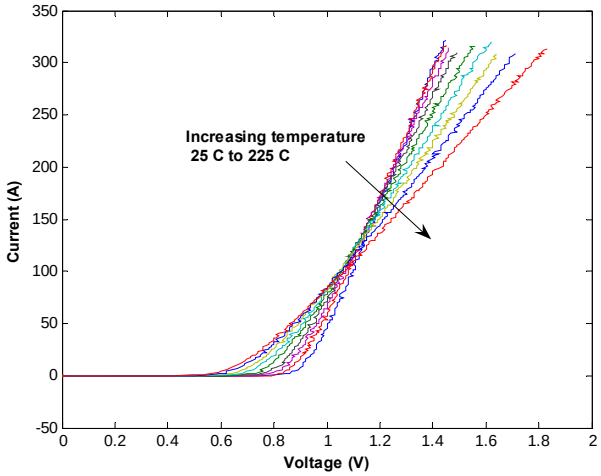


Figure 39. i-v curves of the 450-A diode module.

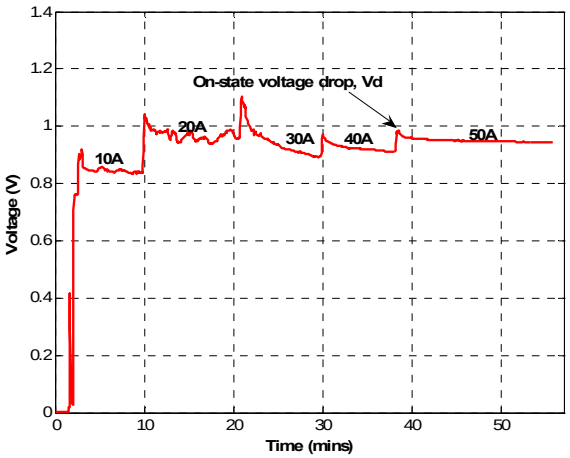


Figure 40. Voltage drop across the diode module at different currents.

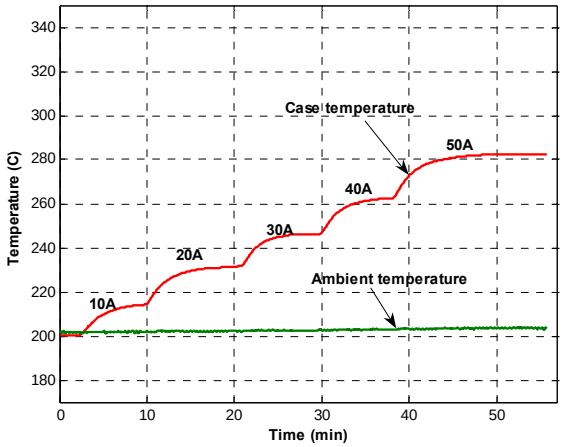


Figure 41. Case temperature of 75-A diode at different current levels measured at 200°C ambient.

D. Hybrid Inverter Tests

The inverter shown in Figure 42 was built at ORNL using power modules delivered by CREE. Two different inverters were built: an all-Si inverter using Si-IGBTs and Si pn diodes, and a hybrid inverter using the same Si IGBTs but SiC Schottky diodes instead of Si pn diodes. The performances of the inverters was compared after an inductive load test. The hybrid inverter and the all-Si inverter were tested with the same test procedure and using the same controller on the same benchtop system.

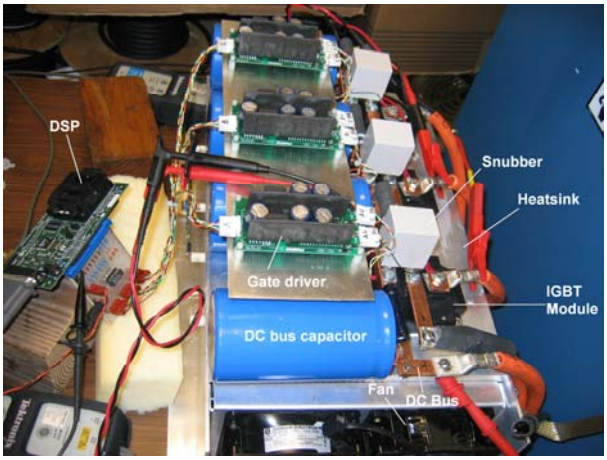


Figure 42. Three-phase inverter built at ORNL.

Test Setup

The output leads of the inverter were connected to a 3-phase star-connected variable resistor bank with a 3-phase inductor in series. The dc inputs were connected to a voltage source capable of supplying

the maximum rated operating voltage and current levels for the inverter. The test setup is shown in Figure 43.

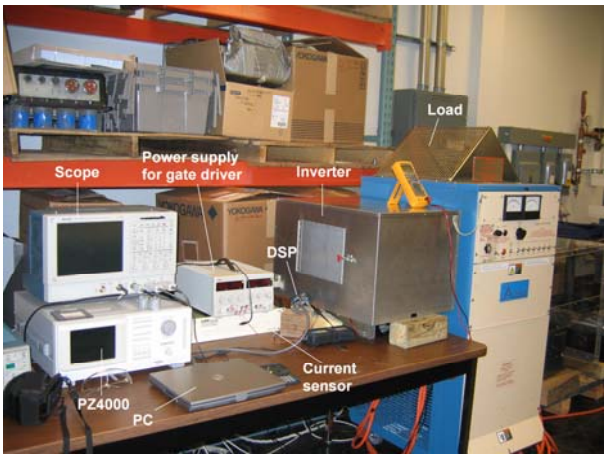


Figure 43. R-L load test setup.

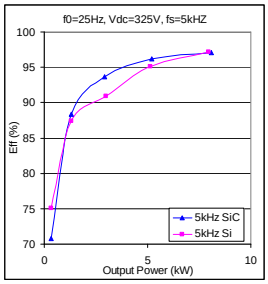
The device modules used in the hybrid inverter were Si IGBT/SiC Schottky diode modules (QID1230009-ES), and the modules used in the all-Si inverter were Si IGBT/Si pn diode modules (CM300DY-24NF). The controls for the inverter were generated using a DSP TMS320F2812. A space vector pulse width modulation technique was used as the control scheme. IGBT modules were driven by a BG2A board (from POWEREX), which used two VLA502-01 gate drivers. The inverter was mounted on a heat sink with fans.

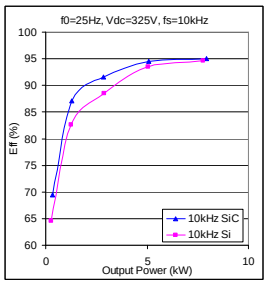
Results

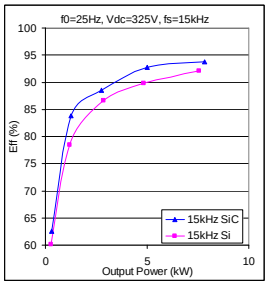
Voltage, current, switching frequency, and the frequency of the output current are important parameters that have significant influences on power losses and efficiency. Thus the tests were conducted under different combinations of these parameters.

dc voltage: 200 V and 325 V
ac side current (rms): 10 A to 50 A
Frequency of output ac current: 25, 50, 75, and 100 Hz
Switching frequency of inverter: 5, 10, and 15 kHz

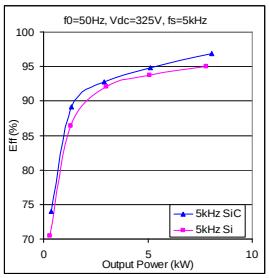
The data obtained for both of the inverters were analyzed and the corresponding efficiencies were calculated. The efficiency versus output power plots for several operating conditions comparing the inverters are shown in Figure 44. The Si-SiC inverter had a higher efficiency than the all-Si inverter. The difference in efficiencies between these two inverters is smaller at low output power and larger at high output power. This is because power losses of both inverters are lower at low output power, and the power losses of the Si inverter increase more quickly as the output power (or current) increases. In some cases, the efficiency of the SiC inverter is even lower than that of the Si inverter at low current levels because the Si pn diode voltage drop is much lower than the SiC Schottky diode voltage drop at low currents; however, most applications will be operating in the higher current regions. The efficiencies of both inverters increase as output power increases (see Figure 44) and decrease as switching frequency increases (see Figure 45), as expected.

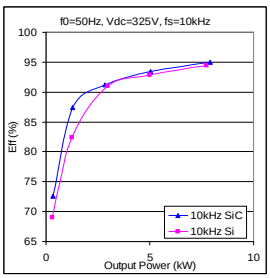


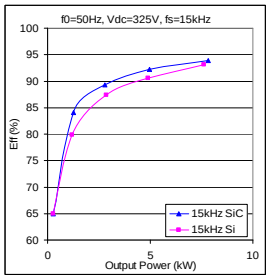




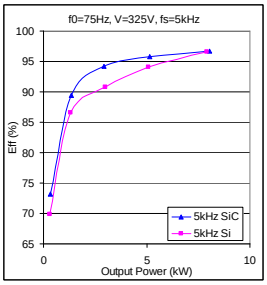
(a) dc voltage 325 V and output frequency 25 Hz

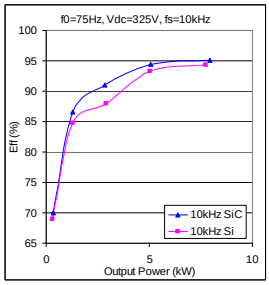


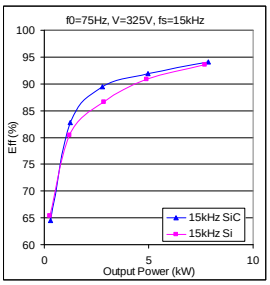




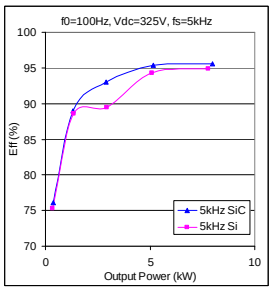
(b) dc voltage 325 V and output frequency 50 Hz

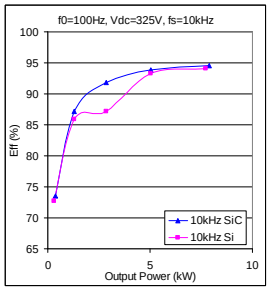


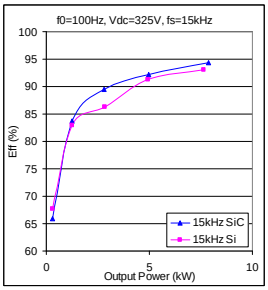




(c) dc voltage 325 V and output frequency 75 Hz

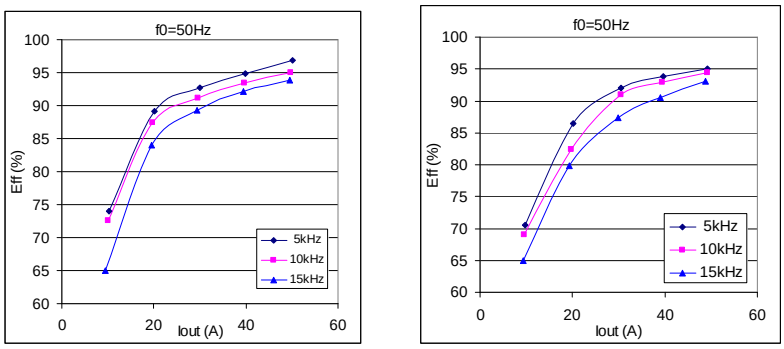






(d) dc voltage 325 V and output frequency 100 Hz

Figure 44. Efficiency vs output power at 325-V dc voltage.



(a) Si-SiC hybrid inverter **(b) All-Si inverter**

Figure 45. Efficiency of inverters at 325 V dc voltage and 50 Hz output.

Conclusion

Several new devices (SiC Schottky diodes, JFETs and GaN Schottky diodes) were acquired, tested, and modeled. There is a significant improvement in performance of the new-generation JFETs, which indicates that SiC switch technology is maturing. The 55-kW inverter simulations showed reduced losses of up to 69% for the all-SiC inverter and up to 28% for the hybrid inverter compared with the all-Si inverter. The inverters were simulated over a FUDS cycle, and the results showed that with natural convection, a two-thirds reduction in heat sink volume can be realized using an all-SiC inverter rather than an all-Si inverter. Two high-temperature packages delivered by the University of Arkansas were tested to demonstrate a high-temperature packaging technology that can operate at 200°C. The diode operated at a temperature of as high as 361°C at 200°C ambient without any failure.

Future Direction

FY 2007 and Beyond

- Acquire, test, and characterize newer-technology WBG power devices.
- Study the impact of SiC devices on plug-in hybrid vehicles.
- Study the fault current limiting capability of SiC devices for safety and protection.
- Study the possibility of using a thermal boundary in SiC power modules where Si gate drivers can be used.

Publications

M. Chinthavali, L. M. Tolbert, B. Ozpineci, and H. Zhang, "High Temperature Power Electronics—Application Issues of SiC Devices," in *International Conference on High Temperature Electronics (HiTEC 2006)*, International Microelectronics and Packaging Society, Santa Fe, New Mexico, May 15–18, 2006.

B. Ozpineci, M. S. Chinthavali, and L. M. Tolbert, "Enhancing Power Electronic Devices with Wide-Bandgap Semiconductors," *Journal of High Speed Electronics*, in press.

B. Ozpineci, M. S. Chinthavali, L. M. Tolbert, A. Kashyap, and A. H. Mantooth, "A 55-kW Three Phase Inverter with Si IGBTs and SiC Schottky Diodes," *IEEE Annual Applied Power Electronics Conference and Exposition*, March 19–23, 2006, Dallas.

H. Zhang, M. Chinthavali, B. Ozpineci, L. M. Tolbert, "Power Losses and Thermal Modeling of 4H-SiC VJFET Inverter," pp. 2630–2634 in *IEEE Industry Applications Society Annual Meeting*, October 2–6, 2005, Hong Kong, China,.

B. Ozpineci, M. S. Chinthavali, and L. M. Tolbert, ”A 55-kW Three Phase Automotive Traction Inverter with SiC Schottky Diodes,” pp. 541–546 in *IEEE Vehicle Power and Propulsion Conference*, Chicago, September 7–9, 2005.

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1. B. Ozpineci, “System Impact of Silicon Carbide Power Electronics on Hybrid Electric Vehicle Applications,” Ph.D. Dissertation, Department of Electrical Engineering, The University of Tennessee, Knoxville, Tennessee, 2005.

Appendix. List of Devices Tested and Their Parameters

Power Diodes

Device type	Ratings	On-resistance (Ω)	Forward voltage drop (Volts)	Manufacturer	Year tested
SiC Schottky Diode	1200 V, 7.5 A	0.15 **Ω** at –50°C to 0.32 **Ω** at 175°C	1.42 **V** at –50°C to 1.21 **V** at 175°C	Rockwell	2004
SiC Schottky Diode	300 V, 10 A	0.15 **Ω** at –50°C to 0.16 **Ω** at 175°C	1.11 **V** at –50°C to 0.83 **V** at 175°C	Infineon	2004
SiC Schottky Diode	600 V, 4 A	0.19 **Ω** at –50°C to 0.39 **Ω** at 175°C	1.09 **V** at –50°C to 0.87 **V** at 175°C	Cree	2004
SiC Schottky Diode	600 V, 10 A	0.14 **Ω** at –50°C to 0.25 **Ω** at 175°C	1.09 **V** at –50°C to 0.82 **V** at 175°C	Cree	2004
SiC Schottky Diode	600 V, 75 A	0.01 **Ω** at –50°C to 0.03 **Ω** at 175°C	0.91 **V** at –50°C to 0.61 **V** at 175°C	Cree	2005
GaN Schottky Diode	600 V, 4 A	0.23 **Ω** at 25°C to 0.47 **Ω** at 175°C	0.83 **V** at 25°C to 0.67 **V** at 175°C	Velox	2006

Power Switches

Device type	Ratings	On-resistance (Ω)	Voltage drop at rated current @ room temperature (Volts)	Manufacturer	Year tested
SiC JFET	1200 V, 2 A	0.36 **Ω** at -50 °C to 1.4 **Ω** at 175 °C	1.3 V @ Vgs = 0V	SiCED	2004
SiC JFET	1200 V, 10 A	0.25 **Ω** at -50 °C to 0.58 **Ω** at 175 °C	2.71 V @ Vgs = 0V	SiCED	2006
SiC JFET	1200 V, 15 A	0.15 **Ω** at -50 °C to 2.2 **Ω** at 175 °C	3.2 V @ V_{gs} = 3V	Rockwell	2006
SiC JFET	600 V, 5 A	0.26 **Ω** at -50 °C to 1.87 **Ω** at 175 °C	2.25 V @ V_{gs} = 3 V	Semisouth	2006
SiC MOSFET	1200 V, 5 A	(0.48 **Ω** at -50 °C to 0.23 **Ω** at 50 °C) (0.24 **Ω** at 75 °C to 0.29 **Ω** at 175 °C)	1.5 V@ V_{gs}= 20 V	Cree	2005

4.2 Integrated dc-dc Converter for Multi-Voltage Bus Systems

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Objectives

- Develop a dc-dc converter topology that
  - — can significantly reduce the component count,
  - — is applicable to both triple-voltage and dual-voltage systems with essentially no hardware modifications,
  - — provides easy power scaling capability to meet power requirements for varying vehicle sizes, and
  - — can incorporate all future advanced components such as silicon carbide (SiC) devices and thermal management technologies as they become available.

- Produce a 4-kW prototype using 2-kW modules as building blocks and testing data to evaluate the prototype's capability to meet the FreedomCAR targets and power scaling capability.
- Establish requirements for dc-dc converters for various power system configurations in fuel cell–powered vehicles (FCVs).

Approach

The following approaches are taken to reduce the cost and size and increase the efficiency and power density of dc-dc converters for multi-bus systems in hybrid electric vehicles (HEVs) and FCVs.

- Increase the level of integration to minimize the number of switches and thus the associated gate drivers in order to reduce component count and still maintain a flexible topology: same circuit applicable to both dual- and triple-voltage systems.
- Increase switching frequency to reduce the weight, size, and volume of passive components.
- Employ soft switching and synchronous rectification to increase efficiency and power density.
- Employ soft switching to lower electromagnetic interference (EMI) noise.
- Use an interleaved modular approach for scaling power up.
- Optimize packaging.
- Conduct a literature search on dc-dc converters for FCV power systems.

Major Accomplishments

- Topology development
  - – A half-bridge–based dc-dc converter has been developed that can interconnect the 14-V, 42-V, and high–voltage (HV) buses and can reduce the component count by 50% over conventional full-bridge–based technologies. Further refinements have eliminated the LC filter for the 14-V bus.

- Interleaved modular configurations using the half-bridge as a building block share the capacitor legs and provide a greater degree of component count reduction as the number of modules increases when the power level is scaled up.
- The capacitor leg current in the interleaved configurations can be significantly reduced, thus decreasing the capacitance.
- A novel control scheme has also been devised that can control the power flow among the three buses and reduce the flux density of the transformers.

- Prototype demonstration
  - A 4-kW prototype has been designed and built using two 2-kW modules.
  - The prototype has been successfully tested at load power levels of up to 4.6 kW.
  - Measured efficiencies are between 93.0 and 95.8 % over a wide power range of 0.5 to 4.6 kW.
  - Evaluation of the prototype indicates that it exceeds the 2015 FreedomCAR targets for specific power and power density, and the 2010 cost target.
- dc-dc converter requirements study for FCV applications
  - Several possible power system configurations and the requirements for dc-dc converters have been identified.

Technical Discussion

Background

As the automotive industry moves to drive-by-wire through the electrification of power steering, braking, and suspension, a 42-V net will probably be needed, as the existing 14-V system cannot efficiently power these loads. The HV bus (200~500V) for traction drives will add to the difficulty in meeting the safety requirements and in coping with EMI issues caused by running HV wires throughout the vehicle. While this move is especially needed for FCVs, which have no internal combustion engines to assist with electrification mechanisms, drive-by-wire technology has already been employed in luxury vehicles. For instance, the Toyota RX400h hybrid sport utility vehicle (SUV) uses dc-dc converters to transform the traction battery voltage to 14 V for onboard electronics and to 42 V for electric power steering. In an SUV, the steering load alone demands a 42-V supply. In summary, a triple voltage bus (14-V/42-V/HV) system is likely to be employed in future HEVs and fuel cell–powered vehicles (FCVs).

Figure 1 illustrates a simplified diagram for power management in future FCVs that employs a triple voltage bus (14-V/42-V/HV) system. With presently available technologies, two separate dc-dc converters are needed to fulfill power management demands among the three buses: one for converting high voltage to 42 V and the other for transforming 42 V to 14 V. The cost and volume of this two-converter solution make it difficult to meet the FreedomCAR power density and cost targets. In addition, the dc-dc converters must provide bidirectional power flow control to enable the use of the 14-V or 42-V battery for fuel cell startup and for storing the energy captured by regenerative braking. During vehicle starting, the HV bus is boosted up to around 300 V by the dc-dc converter drawing power from the 14-V

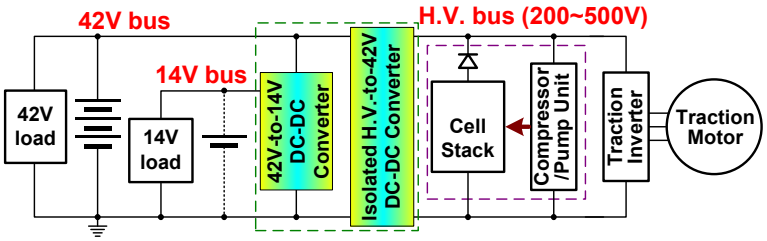


Figure 1. Power management in future fuel cell vehicles.

or 42-V battery. This HV bus then supplies power for the fuel cell compressor motor expanding unit controller and brings up the fuel cell voltage, which in turn feeds back to the HV bus to release the loading from the battery. During normal vehicle operation, power is transferred from the fuel cell stack to the low-voltage nets through the dc-dc converters to supply the vehicle accessory loads. The power management situation is similar in HEVs and plug-in HEVs, where the fuel cell power unit is replaced by an HV battery pack.

Although dc-dc converters are available to interconnect any two of the buses, to reduce component count, size, cost, and volume, it is desirable to employ an integrated dc-dc converter to interconnect the three voltage buses instead of using two separate ones. Aside from the bi-directional power control capability, the converter needs to provide galvanic isolation between the low-voltage and HV buses to meet safety requirements, which dictate the use of a transformer. Further, soft switching is preferred over hard switching because it reduces the level of EMI and switching losses.

In this project, a low-cost, soft-switched, isolated bi-directional dc-dc converter is being developed for interconnecting the three bus nets. The converter is based on a dual half-bridge topology to eliminate half of the switches required in a full-bridge counterpart. Further developments in the topology have led to the elimination of additional components. Figure 2 shows a diagram of the original converter, in which the 14-V bus is connected to the midpoint of the 42-V switch leg through an LC filter. This LC filter is eliminated in the modified topology shown in Figure 3, in which the 14-V bus is derived from the

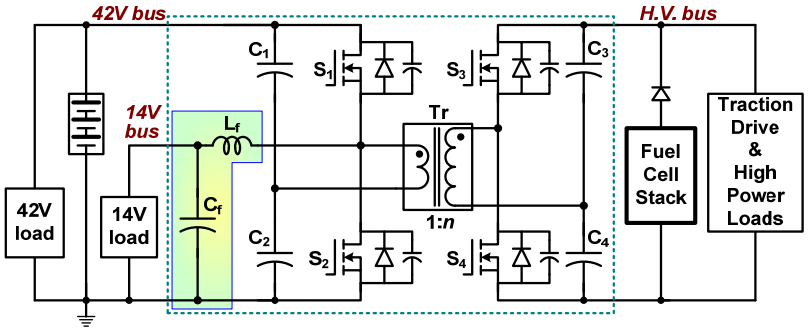


Figure 2. Original topology with LC filter.

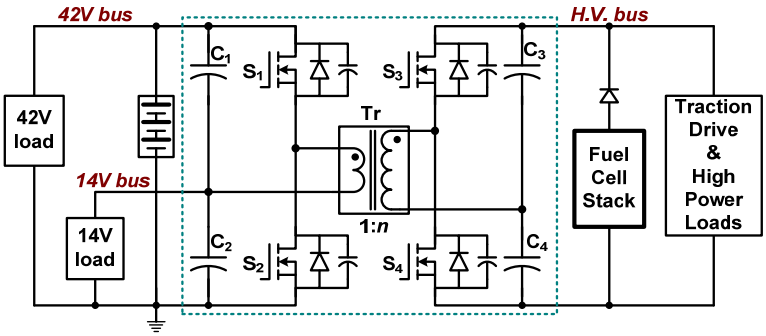


Figure 3. Modified topology that eliminates the LC filter.

capacitor leg. The converter uses the parasitic capacitance of the switches and the transformer leakage inductance to achieve zero-voltage-switching (ZVS). Therefore, no extra resonant components are required for ZVS, further reducing the component count. The inherent soft-switching capability and the low component count of the converter allow high power density, efficient power conversion, and compact packaging. A novel power flow control scheme based on a combined duty ratio and phase shift angle control has also been devised. The operation of the converter at a duty ratio other than the usual 50% reduces the peak flux density of the transformer, and thus a smaller core can be used.

To provide power scaling capability to meet the power requirements of vehicles of various sizes, without incurring the recurring engineering costs, a modular approach employing an interleaved multiphase configuration is the focus of the FY 2006 efforts. To this end, a 4-kW prototype using two 2-kW modules has been designed, built, and tested to evaluate its performance against the FreedomCAR targets.

In FCVs, in addition to the dc-dc converter for power management, higher-power dc-dc converters may be required to interface the fuel cell stack and/or high-power energy storage devices such as batteries and ultracapacitors. A study of dc-dc converter requirements for FCV applications was also performed in FY 2006.

Description of the dc-dc Converter for Triple Voltage Buses

Figure 4 shows a schematic of the 4-kW dc-dc converter, which consists of two half-bridge converter modules with shared capacitor legs. The high-frequency transformers, Tr_a and Tr_b, provide the required galvanic isolation and voltage level matching between the 42-V and the HV buses, while the 14-V and 42-V buses share a common ground. The leakage inductances of the transformers are used as the intermediate energy storage and transferring element between the two low-voltage buses and the HV net. The parasitic capacitors in parallel with the switches in each module resonate with the transformer leakage inductance to provide ZVS for the switches.

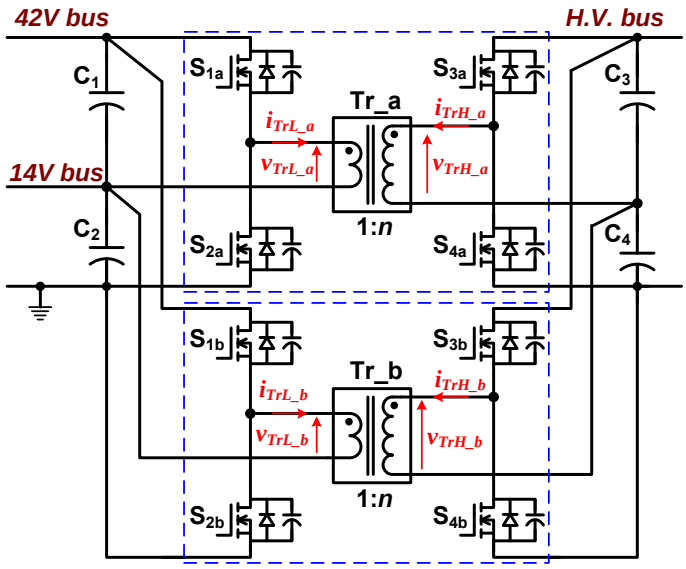


Figure 4. Schematic of the 4 kW dc-dc converter.

Figure 5 shows the transformer terminal voltages and currents waveforms to illustrate the operating principle of the converter. Duty ratio control is used for power flow control between the 14-V and 42-V buses, making the two bus voltages, V_{14V} and V_{42V}, track to each other by $V_{14V} = d \cdot V_{42V}$, where d is the duty ratio of the switches S_{1a} and S_{3a}, and S_{1b} and S_{3b}. It is defined by

$$d = \varphi/2\pi \quad , \tag{1}$$

where φ is the conduction angle of the switches S_{1a} and S_{3a}, and S_{1b} and S_{3b}. For 14-V/42-V systems, the duty ratio is fixed at $d = 1/3$, $\varphi = 2\pi/3$ at steady state for normal operation and can be changed to adjust the state of charge of the low-voltage batteries if necessary. In addition, a phase shift angle, ϕ, between the primary and secondary voltages of each transformer, v_{TrL_a} and v_{TrH_a} and v_{TrL_b} and v_{TrH_b}, is employed for power flow control between the 42-V and HV buses; $\phi > 0$ for low to high, $\phi < 0$ for high to low power transfer. Moreover, the transformer currents, i_{TrL_a} and i_{TrL_b} and i_{TrH_a} and i_{TrH_b}, are interleaved to reduce the capacitor leg currents, $i_{TrL\_a} + i_{TrL\_b}$ and $i_{TrH\_a} + i_{TrH\_b}$, and the capacitance by displacing the voltages of the two transformers by 180°, as shown in Figure 5.

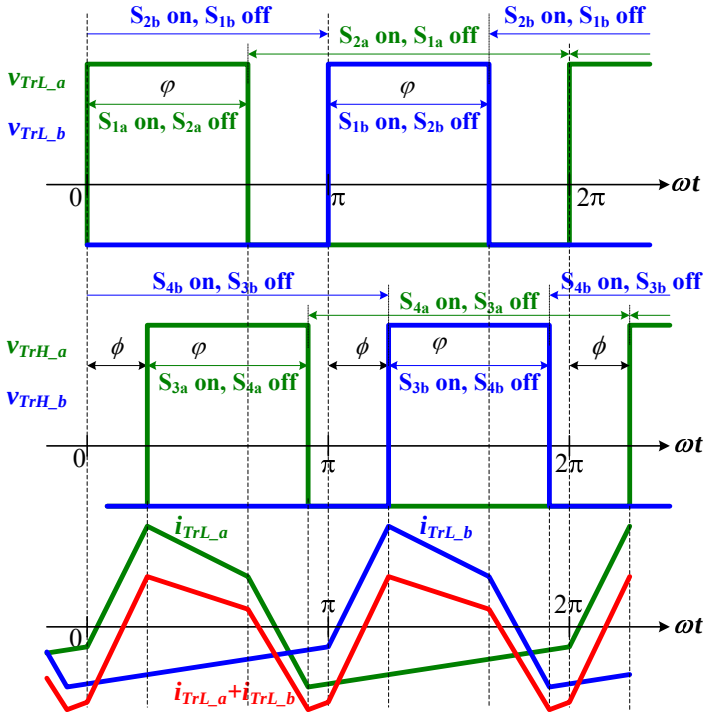


Figure 5. Transformer terminal voltages and currents waveforms illustating the operating principle.

The power transferred through the transformers at steady state with d = 1/3 can be expressed by

$$P = \frac{V_{42v} V_{HV}}{n} \cdot \frac{\phi}{2\pi f_{sw} L_s} \cdot [\frac{4}{9} - \frac{\phi}{2\pi}] \quad , \tag{2}$$

where n—transformer turns ratio, Ls—transformer leakage inductance, and fsw—switching frequency. For a given design, the maximum power is determined by

$$P_{\max} = \frac{V_{42v} V_{HV}}{n} \cdot \frac{4}{81 f_{sw} L_s} \text{ at } \phi_{P_{\max}} = \frac{4\pi}{9} \quad . \tag{3}$$

For a given bus voltage, V_{42V}, and switching frequency, f_{sw}, varying the duty ratio, d, will change the peak flux linkage, ψ_{peak}, of the transformer but will not introduce a dc bias. This is because the positive transformer terminal voltage, V_P, is $(1–d) \times V_{42V}$ at an interval of $t_P = d/f_{sw}$; and the negative transformer terminal voltage, V_N, is dV_{42V} but at an interval of $t_N = (1\text{-}d)/f_{sw}$, leading to the same product of volt × second of $d(1–d)V_{42V}/f_{sw}$ over the positive cycle and negative cycle. Further, operating at a duty ratio other than the usually employed 50% will decrease the peak flux linkage and thereby the transformer stress. The peak flux linkage is determined by $\psi_{peak} = \pm d(1\text{-}d)V_{42V}/(2f_{sw})$. At $d = 50$ %, $\psi_{peak} = \pm V_{42V}/(8f_{sw})$ while at $d = 1/3$ for our converter, the peak flux linkage is reduced to $\psi_{peak} = \pm V_{42V}/(9f_{sw})$ and thus a smaller transformer core can be used at the same switching frequency and number of turns.

Prototype Design and Experimental Results

Simulation study

A detailed circuit simulation was first performed for the 4-kW prototype design. Figure 6 shows simulation results where power is transferred from the 42-V bus to the 14-V and HV net at the level of 4.1 kW. Figure 7 shows simulated waveforms when the power flow is reversed. The simulation results confirm the design goal, that the power rating and the capacitor leg currents can be reduced to half of those in a single channel converter.

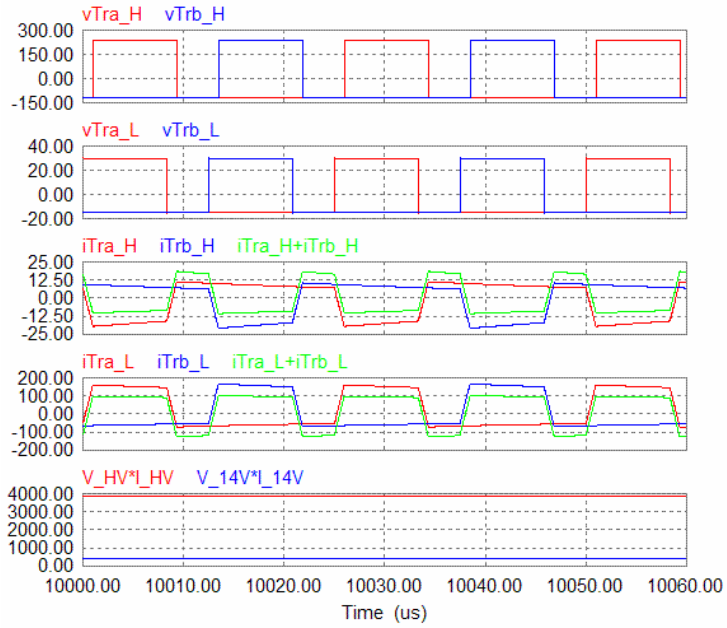


Figure 6. Simulation results showing power transfer from 42 V to 14 V and HV.

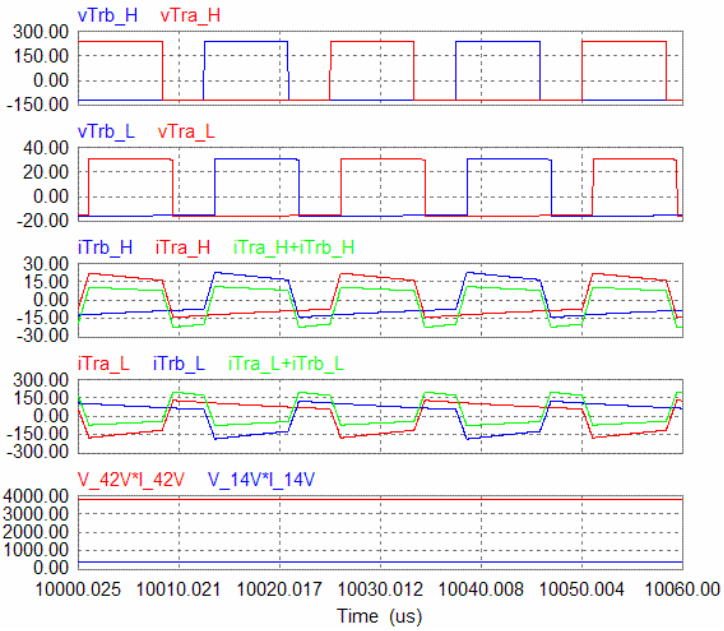


Figure 7. Simulation results showing power transfer from HV to 42 V and 14 V.

Converter design

A 4-kW prototype was then designed and built based on the analytical, simulation, and test results for a single-phase module. The design uses planar transformers, printed circuit power planes, and metal oxide semiconductor field effect transistors (MOSFETs) for both low and high voltages.

- Planar transformer design
  - Core, Ferroxcube E64/10/50
  - 4-layer PCB, 6 oz copper
  - Turns ratio, 1:8

- Power plane, 2-layer PCB
  - Low voltage: 6 oz copper
  - High voltage: 3 oz copper

- Benefits
  - Tight control of the leakage inductance—*important for soft-switching*
  - Easy assembly

- MOSFETS
  - Low-voltage side: SEMIKRON SK 300MB075, 75V/210A
  - High-voltage side: IXYS CoolMOS Power MOSFETVKM40-06P1, 600V/38A

Figure 8 shows a photo of the planar transformer.

Figure 8. Photo of the planar transformer.
Footprint: 4.875 × 2.125 in.

A new digital signal processor (DSP) control board based on a Texas Instruments chip, TMS320F2812, has been designed and fabricated for controlling the MOSFETs. The DSP chip has two sets of pulse width modulation hardware that can control up to three modules simultaneously. Figure 9 shows a photo of the DSP control board.

Figure 9. Photo of the DSP control board. Size: 7.0 × 3.5 in.

Figure 10 shows a 3-dimensional assembly layout of the prototype. As clearly indicated in the side view, there are quite large unoccupied spaces. The total converter volume is 203 in.^{3} with 93 in.^{3} accounted for by the individual components. This is partly because it was intentionally designed to provide space for easy probing access and partly because commercial-off-the-shelf components were used. It is estimated that 65% of the unoccupied space can be eliminated by optimizing the layout and by using customized packages for the major components.

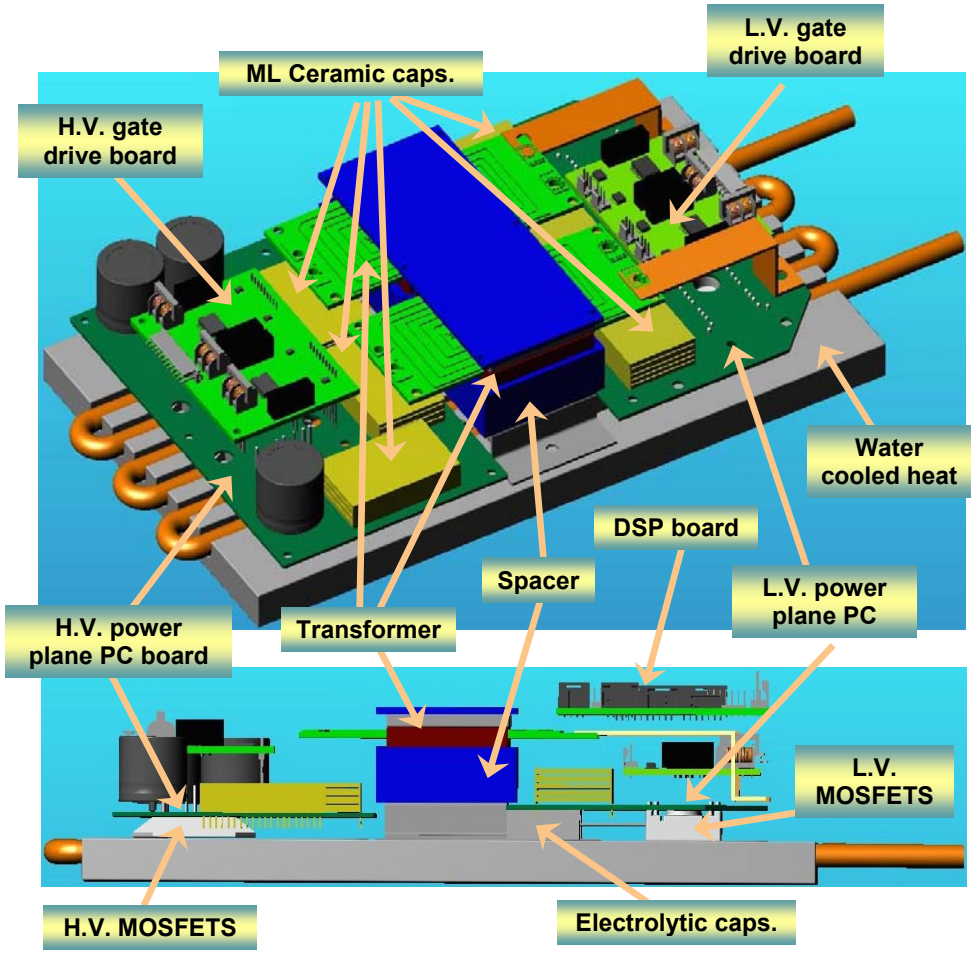


Figure 10. Three-dimensional assembly layout.

Figure 11 shows a photo of the 4-kW prototype. All components are mounted on a water-cooled heat sink 12 in. wide × 7.0 in. deep. The actual occupied footprint is 10.7 in. wide × 7.0 in. deep with a maximum height of 2.7 in. Evaluation of the prototype, assuming 65% of the unoccupied space can be removed, yielded performance numbers of 1.1 kW/kg, 2.1 kW/L, and $60/kW, which exceeds the 2015 FreedomCAR targets for specific power and power density and the 2010 cost target.

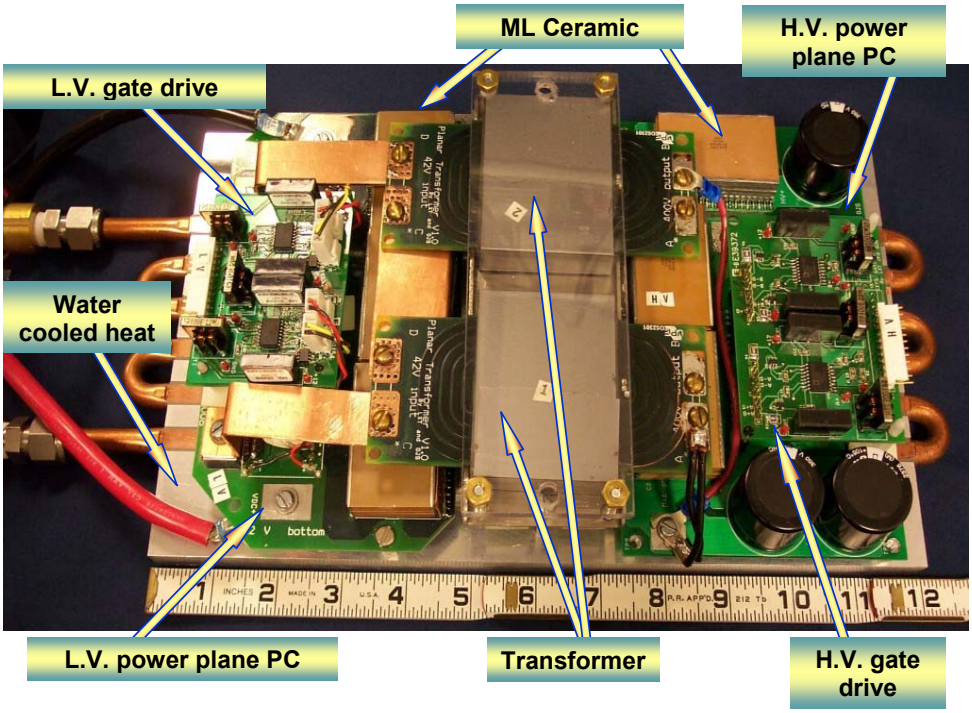
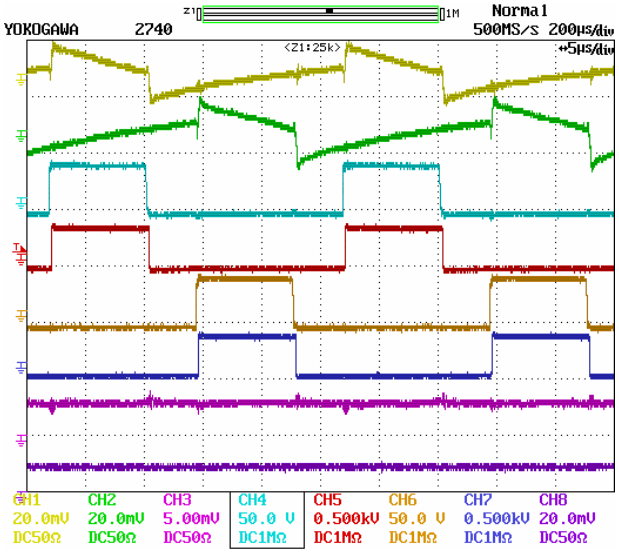


Figure. 11. The 4-kW prototype. Footprint: 10.7 in. wide × 11.0 in. deep × 2.7 in. maximum height.

Experimental results

The prototype was fully tested at power levels of up to 4.6 kW. Figures 12 and 13 show typical testing waveforms at different load power levels when power was transferred from the 42-V bus to the 14-V and HV buses, and from the HV bus to the 14-V and 42-V buses, respectively. The smooth rising and falling edges of the transformer voltages indicate soft-switching operation.

Figure 14 plots power conversion efficiency against the load power for both low-to-high and high-to-low conversion. Measured efficiencies are between 93.0 and 95.8 % over a wide power range of 0.5 to 4.6 kW for low-to-high conversion, against 93.0 to 95.7 % over a power range of 0.7 to 4.2 kW for high-to-low conversion.



i_{TrH_a}: 20A/div

i_{TrH_b}: 20A/div

v_{TrL_a}: 50V/div

v_{TrH_a}: 500V/div

v_{TrL_b}: 50V/div

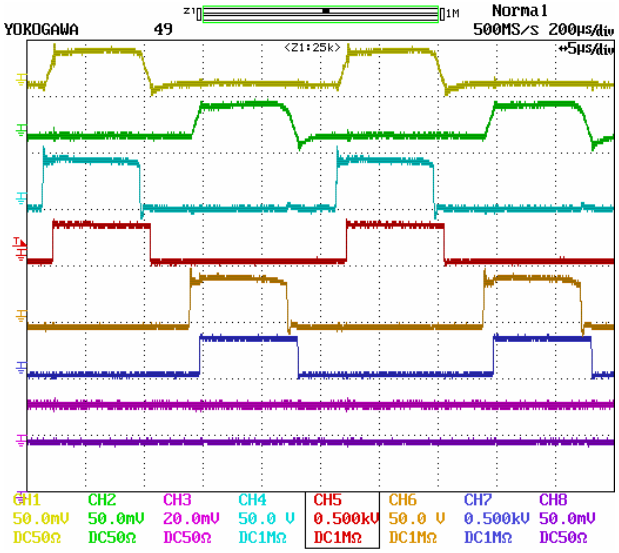
v_{TrH_b}: 500V/div

I_{HV_Load}: 5A/div

I_{14V_Load}: 20A/div

Time: 5µs/div

(a) Load power: 1.18 kW



i_{TrH_a}: 50A/div

i_{TrH_b}: 50A/div

v_{TrL_a}: 50V/div

v_{TrH_a}: 500V/div

v_{TrL_b}: 50V/div

v_{TrH_b}: 500V/div

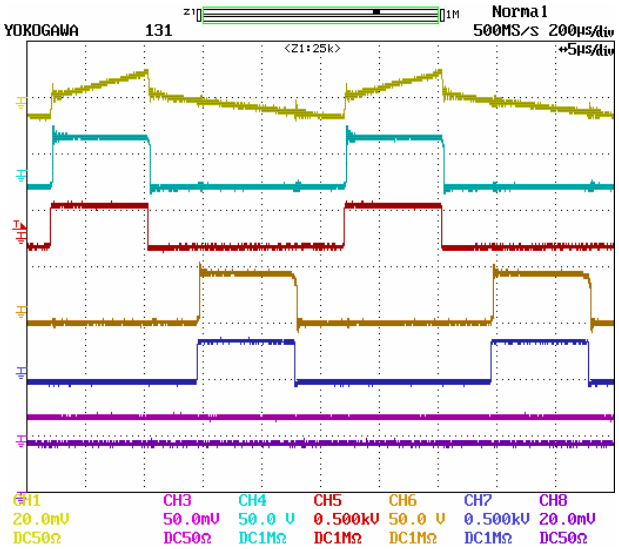
I_{HV_Load}: 20A/div

I_{14V_Load}: 50A/div

Time: 5µs/div

(b) Load power: 4.2 kW

Figure 12. Typical testing waveforms for power transfer from 42 V to 14 V and HV.



i_{TrH_a}: 20A/div

v_{TrL_a}: 50V/div

v_{TrH_a}: 500V/div

v_{TrL_b}: 50V/div

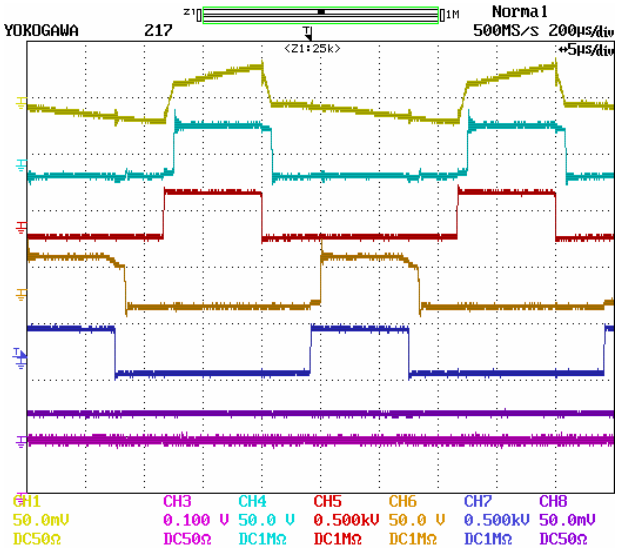
v_{TrH_b}: 500V/div

I_{42V_Load}: 50A/div

I_{14V_Load}: 20A/div

Time: 5µs/div

(a) Load power: 0.991 kW



i_{TrH_a}: 50A/div

v_{TrL_a}: 50V/div

v_{TrH_a}: 500V/div

v_{TrL_b}: 50V/div

v_{TrH_b}: 500V/div

I_{14V_Load}: 50A/div

I_{42V_Load}: 100A/div

Time: 5µs/div

(b) Load power: 4.23 kW

Figure 13. Typical testing waveforms for power transfer from HV to 42 V and 14 V.

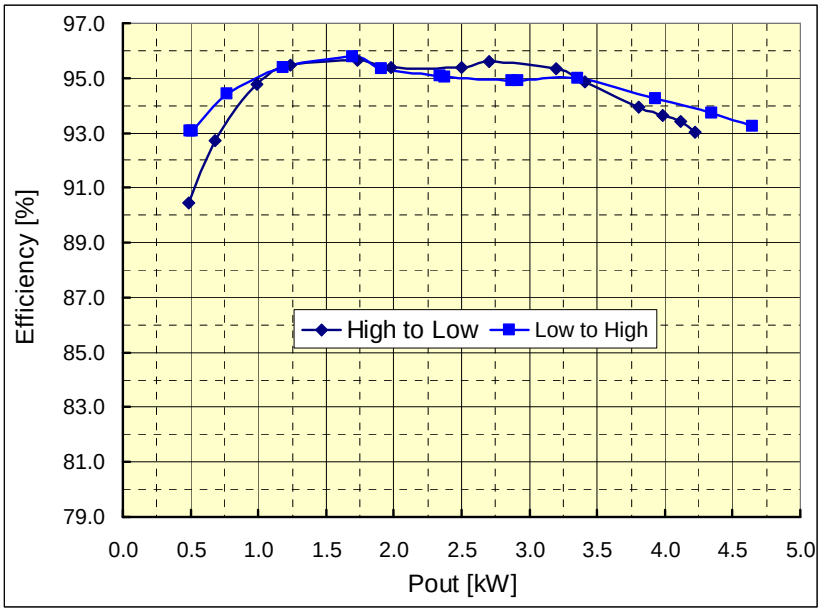
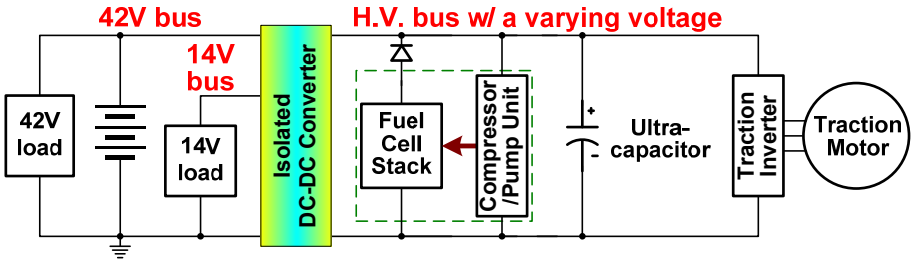


Figure 14. Efficiency chart.

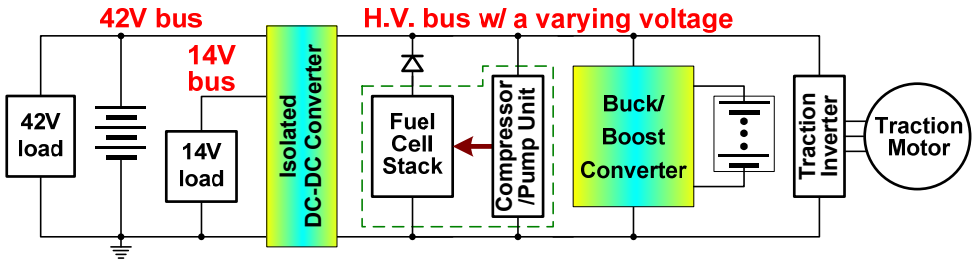
dc-dc Converter Requirements Study for Fuel Cell Vehicle Applications

A literature search was conducted to determine what power system architectures are being considered by original equipment manufacturers. While a few publications did turn up data on the Hyundai Tucson fuel cell electric vehicle, Honda FCX, and Toyota fuel cell hybrid vehicle, published information is presently quite scarce. Based on the limited findings, several possible power system configurations are identified in Figure 15, along with the requirements for the dc-dc converter needed in each architecture.

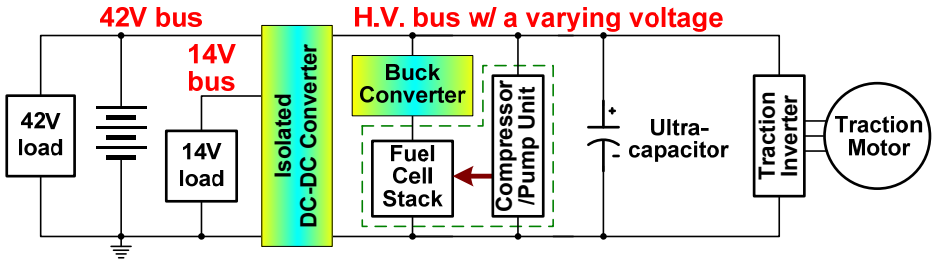


(a) This topology uses the capability of ultracapacitors to operate over a widely fluctuating bus voltage produced by the fuel stack as load power changes. The ultracapacitors compensate for the slow response of the fuel cell stack and store regenerative power during braking. The isolated dc-dc converter must be bi-directional to power the compressor/pump unit for startup of the fuel cell stack and needs to provide a peak power of several kilowatts, typically around 5 kW.

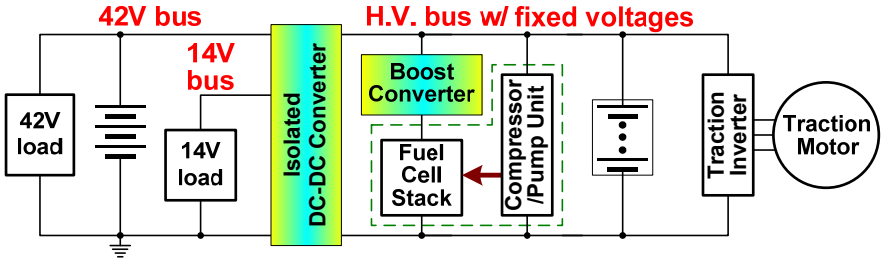
Figure 15. Possible electrical power system architectures for fuel cell vehicles.



(b) In this topology, a buck/boost converter is required to employ batteries at the high-voltage bus because batteries cannot operate at the widely fluctuating bus voltage produced by the fuel stack as load power changes. The peak power rating of the buck/boost is in the range of several tens of kilowatts, typically around 30 kW.



(c) A buck converter is employed in this scenario to control the power of the fuel stack. The benefits of doing so are twofold: it enables the ultracapacitors to capture more regenerative power during braking while keeping the bus voltage below a safe level, and it keeps the bus voltage below a safe level at light load conditions under which the fuel cell stack output voltage rises significantly. The buck converter needs to handle the peak power of the fuel cell stack, typically in the range of 80–100 kW. The isolated dc-dc converter must be bi-directional to power the compressor/pump unit for startup of the fuel cell stack and needs to provide a peak power of several kilowatts, typically around 5 kW.



(d) A boost converter is employed in this topology to regulate the output voltage of the fuel cell stack to provide a stable bus voltage so the batteries can be directly connected to the dc bus. The peak power rating of the boost converter is the same as that of the fuel cell stack, typically 80–100 kW. If desired, a buck/boost converter can be used to interface a lower-voltage battery as in configuration (b), possibly reducing the battery cost and facilitating the use of a higher bus voltage optimized for a more efficient traction drive system.

Figure 15. (continued).

Conclusion

The integrated dc-dc converter for triple-voltage-bus systems (14-V/42-V/HV) for HEVs and FCVs applications has the following features:

- Employs interleaved half-bridge modules with each one using only four switching devices and all modules sharing the capacitor legs, leading to significant cost savings and higher power density.
- Requires no LC filter for the 14-V bus.
- Employs soft switching and synchronous rectification for high efficiency and low EMI.
- Requires no auxiliary circuit or complex control dedicated for soft switching.
- Provides flexible power flow management owing to the capability to transfer power among all three voltage buses by employing the combined duty ratio and phase shift angle control scheme, which also reduces the flux density of the transformers.

A 4-kW prototype has been designed and built using two 2-kW modules and has been successfully tested at load power levels all the way up to 4.6 kW. Measured efficiencies are between 93.0 and 95.8% over a wide power range of 0.5 to 4.6 kW. Evaluation of the prototype indicates that it exceeds the 2015 FreedomCAR targets for specific power and power density and the 2010 cost target.

The information on the possible power system configurations and the requirements of dc-dc converters identified in this report is useful to guide future dc-dc converter development for FCV applications.

Future Direction

- Develop control algorithms to reduce the capacity of the 42-V battery or eliminate it and test with the 4-kW prototype
- Further improve the efficiency through optimization of the topology and packaging

Publications and Presentations

G. J. Su, L. Tang, and X. Huang, "Control of Two Permanent Magnet Machines Using a Five-Leg Inverter for Automotive Applications," presented at IEEE IAS 2006, October 8–12, 2006.

L. Tang, G. J. Su, and X. Huang, "Experimental High Performance Control of Two Permanent Magnet Synchronous Machines in an Integrated Drive for Automotive Applications," presented at IEEE COMPEL 2006 Workshop, July 16–19, 2006.

G. J. Su and J. S. Hsu, "A Five-Leg Inverter for Driving a Traction Motor and a Compressor Motor," *IEEE Trans. on Power Electronics* **21**(3), 687–692 (May 2006).

G. J. Su, "Pulse-Width-Modulation Schemes for an Integrated Traction and Compressor Drive System," pp. 640–645 in *IEEE APEC 2006*, vol. 2, March 19–23, 2006.

Patents

G. J. Su, "Multi-Level DC Bus Inverter for Providing Sinusoidal and PWM Electrical Machine," U.S. No. 6,969,967, November 29, 2005.

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4.3 Cascaded Multilevel Inverter

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Objectives

- To produce a cascade multilevel inverter that combines inverter and converter functions.
- To eliminate the magnetics required for the dc-dc boost converter, therefore reducing the weight, volume, and cost of the system while increasing its efficiency.

Approach

- Assess the performance and cost trade-offs to come up with a viable design.
- Simulate the inverter/converter in PSpice for circuit operation.
- Design simulation of the electric traction drive system (inverter/converter/motor) in Simulink.
- Design a 1.2-kW unit.

Major Accomplishments

- Developed a control algorithm to keep the capacitors charged.
- Simulated the inverter/converter in PSpice and Simulink.
- Developed a design simulation of an electrical drive system with the inverter/converter.
- Designed a 1.2-kW prototype.

Technical Discussion

A cascade multilevel inverter is a power electronic device built to synthesize a desired ac voltage from several levels of dc voltages. Such inverters have been the subject of research in the last several years,[1–4] where the dc levels were considered to be identical because all of them were batteries, solar cells, etc. In Reference 5, a multilevel converter was presented in which the two separate dc sources were the secondaries of two transformers coupled to the utility ac power. Corzine et al.[6] have proposed using a single dc power source and capacitors for the other dc sources. A method was given to transfer power from the dc power source to the capacitor in order to regulate the capacitor voltage. A similar approach was later (but independently) proposed by Du et al.[7] These approaches required a dc power source for each phase. Similar methods have also been proposed by Veenstar and Rufer.[8,9] The approach here is very similar to that of Corzine et al.[6] and Du et al.[7] with the important exception that only a single standard three-leg inverter is required as the power source (one leg for each phase) for the three-phase multilevel inverter.

Specifically, the interest here is in using a single dc power source connected to a standard three-leg inverter, which in turn is connected to capacitors to form a three-phase five-level cascade multilevel inverter to be used as a drive for a permanent magnet (PM) traction motor. The five-level inverter consists of a standard three-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg

and using a capacitor as a dc source. It is shown that one can simultaneously maintain the regulation of the capacitor voltage while achieving an output voltage waveform that is 25% higher than that obtained using a standard three-leg inverter by itself.

Multilevel Inverter Architecture

Figure 1 shows a dc source connected to a single leg of a standard three-leg inverter.

The output voltage v_1 of this leg (with respect to the ground) is either $+V_{dc}/2$ (S_5 closed) or $-V_{dc}/2$ (S_6 closed). This leg is connected in series with a full H-bridge, which in turn is supplied by a capacitor voltage. If the capacitor is kept charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S_1 and S_4 closed), 0 (S_1 and S_2 closed or S_3 and S_4 closed), or $-V_{dc}/2$ (S_2 and S_3 closed). An example output waveform that this topology can achieve is shown in Figure 2.

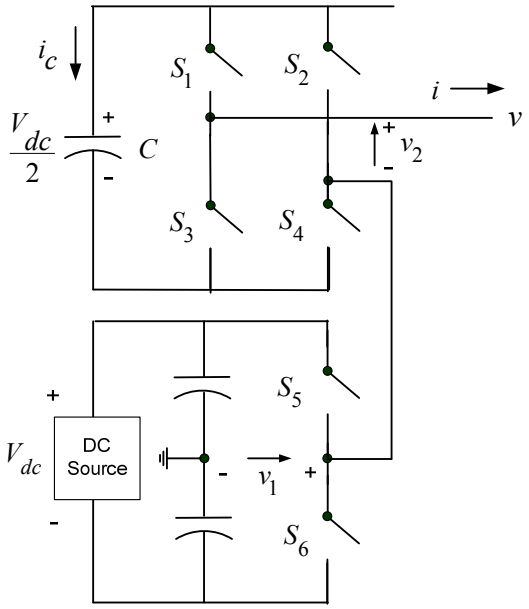

Figure 1. One leg of a three-leg inverter connected to a full H-bridge with a capacitor dc source.

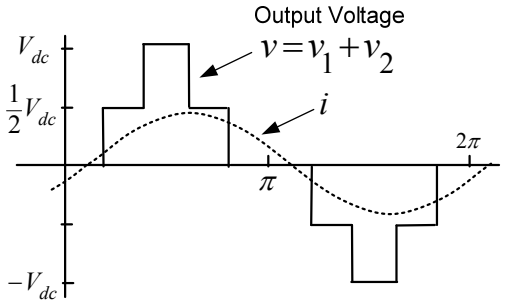

Figure 2. Five-level output waveform of the multilevel inverter.

When the output voltage $v = v_1 + v_2$ is required to be zero, one can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ or $v_1 = -V_{dc}/2$ and $v_2 = +V_{dc}/2$. It is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage. In more detail, consider Figure 3.

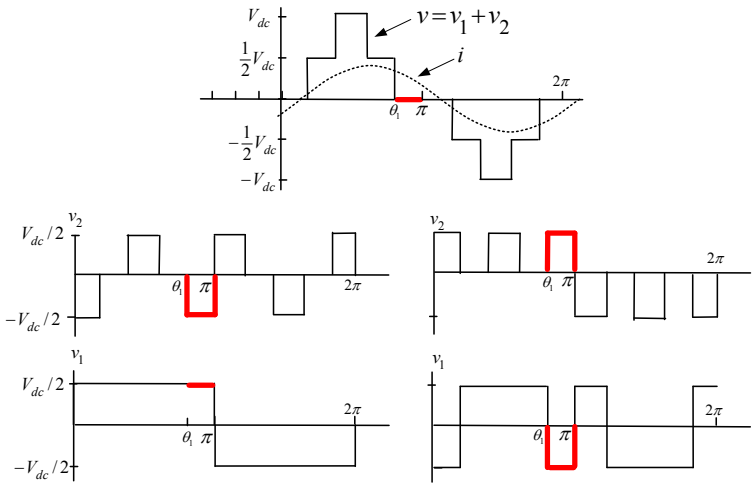

Figure 3. To make the output voltage zero for $\theta_1 \le \theta \le \pi$, one can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ (bottom left) or $v_1 = +V_{dc}/2$ and $v_2 = +V_{dc}/2$ (bottom right).

In the interval $\theta_1 \le \theta \le \pi$, the output voltage in Figure 3 is zero, and the current $i > 0$. If S_1 and S_4 are closed (so that $v_2 = +V_{dc}/2$) along with S_6 closed (so that $v_1 = +V_{dc}$), then the capacitor is discharging ($i_c = -i < 0$; see Figure 1) and $v = v_1 + v_2 = 0$. On the other hand, if S_2 and S_3 are closed (so that $v_2 = -V_{dc}/2$) and S_5 is also closed (so that $v_1 = -V_{dc}/2$), then the capacitor is charging ($i_c = i > 0$; see Figure 1) and $v = v_1 + v_2 = 0$.

The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charge and discharge of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S_1, S_4, and S_6 are closed or the switches S_2, S_3, and S_5 are closed depending on whether it is necessary to charge or discharge the capacitor.

Remark

As Figure 3 illustrates, this method of regulating the capacitor voltage depends on the voltage and current not being in phase. That is, one needs positive (or negative) current when the voltage is passing through zero to charge or discharge the capacitor. Consequently, the ability to regulate the capacitor voltage depends on the power factor.

Simulation Results Using Multilevel PWM

A simulation of the multilevel converter driving a PM synchronous machine was carried out. The basic block diagram for the simulation is shown in Figure 4.

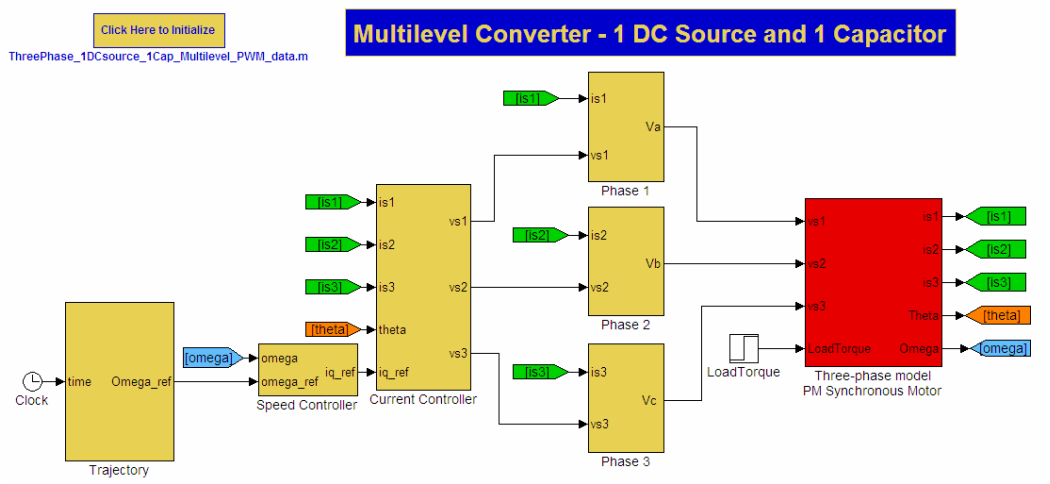

Figure 4. Top level Simulink block diagram.

The motor is controlled using a standard field-oriented controller.[10] The blocks marked phase 1, phase 2, and phase 3 contain the modeling of the multilevel converter. The switching scheme is based on the standard multilevel pulse width modulation (PWM) scheme.[11] The scheme is modified so that during those time periods when the multilevel inverter has an output of zero volts, either the switches S_1, S_4, and S_6 are closed or the switches S_2, S_3, and S_5 are closed, depending on whether the current is positive or negative and whether it is necessary to charge or discharge the capacitor.

The dc link voltage V_{dc} was set to 200 V so that the three-leg inverter supplies ±100 V. The capacitors were regulated to 100 V. The motor's inertia is $J = 0.1$ kg-m^2, the motor has $n_p = 4$ pole-pairs, the stator resistance is $R_S = 0.065\ \Omega$, the stator inductance is $L_S = 3$ mH, the torque/back-emf constant $K_T = K_b = 0.37$ Nm/A (V/rad/s) and the load torque $\tau_L = 19$ Nm. The capacitor value is $C = 0.01$ F.

For comparison purposes, simulations were performed using both the multilevel inverter of Figure 1 capable of supplying up to ±200 V and a standard three-leg inverter (i.e., only the bottom half of Figure 1) capable supplying ±100 V. Though the multilevel inverter can supply up to ±200 V, it cannot do this and maintain regulation of the capacitor voltages. As pointed out earlier, the ability to regulate the capacitor voltage depends on the power factor of the load. The PM motor was run to achieve the highest possible speed under the given load and available voltage. This is shown in Figure 5. The standard three-leg inverter could only achieve a maximum speed of 212 rad/s, while the proposed multilevel inverter could get the motor up to 275 rad/s using the same dc source voltage.

The corresponding voltages for the speed trajectories of Figure 5 are shown in Figure 6. The standard three-leg inverter is supplying a nearly six-step wave form of $V_{dc}/2 = 100$ V maximum corresponding to a fundamental voltage of $(4/\pi)V_{dc}/2 = 127$ V peak, while the multilevel inverter output is 170 V peak in steady state and up to 180 V before steady state.

The corresponding torques for the above trajectories are shown in Figure 7. The chattering shown in the torque response of the standard three-leg inverter results from the voltage undergoing saturation (see the left side of Figure 6).

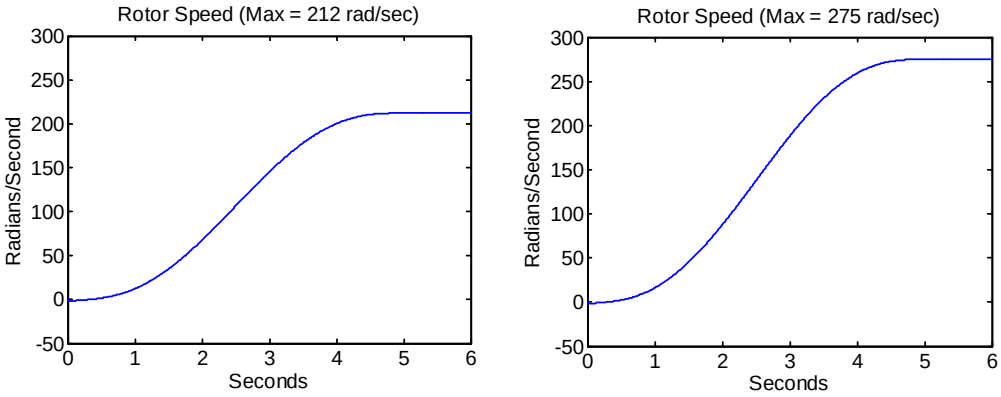

Figure 5. Rotor speeds achievable using a standard three-leg inverter (left) and the proposed multilevel inverter (right).

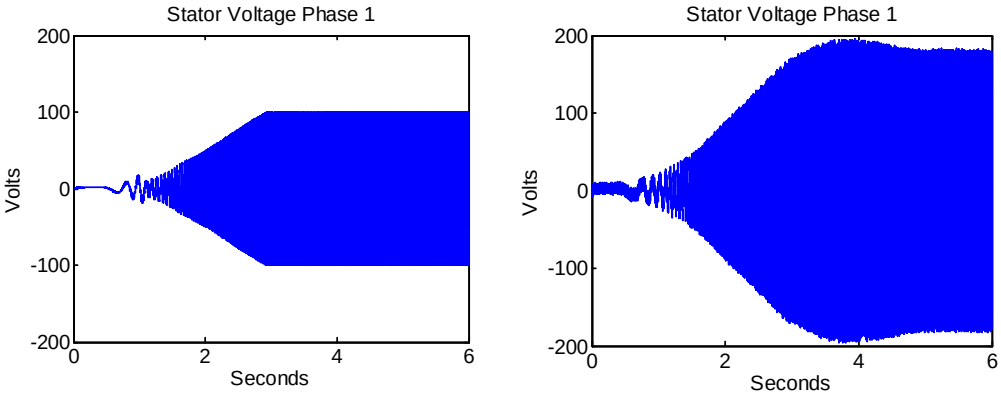

Figure 6. Left: Voltage using a standard three-leg inverter. Right: Voltage obtained using the proposed multilevel inverter.

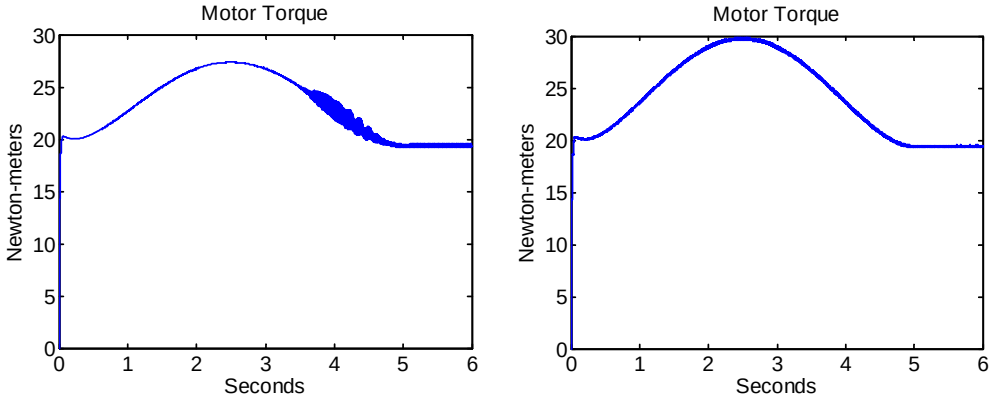

Figure 7. Left: Motor torque using standard three-leg inverter. Right: Motor torque using proposed multilevel inverter.

The stator currents are shown in Figure 8. The current used in the multilevel inverter is higher because it requires more torque to accelerate the motor to its higher speed (see Figure 5).

The capacitor voltage as a function of time is plotted in Figure 9, showing that it is kept within about 2 V of the desired value.

An enlarged view of the capacitor voltage is shown in Figure 10, showing the regulation of the voltage in more detail. The variation in the voltage will be less if a larger value of capacitance is used ($C = 0.01$ F in the simulation).

Note that the capacitor voltage decreases during those times when the inverter is supplying ±100 V, is constant during those times the inverter is supplying ±50 V, and is increasing (recharging) during those times the inverter is supplying 0 V. For example, a little after $t = 5.577$ s, the current becomes positive, and the inverter is required to put out (up to) 200 V (only 100 in the figure due to the scaling) by the PWM scheme. The capacitor voltage (red) then decreases. Then shortly before $t = 5.579$ s, the inverter is only required to supply up to 100 V (only 50 in the figure due to the scaling), and the capacitor voltage is constant. At about $t = 5.579$ s, the multilevel PWM scheme is having the inverter supply 0 V for significant time intervals, so the capacitor voltage increases.

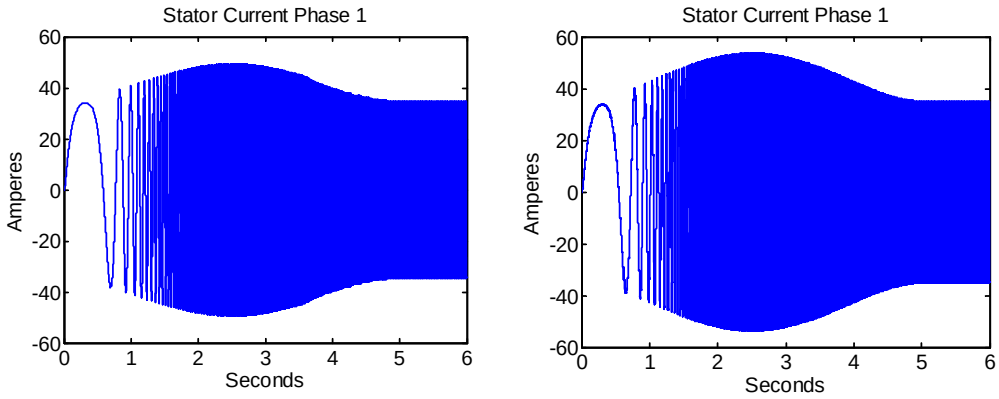

Figure 8. Left: Stator current for the standard three-leg inverter. Right: Stator current for the proposed multilevel inverter.

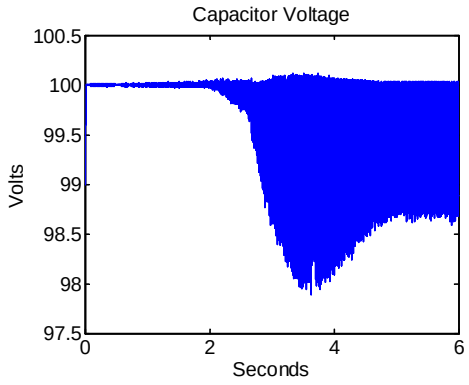

Figure 9. Capacitor voltage vs time.

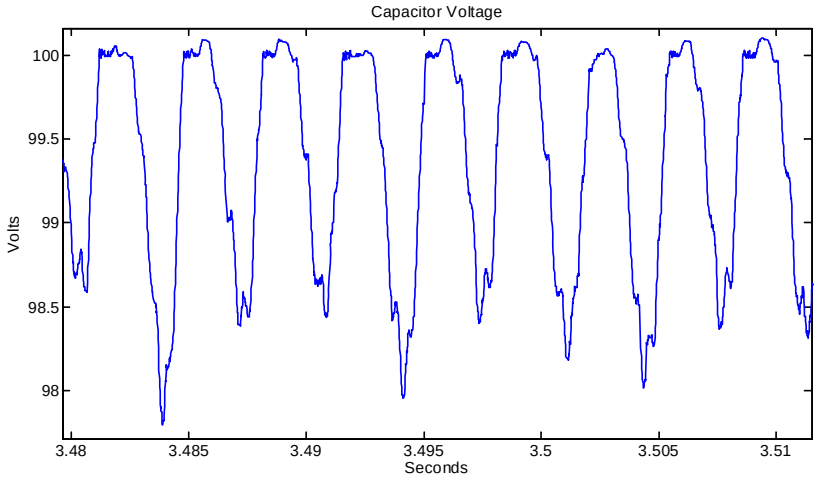

Figure 10. Expanded view of the capacitor voltage as a function of time.

Simulation Results—Fundamental Frequency Switching

In this section a fundamental frequency switching scheme is used. By fundamental frequency switching, it is meant that each device switches once per cycle in contrast to a PWM scheme for which each device turns on and off several times a cycle. Typically a fundamental switching scheme results in a higher harmonic content in the lower frequency spectrum (closer to the fundamental) than a PWM method, but has lower switching losses. In the five-level multilevel inverter under consideration here, a fundamental switching scheme is implemented by choosing two angles θ_1 and θ_2 for when the devices are to be switched on as indicated in Figure 11. By symmetry of the waveform, the rest of the switching occurs at $\pi-\theta_1, \pi-\theta_2, \pi+\theta_1, \pi+\theta_2, 2\pi-\theta_1$, and $2\pi-\theta_2$.

With the nominal capacitor voltage chosen as $V_{dc}/2$, one computes the switching angles θ_1 and θ_2 as in References 12 and 13. Briefly, the Fourier series expansion of the (staircase) output voltage waveform of the multilevel inverter as shown in Figure 11 is

$$V(\omega t)=\frac{4}{\pi}\frac{V_{dc}}{2}\times\sum_{n=1,3,5,\ldots}^{\infty}\frac{1}{n}\left(\cos(n\theta_1)+\cos(n\theta_2)\right)\sin(n\omega t) \quad . \tag{1}$$

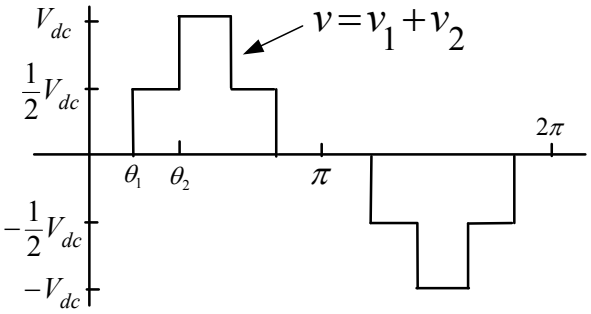

Figure 11. Fundamental frequency waveform.

Ideally, given a desired fundamental voltage V_1, one wants to determine the switching angles θ_1 and θ_2 so that (FS) becomes $V(\omega t) = V_1 \sin(\omega t)$. In practice, one is left with trying to do this approximately. For three-phase systems, the triplet harmonics in each phase need not be canceled as they automatically cancel in the line-to-line voltages. In this case, where there are two dc sources, the desire is to cancel the fifth order harmonic as it tends to dominate the total harmonic distortion. The mathematical statement of these conditions is then

$$\cos(\theta_1) + \cos(\theta_2) = m = \frac{V_1}{\frac{4}{\pi}\frac{V_{dc}}{2}} \quad . \qquad (2)$$

$$\cos(5\theta_1) + \cos(5\theta_2) = 0 \quad .$$

This is a system of two transcendental equations in the two unknowns θ_1 and θ_2. There are many ways one can solve for the angles (see, for example, References 14–16). Here the approach in Reference 12 and Reference 17 is used. It is found that a solution to (conditions1) exists for $0.6 \le m \le 1.909$, and these solution angles are plotted in Figure 12. Note that the fundamental is given by

$$V_1 = m\frac{4}{\pi}\frac{V_{dc}}{2} \quad . \qquad (3)$$

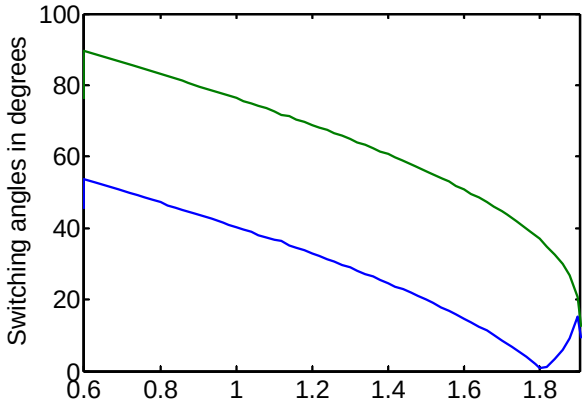

Figure 12. θ_1 and θ_2 vs m.

In the simulations presented here, the same PM motor as chosen for the multilevel PWM scheme was used, but the motor was driven open-loop rather than closed-loop. The voltage magnitude was ramped from 90 V to 180 V during the time interval from 0 to 3 s. The stator electrical frequency f_S was brought up smoothly from 0 to 175 Hz in 5 s resulting in a peak speed of $2\pi f_S / n_p = 275$ rad/s. This is the same speed trajectory as used in the closed-loop multilevel PWM implementation above. The resulting speed response is shown in Figure 13, which is somewhat oscillatory due to the open-loop control. Because it is driven open loop, it is much more difficult to have the machine go up in speed with a significant load torque at the start. As a result, only a viscous friction load torque was used with the viscous friction coefficient chosen as $f = 0.07$ so that at maximum speed the load torque is $f\omega_{\max} = f(2\pi f_S / n_p) = 0.07 * 275 = 19$ Nm, giving the same steady-state load-torque as in the multilevel PWM case.

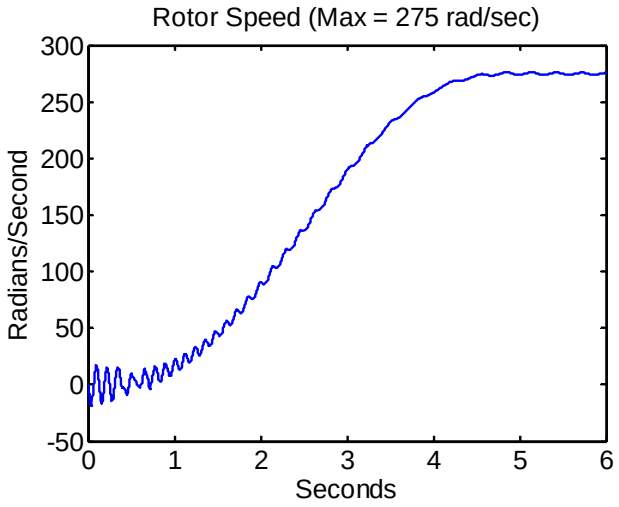

Figure 13. Rotor speed in rad/s vs time in seconds.

The commanded voltage magnitude [see (fund)] and the computed fundamental of the inverter output are given in Figure 14.

The computed fifth harmonic of the voltage is plotted vs time in Figure 15. During the end of the run when the speed is close to being constant, the fifth-harmonic is about 0.7 V compared with the 180 V of the fundamental.

The motor torque is shown in Figure 16, which is oscillatory as a result of the open-loop control. Note that at the end of the run, the torque is oscillating about 19 Nm to counteract the (viscous-friction) load torque.

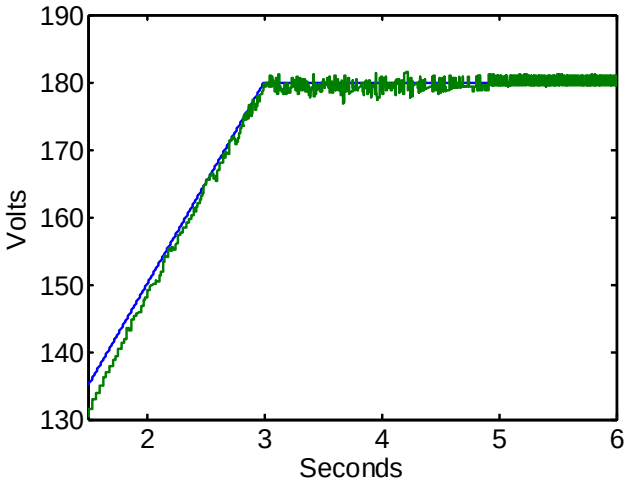

Figure 14. Commanded and computed fundamental voltage in volts vs time in seconds.

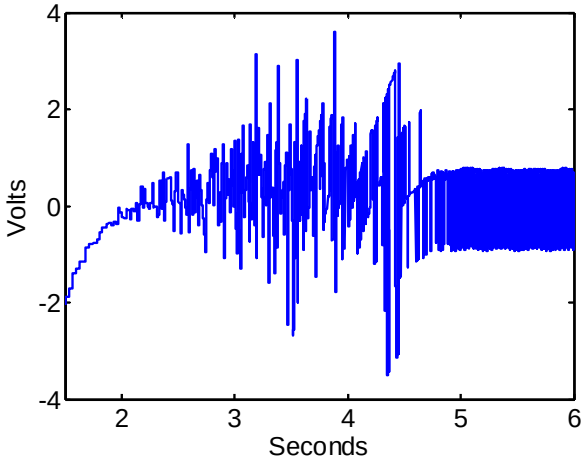

Figure 15. Computed fifth-harmonic of the voltage in volts vs time in seconds.

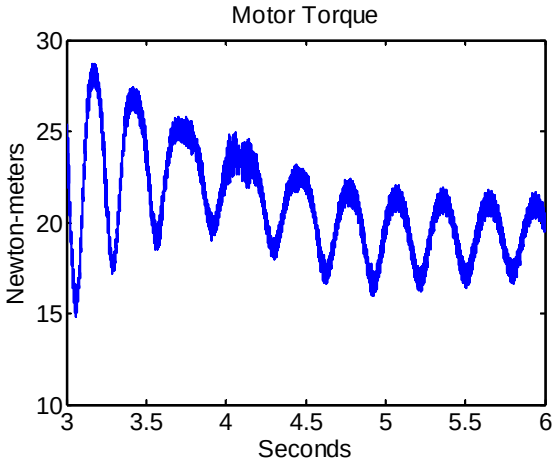

Figure 16. Torque in N-m vs time in seconds.

An enlarged section of the inverter output voltage of phase 1 is given in Figure 17 and shows the fundamental switching scheme for a stator frequency of $f_S = 175$ Hz.

The stator current response of phase 1 is plotted in Figure 18 and uses somewhat more current than the closed-loop PWM scheme (see Figure 8).

The capacitor voltage is shown in Figure 19, showing that the scheme regulates the voltage within 3 V of the nominal value. The value of the capacitance is $C = 0.01$ F as in the multilevel PWM case. An enlarged view of the capacitor voltage for $5.5 \le t \le 5.525$ is shown in Figure 20.

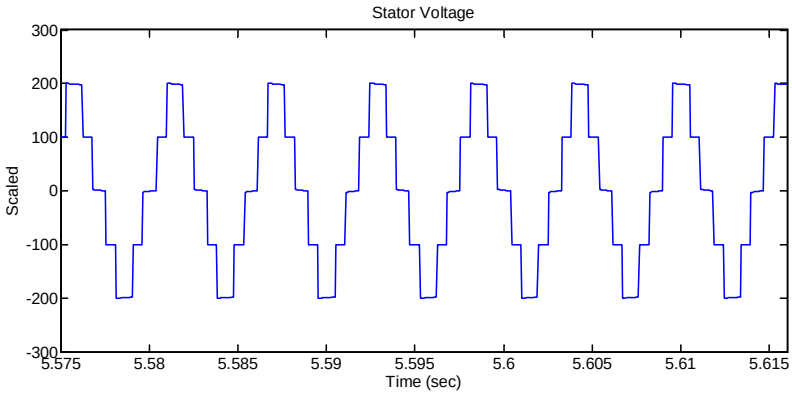

Figure 17. Enlarged view of the phase 1 voltage in volts vs time in seconds.

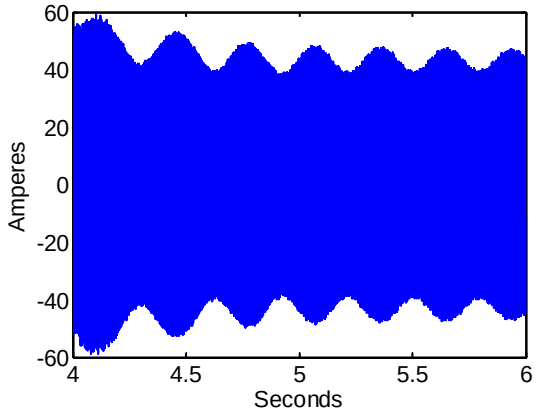

Figure 18. Phase 1 stator current vs time.

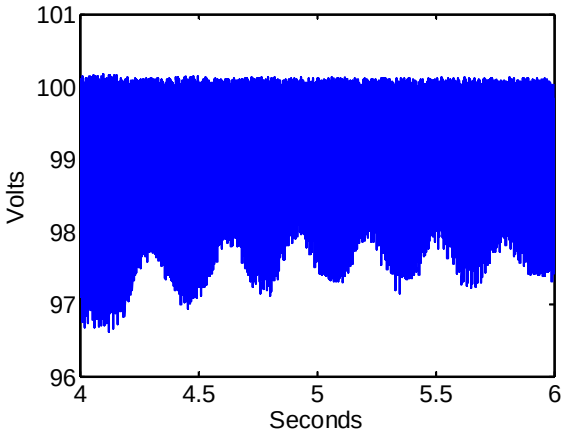

Figure 19. Capacitor voltage in volts vs time in seconds.

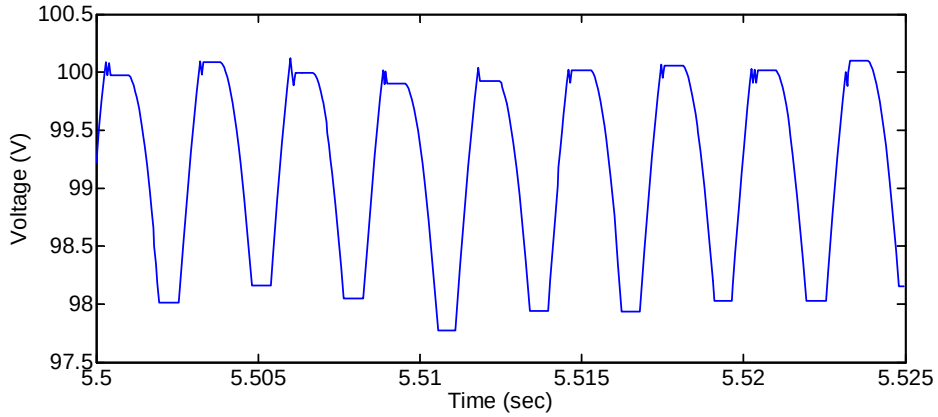

Figure 20. An enlarged view the capacitor voltage in volts vs time in seconds.

Scaled versions of the capacitor voltage, stator current, and stator voltage vs time are shown in Figure 21. Note that the capacitor discharges when the inverter is supplying ±200 V, stays constant when the inverter is supplying ±100 V, and recharges when the inverter is supplying 0 V.

For example, a little after $t = 5.575$ s, the stator current becomes positive, and the inverter is required to supply 200 V. The capacitor voltage then decreases. Following this, when the inverter is only required to supply 100 V, the capacitor voltage is constant. Next, the inverter is putting out 0 V so that the capacitor is charging and its voltage increases.

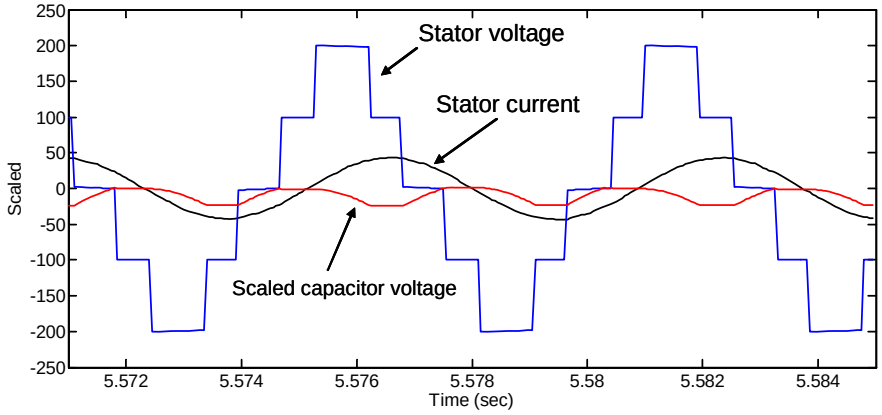

Figure 21. Scaled capacitor voltage, stator current, and stator voltage vs time in seconds.

Conditions for Capacitor Voltage Regulation

Let

$$v_f(\theta) = V\sin(\theta)\ ,$$
$$i(\theta) = I\sin(\theta - \varphi)\ , \tag{4}$$

where $v_f(\theta)$ is the fundamental component of the voltage, $i(\theta)$ is the current, and φ is the power factor angle. The objective here is to compute the conditions on θ_1, θ_2, and φ to ensure the capacitor can be regulated to a desired value.

Interval 1: $0 < \varphi < \theta_1$

Consider the case where $0 < \varphi < \theta_1$ as illustrated in Figure 22. During the interval $\theta_2 < \theta < \pi - \theta_2$, the capacitor loses the amount of charge $\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta$, while during the intervals $0 < \theta < \theta_1$ and $\pi - \theta_1 < \theta < \pi$ the capacitor can be recharged (by choosing the switch positions appropriately) by the amounts $\int_0^{\varphi} I\left|\sin(\theta-\varphi)\right|d\theta + \int_{\varphi}^{\theta_1} I\sin(\theta-\varphi)d\theta$ and $\int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta$, respectively.

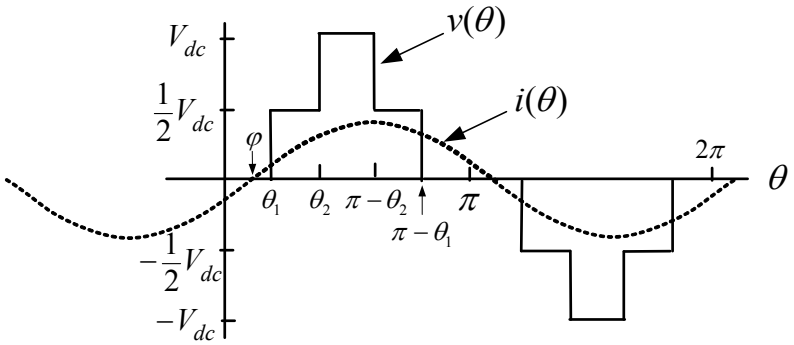

Figure 22. $0 < \varphi < \theta_1$.

In this case, keeping the capacitor charged requires

$$\begin{aligned} \int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta &< \int_0^{\varphi} I\left|\sin(\theta-\varphi)\right|d\theta + \int_{\varphi}^{\theta_1} I\sin(\theta-\varphi)d\theta + \int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta \\ I\cos(\theta_2+\varphi) + I\cos(\theta_2-\varphi) &< \left(I\cos(0) - I\cos(\varphi)\right) + \left(-I\cos(\theta_1-\varphi) + I\cos(0)\right) + \\ &\quad \left(I\cos(\varphi) - I\cos(\theta_1+\varphi)\right) \\ \cos(\theta_2)\cos(\varphi) &< \cos(0) - \cos(\theta_1)\cos(\varphi)\ , \end{aligned} \tag{5}$$

or finally, the condition in this case is

$$\cos(\varphi) < \frac{1}{\cos(\theta_1)+\cos(\theta_2)}\ . \tag{6}$$

Interval 2: $\theta_1 < \varphi < \theta_2$

Consider the case $\theta_1 < \varphi < \theta_2$ as in Figure 23. During the interval $\theta_2 < \theta < \pi - \theta_2$, the capacitor loses the amount of charge $\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta$, while during the intervals $0 < \theta < \theta_1$ and $\pi - \theta_1 < \theta < \pi$ the capacitor can be recharged (by choosing the switch positions appropriately) by the amount $\int_0^{\theta_1} I\left|\sin(\theta-\varphi)\right|d\theta + \int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta$.

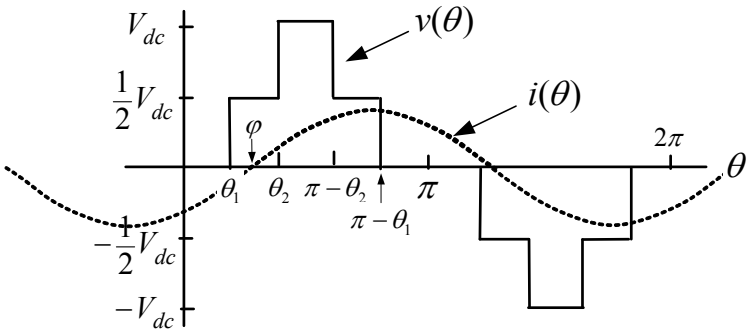

Figure 23. $\theta_1 < \varphi < \theta_2$.

Thus, keeping the capacitor voltage regulated requires

$$\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta < \int_0^{\theta_1} I\left|\sin(\theta-\varphi)\right|d\theta + \int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta \quad . \tag{7}$$

Expanding

$$\begin{aligned} I\cos(\theta_2+\varphi)+I\cos(\theta_2-\varphi) &< \left(I\cos(\theta_1-\varphi)-I\cos(\varphi)\right)+\left(I\cos(\varphi)-I\cos(\theta_1-\varphi)\right) \\ 2I\cos(\theta_2)\cos(\varphi) &< 2I\sin(\theta_1)\sin(\varphi)\,, \end{aligned} \tag{8}$$

or finally, the condition is

$$\frac{\cos(\theta_2)}{\sin(\theta_1)} < \tan(\varphi) \quad . \tag{9}$$

Interval 3: $\theta_2 < \varphi < \pi/2$

Finally, consider the case where $\theta_2 < \varphi < \pi/2$ as shown in Figure 24. During the subinterval $\theta_2 < \theta < \varphi$, the capacitor is being charged as the current is negative while it is discharging in subinterval $\varphi < \theta < \pi - \theta_2$. Thus the total discharge in the interval $\theta_2 < \theta < \pi - \theta_2$ is $\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta$.

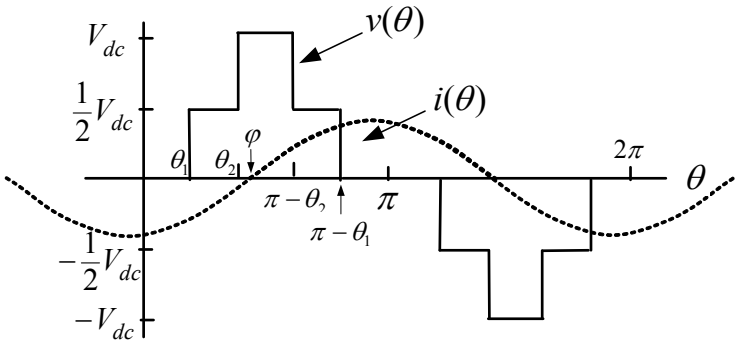

Figure 24. $\theta_2 < \varphi < \pi/2$.

Thus, keeping the capacitor voltage regulated requires

$$\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta < \int_0^{\theta_1} I\left|\sin(\theta-\varphi)\right|d\theta + \int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta \quad . \tag{10}$$

Expanding

$$\begin{aligned} I\cos(\theta_2+\varphi)+I\cos(\theta_2-\varphi) &< \left(I\cos(\theta_1-\varphi)-I\cos(\varphi)\right)+\left(I\cos(\varphi)-I\cos(\theta_1+\varphi)\right) \\ 2I\cos(\theta_2)\cos(\varphi) &< 2I\sin(\theta_1)\sin(\varphi)\,, \end{aligned} \tag{11}$$

or finally, the condition is

$$\frac{\cos(\theta_2)}{\sin(\theta_1)} < \tan(\varphi) \quad , \tag{12}$$

which has the same form as the previous case.

Capacitor voltage regulation as a function of *m* and φ

In summary, the conditions for capacitor voltage regulation in terms of θ_1, θ_2, and φ are

$$\begin{aligned} &0<\varphi<\theta_1 && \cos(\varphi) < \frac{1}{\cos(\theta_1)+\cos(\theta_2)} = \frac{1}{m}\,. \\ &\theta_1<\varphi<\pi/2 && \frac{\cos(\theta_2)}{\sin(\theta_1)} < \tan(\varphi)\,. \end{aligned} \tag{13}$$

Notice at the boundary of the two conditions where $\varphi=\theta_1$, the two conditions are identical. These conditions can be rewritten as

$$\begin{aligned} &0<\varphi<\theta_1 && \varphi > \cos^{-1}(1/m)\,. \\ &\theta_1<\varphi<\pi/2 && \varphi > \tan^{-1}\left(\frac{\cos(\theta_2)}{\sin(\theta_1)}\right). \end{aligned} \tag{14}$$

Figure 12 is a plot of θ_1 and θ_2 in degrees vs *m* (the modulation index is *m*/2). For any given value of *m* and φ, the values of θ_1 and θ_2 are found via Figure 12, and thus whether or not the capacitor voltage can be regulated is straightforwardly checked using the conditions (conditions2). What these conditions say is, for any given value of *m* in the interval $0.6 \le m \le 1.909$ [i.e., where conditions (conditions1) have a solution], the capacitor voltage can be regulated provided the power factor angle is large enough.

Conclusions

A cascade multilevel inverter topology has been proposed that requires only a single standard three-leg inverter and capacitors as the power sources. The capacitors obtain their power from the three-leg inverter, allowing the cascade multilevel inverter to put out significantly more voltage from a given dc power source than just a three-leg inverter alone. Both multilevel PWM and fundamental frequency

switching schemes were considered. Finally, subject to conditions in terms of the power factor and modulation index (= $m/2$), it was shown that the capacitor voltages could be regulated.

Future Direction

- A 1.2-kW prototype will be built to demonstrate the operation of the converter with a fuel cell (FY 2007).
- More simulation studies will be done to add plug-in hybrid capabilities to the cascaded multilevel inverter (FY 2007).
- If the 1.2-kW prototype is successful, a full-power 105-kW unit will be built (FY 2008–2009).

Publications

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Z. Du, L. M. Tolbert, J. Chiasson, B. Ozpineci, H. Li, and A.Q. Huang, "Hybrid Cascaded H-bridges Multilevel Motor Drive Control for Electric Vehicles," Power Electronics Specialists Conference, PESC 2006, Jeju Korea.

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4.4 Advanced Converter Systems for High-Temperature HEV Environments

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Objectives

The goal of this project is to develop a new and unique bidirectional dc-dc power converter that incorporates high-temperature power devices and capacitors with a high-temperature packaging technology and gate drives that will enable the converter to operate in high ambient temperature conditions. This project will develop a converter that has greatly reduced weight/mass, volume, and maintenance/service with high system efficiency, performance, and reliability compared with existing dc-dc converters for hybrid electric vehicles (HEVs).

Air-cooled high-temperature capacitors and SiC power electronics will lead to smaller thermal management systems, which will increase the peak power-to-weight ratio. Reduction of thermal management systems and lack of magnetic devices should offset the higher cost for SiC devices and high-temperature capacitors. Lower switching losses in a multilevel dc-dc converter will increase the efficiency to >97%. The converter topology will allow the battery pack to be subdivided into smaller modules in which the failure of a single cell does not disable the entire battery pack and only a single battery module need be replaced instead of the entire pack.

Approach

Several design tasks are being conducted in parallel by different organizations. These products will be integrated during the final year of this project to achieve a dc-dc converter that can operate at high temperatures. The other reason for the parallel design approach is that some technologies, such as the multilevel converter topologies, can be fabricated and tested now with conventional cooling techniques while other technologies, such as high-temperature packaging, SiC switches, and high-temperature capacitors, mature.

Multiple institutions are involved in this project to draw on the strengths of the particular institutions. Michigan State University, The University of Tennessee (UT), and Oak Ridge National Laboratory (ORNL) have devised two different magnetic-less dc-dc converter topologies. The Pennsylvania State University (Penn State) has used its experience in high-temperature capacitors to determine a figure of merit for new capacitor materials. UT and ORNL have designed a high-temperature gate drive.

Major Accomplishments

During FY 2006, there were major several accomplishments.

1. Michigan State University designed and fabricated a 10-kW dc-dc converter module based on some of its earlier topologies.

2. UT and ORNL devised an alternative dc-dc converter topology and fabricated a low-power proof-of-concept circuit to demonstrate its feasibility. More details on these accomplishments are given in the next section.
3. UT and ORNL designed a high-temperature gate drive using a new silicon-on-insulator (SOI) process by Atmel.
4. Penn State evaluated capacitors for high-temperature applications.

Each of these tasks is further elucidated in the next section.

Technical Discussion

Bidirectional dc-dc Converter Module

The design and fabrication of a 10-kW bidirectional dc-dc converter module was initiated during FY 2006. The converter module is able to output either the battery voltage or twice the battery voltage. Thus a power conversion system with *n* modules is able to output 1 to 2*n* different voltages with an increment of 42 V, as shown in Figure 1.

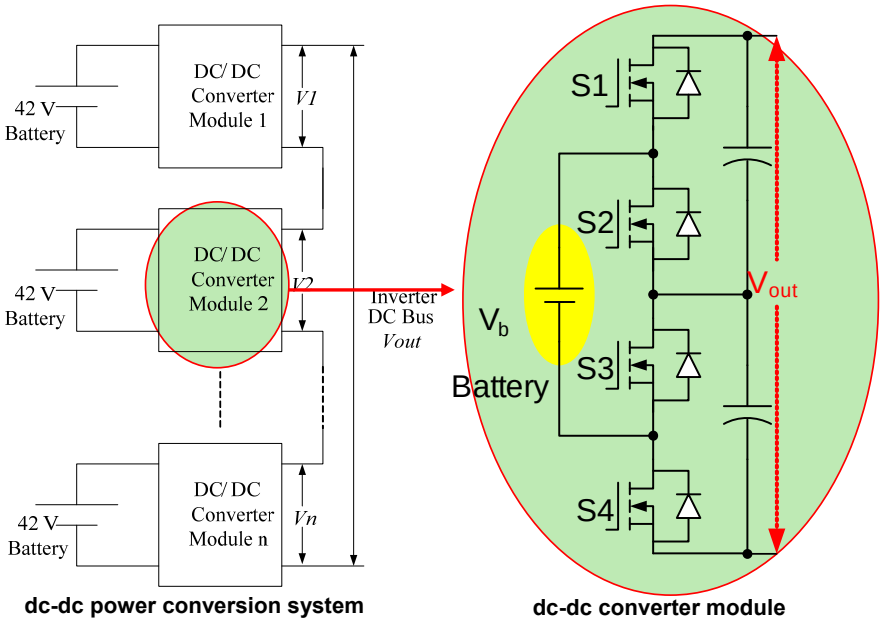


Figure 1. The dc-dc power conversion system and dc-dc converter module.

An individual module has been fabricated and is pictured in Figure 2. Specifications are as follows:

- nominal input voltage—42 V
- minimum input voltage—25 V
- maximum input voltage—45 V
- output voltage—42V/80V for nominal input voltage,
- nominal input current—240 A
- maximum input current—350 A,
- nominal output current—120 A

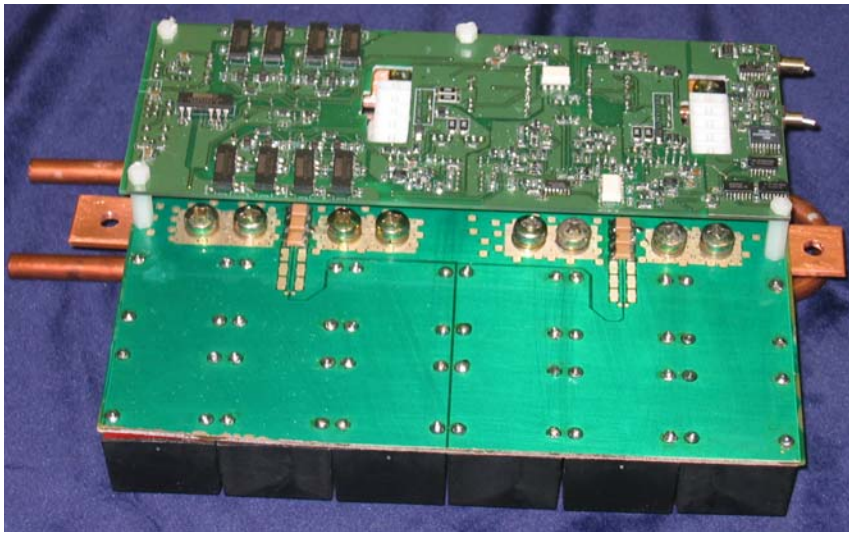


Figure 2. 10-kW dc-dc converter module.

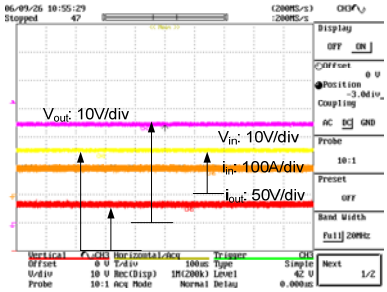
- maximum output current—180 A
- heat-sink—liquid cooled
- devices—2 metal oxide semiconductor field effect transistors (MOSFET) Modules: FM600TU-07A

A custom bus bar was fabricated to reduce the output voltage noise. Some initial tests of the converter were done with conventional car batteries, and converter efficiency was measured. Some experimental results are shown in Figure 3. The efficiency test was conducted using a YOKOGAWA power meter WT1600. The measured efficiency when output voltage equals input voltage was 99.4%, including the losses in the gate drive power supplies; the efficiency when output voltage equaled twice the input voltage was 98.1%, including the gate drive power losses. During the test, the battery voltage was around 30 V. When the input voltage increases to 42 V, the efficiency should be higher because the conduction loss will be less at this higher voltage level and it is the major loss.

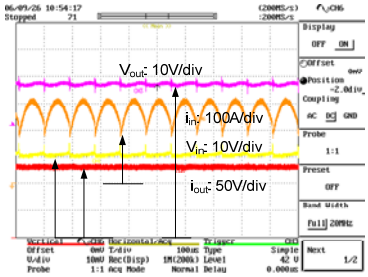
Additional testing of the converter will be conducted during FY 2007 to characterize its efficiency over a wide load and temperature range. The use of high-temperature devices in place of the conventional silicon switches will be made and a high-temperature module will be designed.

Multilevel Modular Capacitor Clamped dc-dc Converter (MMCCC)

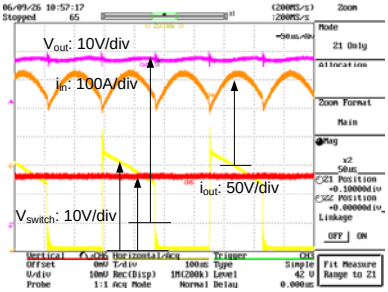
A second magnetic-less dc-dc converter topology explored as part of this project is the multilevel modular capacitor clamped dc-dc converter. The proposed 5-level MMCCC shown in Figure 4 has an inherent modular structure and can be designed to achieve any conversion ratio. For the schematic shown in Figure 4 with four modular blocks, the high-voltage side of the converter will be a factor of 5 greater than the low voltage side. Each modular block has one capacitor and three transistors leading to three terminal points. A modular block is shown in Figure 5. The terminal Vin is connected to either the high-voltage battery or to the output of the previous stage. One of the output terminals Vnext is connected to the input of the next stage. The other output terminal VLB is connected to the low-voltage side + battery terminal. Figure 6 shows the proof-of-concept 6-level MMCCC.



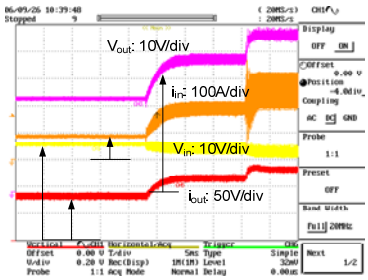
(a) Steady state waveform when outputting 1X



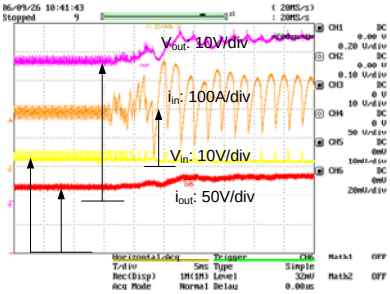
(b) Steady state waveform when outputting 2X



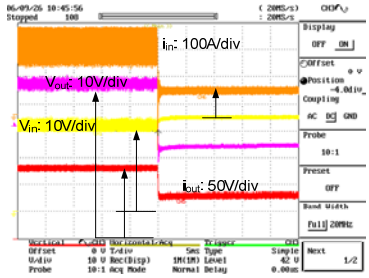
(c) Switch voltage when outputting 2X



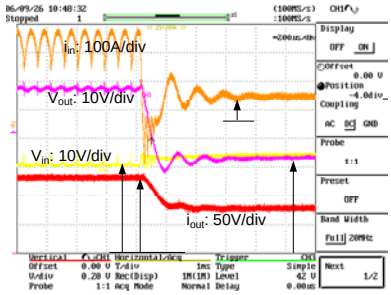
(d) Transition from 1X to 2X



(e) Details of transition from 1Xto 2X



(f) Transition from 2X to 1X



(g) Details of transition from 2X to 1X

Figure 3. Experimental results of the converter. 1X means the output voltage equals to input voltage; 2X means the output voltage is twice the input voltage.

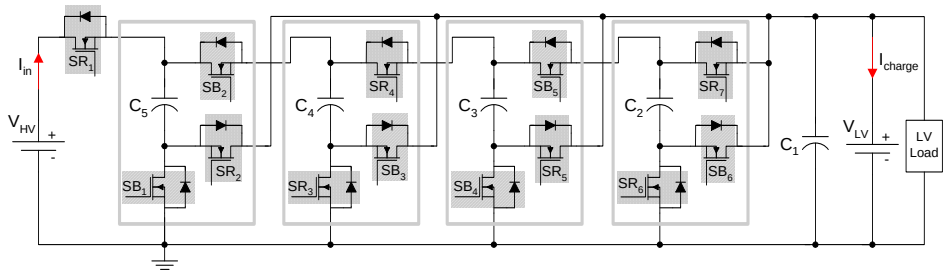


Figure 4. The proposed 5-level MMCCC with four modular blocks.

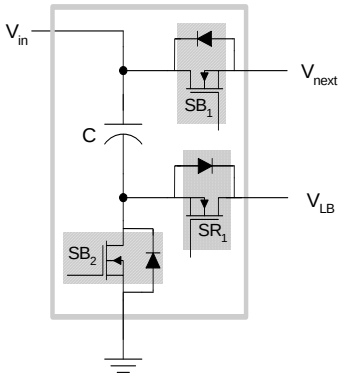


Figure 5. The modular block.

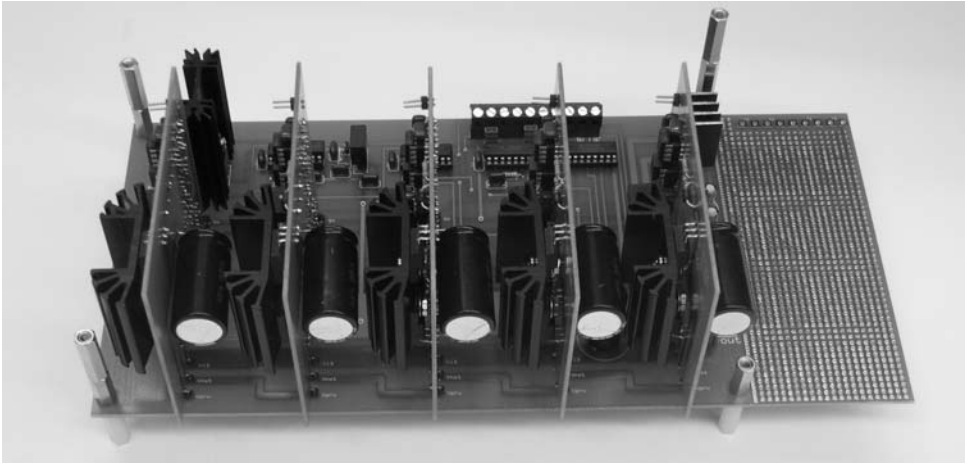


Figure 6. The proof-of-concept six-level MMCCC.

The new converter has much better voltage regulation compared with the conventional converter. In up conversion mode, the conventional converter's input current flows though (N-1) series connected transistors and one diode. The situation will be worse when the conventional converter attempts to deliver current from the high-voltage side to the low-voltage side. During this time the current flows through (N-1) diodes and only one transistor. Usually the voltage drop across the diode is higher than the voltage drop across any transistor, and thereby the regulation is very poor during this time. In contrast, the current flows through at most three transistors or diodes in the new converter irrespective of the conversion ratio. The reduced number of series connected devices in the new converter is responsible for less voltage drop and better regulation.

The new circuit suffers from one limitation. The MMCCC uses more transistors than are required for the conventional flying capacitor multilevel dc/dc converter with the same conversion ratio. For an N-level design, the conventional converter requires 2N transistors, whereas the new converter needs (3N-2) transistors. Thus, for a five- level design, the conventional converter needs 10 transistors; 13 transistors are needed for the new converter. However, the use of more transistors is truly compensated by obtaining all the desirable features from the new converter.

A new topology of the modular multilevel dc-dc converter has been proposed and validated by both simulation and experimental results. The new converter outperforms the conventional converters by having complete modular construction, high power transfer capability, simpler gate drive circuit requirements, high-frequency operation capability, onboard fault bypassing, and bi-directional power management capability. By virtue of the modular topology, the circuit obtains redundancy and the reliability can be increased significantly. The modular nature also introduces the use of one additional level to establish the fault bypassing and bidirectional power flow management. Thus this converter could be a suitable choice in various applications to establish a bidirectional power management between buses having different voltages.

High-Temperature Gate Driver

Layout of a gate driver chip capable of operating from –50 to 200ºC was completed and submitted to Atmel for fabrication in September 2006. Figure 7 is the schematic of the circuit, and Figure 8 shows the complete layout. The process used by Atmel is referred to as a BCD (bipolar-CMOS-DMOS) on SOI commonly known as SMARTIS. The total size of the chip is 5 mm^2 (2240 µm × 2240 µm).

Figure 9 shows the layout of the logic part of the gate driver chip, and Figure 10 shows the layout of the high-voltage (45-V) output stage of the gate driver chip. Two negative channel MOSs (NMOSs) in the output stage are made large enough (total W = 24,000 µm) to provide enough load current to get acceptable rise and fall times. Each of these NMOSs comprises six hundred 45-V NMOSs (W = 40 µm)

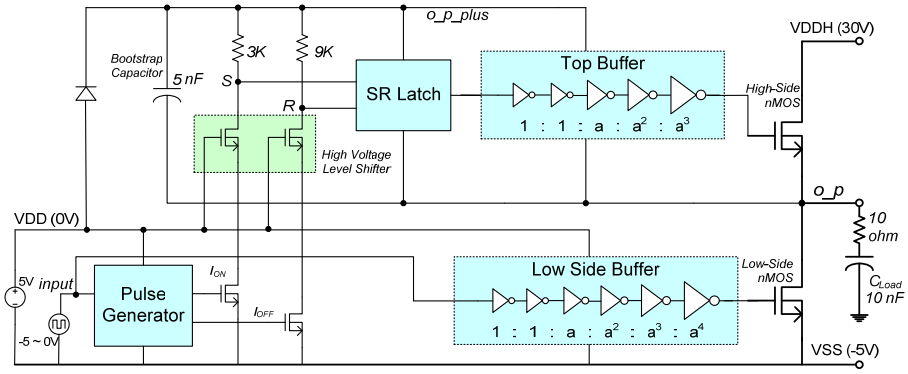


Figure 7. Schematic of the gate driver circuit.

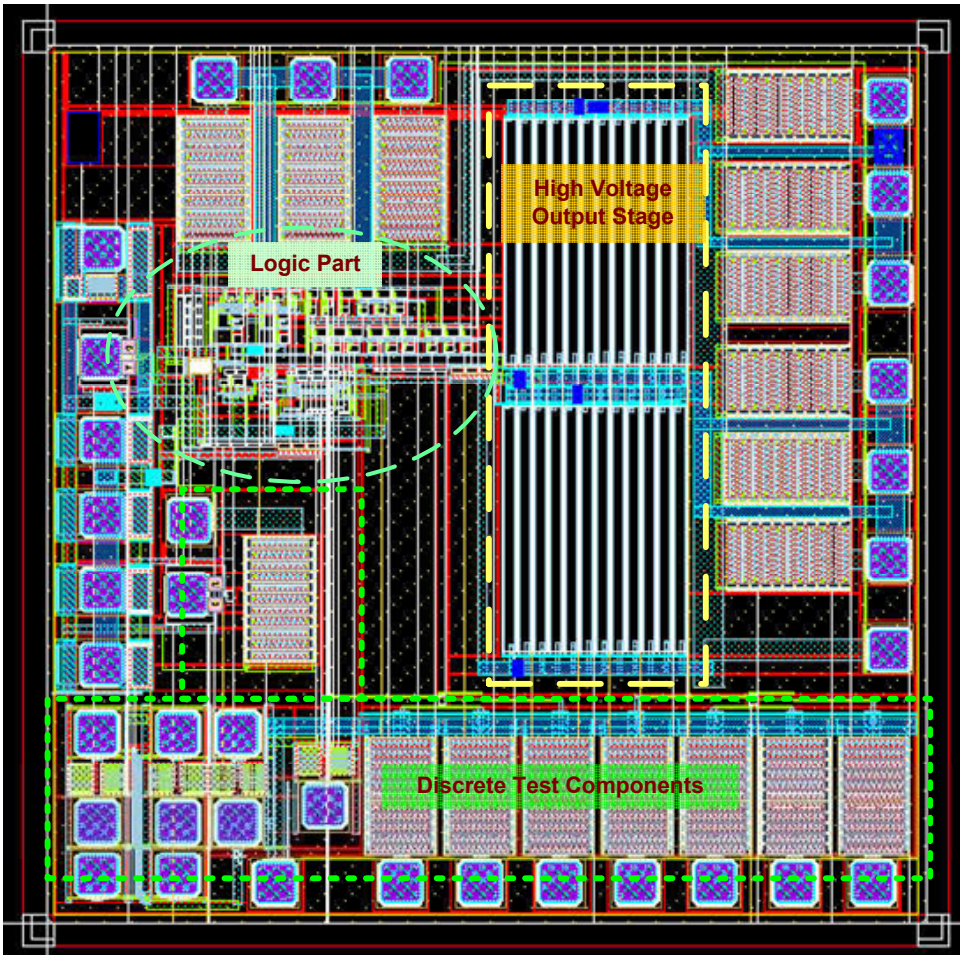


Figure 8. Complete layout of the gate driver chip.

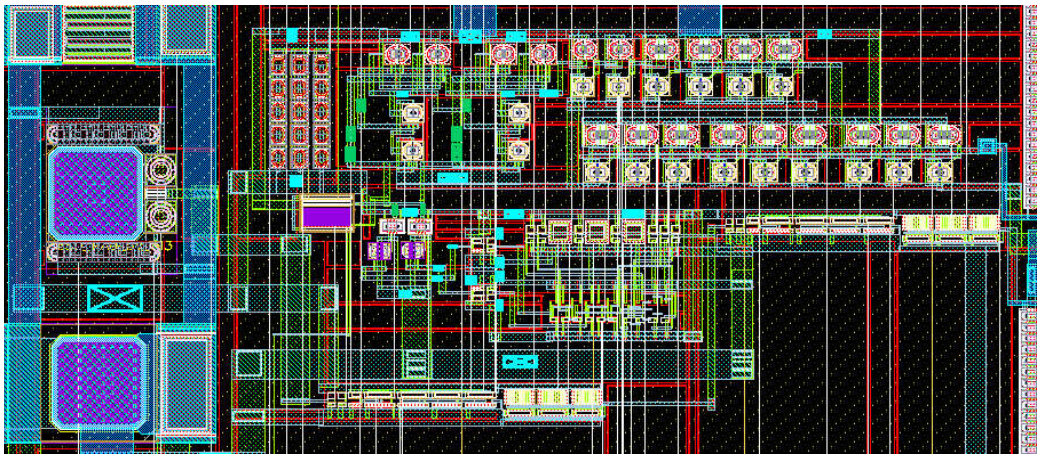


Figure 9. Layout of the logic part of the gate driver chip.

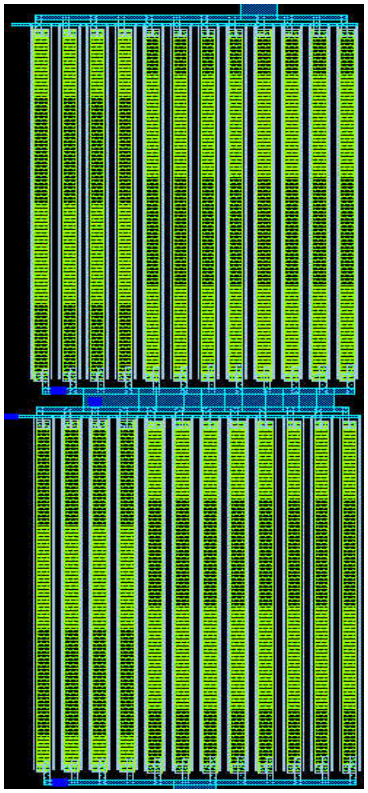


Figure 10. Layout of the high-voltage output stage.

connected in parallel. In the layout, the high-voltage output stage and low-voltage logic sections are carefully laid separately for the safety of the chip. Gate and power supply protections are also ensured in the pad frame. Post-layout simulations were performed to check the functionality of the layout.

Other than the gate driver circuit, some discrete components [45-V NMOS, 5-V NMOS and positive-channel MOS (PMOS), 25 NMOS and PMOS] are also added in the layout for testing and characterization at high temperature so that after these are characterized, we will know if these can be used in future chips.

Fabrication of the gate drive chip by Atmel will occur during the last 3 months of 2006 (first quarter of FY 2007). High-temperature printed circuit boards will be evaluated for use with the gate drive chip.

High-Temperature Capacitors

Penn State contacted a number of capacitor companies and procured samples from several sources. A list of capacitors is shown in Table 1.

Table 1. U.S. capacitor industry products for high-temperature capacitors

Company	Capacitance value (μF)	Temperature range (°C)	Voltage rating (V)	Comments	Size W × H × T (cm)
Johansen Dielectric	0.22	Up to 200	100	NPO type	1.2 × 1.27 × 0.38
	2.70		100	X7R type	
Kemet	0.033	Up to 200	100	NPO type X7R type	0.78 × 0.78 × 0.38
	1.0		100		
Wright Capacitors	0.082	Up to 200	500	NPO type	1.57 × 1.68 × 0.64
	2.75		500	X7R type	
Dearborn Electronics	1.0	Up to 125	50	Metallized film	1.8(h) × 0.625 (diam)
	1.0		250		2.5(h) × 1.5 (diam)
Electronic Concepts	150	Up to 100	500	Metallized film	4.0(h) × 8.3 (diam)
K Systems	<1.0	Up to 300	50	Diamondlike	Not specified
TRS Technologies	1	Up to 300	500	Almost X7R	1.6 × 1.6 × 0.7
	50	Up to 600	2000	Almost NPO	

The largest multilayer ceramic capacitors (MLCCs) are 1 μF, and they need to be stacked in parallel to achieve the total capacitance that is required by the power converter. The highest-temperature polymer film capacitors were found to be 125°C, and MLCCs have substantially higher temperature capability (600°C).

In addition to ac characterization of commercial capacitors, the dc performance was evaluated for commercial capacitors and prototype capacitors made at TRS Technologies and Penn State. An "*RC* figure-of-merit" which combines capacitance and dc resistance results was established. High dc resistance is important for component reliability, and high capacitance is important for volume-efficient inverters. The "figure-of-merit" was derived from the following:

$$R = \frac{\rho d}{A} \quad , \tag{1}$$

$$C = \frac{\varepsilon_r \varepsilon_o A}{d} \quad , \tag{2}$$

$$RC = \rho \varepsilon_o \varepsilon_r \quad , \tag{3}$$

where A is the capacitor area, d is the capacitor thickness, ε_o is the permittivity of free space, ρ and ε_r are the resistivity and relative permittivity (same as dielectric constant) of the dielectric material, respectively. Note that the "*RC*" value only contains material parameters and that the capacitor geometry is factored out of Equation (3). The "*RC*" value shown in Equation (3) is not the standard "time constant" for capacitor discharge, but a figure-of-merit related to capacitor reliability and volumetric efficiency. Low leakage current in a material represents a high R-value and is important for capacitor reliability. A high C-value is important for shrinking capacitor size. Penn State surveyed more than 50 materials, including polymer film and ceramic, and the *RC* values ranged from 10^{-4} to 100 at 200°C. Table 2 shows that the best material was found to be $BaZrO_3$.

Table 2. Summary of high-temperature materials survey (taken from a study of more than 50 materials)

Material	*RC* at 200°C	*RC* at 300°C	*RC* at 400°C
Polypropylene	0.000081	Too low to measure	Too low to measure
$BaZrO_3$	103	59	0.33
JDI NPO	90	Bad terminations	Bad terminations
Average PLZT	280	13	0.04

The *RC* value is very low at 200°C for commercial polypropylene, which is used in film capacitors for pulsed-power applications. As temperature is increased, the resistance "*R*" drops for all dielectric materials. Therefore the *RC* product also decreases for all dielectric materials as temperature is increased. A commercial high-temperature capacitor material, JDI NPO, has a high *RC* value at 200°C; however, we were unable to measure the electrical properties at higher temperatures. The terminations of this commercial capacitor did not work at 300°C.

Experimental materials PLZT and $BaZrO_3$ were explored, and both have excellent *RC* values at 200°C. $BaZrO_3$ is the best overall dielectric material at higher temperatures. The capacitance and loss of a prototype $BaZrO_3$ capacitor is shown in Figure 11. Penn State and TRS Technologies have been collaborating on high-temperature capacitor development, and the results show that $BaZrO_3$ has low losses up to 350°C, well above the DOE FreedomCAR specification of 140°C.

Researchers from Penn State University and TRS Technologies visited Wright Patterson Air Force Base to deliver high-temperature capacitors to its power electronic group. Jim Scofield and coworkers have assembled an all-SiC converter, operating at 2 kW, 200 V, and 200°C. They are presently using commercial Y5V 4.7-μF multilayer ceramic capacitors for the dc bus capacitors. These capacitors are only rated to 125°C and 50 V, but they perform well above these specifications. However, these capacitors were only operated for a short time at these elevated temperature and voltage ratings, and it is expected that the lifetime of the capacitor would be significantly reduced. A summary of commercial capacitor temperature specifications for consumer electronics is shown in Table 3.

Figure 12 shows a typical response for commercial Y5V multilayer ceramic capacitors, and the industry specifications are shown in Table 3 for common capacitor types. Typically NPO capacitors are used for high-temperature operation. Figure 13 shows the dielectric response of the commercial Kemet capacitors under a 200-V bias (which is four times the voltage rating). The capacitance has a peak value of 0.35 μF at 200°C, which is the operating temperature of the SiC converter at Wright Patterson Air Force Base.

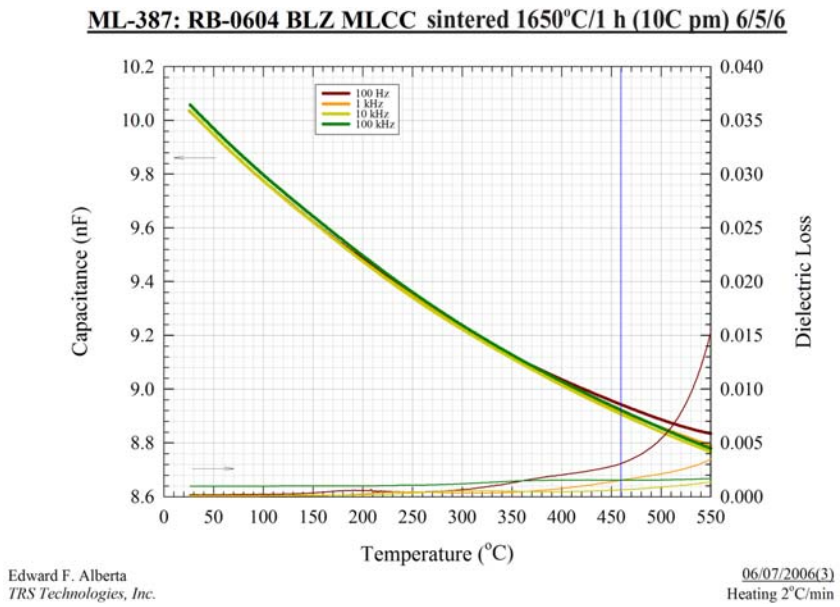


Figure 11. Capacitance and loss for a $BaZrO_3$ prototype capacitor manufactured at TRS Technologies. Note that the capacitance changes approximately 10% from room temperature to 550°C. The loss value at 100 Hz exceeds the DOE FreedomCAR specification at 350°C. High dielectric loss at low frequency suggests that dc conduction is an important factor at high temperature.

Table 3. General commercial capacitor classes (Note the trade-off between dielectric constant and temperature dependence of dielectric constant)

Capacitor specification	Y5V	X7R	NPO
Dielectric constant	6000	2000	60
Temperature range °C	10 to 85	–55 to 125	–55 to 125
Δ°C over temperature range	80%	30%	30 ppm

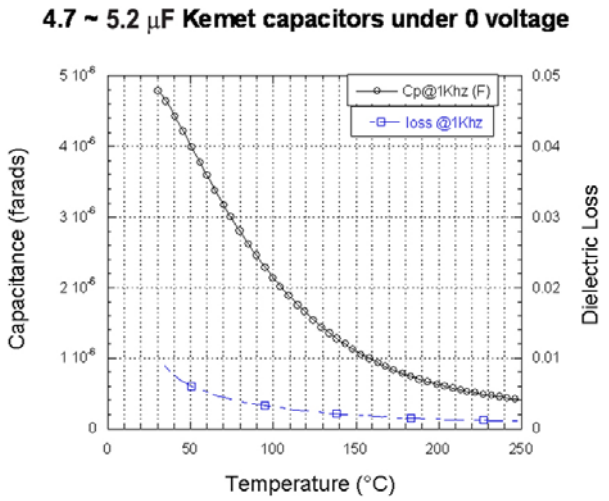


Figure 12. Temperature dependence of capacitance and loss for a commercial multilayer ceramic capacitor. The capacitor is "Y5V" specified and is designed to have a maximum capacitance at room temperature.

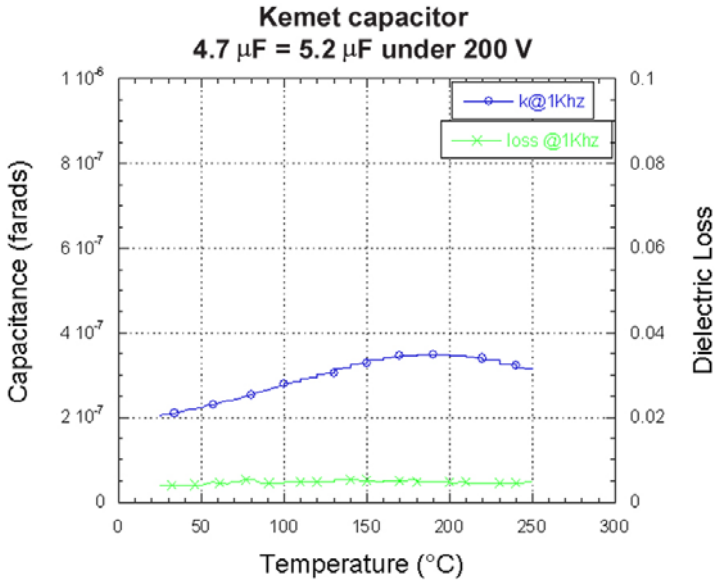


Figure 13. Temperature dependence of capacitance and loss for a commercial multilayer Y5V ceramic capacitor under an applied dc voltage of 200 V.

Both ac and dc tests of commercial and experimental capacitors were carried out as a collaborative effort between Penn State, ORNL, and industrial partners. It was found that high-temperature polymer film capacitors had very low dielectric loss up to temperatures of 120°C. The ac properties of commercial MLCCs were characterized up to 180°C, and the dielectric properties improved continuously as temperature was increased. dc tests were also performed and an RC figure-of-merit was used to compare capacitors. A new dielectric $BaZrO_3$, developed in collaboration with TRS Technologies, was found to have the best high-temperature properties. dc bus capacitors in an all-SiC power inverter which operates at 200°C, are presently being explored at Wright Patterson Air Force Base. Presently, an array of commercial 5-µF MLCCs is employed in a parallel array for the dc bus capacitor. Penn State characterized the high- temperature and high-voltage dielectric properties of these capacitors.

Conclusion

This challenging project involves the development and demonstration of several novel technologies to achieve a converter that can operate at high ambient temperatures. Novel magnetic-less dc-dc converter topologies will result in reduced volume and weight compared with conventional topologies. The multilevel design of these converters will also allow segregation of the battery pack into multiple modules. This will allow only a portion of the battery pack to be replaced if there is a failure. It may also result in an increase in reliability and availability of the battery power, as the converter designs will allow for a damaged or failed battery module or power electronics module to be bypassed.

A high-temperature gate drive has been designed and will be tested in the upcoming year. High-temperature packaging of SiC-based power electronics will transition from diodes to controllable switches in the upcoming year as another step toward a complete high-temperature module. Gains made from this project will likely impact other power electronics projects that need high-temperature packaging, gate drives, or modular conceptual designs.

Future Direction

During FY 2007, detailed design, fabrication, and testing will be conducted of two different magnetic-less dc-dc converters to demonstrate the feasibility of the topologies. These will have conventional packaging and heat transfer technology. The development of converter control will be done during FY 2007 of the necessary algorithms to control power flow in both directions while regulating the voltage at the receiving end of the converter.

In addition, a high-temperature gate drive fabricated in SOI that was submitted for fabrication in September 2006 will be manufactured by Atmel during the first quarter of FY 2007 and then tested to determine its characteristics over a wide temperature range (–50 to 200ºC). Based upon the results of the testing, a revised gate drive design will be done and submitted for fabrication.

A high-temperature power module will be designed and fabricated that leverages some of the high-temperature packaging techniques that were used in the Wide Bandgap Semiconductor project at ORNL. This module will likely consist of several SiC junction field effect transistors, SiC Schottky diodes, and high-temperature capacitors. The module will be a building block of one of the two dc-dc converter topologies that are being tested during FY 2007. The selection of the topology will be based on availability of components (SiC switches and high-temperature capacitors) and which converter looks most promising in terms of meeting FreedomCAR goals after testing.

Upon successful testing of these power modules and gate drives, these will then be ready for a system assembly using five of these units to complete the fabrication of a dc-dc converter capable of bidirectional power transfer. The complete converter assembly and testing will be done during FY 2008.

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F. H. Khan and L. M. Tolbert, “A Multilevel Modular Capacitor Clamped DC-DC Converter,” *IEEE Industry Applications Society Annual Meeting*, *Tampa, Florida*, October 8–12, 2006.

L. M. Tolbert, H. Zhang, M. Chinthavali, and B. Ozpineci, "SiC-based Power Converters for High Temperature Applications," *European Conference on Silicon Carbide and Related Materials (ECSCRM)*, *Newcastle, United Kingdom*, September 3–7, 2006.

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F. H. Khan, L. M. Tolbert, and F. Z. Peng, "Deriving New Topologies of DC-DC Converters Featuring Switching Cells," *IEEE Workshop on Computers in Power Electronics*, Troy, New York, July 16–19, 2006.

M. Chinthavali, L. M. Tolbert, B. Ozpineci, and H. Zhang, "High Temperature Power Electronics—Application Issues of SiC Devices," *IMAPS International Conference on High Temperature Electronics*, *Santa Fe, New Mexico*, May 15–18, 2006.

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4.5 dc/dc Converter for Fuel Cell and Hybrid Vehicle

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Objectives

The goal of this project is to develop and fabricate a 5-kW dc/dc converter with a baseline 14-V output capability for fuel cell and hybrid vehicles. The major objectives for this dc/dc converter technology are to provide

- higher efficiency (92%)
- high coolant temperature capability (105°C)
- high reliability (15 years/150,000 miles)
- smaller volume (5 L)
- lower weight (6 kg)
- lower cost ($75/kW)

Approach

The key technical challenge for this converter is the 105°C coolant temperature. The power switches and magnetics must be designed to sustain higher operating temperatures reliably, without a large cost/mass/volume penalty. The following key technologies are proposed to break through technical barriers to achieve a high-temperature, high-power-density, and lower-cost design.

1. Converter topology

A novel interleaved dc/dc converter topology is proposed as shown in Figure 1. The key merits of the converter are

- lower rms current stresses on components due to interleaving
- reduced ripple current on capacitors due to interleaving
- lower power losses due to low Rds_on and soft-switching
- smaller magnetics due to high switching frequency
- low EMI due to integrated power devices and magnetics

2. Integrated module-based dc/dc converter

Power module-based integration technology has been employed in this design. The thermal requirements are a challenge. The coolant temperature is 105°C. To meet the junction temperature 125°C design criteria, the thermal impedance has to be very small. Power module integration simplifies thermal stack-up layers, obtaining smaller thermal resistance. Furthermore, the customized power module optimizes the high-current interconnection path, reducing conduction losses. By using wirebonds in the

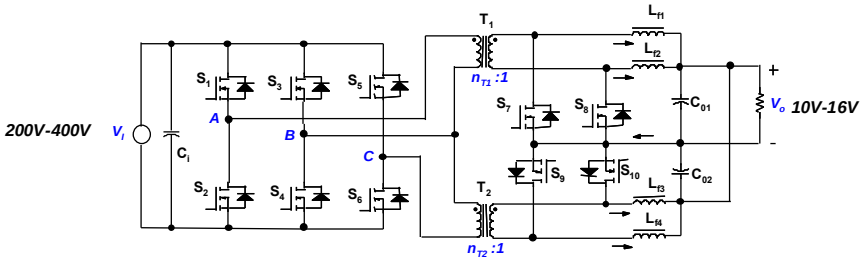


Figure 1. The novel interleaved dc/dc converter topology.

transformer design, rather than the traditional bolts and busbars, the reliability is also improved. The major advantages of the power module based dc/dc converters are

- enhanced thermal performance
- reduced number of devices
- increased reliability
- higher level of integration

3. Planar magnetics with enhanced cooling

This converter has also been designed using planar magnetics, a technology that Ballard thinks is critical for reliable and cost-effective high-volume production of such products. The benefits from this technology are

- lower leakage inductance due to shorter winding termination and smaller circuit paths
- elimination of discrete contacts' Ohmic loss
- reduction of Ohmic loss due to shorter conduction paths
- lower ac loss due to flat winding structure
- higher core window utilization ratio
- smaller core volume and weight
- higher surface to volume ratio for improved heat conduction
- direct cooling of core by direct contact to heat sink
- higher power density

Major Accomplishments of FY 2006

In FY 2006, Ballard focused on the production Beta design to address differences between the DOE goals and the Alpha design results. The major achievement in FY 2006 was the design and verification of the final Beta unit to meet the targets. Tasks included

- electrical improvements over the Alpha design
- cost reduction
- volume reduction
- weight reduction
- thermal design improvement
- manufacturing process improvements

The project timing consisted of four phases: Phase I: Key technologies prove-out; Phase II: Full function Alpha design and test; Phase III: Final Beta prototype design; Phase IV: Final build, DV test, delivery, and report. In FY 2005, we have finished Phase I and part of Phase II. The results have been reported as shown in Table 1.

Table 1. The percentage of goals achieved as of FY 2005 through Alpha design

	Alpha Design	DOE Goal	% Target
Output Power	5.1kW	5kW	102%
Efficiency	93%	92%	101%
Cost Estimation	$545	$375 total, ($75/kW)	69%
Coolant Temperature	90 Deg C	105 Deg C	86%
Volume	6.5 Liter	5 Liter	77%
Weight	7.6kg	6kg	79%
Coolant Pressure Drop	2.3 PSI	0.73PSI (5kPa)	32%

In FY 2006, we continued working on the Alpha prototype testing work, completed the Beta design and part purchasing, and developed the manufacturing process to produce the final prototype. The major tasks follow:

1. Continued electrical evaluation testing on Alpha prototype:

Figure 2 shows the test implementation for the Alpha prototype. At the end of FY 2005, we had finished the efficiency tests at Vi = 200 V, 300 V, 350 V up to 5 kW, and achieved the 92% efficiency target. The remaining issue was when the input voltage reached ~400 V, the efficiency dropped substantially, and excessive switching noise appeared in the synchronized rectifier switches. This problem prevented the dc/dc converter from delivering full power at 400 V.

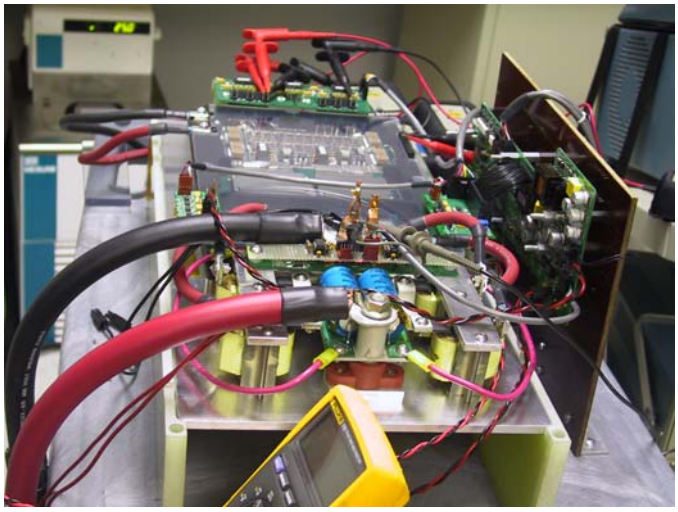


Figure 2. Alpha dc/dc converter under test.

Troubleshooting of the noise problem had been done in early FY 2006 to solve the switching noise problem. It turned out to be that a higher Qrr loss occurred under hot coolant test conditions. When coolant was raised to 90°C, the ambient temperature surrounding the die and gate drive circuit rose. It

caused a small change in signal delay. However, the delay was big enough to cause a higher reverse recovery current in the rectifier turn on/off transitions, leading to excessive Qrr losses on the rectifiers. An improvement was made in the gate drive circuit to compensate the delay due the high-temperature operation. The dc/dc passed the full-input voltage (Vi = 400 V) and full-power (Po = 5 kW) operation with 90°C coolant. The overall efficiency kept above 92%, as shown in the final test results in Figure 3.

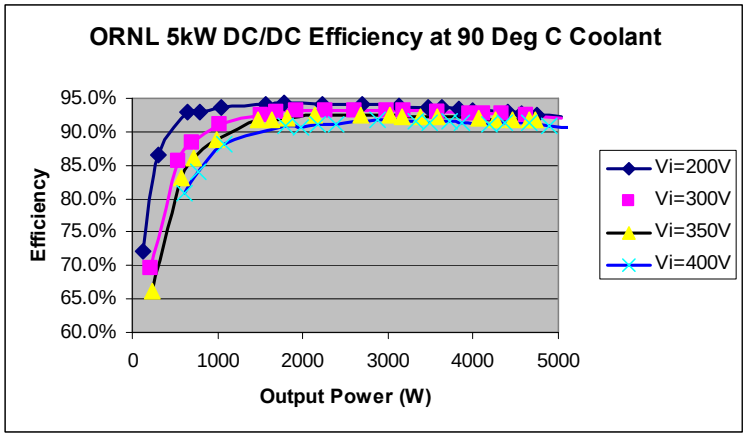
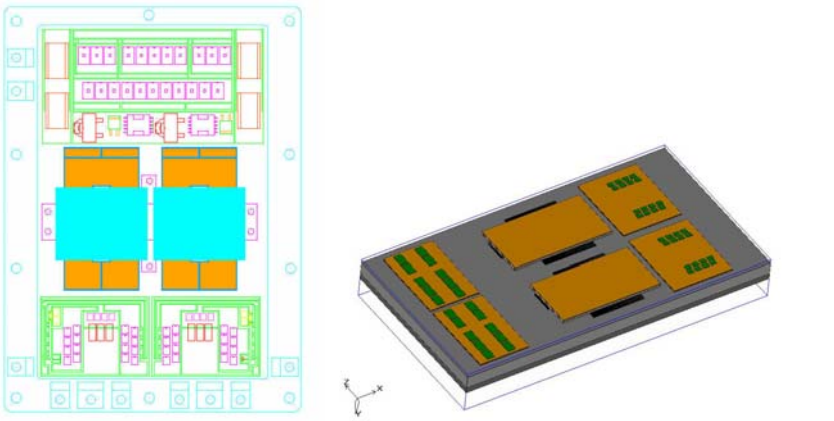


Figure 3. Efficiency test results at Vi = 200 V, 300 V, 350 V, and 400 V.

2. Cost reduction—Beta design

The cost of the customized power module is a major portion of the dc/dc converter costs, making up more than 50% of the total. In the Beta design, a new lead frame design concept was adopted to eliminate signal pin inserts. As a result, the power module baseplate width was reduced by 33 mm. Figure 4 depicts the Alpha and Beta power module design. The reduction of the power module width reduces the power module cost by 7%. The improved lead frame design also saves in the tooling costs. The high-volume cost estimation based on the Beta design is $458 at high volume; this is 82% of the DOE goal.



a) Alpha (203 X 315 mm) **b) Beta (170 X 315 mm)**

Figure 4. Alpha and Beta power module layout.

3. Volume and weight reduction

The 33-mm saving in power module width dimension also contributes to volume and weight reduction in the final packaging. To pass the environmental requirements, an aluminum cast housing was designed for the Beta prototype. The total volume was reduced to 5.1 L in the Beta design, down from the 6.5-L Alpha prototype design. Figure 5 shows the final Beta dc/dc converter packaging without cover.

The adoption of the final power module design greatly simplified the interconnection of the dc/dc converter. The part count was reduced to a total of 42 parts, including 2 wire harnesses and 11 types of fasteners. Table 2 lists the bill of materials of the Beta design and the weight estimation. The total weight is 7.4 kg. Although the aluminum housing is included, the total weight is 0.2 kg less than the Alpha prototype.

Figure 6 illustrates the bottom view of the Beta packaging. It shows the interfaces between the dc/dc converter and the end-user. The high-voltage connector connects the high-voltage input (200–400 V) to the dc/dc converter; the LV studs are the 12-V output to deliver the low-voltage power to the 12-V battery and loads in a vehicle. The coolant in/outlet ports bring a circulating coolant into the unit to remove the heat generated in the dc/dc converter. The signal connector is the control path between the dc/dc converter and vehicle controller. It includes the voltage command and enable signals through a controller area network interface.

4. Thermal design improvement

Two major design improvements have been made in the Beta design: the lead frame material and baseplate material.

To meet 105°C coolant operation requirements, AMODEL A-4133 L had been selected for the high-temperature plastic lead frame. It has high heat resistance, high strength and stiffness over a broad temperature range, low moisture absorption, excellent chemical resistance, and excellent electrical properties. It has been advantageously used for many automotive electrical and electronics applications. Its heat deflection temperature is as high as 300°C. An injection mold was required to manufacture the plastic lead frame. It added a substantial tooling cost for the Beta prototype development.

To design for a 15-year reliability requirement, aluminum silicon carbide (AlSiC) had been selected for the power module baseplate material. The AlSiC composite materials are designed to have a high thermal conductivity and a controlled thermal expansion (CTE) behavior that provides better CTE matching between the substrate and baseplate. A baseplate and substrate assembly was built to perform the thermal cycle test. It passed the thermal shock tests (–40ºC to +125ºC) 100 times without delaminating.

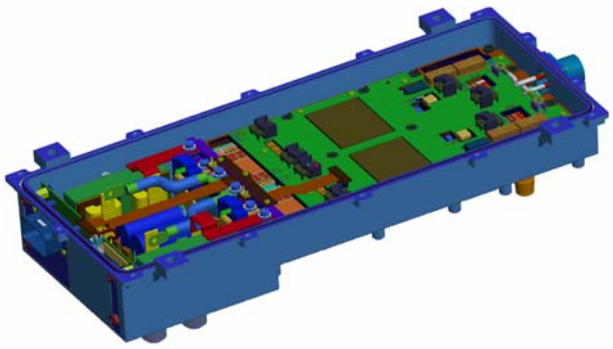


Figure 5. The Beta version of dc/dc converter (5.1 L).

Table 2. The BOM and weight of Beta design

	Part Description/Remarks	Ballard Part No.	Drawing No.	Qty /Per M	Weight (kG)
1	Fasteners, M4X8, (Inductor Bracket to Housing)	5109167		10	0.001
2	Fasteners, M3X10, (HV connector to Housing)	5109391		4	0.002
3	Fasteners, M5X12 , (Cover to Housing)	5109393		17	0.002
4	Sealing Washer, Fastener to Housing	5109394		8	
5	Inductor, 4.5uH, 125A, 100Vpk, 100KHz Ripple	5109397		4	0.295
6	Pad, Silicon Gel Gasket, Inductor Bracket, ORNL	5109605	DRW5106205	2	
7	Fasteners, M5x8, (Control BRD to Stand-off)	5110338		4	0.001
8	Fastener, Hi-Low, Gate DRV to Plastic Bracket,	5110602		13	0.001
9	Fasteners, M4X12, (LV Positive Busbar to PCB Capacitor ASY)	100330-PAA		4	0.002
10	Connector, 2Pin, 1 Row	101666-PAA		1	
11	Fastener, Hi-Low, Control Board to Housing	102264-PAA		4	0.005
12	Capacitor, Ceramic, 200V, 0.01uF, 10%, Radial	5106357-s		2	
13	Fasteners, M5X14, (LV Connections to Power Module)	5108401-s		6	0.003
14	Fasteners, M5X10, (Inductor Cables to Inductor)	5108404-s		2	0.002
15	Capacitor, Ceramic, 200V, 0.15uF, 10%, Radial	5106359-s		1	
16	Gasket, HV Connector to Housing	5109392		1	0.005
17	Fasteners, M6X16, (AC Connector, Negative)	5109511-s		2	0.005
18	Brass Hose Fitting, Barb X Male Pipe for 3/4" Hose Id, 3/4" Pipe	5110760		2	0
19	HEX Nut, M5, (Inductor Cable to Inductor)	5110481-S		6	0.005
20	LV Positive Busbar Cable, Inductor(3&4) to Power Module, ORNL	5109603	DRW5106203	2	0.01
21	Connector, High Voltage, ITT Cannon ORNL	5111030		1	0.07
22	O-ring, Inside coolant channal, ORNL	5110400	DRW5106911	1	0.005
23	O-ring, Outside, Cooling Channel, ORNL	5110407	DRW5106911	1	0.005
24	O-Ring, Electronic Housing, ORNL	5110528	DRW5106911	1	0.005
25	O-Ring Seal, Divider Coolant, ORNL	5110550	DRW5106913	1	0.005
26	Harness, 2-Pin, Control BRD to Capacitor BRD	5109387	DRW5105907	1	0.005
27	Current Sensor	5109144		2	0.023
28	Electronic Box Cover - Oakridge	5109098	DRW5105707	1	0.76
29	Capacitor, Electrolytic, 8200uF, 25V, 150Deg C	5109637		2	
30	Busbar Assembly, LV Positive	5109105	DRW5105712	1	0.09
31	LV Positive Busbar, Inductor(1) to Power Module, ORNL	5109600	DRW5106199	1	0.025
32	LV Positive Busbar, Inductor(2) to Power Module, ORNL	5109601	DRW5106200	1	0.025
33	Busbar Assembly, LV Negative	5109102	DRW5105709	1	0.023
34	HSG - ELEC BOX	5109101	DRW5105708	1	2.295
35	AC Connector, LV Positive	5109808-s		2	0.145
36	Inductor Bracket, ORNL	5109104	DRW5105711	2	0.01
37	Stand-off, Female-Female, 15mm Body, M5 thread	5109604	DRW5106204	4	0.005
38	Fastener, M5X30, (Power Module to Housing)	5108406-s		15	0.006
39	Flex Circuit, Gate Drive Board to Control Board, ORNL	5109141	DRW5105742	1	0.05
40	PCB Bare Board, LV Capacitors, ORNL	5109650		1	0.1
41	Power Module			1	1.535
42	PCB Assembly, Control Board, ORNL	5109173	DRW5105735	1	0.55

Weight (kg)	7.378
DOE Target (kg)	6
% of Target	81%

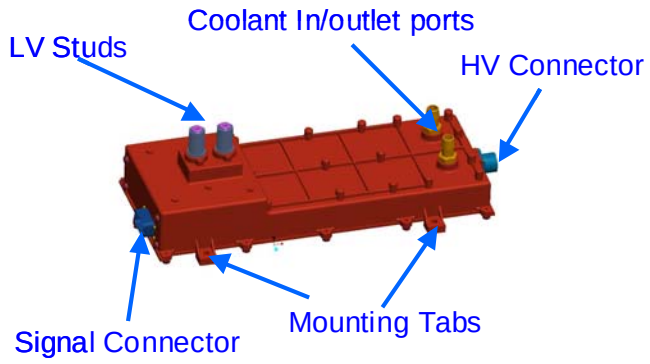


Figure 6. Beta dc/dc converter interfaces.

5. Coolant channel final design

The 105°C coolant operation requirement poses a significant challenge to the thermal design. The junction temperature is targeted at 125°C to allow metal oxide semiconductor field effect transistor switches to operate at a higher efficiency. There is only 20°C of temperature rise budgeted from die to coolant. In the Alpha design, a pin-fin pattern was designed in the coolant channel to achieve lower thermal impedance, as shown in Figure 7.

The pin-fin structure increases the surface area of the baseplate and increases the velocity of fluid in the coolant channel. As a result, the thermal resistance can be very low. However, the test result for the Alpha baseplate design revealed that the pressure drop with the pin-fin design was as high as 2.3 psi at 7 L/min, which is three times higher than the DOE goal (0.73 psi). In the Beta design, a decision was made to eliminate all pin-fins to meet the pressure drop target. The baseplate was redesigned as shown in Figure 8. A sample plate was made to test the pressure drop. The test result verified that the pressure drop in the baseplate coolant channel drops to 0.25 psi at 25ºC with a 7-L/min coolant flow rate. This meets the DOE target of 0.73 psi.

The location of inlet and outlet ports was also adjusted accordingly to minimize the turbulence of the coolant inside the channel. A 15-mm chamfer was added to the inlet/outlet chamber. The simulation result of the fluid field is shown in Figure 9.

Figure 7. Alpha baseplate pin-fin design with pin-fin.

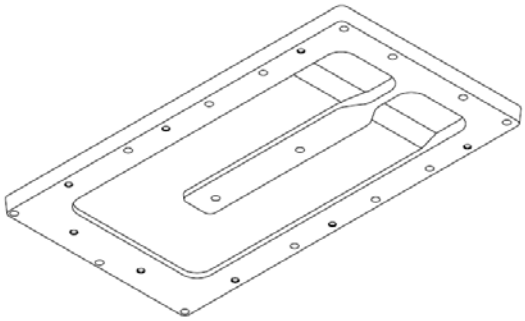


Figure 8. Beta baseplate design without pin-fin.

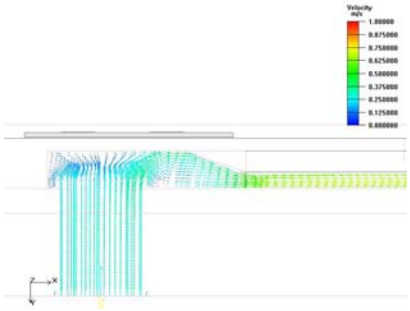


Figure 9. Coolant channel fluid simulation.

Thermal simulations were also performed using ICE pack to verify the junction temperature was within the 125 °C limit. The maximum junction temperature is 122.4°C for the worst case, as shown in Figure 10.

6. Solving practical issues

Given the coolant temperature range of –40ºC to +105ºC, a coolant pressure peak was detected as high as 60 psi. It broke the O-ring seal of the baseplate and caused leaking of coolant. Figure 11 illustrates

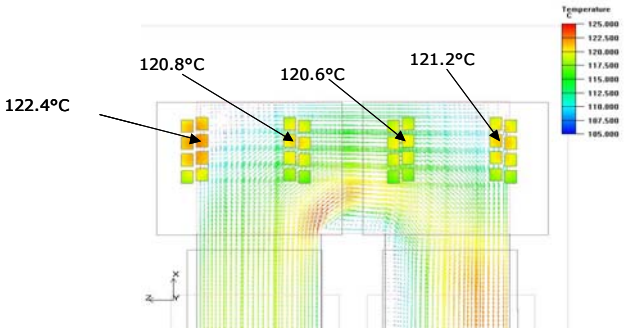


Figure 10. The thermal simulation results.

Figure 11. Baseplate leak test setup.

the baseplate coolant leak test setup. Figure 12 demonstrates the initial seal design leaked at –18ºC. After a few iterations, the seal design was improved and passed the leakage test over the entire range of –40ºC to +105ºC.

Figure 12. Baseplate leaks with initial seal design.

Technical Discussion

In FY 2006, the Beta version of dc/dc converter design has been completed. Several improvements have been made to meet DOE targets; however, there are still some gaps existing in the weight and cost goals.

1. Weight target—6 kg

The Beta design is 7.4 kg, which is 1.4 kg over the target. There are two opportunities to meet the weight target. The first opportunity is in housing weight reduction. Currently, we use sand casting for the Beta housing design to reduce the development costs. The housing itself occupies 3.1 kg. Using die casting in high-volume production instead of sand casting, we will be able to reduce the wall thickness from 4 mm to 2.5 mm, resulting in 30% weight reduction. The second opportunity is in power module baseplate weight reduction. The power module baseplate is 1.2 kg. Because the pin-fin is removed from the coolant channel, we can move the coolant channel into the molded housing, allowing us to make a thinner flat baseplate. This change will gain 45% weight reduction in the baseplate. The above two improvements will potentially lead to a 1.47-kg weight saving, which will eventually meet the DOE 6-kg target in high-volume production.

2. Cost target—$375 for the 5-kW dc/dc converter

The Beta design result reached 82% of the DOE target. The use of two expensive materials in this design can be revisited to reduce the cost. They are (1) AlSiC power module baseplate and (2) silicon nitride planar transformer windings. The opportunities are to (1) improve the material utilization factor and (2) work with the suppler to identify the major cost driver and improve the yield.

Conclusion

In the FY 2006, the testing of the Alpha prototype was completed. Based on the Alpha test results, we have implemented dramatic improvements in the design of the production Beta design. The status summary of the Beta design is presented in Table 3.

Table-3. Status summary from the Beta design during FY 2006

	DOE Goal	Beta Design Results (7/25/06)	Beta Design % Target
Output Power	5kW	5.1kW	102%
Efficiency	92%	93%	101%
Cost Estimation	$375 total, ($75/kW)	$458	82%
Coolant Temperature	105 Deg C	105 Deg C	100%
Volume	5 Liter	5.1 Liter	98%
Weight	6kg	7.4kg	81%
Coolant Pressure Drop	0.73PSI (5kPa)	0.25 PSI	292%

Publications and Presentations

Presentation on U.S. Council for Automotive Research meeting, Southfield, Michigan, March 30, 2006.

Presentation on 2006 DOE FreedomCAR APEEM Annual Review, Pollard Technology Conference Center, Oak Ridge, Tennessee, August 16, 2006.

Presentation on Industrial Power Converter Products and Services Session in IEEE IAS 2006, Tampa, Florida, October 12, 2006.

Patents

"An Interleaved High Power DC/DC Converter," PAT0589-01US, filed on June 4, 2004.

"Integration of Planar Magnetics Transformer and Power Switching Devices in a Liquid-cooled High Power DC/DC Converter," PAT0588-02US, filed on October 12, 2004.

4.6 High Temperature Film Capacitors

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Contractor: Sandia National Laboratories, Albuquerque, New Mexico
Prime Contract No.: 04-94AL85000

Objectives

Develop high operating temperature (150 ^{o}C) polymer film and nanoceramic capacitor technologies for dc bus capacitors used for FreedomCAR fuel cell/electric hybrid vehicles

Develop nanoceramic dielectrics for two different material families: 1) high dielectric constant PLZT and 2) high breakdown field, low dielectric constant TiO_2 dielectrics

Develop a high-temperature polymer dielectric film technology that has dielectric properties technically superior to the best commercial polymer film capacitors and will result in comparable or smaller size.

Perform extensive high temperature testing of nanoceramic and polymer film dielectrics

Scale up cost-competitive polymer film and nanoceramic dielectric technologies.

Fabricate prototype capacitors.

Approach

Contact DOE program managers, automobile design and component engineers, dielectric powder and polymer film suppliers, and capacitor manufacturers to determine state-of-the-art capabilities and to define market-enabling technical goals.

Develop a project plan with DOE Program Managers, automobile manufacturers and large and small capacitor companies to fabricate polymer dielectric sheets suitable for FreedomCAR capacitor manufacturing.

Synthesize unique norbornene chemical solution precursors that result in dielectric films with low dissipation factors (DFs) and excellent high-temperature dielectric properties.

Develop norbornene polymer film dielectric processes and technologies that will lower costs to permit competitive high-volume capacitor manufacturing.

Develop chemically prepared nanoceramic powders and high density layers of two classes of dielectrics: 1) High K PLZT materials and 2) lower K, High breakdown field TiO_2 materials

Fabricate capacitors to be tested at high temperatures for ripple current voltages.

Interact with Oak Ridge National Laboratory (ORNL) with regard to mechanical characterization and ripple current measurements of dielectric films.

Major Accomplishments

Invented chemical synthesis procedures for three different polymer film families: (1) low cost polyphenylated polyethylene dielectrics, (2) polyaryl ether dielectrics, and (3) Norbornene based purified product.

Developed a chemical synthesis route that resulted in lower cost polyphenylated polyphenylene product that should reduce cost of these polymer films by more than a factor of ten compared to previous synthesis routes.

Demonstrated excellent high temperature electrical performance for low cost polyphenylated polyphenylene polymer dielectrics spin deposited on Al Coated Si wafers (dissipation factor less than 0.01 at 150^{o}C).

Performed mechanical property characterization of the low cost polyphenylated polyethylene dielectrics and polyaryl ethers - these materials were too brittle to be wound into capacitors.

Invented chemical synthesis procedures for Norbornene purified product, this material has high glass transition temperature, good high temperature electrical performance and is potentially mechanically flexible.

Synthesized three different types of nanoceramic powders: 1) relaxor PLZT, 2) field enforced Antiferroelectric to Ferroelectric (AFE – FE) PLZT, and 3) second generation TiO_2 powders.

Fabricated high quality chem-prep nanoceramic dielectric layers of 50 micrometer thickness using our direct write aerosol spray deposition (ASD) process to evaluate these three types of dielectric materials

Using ASD, we down selected to a PLZT composition that exhibited a dielectric constant of 2000 and a dissipation factor of 0.003 at 150^{o}C, this will result in a factor of two reduction in volume compared to state of the art barium titanate capacitors.

Collaborated with Honeywell to develop the technology for tape casting 20 layer chem-prep multilayer PLZT capacitors.

Improved the capacitance of the chem-prep PLZT multilayer capacitors by a factor of three in development efforts over the last 9 months.

Collaborated with ORNL (Andy Wereszczak) to mechanically characterize both polymer film dielectrics and PLZT nanoceramic thick film layers.

Technical Discussion

Strategy and Interactions

SNL has interacted with DOE program managers, representatives from the automobile industry and industrial representatives from industry to obtain their perspective on what is needed for capacitors for 2010 automobiles. There is no clear consensus as to whether polymer film or ceramic multilayer capacitors are better for FreedomCAR capacitor applications. Because of the interest in both technologies and Sandia's long standing expertise in chemical preparation of electronic ceramic materials and components, in FY 2006, SNL increased the portion of its development efforts of nanoceramic capacitors. Development of high operating temperature polymer film dielectrics was also continued. DOE and EE tech team members have retained their position that soft breakdown dielectric film technology is highly

desired. Soft breakdown is a phenomenon that large volume manufactured polymer film capacitors inherently possess. Sandia, for the present, is relying on the developments of Mike Lanagan and coworkers at Penn State for benign breakdown technology for ceramic capacitors. Our interactions with DOE program managers, experts from the capacitor industry and automobile manufacturers led us to the conclusion that the most viable technology for improvement of DC bus capacitor performance by 2010 is either multilayer polymer film or multilayer ceramic capacitors. Reducing the size of the polymer capacitors was most often cited by automobile design engineers and capacitor manufacturers as a needed technology-enabling breakthrough. In addition, it is necessary to improve high-temperature (150^{o}C) performance while keeping the technology cost-competitive. Further, high temperature nanoceramic multilayer capacitors may result in an overall decrease in system cost, since cooling loops could be eliminated. Thus SNL is pursuing development of both polyfilm and nanoceramic MLC technologies in FY07. There is a decision point to continue development of polymer film capacitors at the end of FY07.

Sandia scientists have continued our efforts to interact with industry and automobile manufacturers. In FY06, SNL began an extensive collaboration with Honeywell in Kansas City to develop procedures for chem-prep PLZT multilayer capacitor fabrication. At the end of FY06, 0.2 μF, 20 layer chem-prep PLZT MLCs were fabricated. Based on initial electrical measurements of these capacitors, a design for a 138 μF replacement PLZT capacitor for the Prius capacitors was developed. The chem-prep PLZT MLC would consist of 85 each 5 cm by 10 cm dielectric layers of 40 microns each. These capacitors would be roughly one sixth the size of the Prius capacitors. Sandia also consulted with the Advanced Technology Vehicles Division of GM, Custom Electronics, AVX, TPL, Hydrosize, Inc., and Brady Corporation about polymer film and nanoceramic MLC technologies and future scale up operations. Hydrosize, Inc. was contacted for scale up of polymer solution synthesis processes to enable fabrication of large area polymer films suitable for fabrication of 0.2 microfarad to 200 microfarad capacitors. Sandia has worked with Brady Corporation in the past and fabricated rolls of polymer film that were 1 foot wide and 1000 feet long. Polymer films of this size can be used to fabricate either six 200 μF capacitors or sixty 20 μF capacitors for prototype testing. These capacitors would be roughly a factor of two smaller in volume compared to the polyfilm capacitors used in the 2004 Toyota Prius.

Details of the calculations for these prototype polymer film capacitors are described. An individual dielectric layer thickness of approximately 3 μm for polyfilm capacitors is projected to reduce capacitor size. These thickness values are based on operating field strengths of 2 MV/cm for the newly developed polyfilm capacitors. Based on these assumptions and on measurement of presently available commercial capacitors, size comparisons and capacitance densities were obtained for 500 μF dc bus capacitors for different technologies. The projected polymer film capacitor volume was calculated assuming that there is 40% non-active capacitor space and 200-nm thick electrodes are used. Note that the volumetric capacitance efficiency for a K = 4.5 polyfilm capacitor of 2.4 μF/cm^3 exceeds the near-term commercialization goal of 2 μF/cm^3. In order to meet the 2010 EE Tech team specification of 5μF/cm^3, a polymer with dielectric constant of 6 and operating field of 2.7 MV/cm will be required. From recent discussions, it is expected that DOE program managers and the EE Tech team will support SNL scale up of dielectric film technology that is more volumetrically efficient than present state of the art commercial technologies.

Polymer Film Dielectric Development

SNL polymer film dielectric development has been based on the request from manufacturers that the new polyfilm dielectrics have voltage and temperature stability equivalent to that of present polyphenylene sulfide (PPS) technology. Thus a structural family of polymer dielectrics has been designed and synthesized to meet two of the most stringent FreedomCAR requirements: (1) low dielectric loss and (2) extremely good temperature stability. Very low dissipation factors on the order of 0.003 were measured at 150^{o}C for these SNL fabricated films. A patent disclosure has been initiated covering

the design and synthesis techniques for this polymeric family [1] based on phenylated polyphenylene (PPP). A previous drawback to this technology was the high synthesis costs of these materials. In FY 2006, our team developed procedures that substantially lowered the cost of synthesis of scale up quantities. Lower cost was achieved by developing new procedures that eliminated two chemical synthesis steps and the identification of less expensive raw materials.

A total of three different major polymer film chemistries were developed and investigated in FY06. These three polymer film families were low cost polyphenylated polyphenylene, polyaryl ethers, and norbornene chemistries. Modifications to these major families resulted in the fabrication and characterization of over 50 different types of polymer films. Our metrics were synthesis of purified product, film fabrication, mechanical properties and electrical properties. Specifically, the structure of low cost hydroxylated phenylated polyphenylene synthesized by SNL is shown in Figure 1.

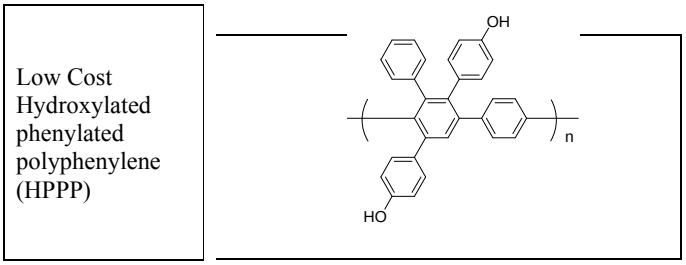

Figure 1. Structure of low cost hydroxylated phenylated polyphenylene

Excellent high temperature dielectric properties are shown in Figure 2 for the low cost (PPP) films developed by SNL in FY06. These films were spin deposited on Al coated Si wafers and were approximately 0.7 micrometers thick. Unfortunately, we were not able to spin deposit these films on Mylar due to poor adherence during processing or cracking. It is necessary to deposit polymer films on Mylar to create free standing films for mechanical evaluation. Free standing polymer films, both commercial and developed by SNL, have been sent to Andy Wereszczak at Oak Ridge National Laboratories in FY06. From this work, the metric of strain to failure rather than the strength of the film has been adopted as the primary metric for suitability for high volume winding of polymer thin films. ORNL measured a strain to failure of 25% for the polymer film in the Prius capacitors compared to 5% strain to failure for SNL high temperature polymer films. A second reason for the need to deposit polymer films on Mylar is that this substrate permits release of free standing films for subsequent capacitor manufacturing. Large area, free standing films are necessary to fabricate either wound or stacked polymer film capacitors. These capacitors are needed in order to fabricate prototype capacitors for testing by OEM and ORNL engineers for ripple current tests. The dissipation factors measured to 140^{o}C and shown in Figure 2 for the SNL low cost hydroxylated phenylated polyphenylene film were exceedingly low, on the order of 0.005, and encouragingly decreased with increasing temperature. This result is promising for high temperature inverter operation. Dielectric constants for these films are approximately 3.5 and are very insensitive to temperature. The dielectric constants of the low temperature polyphenylated polyphenylene films are almost 20% greater than those of commercial state of the art polyphenylene sulfide films.

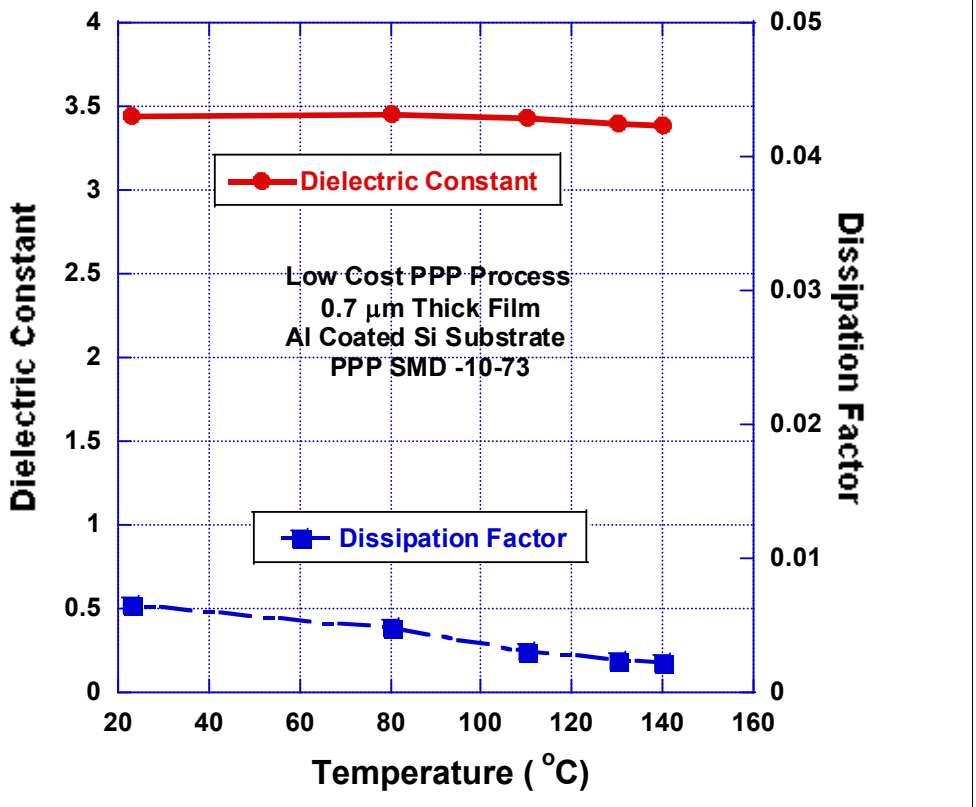

Figure 2. Dielectric Constant and Dissipation Factor Versus Temperature for Low cost PPP film

High quality nanoceramic powders of three different types of high energy density materials were fabricated in FY06 by SNL scientists. These different types of materials were: 1) low dielectric constant, high breakdown strength TiO_2, 2) relaxor ferroelectric PLZT and 3) Field enforced AFE to FE phase transition PLZT were fabricated in FYO6 by SNL scientists. The chem-prep nanopowder synthesis facility and computer controlled aerosol spray deposition apparatus are shown in Figure 3. The SNL patented process [2] consists of an acetic acid solution of Pb acetate, Zr butoxide and Ti isopropoxide precursors precipitated with oxalic acid using high shear rate mixing. Extremely homogenous, fine particles are created with a crystallite size on the order of 60 nm. Figure 3 shows the powder synthesis precipitation step and SNL lab facilities for 1.5 kg batches. Ten kilogram PZT batches can be fabricated at SNL facilities. In addition, the latest version of the SNL ASD direct write apparatus is shown. The desired substrate is rastered under the nozzle head by LabView programmed linear drive motors. Six layer multilayer PLZT capacitors have been fabricated by the direct write process [3,4] using a single fire process. Capacitors of 1 cm^2 area that are 50 μm thick can be deposited in less than a minute. We have fabricated aerosol spray deposited PLZT films of 50 micrometer thickness [5] that have breakdown strengths that exceed 200 kV/cm.

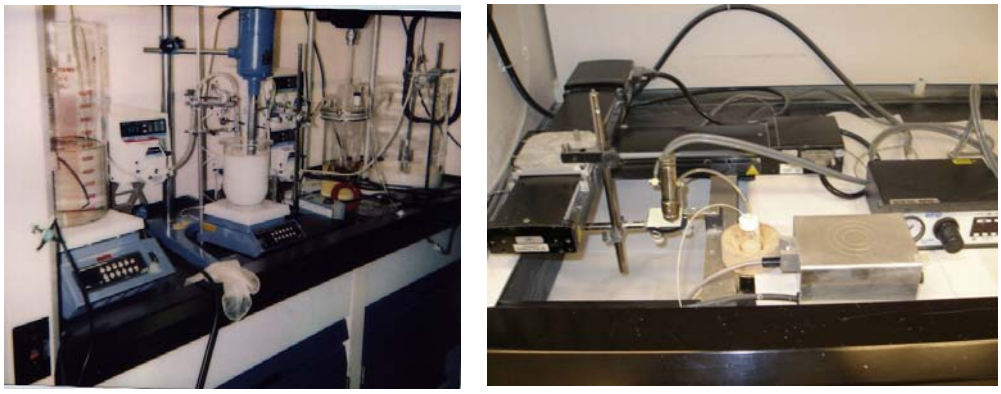

Figure 3: Chemical powder synthesis facility and aerosol spray deposition apparatus for nanoceramics.

SNL scientists used direct write ASD to fabricate high quality 50 micron thick layers of the three different types of high energy density nanoceramic dielectrics in FY06. TiO_2 was chosen as the first lower dielectric constant, higher breakdown strength dielectric to investigate. Powders of titania with less than 20 nm particle size were synthesized. These nanopowders were fabricated using a Ti-n butoxide based synthesis. The solution was pumped/sheared at 6000 RPM to create a homogeneous mixture of fine particles. In-situ densification studies were performed to determine optimum firing conditions for densification. An analogous procedure was used to fabricate PLZT powders for dielectrics with either relaxor or field enforced AFE to FE characteristics. While titania films withstood fields of 600 kV/cm or 3000 volts, the PLZT materials withstood fields in excess of 200 kV/cm. The overall energy densities of the PLZT thick films were greater than those of the titania films due to their larger dielectric constants. We down selected the PLZT relaxor composition for further development over the AFE to FE phase

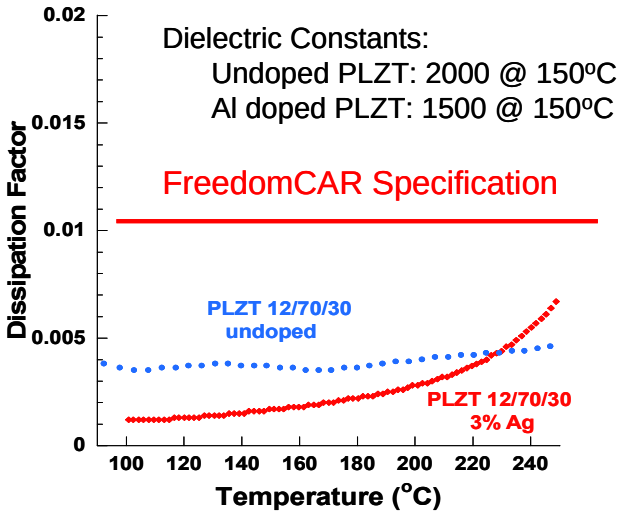

Figure 4. High Temperature Dielectric Properties of SNL ASD Chem-Prep PLZT Dielectric

transition material due to less variation in dielectric properties over the -40°C to 150°C temperature range. The excellent high temperature dielectric properties of the relaxor composition with and with out silver oxide additions are shown in Figure 4. A very low dissipation factor of 0.003 and a dielectric constant of 2000 were measured at 150°C for the undoped material. The PLZT dielectric with 3% Ag addition also exhibits very low loss at high temperature and has a dielectric constant of 1500 at 150 °C. Both materials have dissipation factors that are less than the 0.01 dissipation factor FreedomCAR requirement. Unlike SNL PLZT, state of the art barium titanate materials do not meet the FreedomCAR standards for loss with measured values in the range of 0.015. The low dissipation factors measured at high temperatures for the chem-prep PLZT thick films indicates that ripple current handling capability should be very good.

Sandia National Laboratories initiated technical efforts with Honeywell FM&T in Kansas City to fabricate multilayer chem-prep PLZT capacitors for eventual evaluation by engineers associated with the DOE FreedomCAR program. SNL and HW worked together to solve process issues for tape rheology, pyrolysis treatment, firing procedures and delamination. Multilayer chem-prep PLZT capacitors were successfully fabricated (Figure 5) that exhibited nominal 0.2 μF capacitance at low voltage (1 volt ac rms). During FY06, several technical accomplishments enabled chem-prep PLZT MLC fabrication. First, chem-prep PLZT powders were synthesized in sufficient quantities - approximately 6 kilograms – for MLC development by SNL and delivered to HWFM&T. Second, high quality tape cast rheology was developed by HWFM&T for research scale tape casting and then the rheology was modified such that high quality tapes were produced using the larger prototype development tape caster at HWFM&T.

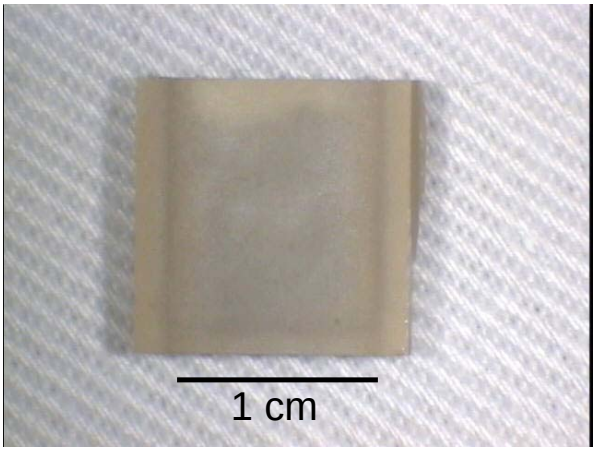

Figure 5. SNL/HW 20 Layer Chem-Prep Multilayer Capacitor

Third, pyrolysis and sintering procedures were developed and modified for chem-prep PLZT single layer tapes and multilayer capacitors. Further, proper lamination and electrode procedures were developed for these capacitors such that delamination and electrical shorting did not occur. A key development was determining the proper sintering procedures using weighted assemblies to prevent delamination of PLZT and electrode tapes during firing. SNL scientists are in the process of performing an extensive set of low voltage measurements. After these low voltage (less than 10 volt) measurements are completed, prototype capacitors will be evaluated for their high field properties. If these high voltage tests are successful, then these units will be delivered to ORNL for ripple current testing. During FY06, process improvements resulted in an increase of the low voltage measured capacitance of our chem-prep PLZT MLCs from 30% to 100% of the projected 0.2 μF capacitance value.

Conclusion

Discussions with DOE program managers, DOE consultants, automotive engineers and capacitor industry representatives in FY06 reinforced the importance of pursuing both high temperature polymer film and nanoceramic dielectric development. There is no clear consensus to date as to which technology, multilayer ceramic capacitor or multilayer polymer film capacitors, is best for achieving FreedomCAR program goals. In general, while polyfilm multilayer capacitors have advantages with regard to cost, the volumetric efficiency and the temperature handling capability of ceramic based multilayer capacitors is superior. The 2010 temperature specifications put forth by DOE and the EE TECH team of –40°C to 150°C will not be met by recently developed state of the art polyethylene dielectrics or state of the art barium titanate dielectrics. Thus development of high temperature polymer and nanoceramic dielectric materials is necessary to reduce volume and improve temperature performance of DC bus capacitor dielectrics to meet the FreedomCAR specifications. In FY06, SNL launched a multifaceted program of chemical synthesis, electrical characterization, film processing, and mechanical characterization for development of low volume, high temperature DC bus capacitors. Among the FY06 accomplishments was the development of a low cost norbornene synthesis procedure. Capacitors fabricated on aluminum coated silicon wafers exhibited low loss and had dielectric constants that exceeded that of state of the art polyphenylene sulfide. Further, SNL scientists synthesized high quality nanoceramic dielectric powders of PLZT and TiO_2. We used our recently developed direct write aerosol spray deposition process to fabricate high quality ceramic layers for the evaluation of three different nanoceramic materials. From extensive electrical testing of these materials at high temperatures, a PLZT composition was chosen for further development. Aerosol spray deposited layers of this material exhibited a dielectric constant of 2000 and a dissipation factor of 0.003 at 150°C. Unlike for $BaTiO_3$ based dielectrics, the dissipation factor at 150°C meets FreedomCAR specifications. Sandia scientists have collaborated extensively with Honeywell engineers to fabricate 20 layer multilayer chem-prep PLZT capacitors of the chosen PLZT composition. These capacitors exhibited capacitance values that were in agreement with the original engineering design values.

Future Directions

In FY 2007, we will develop the processes necessary for the development of lower sintering temperature nanoceramic dielectrics with no porosity. This development will permit integration with low temperature cofired ceramic technology and permit further reduction in capacitor size due to higher operating fields. High quality chem-prep PLZT nanoceramic multilayer capacitors will be developed for evaluation by SNL, ORNL and OEMs. For our polymer film development, we will develop synthesis procedures and fabricate Norbornene based polymer films. Further, a systematic study entailing the modification of Oxynorbornene and Norbornene polymers will be undertaken. There will be a go / no go decision for the continuation of the polymer film synthesis effort at the end of FY07. Specific tasks for our FY07 efforts are shown below.

Task 1: Chemical Synthesis: Develop new chemistry of low cost Norbornene polymer film dielectrics

Task 2: Fabricate and characterize spin deposited Norbornene films on Al coated Si and on Mylar coated Si wafers and characterize electrical and mechanical properties of these films.

If these film properties are acceptable to DOE program managers initiate scale up to 1 to 5 liter batches of solution (Hydrosize, Inc) and have polymer sheets fabricated of 500 foot length for fabricating wound polymer capacitors.

If the processing and electrical measurements of the SNL polyfilms are successful, then large-value (20 μF to 200 μF) capacitors will be fabricated by vendor(s) and evaluated by SNL, ORNL and auto manufacturers in simulated electric hybrid and fuel cell vehicle environments.

Task 3: Mechanically and Electrically Test New Polymer Films and Provide Report

Task 4: Develop Chem-Prep Nanoceramic Dielectrics with Lower Sintering Temperatures and No Porosity

Task 5: Fabricate High Quality Multilayer Capacitors for Electrical Testing (SNL, ORNL, OEMs) via Industrial Collaborations

Publications

1. Bruce Tuttle, David Williams, Jill Wheeler, Luke Brewer, Mark Rodriguez and T. Headley, "Characterization of PLZT Based Materials For High Energy Density Applications," Proceedings of the 12th Annual US-Japan Seminar, Annapolis, MD, November 8-11, 2005.

2. Duane Dimos, Nelson S. Bell, Joseph Cesarano III, Paul G. Clem, Kevin G. Ewsuk, Terry J. Garino, Bruce A. Tuttle, "Integration and Process Strategies for Ceramics in Advanced Microsystems, Proceedings First International Congress on Ceramics, Toronto, Canada, p. 385-389, June 25-29, 2006.

3. G. Samara, E. Venturini, B. Tuttle, D. Williams, M. Rodriguez, C. Frazer, R. Grubbs, L. Brewer and P. Hlava, "Ferroelectric and Antiferroelectric Properties and Behavior of La-Substituted Zr-Rich Pb($Zr_{1-x}Ti_xO_3$ (PLZT): Sandia Report SAND2-006-5002, September, 2006.

Patents

1. D. Wheeler and G. Jamison, "Novel Polymer Film Synthesis Routes of Voltage and Temperature Stable Dielectrics," October 5, 1999.
2. J. A. Voigt, D.L. Sipola, B.A. Tuttle, and M. T. Anderson, U.S. Patent No. 5,908,802, "Nonaqueous Solution Synthesis Process for Preparing Oxide Powders of Lead Zirconate Titanate and Related Materials, issued June 1, 1999.

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2. J. A. Voigt, D.L. Sipola, B.A. Tuttle, and M. T. Anderson, U.S. Patent No. 5,908,802, "Nonaqueous Solution Synthesis Process for Preparing Oxide Powders of Lead Zirconate Titanate and Related Materials," issued June 1, 1999.
3. B. Tuttle, "Materials Aspects of High Energy Density Dielectrics," University of Arizona Materials Science Seminar Series," March 27, 2006 (Invited Presentation).
4. B. Tuttle, D. Williams, G. Brennecka, J. Voigt, and D. Moore, "High Energy Density Capacitor Development," TCGX-10 Meeting Los Alamos, NM April 12, 2006.
5. D. Williams*, B. Tuttle, J. Voigt, D. Moore, M.Niehaus, and J.Cesarano, "Fabrication of Integrated Multilayer PLZT Capacitors," IEEE International Symposium on Applications of Ferroelectrics, Sunset Beach NC, July 28 – August 2, 2006.

4.7 Embedded Capacitors for (P)HEV Power Electronic Systems

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Objectives

This R&D program is developing high performance and economical DC bus capacitor technologies that will achieve APEEM specifications for (P)HEV power electronic systems. Current DC bus capacitors occupy a large fraction of the volume and weight of the inverter module, cannot tolerate temperatures >120°C, suffer from poor packaging and reliability, and deleterious failure modes. Traditional capacitor architectures with conventional dielectrics cannot adequately meet all of the performance goals for capacitance density, weight, volume, and cos. This requires a high permittivity, high temperature rated dielectric packaged in a high volumetric efficiency architecture with benign failure features.

Approach

Argonne National Laboratory's (Argonne) capacitor R&D program addresses the technology gap in an innovative manner. We are developing high performance, low cost capacitors embedded directly into the printed wire board (PWB). In these "embedded film-on-foil capacitors" a base-metal foil (Nickel or Copper) is coated with a high permittivity ferroelectric material, $(Pb,La)(Zr,Ti)O_3$ (abbreviated as PLZT). Ferroelectrics possess high permittivity, breakdown electric fields, and insulation resistance. They can withstand high temperatures such that high ripple currents can be tolerated at under hood temperatures. Use of base-metals and solution-based deposition techniques reduces the cost. An embedded capacitors approach significantly reduces component footprint, improves device performance, provides greater design flexibility, and offers an economic advantage. This technology will achieve the highest degree of packaging volumetric efficiency with lowest weight.

Our R&D efforts focus on examining the underpinning issues of film-on-foil embedded capacitor performance, developing low cost capacitor designs, establishing robust commercially and economically viable fabrication protocols, and transferring the technology to industry for manufacturing.

Major Accomplishments

- Refined $LaNiO_3$ (LNO) buffer layers to avoid deleterious effects of a parasitic low capacitance interfacial oxide layer.
- Developed a core technology of PLZT/ LNO/ Ni capacitor foils with dielectric constants > 1150 (1.5 $\mu F/cm^2$) and loss ≤ 0.06.
- Developed PLZT/LNO/Ni capacitor foils reaching 580 V with breakdown fields ≥ 1.2 MV/cm.

- Designed electrode architectures to achieve benign failure via self-clearing. In such a mode evolving faulted areas become removed from the larger structure and the capacitor continues to operate with a nearly undetectable loss in performance. This mechanism parallels fail-safe designs hailed in metallized polymer capacitors.
- Began an alliance with a PWB manufacturer and an automotive electronics company to embed our 'film-on-foil' dielectric elements and fabricate embedded (P)HEV capacitor prototypes.

Technical Discussion

The replacement of bulky inefficient discreet capacitors with capacitors embedded within the layers of a printed wire board is an innovative solution to high capacitance density and high volumetric efficiency capacitors. Embedded capacitors can be located directly underneath the active devices, greatly reducing component footprint and improving reliability. While this technology has primarily received attention for low voltage, high frequency decoupling capacitors, it can be extended to the higher voltages of (P)HEV systems. The vision of embedded DC bus capacitors is compelling and offers US automotive companies a substantial technological advantage over their foreign counterparts. The bulky coke-can-like banks of capacitors will be replaced instead by lengths of capacitors tucked flat and neatly underneath the active components and bus structure.

The key provision is the integration of high-k ferroelectric dielectric layers within the printed wire board. Since high temperature processing (~650°C) is required to obtain crystalline ferroelectric materials, direct deposition on the polymeric printed wire board is not possible. Instead, a pre-fabricated 'film-on-foil' approach is adopted whereby the ferroelectric is first deposited via chemical solution deposition (CSD) on a thin base metal foil, crystallized at high temperatures, and the coated foil subsequently embedded within the printed wire board.

A principal concern in the fabrication of 'film-on-foil' capacitors is eliminating the deleterious effects of a low-k parasitic oxide at the metal-ferroelectric interface. This would act as a series capacitor and reduce the overall capacitance. To negate the influence of the interfacial oxide two approaches have been pursued: 1- A conductive oxide buffer layer is interposed between the ferroelectric and the metal foil. The buffer layer acts as the bottom electrode and any secondary oxide that may form below it at the metal interface is inconsequential to the parallel plate capacitor. 2- Crystallizing the ferroelectric in a controlled reduced pO_2 environment such that formation of an interfacial oxide is prevented, yet the oxide dielectric is not decomposed.

1-PLZT/LNO/Ni Capacitors

We have developed a core technology for CSD PLZT on Ni film-on-foil capacitors with $LaNiO_3$ [LNO] buffer layers. CSD solutions were synthesized at Argonne and the films deposited by spin coating. All annealing and pyrolosis were done in air and repeated to build up layers of sufficient thickness.

Even a single layer of LNO (~0.15 microns) is sufficient to obviate the parasitic influence of any interfacial NiO formation (Figure 1). LNO film metrology exerts a pronounced influence on dielectric loss and breakdown strength. Three layers of LNO are required to completely cover and ameliorate the roughness of the Ni substrate. The planarizing influence of the LNO layer is highlighted in the cross-sectional SEM image shown in Figure 2. Besides obviating any NiO formation along the Ni interface, the LNO provides a smooth interface for nucleation and growth of dense PLZT. These PLZT/LNO/Ni capacitors achieved capacitance densities of 1.5 microfarads/cm^2, nearly equivalent to that obtained using inert platinized Si substrates. The smooth interfaces and dense microstructure both contribute to high breakdown strengths.

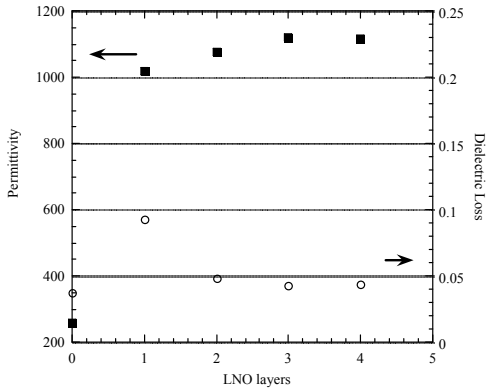

Figure 1. Dielectric properties of a PLZT film on LNO buffer layers of various number.

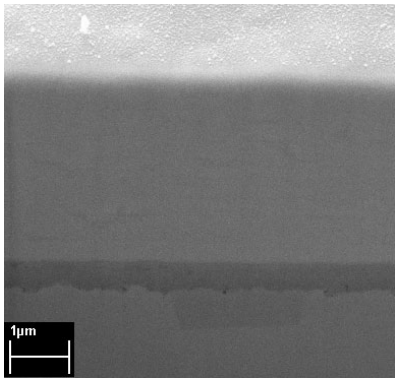

Figure 2. Cross sectional SEM micrograph of a PLZT/LNO/Ni film-on-foil heterostructure.

2-PLZT/Cu Capacitors

Cu is the primary material for PWB interconnects and metallization. We have initiated development of PLZT on bare Cu foils. Here a controlled reduced pO_2 environment is used to prevent formation of a parasitic interfacial oxide layer. The pO_2 must be low enough to prevent oxidation of the Cu-PLZT interface, yet not too low to induce decomposition of the PLZT oxide chemistry. Thermodynamic models aid in determining the appropriate pO_2 for the heating, crystallization, and cooling cycles.

Graceful Failure

We have developed film-on-foil capacitors that exhibit graceful failure – a gradual loss in capacitance upon localized breakdown events. Following a breakdown occurrence the capacitor continues to function and is only considered to have failed at such time that a defined leakage current or dielectric loss is reached.

At sufficiently high voltages, dielectric breakdown occurs at a discrete faulted area. This discharges the stored energy of the dielectric in that localized spot. In a matter of microseconds the discharge heats the immediate area, which physically "clears" away the dielectric from the defect site, and vaporizes the

metal top electrode in a small region surrounding the defect. By this process the breakdown site becomes electrically isolated and removed from the remainder of the capacitor structure. The capacitor continues to operate to even higher voltages. Self-clearing capacitors can sustain many breakdown events during their lifetime and can tolerate higher voltages. A small loss in capacitance is observed only after several breakdown/clearing events occur. Indeed, it usually takes hundred to thousands of such clearings to cause a few percent loss in capacitance. In such a manner, instead of shorting, the capacitor effectively "self-heals", and failure occurs gracefully. Such self-clearing failure modes are the same as those in metallized polymer capacitors

Prototype Development

We have demonstrated proof-of-concept film-on-foil capacitors. To proceed towards the next step of prototype embedded capacitors we have begun an alliance with Delphi Electronics and Safety, a leading automotive electronics supplier, and Diversified Systems, Inc., a PWB manufacturer. Together with these partners we will begin to develop technologies for integration of the film-on-foils into PWB fabrication. This will include embedding, imaging and etching, and interconnects and terminations. Novel PWB circuit designs will be conceived to maximize the capacitance and voltage in as small a volume. The embedded capacitors will be assembled and analyzed under (P)HEV inverter conditions.

Conclusion

We have developed a core technology for high capacitance density, high breakdown strength film-on-foil capacitors exhibiting graceful failure. PLZT film-on-foil capacitors have been fabricated with LNO buffer layers atop the Ni foils allowing the capacitors to be processed in air. Additionally, the LNO ameliorates the roughness of the Ni foil and provides a smooth interface for the PLZT films, resulting in higher breakdown strengths. Low pO_2 processing will be used to fabricate PLZT capacitor on Cu foils without the need for a buffer layer. Top electrode metallization design enables self-clearing of faults and graceful failure. This film-on-foil technology will be used to fabricate (P)HEV embedded DC bus capacitors with significant size and weight reduction, and improved performance and reliability.

Future Directions

The R&D achieved thus far sets the stage for developing prototype PWBs with embedded (P)HEV capacitors. This will require refinement of our technology and alignment with PWB fabrication routines. An ultrasonic aerosol coater will be used to fabricate PLZT dielectric films on large area Cu foil sheets. Robust processing condition will be developed to crystallize the film without formation of a parasitic interfacial capacitance. We will evaluate the high voltage and high temperature behavior of the ferroelectric film-on-foils with a perspective on reliability. We will investigate the microstructural aspects of dielectric breakdown and degradation and tailor devices based on those findings.

These film-on-foil sheets will be integrated into a PWB manufacturing process and embedded into the boards. Working with our alliance partners we will address the challenges posed by embedding, imaging the inner-layers, metallization, and circuit design. Prototype embedded capacitors will be evaluated for device performance and benchmark against APEEM goals. These initial prototypes will be evaluated by ORNL as well.

Publications

"PLZT Film-on-Foil Capacitors for Embedded Passives", D. Y. Kaufman, S. Saha, and K. Uprety, Proceedings of the 12th US-Japan Seminar on Dielectric and Piezoelectric Ceramics, November 2005, Annapolis, MD, pp. 305-308.

"Dielectric Performance of PLZT Film-on-Foil Capacitors for Embedded Passives", S. Saha and D.Y. Kaufman, in preparation.

Patents

"Ceramic Capacitor Exhibiting Graceful Failure by Self-Clearing", D.Y. Kaufman and S. Saha, U.S. Patent 7,099,141.

4.8 Glass Ceramic Dielectrics for DC Bus Capacitors

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Objectives

Power converters play a major role by converting energy stored in electrochemical batteries and fuel cells from direct current (DC) into alternating current (AC) for electric and hybrid vehicles. The conversion from DC into AC is not ideal; however, and the operation of a typical switch mode inverter leads to alternating currents on the DC bus at harmonics associated with the switching frequency. DC bus capacitors are required to reduce ripple current. The overall goal of this program is to reduce the cost, volume, and weight of power electronic inverter modules by focusing research efforts on capacitor components and dielectric materials for capacitors

Targets

Recently, U.S. capacitor manufacturers are focusing on high voltage high power capacitors. These companies see increased demand from the medical, telecommunication, and automotive industries for high voltage capacitors. Major manufacturers include: AVX, Kemet, Taiyo Yuden, Murata, TDK and EPCOS. The comparison of Multilayer Ceramic Capacitors (MLCCs) with EE tech team specifications is shown in Figure 1.

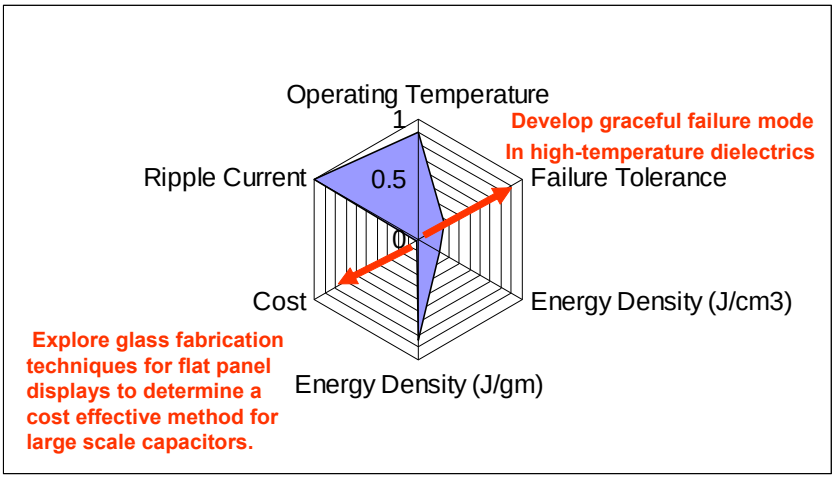

Figure 1: Comparison of MLCC Capacitor Parameters with DOE FreedomCAR specifications.

As shown in Figure 1, the ripple current and operating temperature specifications are close to meeting the Department of Energy inverter specifications; however, failure tolerance, energy density and cost targets are substantially below what is required for hybrid vehicles. The multilayer ceramic capacitor temperature specification is generally limited by the dependence of dielectric constant on temperature. One of the major drawbacks of MLCCs is the failure mode, which often results in a short circuit. Generally, the fabrication process involves deposition of thick electrode layers which melt and fuse together at high temperature. For this reason, the voltage ratings for MLCCs substantially below the failure voltage, which limits the energy density and increases cost. Future research and development activities need to focus on graceful failure mechanisms in multilayer ceramic capacitors. The ripple current capability of MLCCs, especially at high temperature, is superior to all of the other capacitor types.

Approach

In order to address the critical gaps shown in Figure 1, the major focus is on developing graceful failure mechanisms in glass capacitors and finding a large-scale manufacturing process for D.C bus capacitors. We have had several fruitful interactions with flat-panel display manufacturers, Corning and Schott, to determine if their materials are appropriate for capacitors. As shown in Figure 2, very large glass sheets can be manufactured for the high-volume low-cost consumer market.

Figure 2: Large area glass panels for flat panel displays were studied for high temperature D.C. bus capacitors for hybrid electric vehicles. This project explores the electrical properties of display glass at high temperatures.

The first task was to characterize dielectric material and capacitor performance (capacitance, loss, ESR) as a function of frequency, temperature, and voltage. These properties are directly related to reducing capacitor volume in the inverter.

Task two identified capacitor failure mechanisms in which capacitors fail in the “open mode” instead of a short circuit.

Task three focused on a low-cost glass process for manufacturing recrystallized glass capacitors which can operate at high temperatures in automotive applications. We found that recrystallized glass was difficult to synthesize in large areas and discontinued this line of research. Task three will not be discussed in this final report and there are several publications from this research (see Publications section of this report).

Prototype capacitor designs, based on flat panel display glass, are shown in Figure 3. The designs were given to Schott and Corning to determine if this geometry is feasible with current manufacturing processes. In addition, we have contacted AVX for more information on their glass capacitor manufacturing line.

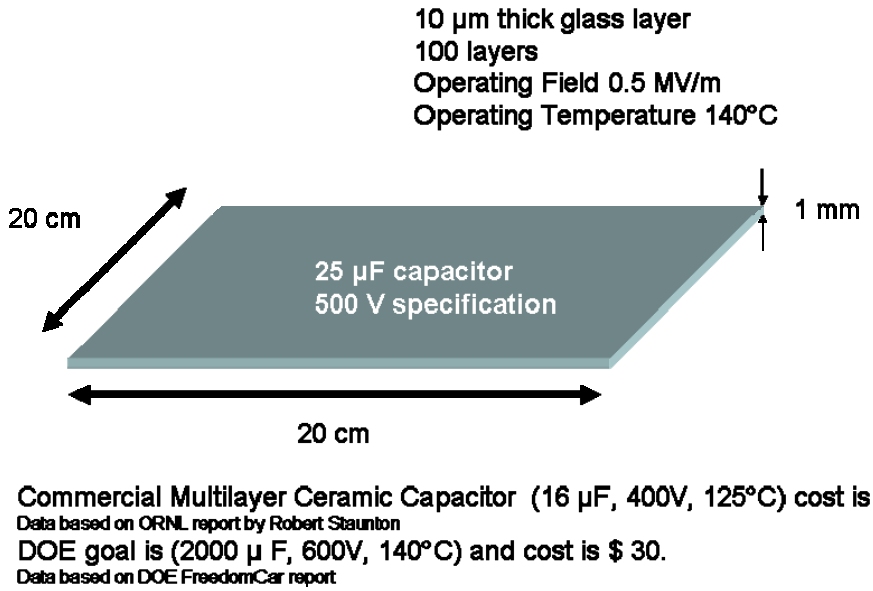

Figure 3: Prototype capacitor design based on flat panel display glass. Current commercial capacitor specifications are shown with DOE freedom car projections for capacitors in hybrid vehicles.

Major Accomplishments

In FY2005 we explored flat panel display glass from Corning. In FY2006 we evaluated flat panel display glass from Schott North America and the results are shown in Figures 4 and 5. As with the Corning glass samples, the dielectric properties of the flat panel display glass exceed the DOE freedom car goals up to temperatures of 350°C.

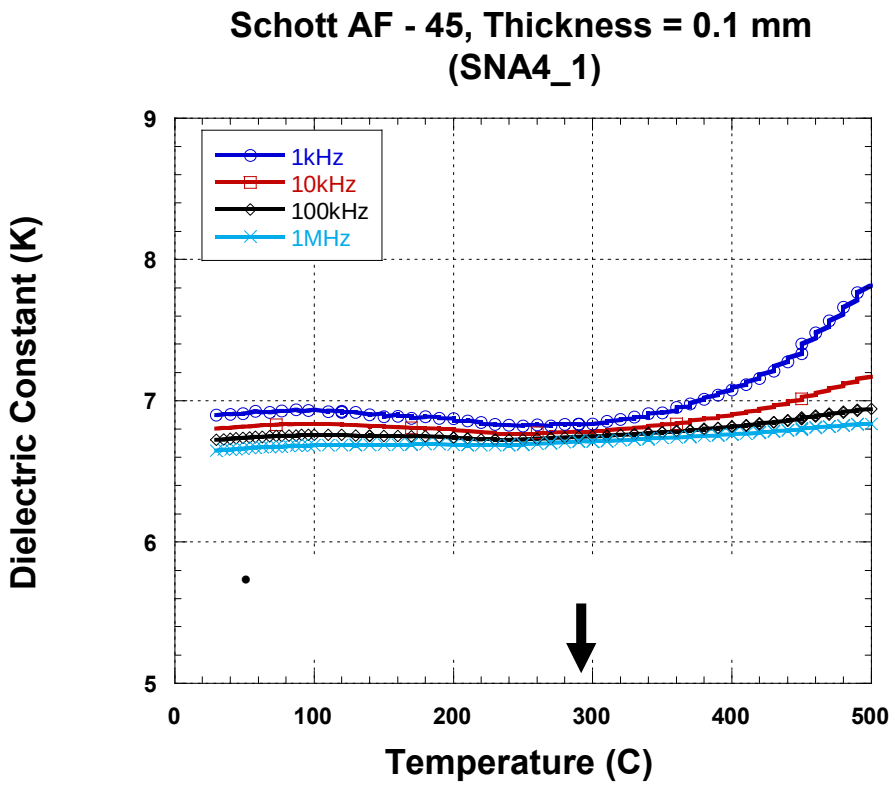

Figure 4: The dielectric constant of Schott glass as a function of temperature and frequency. The materials were characterized in the typical frequency range for a DC bus inverter (1 kHz to 1 MHz). The dielectric constant of 7 is triple that of conventional polymers, which will decrease the capacitor size by over 60%. In addition the permittivity is constant up to 400°C which far exceeds the DOE FreedomCAR goal of 140°C.

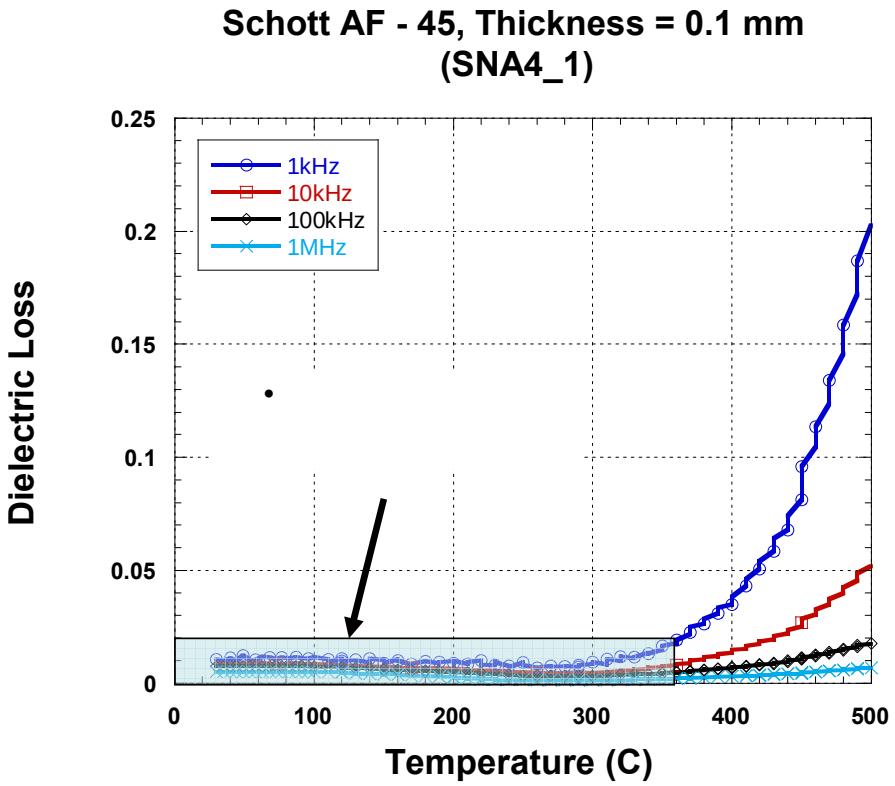

Figure 5: The dielectric loss of Schott AF glass as a function of temperature and frequency. The dielectric loss is within DOE Freedom Car specifications up to a temperature of 350°C.

Technical Discussion

Since DC bus capacitors store large amounts of energy and are positioned between the high voltage terminal and ground, the failure mechanism is a critical factor. A open circuit failure mode can be developed in capacitors with thin manganese oxide (MnO_2) electrodes. MnO_2 is semiconductor material having ~1 Ω·cm of resistivity and is commonly used in electrolytic capacitors. The benefit of using the semiconductor MnO_2 for electrode is realized because the higher temperature phase, Mn_2O_3 has a higher resitivity, an unusual property for metal oxides. If a current path occurs in the dielectric, then the current into that defect site is concentrated in a small area in MnO_2 and causes joule heating at the localized area. The MnO_2 phase is unstable at high temperature and converts to Mn_2O_3, which is an insulator (resititivity $\approx 10^5$ to 10^6 Ω·cm).

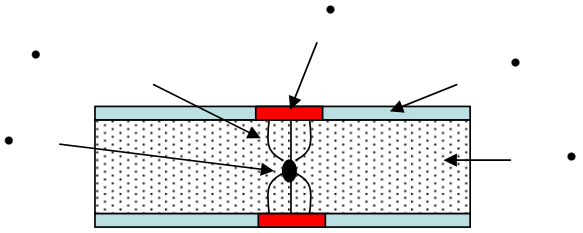

Figure 6: Open circuit formation by a phase transition of conducting MnO_2 to insulating Mn_2O_3 at a localized high temperature region.

Mn solution for spin coating on glass

Thin layers of MnO_2 were deposited on commercial flat panel display glass substrates by a sol-gel process. Two kind of precursors, manganese acetate ($Mn(C_2H_3O_2)_2{\cdot}4H_2O$) and manganese nitrate ($Mn(NO_3)_2{\cdot}xH_2O$) were dissolved in DI-water, acetic acid, 2-metoxyethanol (2MOE), and ethanol. Manganese nitrate was more soluble than manganese acetate in any of the solvent. However, the wetting of manganese nitrate solutions on glass substrates was not as good. Manganese acetate completely dissolved in acetic acid and 35% DI water mixed solution. A stable manganese solution was prepared with 0.35 M of concentration and its PH was 2.7. The solution nicely wet on glass surfaces and films were fabricated by spin coating. Film thicknesses of 300 nm were achieved. Figure 7 shows the process to deposit MnO_2 thin films on glass substrates.

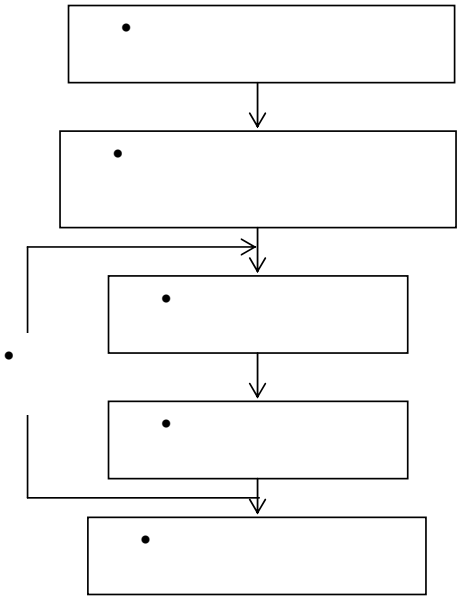

Figure 7: Processing flow chart for chemical deposition of MnO_2 thin films on glass.

Conclusion

This project has two major thrusts: 1) Explore commercial glass as a dielectric material for high temperature DC bus capacitors and 2) Synthesize electrodes that support an open failure mode. Capacitors made from glass will have the energy density, reliability, and the low-loss needed for high frequency power conditioning and filtering. This material exhibits high temperature capability (> 200°C) that will be required for next generation power converters based on silicon carbide (SiC). Thin manganese oxide electrodes were successfully deposited on commercial glass in order to establish graceful failure modes in DC bus capacitors.

Future Direction

Future research and development activities will further explore graceful failure modes in glass capacitors with thin MnO_2 electrodes. We will explore breakdown test of the glass capacitors under high voltage (up to 30kV). The failure behavior of glass capacitors with MnO_2 electrodes will be compared with that of glass capacitors with metal electrodes. Future research activities for DC bus capacitors will focus on polymer, glass, and ceramics, with high dielectric constant and high temperature operation. Current work at Sandia National Laboratories on hydroxylated polystyrene (PVOH) has demonstrated dielectric constants between 4.5 and 6 and excellent high temperature properties. Glass research at Penn State University has shown that high temperature operation can be achieved. Research at Argonne National Laboratory on $(Ba_xSr_{1-x})Ti\ O_3$ films has demonstrated the possibility of operating these films up to 150ºC. Critical Issues will be in achieving the energy density and temperature goals set forth by the EE Tech Team, and in the scale-up of the processes being developed under the current program.

Publications

M. Lanagan, J. Du, C. Wang, B. Jones, B. Rangarajan*, T. Perrotta, and T. Shrout, "Glass Ceramic Dielectrics," The 12th US-Japan Seminar on Dielectric and Piezoelectric Ceramics, Annapolis, Maryland, p. 401-404 (Nov 6-9, 2005).

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