Homoepitaxial and Heteroepitaxial Growth on Step-Free SiC Mesas

Philip G. Neudeck

NASA Glenn Research Center, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH 44135, USA

J. Anthony Powell

Sest, Inc., 21000 Brookpark Road, M.S. 77-1, Cleveland, OH 44135, USA

This article describes the initial discovery and development of new approaches to SiC homoepitaxial and heteroepitaxial growth. These approaches are based upon the previously unanticipated ability to effectively supress two-dimensional nucleation of 3C-SiC on large basal plane terraces that form between growth steps when epitaxy is carried out on 4H- and 6H-SiC nearly on-axis substrates. After subdividing the growth surface into mesa regions, pure stepflow homoeptixay with no terrace nucleation was then used to grow all existing surface steps off the edges of screw-dislocation-free mesas, leaving behind perfectly on-axis (0001) basal plane mesa surfaces completely free of atomic-scale steps. Step-free mesa surfaces as large as 0.4 mm x 0.4 mm were experimentally realized, with the yield and size of step-free mesas being initally limited by substrate screw dislocations. Continued epitaxial growth following step-free surface formation leads to the formation of thin lateral cantilevers that extend the step-free surface area from the top edge of the mesa sidewalls. By selecting a proper pre-growth mesa shape and crystallographic orientation, the rate of cantilever growth can be greatly enhanced in a web growth process that has been used to (1) enlarge step-free surface areas and (2) overgrow and laterally relocate micropipes and screw dislocations. A new growth process, named step-free surface heteroepitaxy, has been developed to achieve 3C-SiC films on 4H- and 6H-SiC substrate mesas completely free of double positioning boundary and stacking fault defects. The process is based upon the controlled terrace nucleation and lateral expansion of a single island of 3C-SiC across a step-free mesa surface. Experimental results indicate that substrate-epilayer lattice mismatch is at least partially relieved parallel to the interface without dislocations that undesirably thread through the thickness of the epilayer. These results should enable realization of improved SiC homojunction and heterojunction devices. In addition, these experiments offer important insights into the nature of polytypism during SiC crystal growth.

1. Introduction

Presently, SiC devices are implemented in homoepitaxial films grown on large 4H- and 6H-SiC wafers cut from large SiC boules and with surfaces polished 3° - 8° *off-axis* from the (0001) basal plane. This conventional approach has been largely unable to prevent many substrate crystal defects from propagating into SiC epilayers where they have been shown to harm the performance of the electronic devices. Furthermore, this approach has also not supported the implementation of potentially useful SiC heterojunction devices.

This article describes recent advancements in SiC epitaxial growth that begin to overcome the above shortcomings for arrays of mesas patterned into commercial nearly *on-axis* SiC wafers. These advancements are largely based upon properly controlling the SiC growth surface step structure to a degree not possible with off-axis wafer polish. First, we show that atomic-scale surface steps can be completely eliminated from 4H- and 6H-SiC mesas via on-axis homoepitaxial step-flow growth, forming (0001) basal plane surfaces (up to 0.4 mm x 0.4 mm) far larger than previously attained or thought possible. Step-free surface areas are then extended by growth of thin lateral cantilevers from the mesa tops. These lateral cantilevers enable substrate defects to be controllably reduced and relocated in homoepitaxial films in a manner not possible with conventional off-axis SiC growth. Finally, growth of vastly improved 3C-SiC was achieved on 4H-SiC and 6H-SiC mesas using a newly developed step-free surface heteroepitaxy process. The new growth developments described in this article should enable a variety of improved homojunction and heterojunction silicon carbide electronic devices.

2. Background

In order to appreciate the progress described in the remainder of this article, the relevant background and state of prior understanding of SiC epitaxial growth on conventional SiC wafers cut to within 10 degrees of the (0001) plane is briefly reviewed in this section. Herein, any wafer surface within 0.5° of the basal plane shall be called *on-axis*. The topic of SiC epitaxial growth and defects on non-SiC substrates (such as silicon) and on non-standard SiC surface orientations, such as $(1\bar{1}00)$, $(11\bar{2}0)$, and $(03\bar{3}8)$, is beyond the scope of this article [1,2].

There are many possible different crystal structures (i.e., polytypes) for SiC, each of which has its own set of semiconductor physical properties. As better described in [3], the crystal structure of each polytype is described by a repeated stacking sequence of tetrahedrally bonded Si-C bilayers. The atoms in any bilayer can take on one of three positions (labeled as "A", "B", or "C") relative to other bilayers in the lattice. The cross-sectional structure and associated bilayer stacking sequences of the most commonly produced polytypes are shown in Fig. 1. 3C-SiC is the only SiC polytype with a cubic crystal structure, and thus is the only SiC polytype with four geometrically equivalent <111> stacking directions. There are

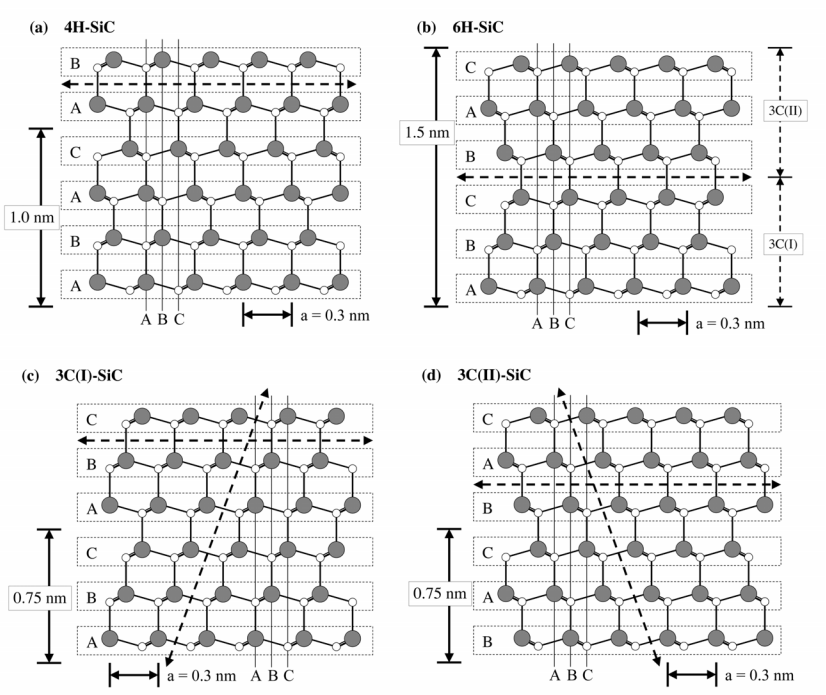

Fig. 1. Crystal structure of major SiC polytypes projected onto $(11\bar{2}0)$ plane. The bilayer stacking sequence, c-axis stacking repeat height, in-plane lattice parameter (a = 0.3 nm), and corresponding lateral positions of silicon (dark) atoms are illustrated. The (0001) basal plane for 4H-SiC and 6H-SiC and two of the four equivalent (111) planes for 3C-SiC are illustrated by the dashed lines.

two rotational variants of 3C-SiC, denoted as 3C(I) and 3C(II), that are related to each other by a 180° rotation about a stacking direction. The other SiC polytypes have only one stacking direction, the <0001> crystallographic c-axis. The closed packed planes normal to the stacking directions (i.e., {111} for 3C-SiC and (0001) for the other SiC polytypes) have the lowest defect propagation energies, and are thus most favorable for dislocation defect propagation [3,4].

Most SiC electronic devices realized to date are fabricated in well-controlled homoepitaxial layers grown on top of commercial 4H and 6H SiC wafers cut from large boules. To date, 3C-SiC crystals have suffered from excessive densities of extended crystallographic defects, which has largely rendered them unsuitable for the realization of beneficial semiconductor electronics compared to silicon or 4H- or 6H-SiC. The chemical vapor deposition technique is widely accepted as offering the most promise for well-controlled homoepilayer growth required for mass-production of most SiC electronic devices. There are many variations of SiC CVD epitaxial growth, and many rely on heating a 4H or 6H-SiC substrate to growth temperatures of around 1300 °C to 1600 °C in the presence of flowing silicon

(often SiH_4) and carbon (often C_3H_8) containing gas species in a carrier gas (often H_2) at various pressures near or below atmospheric pressure [5-10].

2.1 Role of Steps and Terraces in Epitaxial Growth of SiC

Control of crystal polytype and minimization of extended crystal defects (i.e., dislocations) during SiC epitaxial growth is necessary for the manufacture of reproducible SiC electronic devices. The microscopic structure and growth evolution of the SiC epitaxial growth surface has a large impact on polytype and quality of the grown SiC crystal.

Fig. 2 shows a simplistic microscopic depiction of a SiC growth surface, which is prepared by polishing the surface of a SiC wafer cut from a large boule to within 10° of parallel to the (0001) crystallographic basal plane. Due to the off-cut angle (i.e., tilt angle) of the surface polish, the growth surfaces have atomic scale steps separated by basal plane terraces, as schematically depicted in Fig. 2. Single crystal growth usually takes place when gas source molecules are chemisorbed onto the crystal growth surface in a weakly bound highly mobile state. The adsorbed molecules diffuse across the wafer surface until they reach a favorable bonding site, where they are then incorporated into the crystal. The favorable bonding site is often a step or defect on the crystal surface. Instead of growing in monolayers (e.g., a silicon monolayer growing followed by a carbon monolayer), the CVD epitaxial growth of SiC is observed to proceed via lateral extension of bilayers, or as multiple bilayers [9,11,12]. Step heights observed on all as-CVD-grown SiC surfaces are multiples of 0.25 nm, the height of a single Si-C bilayer. The tetrahedral bonding configuration of SiC supports lateral stepflow growth of bilayers across the crystallographic basal plane during CVD growth. The tetrahedral bonding of SiC is such that the step edge has a higher bond density available to facilitate reactant incorporation into the crystal (i.e., growth) than the top surface of a basal plane terrace.

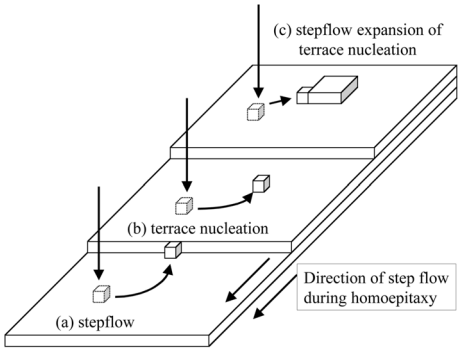

Fig. 2. Simplified schematic illustration of steps and adatoms on SiC epitaxial growth surface.

2.1.1 Stepflow Growth of Homoepitaxial 4H- and 6H-SiC

Presently, all SiC devices are implemented in homoepitaxial films of the 4H- and 6H-SiC polytypes grown on commercial SiC wafers with surfaces polished 3° to 8° off the (0001) basal plane. This off-axis polish provides a high density of steps so that step-controlled epitaxy can be used to grow 6H-SiC and 4H-SiC homoepilayers [5,7,13]. The high step density and small terrace width ensures migration of mobile surface-adsorbed growth adatoms to step edges where they incorporate into the crystal, as depicted on terrace (a) of Fig. 2. Thus, homoepitaxy of 4H-SiC or 6H-SiC is kinetically controlled growth, in that it relies on lateral bilayer expansion (i.e., lateral stepflow) from substrate step edges for growth and structural stacking replication.

2.1.2 Terrace Nucleation of Heteroepitaxial 3C-SiC

It is well known that 3C-SiC layers, usually with many extended crystal defects, can be nucleated and grown on 6H-SiC or 4H-SiC "on-axis" wafers, in which the wafer surface is polished to within a few tenths of a degree of being parallel to the crystallographic (0001) basal plane [7,9,13,14]. Such a low polish angle greatly increases the length of terraces (i.e., distance between steps) of the growth surface (Fig. 2). The nucleation of 3C-SiC occurs in epitaxial growth situations where growth reactants adsorbed onto the substrate surface two-dimensionally (2D) nucleate and incorporate into the crystal on top of basal plane terraces between the steps. Such nucleation, schematically depicted on terrace (b) of Fig. 2, occurs when adsorbed surface adatom diffusion length becomes small (i.e., surface adatom mobility is low) compared to average terrace length (i.e., distance between steps). The sides of terrace nucleated islands form additional steps (i.e., favorable adatom bonding sites) on the growth surface, so that islands can stepflow expand as depicted on terrace (c) of Fig. 2.

The fact that 2D terrace nucleation consistently produces the 3C polytype in conventional SiC CVD epitaxy processes suggests that the cubic bilayer stacking sequence is thermodynamically preferred for standard SiC epitaxial growth conditions. Some prior works, such as Fig. 3 of [7], suggest that either rotational variant of 3C-SiC (3C(I) or 3C(II)) could nucleate on the same (0001) 4H- or 6H-SiC basal plane terrace.

2.2 Extended Defects in SiC Epilayers

2.2.1 Defects in 4H- and 6H-SiC Homoepilayers

There are numerous extended crytallographic defects found in 4H- and 6H-SiC homoepitaxial layers. Many of these defects originate in the initial substrate and propagate into the epilayers during growth [10,15-18]. Axial screw dislocations (SD's) have the most impact on the homoepitaxial growth described in this article. Axial screw dislocations, both hollow core micropipes (with large dislocation

Burgers vectors) and closed-core screw dislocations (with small dislocation Burgers vectors), are examples of extended defects that originate in the substrate and propagate along the crystallographic c-axis through SiC epilayers to adversely affect many SiC electronic devices [10,17,19-22]. The self-replicating structural nature of screw dislocations assists the growth of many crystals, including 4H- and 6H-SiC c-axis boules, by providing a continual spiral pattern of new growth steps on the crystal surface [3,23,24]. Thus, screw dislocation growth spirals lead to the formation of hexagonal growth hillocks in 4H- and 6H-SiC homoepilayers grown on substrates with surface angles of less than a degree [3,9,11]. However, it is important to note that growth of conventional off-axis 4H- and 6H-SiC homoepilayers is dominated by steps supplied by the relatively high wafer miscut angle, so that steps provided by screw dislocations have only a small localized impact on the morphology (formation of a small surface pit) of standard SiC epifilms used for present-day SiC electronic devices [25].

2.2.2 Defects in 3C-SiC Heteroepilayers

As discussed above in Section 2.1.2, terrace nucleation and growth of 3C-SiC becomes much more probable when SiC epitaxy is carried out on low offcut angle (0001) 4H- or 6H-SiC substrates. The resulting 3C-SiC heteroepitaxial films have a (111) surface orientation, and were (prior to work reviewed in the present article) known to contain high densities of extended crystallographic defects that rendered them unsuitable for most electronic device applications [3,7]. The two major defects observed in previous 3C-SiC films on (0001) 4H- and 6H-SiC substrates are double-positioning boundary (DPB) defects and stacking fault (SF) defects [7,14,26].

As illustrated in Fig. 3a, DPB defects are essentially a boundary where opposite rotational variants of 3C-SiC meet. A DPB defect can be created when islands of the two different rotational variants of 3C-SiC (i.e., 3C(I) and 3C(II) of Fig. 1) nucleate at separate locations on a 4H- or 6H-SiC substrate and then laterally coalesce [7,13]. Stacking faults are planar defects that are essentially a disruption (or misalignment) of the same cubic stacking, as simplistically illustrated in Fig. 3b. Stacking fault defects propagate along the {111} planes. As noted previously, the

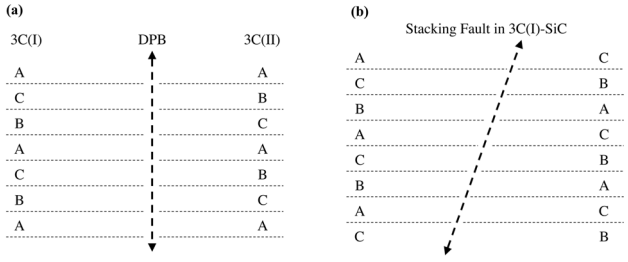

Fig. 3. Examples of discontinuous bilayer stacking associated with (a) double-positioning boundary (DPB) defect, and (b) stacking fault (SF) in 3C-SiC.

{111} planes in 3C-SiC and the (0001) plane in hexagonal SiC polytypes are the lowest energy fault planes, so that most movement of dislocations takes place along these crystal planes [3,4,27].

2.2.3 Role of Steps in Heteroepitaxial Film Defects

Several previous works have indicated that atomic-scale steps in the surface of a 6H-SiC or 4H-SiC substrate are one source of defects in heteroepitaxial films grown thereon. In the case of Group III-nitride (III-N) growth on hexagonal SiC substrates, recent studies have shown that many dislocations propagating from the substrate/epilayer interface originate at atomic-scale steps that are left behind on the substrate surface prior to epitaxial growth [28]. The step-related epitaxial film defects have been shown to arise even when III-N growth is carried out on well-ordered 6H-SiC terraces with c-axis unit repeat height (i.e., 1.5 nm for 6H-SiC) step heights defined by in-situ pregrowth etching [29,30]. Similar observations have also been reported for heteroepitaxial 3C-SiC films grown on 6H-SiC substrates [7,12,13]. Thus, these works allude to step-free SiC surfaces as being highly beneficial for realizing improved heteroepitaxial films.

2.3 Impact of Pre-Growth Surface Treatments on SiC Epitaxial Growth

Previous works have established surface defects and morphology as important factors in on-axis epitaxial SiC growth. In growth of 3C-SiC on as-grown 6H-SiC Lely substrates it was found that surface contamination played a role in the formation of DPB's in the 3C-SiC films [31]. Subsequently, both 6H-SiC and 3C-SiC epitaxial films were grown on nearly on-axis (about 0.2° tilt angle) commercial SiC wafers [14]. *It was found that, if the 6H-SiC substrate was subjected to a HCl etch at 1375 °C, homoepitaxial 6H films could be grown at 1450 °C over large areas (several mm across) without 3C-SiC inclusions*. It was also found that by intentionally damaging the substrate at a specific location, 3C-SiC films with reduced DPB density could be grown. It was concluded that the HCl etch at intermediate temperatures was very effective in removing surface damage due to wafer polishing and surface contamination. *A growth model was proposed wherein the 3C terrace nucleation was facilitated by dislocations and surface contamination, and not a result of insufficient surface mobility of precursor adatoms*.

In further growth studies, 1 mm square growth mesas were cut into the surface of the nearly on-axis 6H-SiC substrates [32,33]. Following etching and growth, some of these mesas yielded 3C-SiC heterofilms and some mesas yielded 6H-SiC homofilms. In most cases the 3C-SiC films nucleated at a corner of a mesa and then grew laterally across the mesa. It was suggested that in the early stages of growth a locally atomically flat 6H-SiC region forms at the uppermost atomic layer of the mesa, and that this region becomes a preferred site for terrace nucleation of 3C-SiC. Most 3C-SiC mesas films grown by this technique were free of DPB's with a reduced incidence of stacking faults. Diodes fabricated from these films exhibited the best blocking characteristics ever reported for 3C-SiC, but the

remaining defects nevertheless rendered them significantly inferior to the 6H-SiC diodes in other 1 mm square regions of the same wafer [34].

3. Step-Free Basal Plane Mesa Formation

3.1 Process

As discussed in Section 2.3, on-axis homoepitaxy of (0001) 4H- and 6H-SiC is possible when proper pre-growth surface treatment and epitaxial growth conditions are employed. In the absence of terrace nucleation of 3C-SiC, kinetic dominated homoepitaxial growth occurs from screw dislocation step spirals. By etching a pattern of deep trenches into an on-axis SiC wafer surface to form mesas prior to epitaxial growth, some surface regions without screw dislocations can be isolated from the kinetic growth steps produced by screw dislocations.

The process schematically depicted in Fig.4 has enabled the realization of large (up to 0.4 mm x 0.4 mm) (0001) basal plane surfaces completely free of bilayer steps on top of 4H- and 6H-SiC mesas [35,36]. Fig. 4a depicts the mesa cross-section and initial (due to unavoidable polish error) surface steps prior to epitaxial growth. Fig. 4b depicts the mesa after pure stepflow homoepitaxy grows all initial surface steps over to the edge of the mesa, leaving behind a perfectly flat (0001) basal plane top surface that is completely free of atomic steps (i.e., is a single large terrace). For simplicity, growth that occurs on the mesa sidewall and bottom of the trenches is not shown in Fig. 4b. The growth process, more fully described in [35], consisted of (1) an in-situ H_2 etch for 5 minutes at 1600 - 1650 °C at a pressure of 100 - 200 mbar followed by (2) growth using SiH_4 (2.7 cm^3/min) and C_3H_8 (0.3 cm^3/min) in H_2 (total flow 4400 cm^3/min) at 1600 - 1650 °C at a pressure of 200

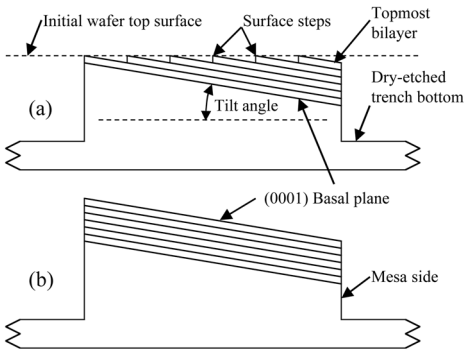

Fig. 4. Simplified cross-sectional depiction of process for realizing step-free SiC mesas. Bilayers and surface step structure of mesa (a) before growth and (b) following stepflow homoepitaxy without terrace nucleation or screw dislocation [35].

mbar. It should be noted that the uncoated graphite in the reactor supplies additional carbon to the growth environment, as we have observed some SiC growth in this reactor configuration even when C_3H_8 gas flows are reduced to zero. As discussed in Section 2.3, the in-situ etch crucially removes surface damage and contamination that could otherwise lead to undesired terrace nucleation of 3C-SiC during the initial stages of epitaxial growth. For 4H-SiC epilayers grown on 8° off-axis wafers in these reactor conditions, 2 μm/hour growth rates were obtained.

3.2 Results

Following growth, numerous mesas on over a dozen wafer samples have been characterized by differential interference contrast (DIC) optical microscopy and atomic force microscopy (AFM). The typical findings can be summarized by comparing two adjacent mesas shown in the DIC optical micrographs of Fig. 5. The left mesa of the Fig. 5 micrograph has an optically featureless top surface. A 50 μm x 50 μm AFM scan, one of 16 taken to span the entire top surface area of the left mesa, is shown in Fig. 6a [35]. Despite some particulate contamination, *no atomic steps were revealed in AFM scans of the entire left mesa*. In contrast, a hexagonal growth hillock due to a screw dislocation is readily apparent in the optical micrograph of the right Fig. 5 mesa. The AFM scan measured at the center of the hexagonal growth hillock, shown in Fig. 6b, reveals organized growth steps (0.5 nm and 1.0 nm high) emanating from an elementary screw dislocation (i.e., screw dislocation with Burgers vector equal to the 1.0 nm stacking repeat height of 4H-SiC). The interleaved step pattern of Fig. 6(b) evolves due to the anisotropic bonding of 4H-SiC bilayers as a function of crystallographic direction [9,11].

The primary factor limiting the size and yield of step-free surfaces produced in these experiments was the presence of screw dislocations in the substrates. As with the example mesas illustrated in Figs. 5 and 6, mesas with screw dislocations were identifiable using DIC optical microscopy due to the presence of hexagonal

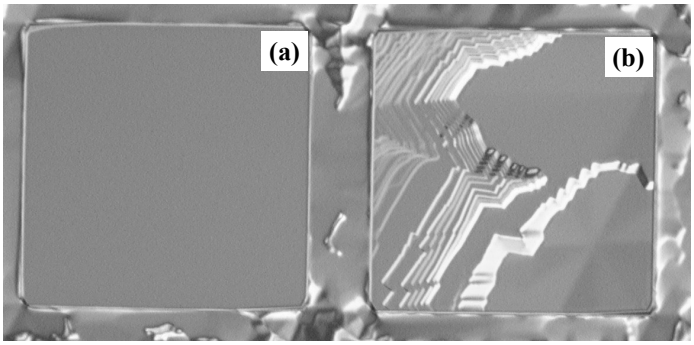

Fig. 5. DIC optical micrographs of two 200 μm x 200 μm mesas following homoepitaxial growth. Mesa (a) formed a step-free surface, while mesa (b) exhibits bunched steps and a hexagonal growth hillock from a screw dislocation in the lower right of the mesa [35].

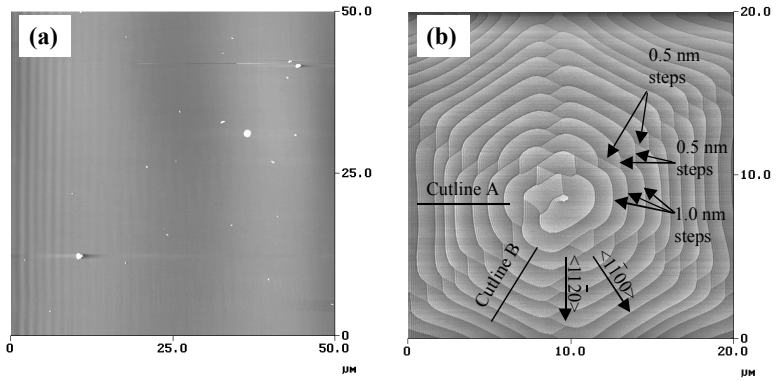

Fig. 6. AFM measurements recorded on mesas shown in Fig. 5. (a) Mesa (a) exhibiting no steps, and (b) peak of hexagonal hillock of mesa (b) [35].

growth hillocks. Over 90% of mesas that failed to become step-free following epitaxial growth contained at least one screw dislocation. Wafers with regions of relatively low substrate screw dislocation density enabled the realization of some 0.4 mm x 0.4 mm (the largest mesa size patterned) step-free surfaces. The mesa film polytypes were spatially mapped by both thermal oxidation color mapping and X-ray topography [26,37]. Over 90% of mesa tops in wafer central regions maintained the 4H-SiC polytype, exhibiting no evidence of 3C-SiC nucleation.

3.3 Impact on SiC Growth Understanding

The above experiments show that (0001) basal plane surfaces several hundred micrometers in dimension can be homoepitaxially grown on 4H- and 6H-SiC mesas without screw dislocations. These results could not have been achieved without complete suppression of 3C-SiC terrace nucleation on mesas during growth. *The suppression of 3C-SiC nucleation over tenth-millimeter scale terrace dimensions during SiC epitaxial growth had never previously been demonstrated,* especially at growth temperatures below 1700 °C. In fact, the above experimental results are quantitatively inconsistent with the previous experimental SiC growth nucleation studies at Kyoto University [7,38]. However, the Kyoto studies failed to employ important pre-growth etching processes discussed above in Section 2.3. *As discussed in Section 2.3, proper surface preparation, pre-growth etching, and growth procedures are crucial toward preventing terrace nucleation to obtain high-quality stepflow homoepitaxial film growth on low offcut angle (0001) surfaces*. Following publication of our recent studies described in this section, the Kyoto group has subsequently adopted and further investigated in-situ pre-growth etching to also obtain high quality homoepitaxial growth while suppressing terrace nucleation on low-offcut angle substrates [39].

The above experiments also show that once a step-free surface is established, homoepitaxial growth up the crystallographic c-axis direction completely ceases.

Therefore, the above experiments in forming step-free mesas are a confirmation that well-ordered homoepitaxial growth of hexagonal SiC polytypes in the crystallographic c-axis direction cannot be carried out without screw dislocations providing new growth steps. However, where screw dislocations are present, these experiments demonstrate that homoepitaxial growth of 4H- and 6H-SiC can be carried out at substrate surface miscut angles as low as zero degrees (i.e., perfectly on-axis) at 1600 - 1650 °C growth temperatures.

4. Homoepitaxial Growth of Thin SiC Cantilevers

4.1 Growth Process and Results

Continued epitaxial growth of a screw-dislocation-free mesa following achievement of a step-free surface leads to the formation of thin lateral cantilevers that extend the step-free surface area from the top edge of the mesa sidewalls [40,41]. By selecting a proper pre-growth mesa shape and crystallographic orientation, the rate of cantilever growth can be greatly enhanced in a web growth process that has been used to enlarge step-free surface areas and overgrow and laterally relocate micropipes and screw dislocations.

4.1.1 General Growth Properties

The cantilevered web growth process is briefly illustrated in Figs. 7-10. The specific experimental processes employed were identical to those stated in Section 3.1, except for the fact that more complex mesa shapes and longer epitaxial growth times were sometimes employed [40]. Fig. 7 shows a schematic cross-section of cantilever formation as a mesa (already rendered step-free as depicted in Fig. 4b) is subjected to additional growth time with terrace nucleation remaining completely suppressed. Growth adatoms, harvested by the step-free surface, migrate to the mesa edges where the more favorable sidewall bonding leads to incorporation into the crystal near the top of the mesa sidewall. *This leads to the growth of thin cantilevers, on the order of one to two micrometers in thickness, that seamlessly extend the step-free top surface area of a mesa*. As depicted in Fig. 7,

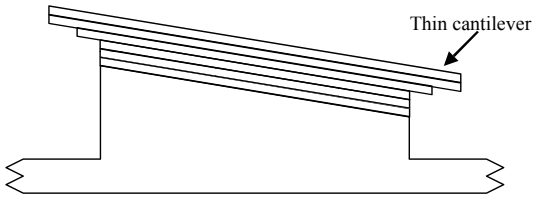

Fig. 7. Simplified cross-sectional illustration of cantilever growth at the top edges of a step-free mesa [40].

growth on the underside of the thin cantilevers is not uniform, partially due to mesa sidewall growth steps. It is important to note that almost no cantilevering is observed when the pre-growth mesas contain substrate screw dislocations, due to the previously discussed fact that screw dislocations provide steps for vertical (instead of lateral) growth of such mesas.

Figs. 8 and 9 illustrate that the lateral propagation of the step-free cantilevered surface is significantly affected by pre-growth mesa shape and crystallographic orientation. The highest lateral expansion rates of thin cantilevers were observed to occur at the inside concave corners of mesas. When complete spanning of the interiors of V's (Fig. 8) and other (Fig. 9) non-hollow mesa shapes by thin cantilevers was achieved, step-free surfaces with significantly enlarged surface area over the pre-growth mesa area were formed. As such growth loosely resembles the webbed feet of a duck, we refer to such interior-corner enhanced cantilevered growth as *cantilevered web growth*. The thin cantilevers exhibit $\{1\bar{1}00\}$ growth facet formation typical of hexagonal polytype SiC crystals. Some lateral enlargement of the mesa support structure takes place during the web growth process. Non-uniform underside growth is evident in the interference fringes seen in the cantilevered regions shown in the Figs. 8 and 9 optical micrographs.

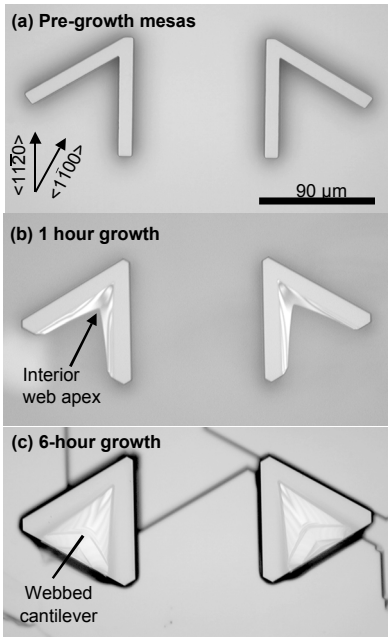

Fig. 8. Optical micrographs illustrating thin webbed cantilever formation on a V-shaped pre-growth mesa [40].

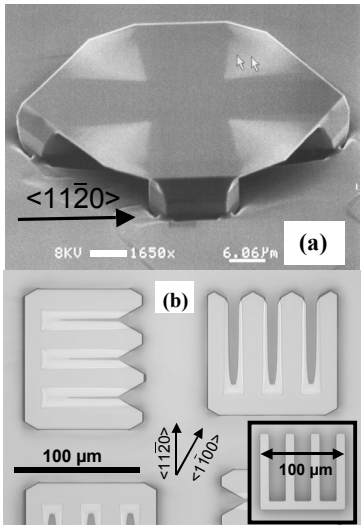

Fig. 9. Thin lateral cantilevers grown from (a) plus-shaped pre-growth mesa and (b) comb-shaped (inset) pre-growth mesas [40].

4.1.2 Cantilever Coalescence

It is important to note that when thin cantilevers from separated pre-growth mesa shapes (such as side-by-side rectangles) converged during growth, imperfect coalescence was almost always observed [40]. In order for a step-free surface to be realized following growth, mesas must have continuous top surface shapes that (like the V-shape of Fig. 8a) promote a progressive zippering of thin cantilevers from opposite arms. Using a much larger multi-armed pre-growth mesa shape that promoted zipper-like cantilever coalescence, webbed surfaces as large as 1 x 10^{-3} cm^2 were achieved, representing a more than 4-fold enlargement from pre-growth mesa surface area. As discussed below in Section 4.1.4 and in [42], dislocations were sometimes observed to form when cantilevers from the same mesa shape coalesced down to a point from more than two sides.

4.1.3 Dislocation Reduction Properties

Because the crystal structure of the thin cantilevers is established laterally from the mesa sidewalls, *cantilevered films can successfully overgrow substrate regions with dislocations, including axial screw dislocations*. Detailed analysis of cantilevered web films formed directly over axial screw dislocations show that these defects are completely absent from the cantilevered material [40,41]. For example, the webbing of the rightside mesa of Fig. 8c resides directly over a micropipe (screw dislocation), yet its surface was measured by AFM to be completely free of any atomic steps (in stark contrast to the screw dislocation steps shown in Fig. 6b). In addition, recent defect-preferential etching studies (using molten potassium hydroxide) of thin cantilevered webs failed to reveal any etch pits in properly coalesced web film regions, despite the fact that hexagonal etch pits due to non-screw dislocations were observed in adjoining pre-growth mesa regions [42].

4.1.4 Lateral Relocation of Screw Dislocations

In contrast to open pre-growth mesa surface shapes (such as the V-shape of Fig. 8a), homoepitaxial web growth can also be applied to mesa surface shapes that form enclosed hollow geometries. An example of an enclosed hollow pre-growth mesa geometry is shown in the upper right inset of Fig. 10, wherein the raised pre-growth mesa surface forms six triangular hollow trench regions in the interior [42]. By carrying out web growth on such a structure until webbed cantilevers coalesce in the middle of each triangular hollow region forming a complete roof, substrate screw dislocations that reside within each hollow region can be laterally relocated and combined to the central point of final cantilevered film coalescence. Fig. 10 shows an optical micrograph of a mesa following complete webbed cantilever coalescence. Most of the optical features in the webbed regions arise from non-uniform growth on the undersides of the cantilevers [40]. AFM measurements revealed that three elementary screw dislocation growth spirals, each shown in AFM insets of Fig. 10, formed in the film roof at three respective points of film coalescence. For reasons that are not yet understood, these growth spirals lack the

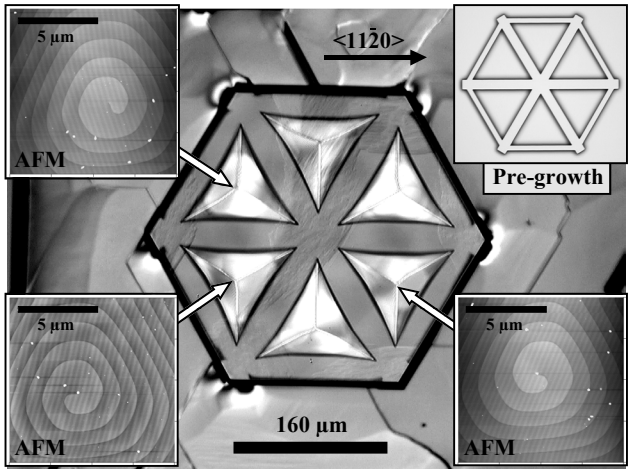

Fig. 10. Optical micrograph of spoked hexagonal mesa following web growth that completely overgrew six enclosed triangular trench regions. The AFM insets show the three screw dislocation growth spirals that formed exactly where roof closures occurred [42].

interleaving step pattern observed Fig. 6b. No other growth spirals were observed elsewhere on the mesa surface, even over the pre-growth mesa and the other three cantilever coalescence points.

The above results clearly demonstrate that coalesced web growth from hollow enclosed mesa shapes can produce screw dislocations in predictable lateral locations. The point of final coalescence can be designed into the pre-growth mesa pattern using a basic understanding of the cantilever growth and faceting behavior of SiC as a function of crystallographic direction. Following coalescence, the pre-placed screw dislocation can then provide steps for c-axis growth of on-axis homoepilayers on top of the mesa structure. Devices fabricated on top of such mesas can then be patterned to avoid the pre-placed screw dislocations.

4.2 Process Limitations and Further Optimization

It is important to note that uncontrolled material growth in the trench regions, (visible in Figs. 8-10) can rise up to interfere with laterally expanding cantilevers whose growth is confined along the (0001) basal plane. The merging of webs with trench growth actually limited the step-free yield of the largest webbed surfaces produced during initial experiments [40]. However, trench growth can be selectively prevented in a more optimized process using patterned growth masking techniques [43,44].

A more fundamental limitation of the homoepitaxial SiC web growth process is the fact that almost no cantilevering occurs when pre-growth mesas contain substrate screw dislocations, due to the previously discussed fact that screw dislocations provide steps for vertical growth of such mesas. Pre-growth mesa shapes

with long narrow fingers joined on one end (such as the comb shape of Fig. 9b) can be employed to maximize the webbing area while minimizing the chances that a pre-growth mesa will undesirably contain a screw dislocation. Such pre-growth mesa designs may require longer lateral cantilever extensions (i.e., growth of more material) in order to achieve a completely webbed structure. Higher temperature CVD epitaxial techniques should enable increased growth rate and surface adatom mobility favorable to realizing larger step-free webbed cantilevers [8]. The degree to which these goals can be achieved, coupled with the substrate screw dislocation density, will determine practical limits as to the size of step-free surfaces that can be realized using further optimizations of the SiC web growth process.

5. Step-Free Surface Heteroepitaxy of 3C-SiC

For many years researchers have attempted to grow 3C-SiC heteroepitaxial films of sufficient quality to better enable high-performance wide bandgap electronic devices. However, all previous efforts resulted in 3C-SiC with too many extended crystal defects to be useful for important electronic applications. In this section, we describe a step-free surface heteroepitaxy technique that has reproducibly grown high-quality 3C-SiC on step-free 4H- and 6H-SiC mesa surfaces [45,46].

5.1 Experimental Process Description

The step-free surface heteroepitaxy process starts by first etching mesas and growing step-free 4H- and 6H-SiC surfaces using the same procedures described above in Sections 3 and 4. Once homoepitaxial growth has achieved step-free mesas, heteroepitaxial nucleation and growth of 3C-SiC is then initiated in a controlled manner in-situ by lowering the growth temperature. As previously discussed in Section 2.1, the decreased growth temperature decreases surface adatom mobility, thereby increasing the chances (rate) of 2D terrace nucleation that initiates 3C-SiC growth on the (0001) basal plane surface. Temperature decreases to achieve nucleation were carried out with well-controlled ramps to avoid rapid thermal and chemical transient effects. The specifics of the 3C film nucleation and growth temperature ramps are given in Table 1.

Table 1. Experimental 3C-SiC Initial Nucleation Processes [46]

Sample	Temperature Profile (from 1620 °C)	SF Density
A	Ramp down 190 °C over 5 min.	$> 10^4/cm^2$
B	Ramp down 120 °C over 5 min.	0
C	Ramp down 190 °C over 60 min.	0

5.2 Experimental Results

Following epitaxial growth, films were characterized initially by DIC optical microscopy and AFM. Samples were dry thermally oxidized for 5 hours at 1150 °C to color-map polytype and reveal DPB and SF defects [26]. Detailed polytype mapping of some samples was carried out using X-ray topography. Substrate defects (e.g., screw dislocations) in the substrate were mapped using the back-reflection geometry, while forward-reflection geometry was used to spatially map 3C(I) and 3C(II) heteroepilayers [37]. High-resolution X-ray diffractometry (HRXRD) was employed to measure substrate and film lattice parameters [47,48]. A few 3C mesas were also studied by high-resolution cross-sectional transmission electron microscopy (HRXTEM) and molten potassium hydroxide (KOH) etching [45].

5.2.1 Defective 3C Films on Mesas with Screw Dislocations

Fig. 11 shows an optical micrograph typical of many 3C-SiC heterofilms that were grown on the top of 4H- or 6H-SiC substrate mesas *that contained a screw dislocation*. The defect-enhanced oxidation reveals an abundance of both DPB and SF defects that arose due to the fact that the 3C-SiC film was nucleated on a stepped 4H-SiC surface (due to growth steps provided by the screw dislocation), instead of on a step-free surface. The region of lighter oxide color denotes a region of 4H-SiC, and the peak of a hexagonal screw dislocation resides roughly at the center of this region. 3C-SiC, denoted by the darker (thicker) oxide color, surrounds the screw dislocation. As more thoroughly described in [37], a mixed polytype structure of this kind is anticipated when nucleation and growth of 3C-SiC competes with stepflow growth from screw dislocations.

The typical defect structure observed in the 3C-SiC surrounding the screw dislocation is extremely noteworthy. In addition to numerous stacking faults, DPB defects surround the screw dislocation, roughly corresponding to the $<11\bar{2}0>$ directions of the underlying 4H-SiC. This defect structure indicates that opposite rotations of 3C-SiC were nucleated roughly every 60° surrounding the screw dislocation. As described in [9,11], the stacking termination of step terraces interleaved around a 4H-SiC screw dislocation (such as shown in Fig. 6b) alternates between AB and AC every 60° surrounding the screw. Thus, the Fig. 11 defect structure supports a terrace nucleation model in which the initial 3C-SiC bilayers that nucleate on a terrace acquire the stacking that continues the local cubic stacking established by the topmost two bilayers [12,36,49]. For example, if terraces along cutline A of Fig. 6b ended with AB stacking (B being the topmost bilayer), 2D nucleation would yield 3C(I) with ABC stacking. Terrace nucleation along cutline B would then result in 3C(II). Thus, in the absence of kinetic "stepflow" polytype control, experimental evidence indicates that there is a strong thermodynamic driving force for new bilayers to continue the local cubic stacking of the immediately underlying bilayers.

5.2.2 3C-SiC Films on Step-Free Mesas

Consistent with the thermodynamic cubic stacking nucleation model discussed in the preceding section, DPB defects were experimentally eliminated from almost all 3C-SiC heterofilms nucleated on step-free 4H- and 6H-SiC mesas. Fig. 12 shows data typical of the screw-dislocation-free mesas on Sample B of Table 1. In contrast to the defects readily apparent in Fig. 11, the Fig. 12 optical micrograph of the oxidized mesa reveals that *no DPB's and no SF's intersect the film surface. The HRXTEM from an SF-free mesa (on Sample C of Table 1) shown in Fig. 13 also indicates a structurally perfect 3C-SiC film* with no defects and no stacking disorder detected within the field of view. The lack of any stacking disorder throughout the thickness of the 3C-SiC film is consistent with the thermodynamic model for continuation of local cubic bilayer stacking in growing layers. The apparent 3C/4H interface was perfectly flat and atomically abrupt with no evidence of growth steps and/or dislocations. Spatial mapping of the sample by X-ray topography confirmed that only one phase of 3C-SiC (either variant I or variant II) was present on each screw-dislocation-free mesa, and that no other polytypes grew to a detectable extent [48]. Single Si-C bilayer height (0.25 nm) steps were observed on all 3C-SiC mesa films studied by AFM.

While the step-free surface successfully eliminated DPB defects, the SF content of 3C-SiC films varied greatly as a function of the heterogrowth initiation process [46]. The data of Table 1 indicates a correlation between the in-situ temperature rampdown parameters and the SF-content of the resulting 3C-SiC mesa films. In particular, 3C-SiC films that were nucleated by more rapid temperature decreases (such as Sample A of Table 1) exhibited 3C-SiC mesas with a high incidence of stacking fault defects. *In contrast, 3C-SiC films nucleated by more gradual tem-*

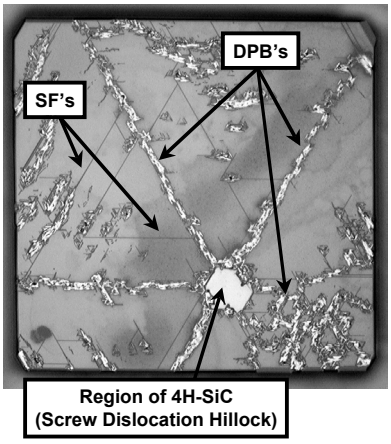

Fig. 11. Optical micrograph of 200 μm x 200 μm oxidized mesa showing defective 3C-SiC film (darker oxide) nucleated on 4H-SiC mesa *with steps from a screw dislocation.*

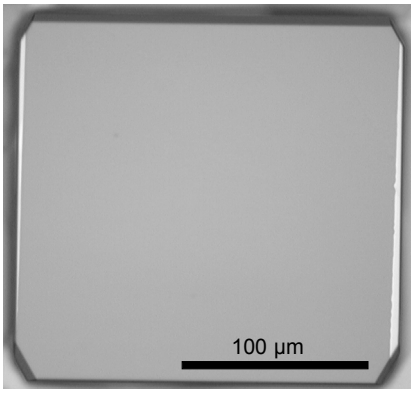

Fig. 12. Optical micrograph of oxidized 200 μm x 200 μm 3C-SiC heterofilm mesa nucleated on step-free 4H-SiC mesa. *No SF's and no DPB's are observed* [46].

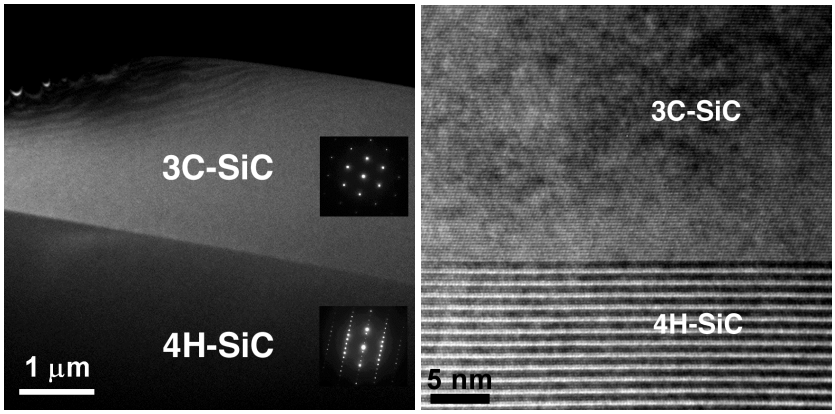

Fig. 13. HRXTEM of SF-free 3C-SiC heterofilm on 4H-SiC mesa (left) at low magnification and (right) high magnification. No defects and no stacking disorder were observed in the 3C heterofilm, and the 3C/4H interface was atomically flat with no steps observed [45].

perature decreases (such as Samples B and C of Table 1) exhibited high SF-free mesa yields, over 60% on screw dislocation free mesas. The 3C-SiC films subjected to low growth temperatures (i.e., high nucleation rates) after an initial thickness of 3C-SiC had been slowly nucleated (such as Sample C) did not exhibit SF's.

Defect preferential etching of 3C-SiC heterofilm mesas (using molten KOH) indicate the possible presence of additional dislocation defects in 3C-SiC films besides DPB's and SF's previously revealed by thermal oxidation [45]. Most 200 μm x 200 μm mesas free of DBP and SF defects typically exhibited 1 to 5 isolated triangular etch pits, which is comparable to (hexagonal-shaped) etch pit densities reported for commercial 4H- and 6H-SiC homoepilayers [15]. 3C-SiC mesas that contained SF and DPB defects typically exhibited at least an order of magnitude higher triangular etch pit density than SF-free mesas. These etch pits remain a subject for further investigation.

The 3C-SiC mesa heterofilms have also been studied by HRXRD [47,48]. The measurements distinctly resolve a 3C-SiC epilayer peak and a 4H-SiC substrate peak, definitively indicating a difference in lattice constants (both a and c parameters) for the two materials in the mesa heterostructure. The higher quality 3C-SiC films exhibited comparable FWHM as the 4H- or 6H-SiC substrate and no measurable rotational misorientation with the substrate lattice. In-plane substrate/epilayer lattice constant mismatch ($\Delta a/a$ range of 0.02% to 0.09%) was observed on all samples indicating that some in-plane lattice mismatch strain relief occurred in the 3C film. Meanwhile, the measured out-of-plane lattice constant difference $\Delta c/c$ was –0.13% to –0.15% for 3C on 4H and around –0.092% for 3C on 6H. The 3C-SiC films are not fully relaxed, as the HRXRD measured 3C lattice constants slightly deviated from those of the ideal cubic structure. In particular,

the measured 3C heterofilm lattice is slightly compressed along the in-plane direction and slightly elongated along the out-of-plane direction.

5.3 Heteroepitaxial Growth and Defect Formation Model

As discussed in Section 2.2, the probability (and rate) of 2D terrace nucleation of 3C-SiC increases as growth temperature decreases due to decreased adatom surface mobility. Once a 3C-SiC island nucleates, it then laterally expands via stepflow as depicted for terrace (c) of Fig. 2. Faster temperature drops increase the probability that multiple 3C-SiC islands will be nucleated on a relatively large step-free 4H/6H surface, as the resulting fast increase in nucleation rate leaves less time for new islands to enlarge via stepflow before additional islands nucleate elsewhere on the surface. In contrast, more gradual temperature drops provide more time for stepflow expansion of an initial island before other islands are nucleated on the step-free 4H/6H surface.

Based upon the above, we have hypothesized that the more gradual nucleation temperature ramps permit 3C-SiC heteroepitaxial growth to initiate from a single 3C-SiC island, which subsequently expands laterally via stepflow to cover the entire 4H (or 6H) mesa before nucleation of a second 3C-SiC island can occur elsewhere on the 4H (or 6H) mesa surface [46,49]. This growth model conversely suggests that stacking faults arise when multiple 3C islands terrace nucleate on a single mesa, laterally expand (via stepflow) across the step-free hexagonal-SiC growth surface, and coalesce in a defective manner. Coalescence-related stacking faults have been previously observed in other heteroepitaxial material systems [50,51]. However, after an initial thickness of 3C-SiC has been grown via low (i.e., single-island) terrace nucleation conditions, the film quality (i.e., SF-density) does not degrade when the temperature is lowered to increase terrace nucleation probability (such as Sample C of Table 1). Therefore, the experimental results indicate that a key mechanism promoting stacking fault formation is only present when the initial bilayers of the 3C-SiC heterofilm are grown. We have also proposed that a possible driving force for the defective 3C island coalescence is strain, which is largest at the substrate/film heterointerface, and/or strain relief effects that arise from in-plane lattice mismatch between the 3C-SiC film and the step-free 4H (or 6H) mesa [46,49].

6. Summary and Future Directions

6.1 Summary of New Results and Understanding

The work reviewed in this article demonstrates that device-sized step-free surfaces can be homoepitaxially grown on the hexagonal polytypes of SiC. Growth of such surfaces was accomplished on trench-isolated screw-dislocation-free mesa regions of nearly on-axis wafers by carrying out stepflow homoepitaxial growth with 2D

nucleation completely suppressed. The complete suppression of terrace nucleation across terrace widths of hundreds of micrometers had never been demonstrated in SiC prior to this work. The fact that c-axis growth became completely arrested (following step-free surface formation) on screw-dislocation free mesas confirms that these defects are necessary stepsources for c-axis growth of hexagonal SiC polytypes.

Continued homoepitaxial growth on 4H- or 6H-SiC step-free mesas (with terrace nucleation still supressed) resulted in evolution of thin lateral cantilevers emanating from mesa tops that seamlessly extended the step-free surface area. The rate of cantilever expansion was observed to depend upon pre-growth mesa shape and crystallographic orientation. The highest cantilever extension rates were observed at the inside corners of concave pre-growth mesa shapes, leading to a process we have named cantilevered web-growth. Thin webbed cantilevers demonstrated the ability to successfully enlarge the step-free surface area directly over micropipes and closed-core screw dislocations. Defect-preferential molten KOH etching failed to reveal hexagonal etch pits on properly coalesced webbed cantilevers. Substrate screw dislocations enclosed by hollow pre-growth mesa shapes were laterally confined in the cantilever films to the point where cantilevers converged to form a complete roof over each hollow region. The screw dislocations with lateral position determined by the final convergence points can then be used to provide new growth steps necessary for growth of an 4H- or 6H-SiC epitaxial layer with lower screw dislocation density than the substrate.

The step-free surface heteroepitaxy growth process has achieved 3C-SiC mesa films completely free of double positioning boundary and stacking fault defects. This process is based upon the initial 2D terrace nucleation and lateral expansion of a single island of 3C-SiC on the step-free (0001) 4H-SiC (or 6H-SiC) mesa surface. Our experimental results indicate that extremely high 3C-SiC film quality was achieved, despite the fact that substrate/film lattice mismatch stress was not fully relieved. The experiments also indicate that terrace-nucleated SiC bilayers will continue the local cubic stacking structure of the immediately underlying bilayer pair.

6.2 Major Material Issues for Further Study

The new fundamental SiC growth understanding gained in these initial studies naturally raise a variety of important follow-up questions for future investigation. For example, quantitative limits of terrace nucleation suppression have not yet been explored as a function of wider ranging growth conditions and larger mesa sizes. In addition, none of the growth processes described in this article have been carried out on carbon-face $(000\bar{1})$ wafers. The impact of intentional film doping (both n-type and p-type) on both step-free surface formation and subsequent 3C-SiC film growth must also be explored. Also, the durability of 3C-SiC films subjected to various processes (such as ion implantation and high temperature annealing) is also a major materials question remaining to be investigated.

6.3 Future Device Applications

The crystal growth processes described in this article lay a unique foundation for the experimental realization of a variety of novel prototype device structures. In addition to being an ideal surface upon which to construct atomic-scale nanostructures, the perfectly flat SiC surfaces should also enable better fundamental understanding of SiC interfaces and surfaces.

6.3.1 4H/6H-SiC Devices

The perfectly on-axis step-free 4H- and 6H-SiC surfaces are structurally and chemically different from the stepped surface structure of conventional off-axis SiC. The flat surfaces should enable the experimental formation and study of nearly ideal metal-semiconductor Schottky barriers with atomic smoothness and interfacial abruptness over the entire contact area. Such contacts are likely to exhibit less barrier inhomogeneity than those exhibited by off-axis SiC Schottky contacts. Similarly, it seems possible that higher quality inversion-channel MOSFET devices might be realized using such surfaces [52,53].

The lateral growth techniques described in Section 4 offer some interesting new structures and/or benefits to 4H- and 6H-SiC devices. The ability demonstrated in Section 4 to reduce and/or relocate dislocations in webbed films could improve the reproducibility, performance, and leakage properties of junctions used for switching or photodetection. In particular, small-area devices could be fabricated in etch-pit free regions of the crystal, and their electrical performance and reliability compared to devices in bulk crystal regions known to contain defects. The cantilevered geometry also makes it possible to implement lateral SiC device geometries with active areas free of substrate parasitics. In addition, the cantilevers may also be useful in the realization of new single-crystal 4H/6H microelectromechanical device structures, such as accelerometers and pressure sensors for harsh environment applications.

6.3.2 3C-SiC Devices

Almost all previous 3C-SiC electronic devices have been realized using inferior crystals with high densities of extended crystallographic defects. This has generally resulted in poor electrical characteristics of 3C-SiC diodes and transistors compared to similar devices implemented in silicon, 4H-SiC, and 6H-SiC. For example, experimental 3C-SiC pn junctions are unable to support high electric fields without excessive leakage through the crystallographic defects [34].

Now that device-sized regions of low-defect 3C-SiC can be realized (as described above in Section 5), the further exploration of potentially important electrical device benefits of 3C-SiC is warranted. For example, 3C-SiC MOSFET's have recently demonstrated much higher inversion channel mobilities than those demonstrated in 4H-SiC MOSFET's [54]. This mobility advantage is believed to arise from the fact that the lower 3C-SiC conduction band energy removes the high density of interface states known to exist close the conduction bands of 4H-

and 6H-SiC [55-57]. The reduction of interface states should enable a reduction in surface-related generation and recombination phenomenon known to affect bipolar junctions and MOS charge storage (i.e., non-volatile random access memories) and transfer (charge coupled) devices [58-62]. In addition, the oxide-semiconductor conduction band potential barrier is close to 0.8 eV higher for 3C-SiC than for 4H-SiC, which should reduce field-assisted carrier tunneling harmful to oxide reliability [55,63].

The wide 3.2 eV bandgap of 4H-SiC enables high breakdown field beneficial for high voltage power device off-state blocking properties. However, 4H-SiC bipolar power devices must overcome the associated higher built-in potential of the pn junction before high on-state current density is achieved, which leads to undesired on-state power losses. Therefore, even though the breakdown field of 3C-SiC is somewhat less than 4H-SiC, the lower (by nearly a volt) pn junction turn-on voltage (due to 2.3 eV bandgap) offers interesting bipolar power device design tradeoffs versus 4H-SiC bipolar devices, and far superior current density performance compared to silicon. Recently, stacking faults have been observed to degrade the operational properties of 4H-SiC bipolar devices [18]. In addition, thermal processing has also been shown to induce stacking faults into heavily doped 4H-SiC epilayers [64]. The faults that form have been shown to be localized transformations of hexagonal-stacked bilayers towards cubic stacking structure [64, 65]. By starting with a SiC crystal structure that is entirely cubic, this degradation mechanism might be absent from 3C-SiC bipolar device structures. A high quality 3C/4H-SiC heterojunction, such as the one shown in Fig. 13, should enable beneficial SiC/SiC heterojunction devices to be realized, including heterojunction bipolar transistors and high electron mobility field-effect transistors [66].

The 3C-SiC step-free surface heteroepitaxy process demonstrated in Section 5 should enable experimental exploration of all these potential benefits in small-area prototype device structures. If experimental studies validate sufficient electrical device benefits, further scale-up development of 3C-SiC crystal growth should be pursued.

6.3.3 III-N Growth and Devices

On-axis hexagonal SiC substrates are often used for the growth of heteroepitaxial Group III-nitride (III-N) devices used in short-wavelenght light emitting diodes, lasers, and heterojunction radio frequency transistors [67]. These devices typically contain numerous extended crystal defects that originate at the substrate/epilayer interface and harm the performance and reliability of III-N devices [28]. In particular, previous works indicate that many of these defects correspond to the locations of steps on the SiC growth surface, even in cases where pre-growth etching produces well-ordered surface steps [30]. By carrying out III-N growth on step-free SiC surfaces, interface-step-related defects are eliminated, which should result in some improvement in III-N film quality.

6.4 Conclusion

This article has described significant new understanding and approaches to SiC homoepitaxial and heteroepitaxial growth using on-axis (0001) 4H- and 6H-SiC mesa surfaces. These advancements demonstrate far better control of the SiC growth surface structure and epitaxial film defect structure than previous SiC growth approaches. The superior films should enable a variety of improved small-area devices to be demonstrated in the near future. With further upscaling and process improvements, the demonstrated growth principles may potentially displace conventionally-grown SiC materials in a variety of applications.

Acknowledgments

The authors are most grateful to the following people for their contributions to the works reviewed in this article: A. Trunek, D. Spry, G. Beheim, P. Abel, L. Matus, R. Hoffman, Jr., D. Larkin, E. Benevage, B. Osborn, J. Heisler, D. Androjna, L. Keys, R. Okojie, M. Mrdenovich, S. Elder, C. Blaha and G. Hunter at NASA Glenn Research Center; M. Dudley, X. Huang and W. Vetter at State University of New York at Stony Brook, M. Skowronski, T. Kuhr and J. Liu at Carnegie Mellon University. This work was primarily funded and carried out at NASA Glenn Research Center under the Aerospace Propulsion and Power Program.

References

[1] T. Kimoto, T. Yamamoto, Z. Y. Chen et al., in *Silicon Carbide and Related Materials 1999*, edited by C. H. Carter, Jr., R. P. Devaty, and G. S. Rohrer, Mat. Sci. Forum (Trans Tech Publications, Switzerland, 2000), vol. 338-342, p. 189.

[2] T. Kimoto, S. Nakazawa, K. Fujihira et al., in *Silicon Carbide and Related Materials 2001*, edited by S. Yoshida, S. Nishino, H. Harima et al., Mat. Sci. Forum (Trans Tech Publications, Switzerland, 2002), vol. 389-393, p. 165.

[3] J. A. Powell, P. Pirouz, and W. J. Choyke, in *Semiconductor Interfaces, Microstructures, and Devices: Properties and Applications*, edited by Zhe Chuan Feng (Institute of Physics Publishing, Bristol, United Kingdom, 1993), p. 257.

[4] M. H. Hong, A. V. Samant, and P. Pirouz, Philos. Mag. **80** (4), 919 (2000).

[5] J. A. Powell, D. J. Larkin, L. G. Matus et al., Appl. Phys. Lett. **56** (15), 1442 (1990).

[6] A. A. Burk, Jr. and L. B. Rowland, Phys. Status Solidi B **202** (1), 263 (1997).

[7] T. Kimoto, A. Itoh, and H. Matsunami, Phys. Status Solidi B **202** (1), 247 (1997).

[8] O. Kordina, C. Hallin, A. Henry et al., Phys. Status Solidi B **202** (1), 321 (1997).

[9] J. A. Powell and D. J. Larkin, Phys. Status Solidi B **202** (1), 529 (1997).

[10] A. R. Powell and L. B. Rowland, Proc. IEEE **90** (6), 942 (2002).

[11] J. A. Powell, D. J. Larkin, P. B. Abel et al., in *Silicon Carbide and Related Materials1995*, edited by S. Nakashima, H. Matsunami, S. Yoshida et al., IOP Conf. Series (Institute of Physics Publishing, Bristol, UK, 1996), no. 142, p. 77.

[12] S. Tyc, in *Silicon Carbide and Related Materials: Proceedings of the Fifth International Conference*, edited by M. Spencer, R. Devaty, J. Edmond et al., IOP Conf. Series (Institute of Physics Publishing, Bristol, United Kingdom, 1994), no. 137, p. 333.
[13] H. Matsunami, K. Shibahara, N. Kuroda et al., in *Amorphous and Crystalline Silicon Carbide*, edited by G. L. Harris and C. Y.-W. Yang, Springer Proc. Phys. (Springer-Verlag, Berlin, Heidelberg, 1989), vol. 34, p. 34.
[14] J. A. Powell, J. B. Petit, J. H. Edgar et al., Appl. Phys. Lett. **59** (3), 333 (1991).
[15] S. Ha, P. Mieszkowski, M. Skowronski et al., J. Cryst. Growth **244** (3-4), 257 (2002).
[16] S. Wang, M. Dudley, C. H. Carter, Jr. et al., in *Diamond, SiC and Nitride Wide Bandgap Semiconductors*, edited by C. H. Carter, Jr., G. Gildenblat, S. Nakamura et al., MRS Symp. Proc. (Materials Research Society, Pittsburgh, PA, 1994), vol. 339, p. 735.
[17] P. G. Neudeck, in *Silicon Carbide and Related Materials 1999*, edited by C. H. Carter, Jr., R. P. Devaty, and G. S. Rohrer, Mat. Sci. Forum (Trans Tech Publications, Switzerland, 2000), vol. 338-342, p. 469.
[18] H. Lendenmann, F. Dahlquist, J. P. Bergman et al., in *Silicon Carbide and Related Materials 2001*, edited by S. Yoshida, S. Nishino, H. Harima et al., Mat. Sci. Forum (Trans Tech Publications, Switzerland, 2002), vol. 389-393, p. 389.
[19] W. Si, M. Dudley, R. Glass et al., J. Electronic Materials **26** (3), 128 (1997).
[20] W. Si, M. Dudley, H. S. Kong et al., J. Electronic Materials **26** (3), 151 (1997).
[21] P. G. Neudeck and J. A. Powell, IEEE Electron Device Lett. **15** (2), 63 (1994).
[22] P. G. Neudeck, W. Huang, and M. Dudley, Solid-State Electron. **42** (12), 2157 (1998).
[23] J. Giocondi, G. Rohrer, M. Skowronski et al., J. Cryst. Growth **181** (4), 351 (1997).
[24] R. C. Glass, D. Henshall, V. F. Tsvetkov et al., Phys. Status Solidi B **202** (1), 149 (1997).
[25] P. G. Neudeck, M. A. Kuczmarski, M. Dudley et al., in *Wide-Bandgap Electronic Devices*, edited by R. J. Shul, F. Ren, M. Murakami et al., MRS Symp. Proc. (Materials Research Society, Warrandale, PA, 2000), vol. 622, p. T1.2.1.
[26] J. A. Powell, J. B. Petit, J. H. Edgar et al., Appl. Phys. Lett. **59** (2), 183 (1991).
[27] P. Pirouz, Solid State Phenomena **56**, 107 (1997).
[28] S. Tanaka, R. S. Kern, and R. F. Davis, Appl. Phys. Lett. **66** (1), 37 (1995).
[29] S. Nakamura, T. Kimoto, H. Matsunami et al., Appl. Phys. Lett. **76** (23), 3412 (2000).
[30] S. Yamada, J. Kato, S. Tanaka et al., presented at the Fall 2000 Materials Research Society Meeting, Boston, MA, 2000 (unpublished).
[31] J. A. Powell, D. J. Larkin, L. G. Matus et al., Appl. Phys. Lett. **56** (14), 1353 (1990).
[32] D. J. Larkin and J. A. Powell, U.S. Patent No. 5,363,800 (1994).
[33] J. A. Powell, J. B. Petit, L. G. Matus et al., in *Amorphous and Crystalline Silicon Carbide III*, edited by G. L. Harris, M. G. Spencer, and C. Y. Yang, Springer Proc. Phys. (Springer-Verlag, Berlin-Heidelberg, 1992), vol. 56, p. 313.
[34] P. G. Neudeck, D. J. Larkin, J. E. Starr et al., IEEE Trans. Electron Devices. **41** (5), 826 (1994).
[35] J. Powell, P. Neudeck, A. Trunek et al., Appl. Phys. Lett. **77** (10), 1449 (2000).
[36] J. A. Powell, D. J. Larkin, P. G. Neudeck, and L. G. Matus, U.S. Patent No. 5,915,194 (1999).
[37] M. Dudley, W. M. Vetter, and P. G. Neudeck, J. Cryst. Growth **240** (1-2), 22 (2002).
[38] T. Kimoto and H. Matsunami, J. Appl. Phys. **78** (5), 3132 (1995).
[39] S. Nakamura, T. Kimoto, and H. Matsunami, to appear in *Silicon Carbide and Related Materials 2002* Mat. Sci. Forum (Trans Tech Publications, Switzerland, 2003).

[40] P. G. Neudeck, J. A. Powell, G. M. Beheim et al., J. Appl. Phys. **92** (5), 2391 (2002).
[41] P. G. Neudeck, J. A. Powell, A. Trunek et al., in *Silicon Carbide and Related Materials 2001*, edited by S. Yoshida, S. Nishino, H. Harima et al., Mat. Sci. Forum (Trans Tech Publications, Switzerland, 2002), vol. 389-393, p. 251.
[42] P. G. Neudeck, D. J. Spry, A. J. Trunek et al., in *Silicon Carbide 2002--Materials, Processing and Devices*, edited by S.E. Saddow, D.J. Larkin, N.S. Saks et al., MRS Symp. Proc. (Materials Research Society, Warrendale, PA, 2003), vol. 742, p. K5.2.1.
[43] Y. Khlebnikov, I. Khlebnikov, M. Parker et al., J. Cryst. Growth **233**, 112 (2001).
[44] E. Eshun, C. Taylor, M. G. Spencer et al., in *Wide-Bandgap Semiconductors for High Power, High Frequency and High Temperature Applications - 1999*, edited by S. C. Binari, A. A. Burk, M. R. Melloch et al., MRS Symp. Proc. (Materials Research Society, Warrandale, PA, 1999), vol. 572, p. 173.
[45] P. G. Neudeck, J. A. Powell, D. J. Spry et al., to appear in *Silicon Carbide and Related Materials 2002*, Mat. Sci. Forum (Trans Tech Publications, Switzerland, 2003).
[46] P. G. Neudeck, J. A. Powell, A. J. Trunek et al., in *Silicon Carbide and Related Materials 2001*, edited by S. Yoshida, S. Nishino, H. Harima et al., Mat. Sci. Forum (Trans Tech Publications, Switzerland, 2002), vol. 389-393, p. 311.
[47] X. Huang, M. Dudley, P. G. Neudeck et al., in *Silicon Carbide 2002--Materials, Processing and Devices*, edited by S.E. Saddow, D.J. Larkin, N.S. Saks et al., MRS Symp. Proc. (Materials Research Society, Warrendale, PA, 2003), vol. 742, p. K3.8.1.
[48] M. Dudley, X. Huang, W. M. Vetter, and P. G. Neudeck, to appear in *Silicon Carbide and Related Materials 2002,* Mat. Sci. Forum (Trans Tech Publications, Switzerland, 2003).
[49] J. A. Powell and P. G. Neudeck, U.S. Patent No. 6,488,771 B1 (2002).
[50] J. W. Matthews, Philos. Mag. **4**, 1017 (1959).
[51] J. W. Matthews, Philos. Mag. **6**, 915 (1961).
[52] S. Bai, Y. Ke, Y. Shishkin et al., in *Silicon Carbide 2002--Materials, Processing and Devices*, edited by S.E. Saddow, D.J. Larkin, N.S. Saks et al., MRS Symp. Proc. (Materials Research Society, Warrendale, PA, 2003), vol. 742, p. K3.1.1.
[53] M. Bhatnagar, B. J. Baliga, H. R. Kirk et al., IEEE Trans. Electron Devices **43** (1), 150 (1996).
[54] J. Wan, M. A. Capano, M. R. Melloch et al., IEEE Electron Device Lett. **23** (8), 482 (2002).
[55] V. V. Afanasev, M. Bassler, G. Pensl et al., Phys. Status Solidi A **162** (1), 321 (1997).
[56] J. R. Williams, G. Y. Chung, C. C. Tin et al., in *Silicon Carbide - Materials, Processing, and Devices*, edited by A. Agarwal, M. Skowronski, J. A. Cooper, Jr. et al., MRS Symp. Proc. (Materials Research Society, Warrandale, PA, 2001), vol. 640, p. H3.5.1.
[57] R. Schörner, P. Friedrichs, D. Peters et al., IEEE Electron Device Lett. **20** (5), 241 (1999).
[58] A. Agarwal, S.-H. Ryu, C. Capell et al., in *Silicon Carbide 2002--Materials, Processing and Devices*, edited by S.E. Saddow, D.J. Larkin, N.S. Saks et al., MRS Symp. Proc. (Materials Research Society, Warrendale, PA, 2003), vol. 742, p. K7.3.1.
[59] P. A. Ivanov, M. E. Levinshtein, S. L. Rumyantsev et al., Solid-State Electron. **46** (4), 567 (2002).
[60] P. G. Neudeck, J. Electronic Materials **27** (4), 317 (1998).
[61] S. Dimitrijev, K. Y. Cheong, J. Han et al., Appl. Phys. Lett. **80** (18), 3421 (2002).
[62] S. T. Sheppard, M. R. Melloch, and J. A. Cooper, Jr., IEEE Electron Device Lett. **17** (1), 4 (1996).

[63] A. K. Agarwal, S. Seshadri, and L. B. Rowland, IEEE Electron Device Lett. **18** (12), 592 (1997).
[64] R. S. Okojie, M. Xhang, P. Pirouz et al., Appl. Phys. Lett. **79** (19), 3056 (2001).
[65] M. Skowronski, J. Q. Liu, W. M. Vetter et al., J. Appl. Phys. **92** (8), 4699 (2002).
[66] G. Gao, J. Sterner, and H. Morkoc, IEEE Trans. Electron Devices **41** (7), 1092 (1994).
[67] S. J. Pearton, J. C. Zolper, R. J. Shul et al., J. of Appl. Phys. **86** (1), 1 (1999).