Stability Analysis of the Multimegabit Telemetry Demodulator/Detector Design

J. K. Holmes
Communications Systems Research Section

Stability of the multimegabit telemetry digital Costas loop is considered. It is shown that the present design is stable with about 35.2 dB gain margin, and therefore is quite stable. This paper considers the bandpass filter implementation of the data filters.

I. Introduction

The purpose of this article is to demonstrate analytically that the multimegabit telemetry Costas loop demodulator is stable over the expected signal dynamic range. The gain margin is about 35.2 dB when $M = 4$ (see Fig. 1). It is well known that a digital Costas loop becomes more unstable as internal delays increase and this fact is verified by the analysis contained herein.

Two methods of stability analysis were employed. First, Jury's stability condition was used and secondly, a root locus was constructed for the digital loop. Both methods yield the same stability criteria.

II. Stability Analysis

First we develop the system loop equation expressed in z transforms. Consider Fig. 1, where the digital Costas loop under consideration is displayed. A portion of the phase detector is analog with the filtering accomplished digitally.

An equivalent loop model is shown in Fig. 2. Because the filtering is done digitally, the loop filter can be expressed directly in the Z variable where $Z = e^{ST_M}$ with S being the La Place transform variable. The internal updating duration into the loop filter is T_M where $T_M = MT_S$ with T_S being the data symbol[1] duration. At present, at all data rates, there are four samples per symbol out of the rate buffers (Fig. 1), so averaging over four samples is equivalent in terms of delays in sampling every symbol (at rate R_S). First we obtain $F(Z)$, the loop filter z-transform.

If the input of the summer branch of the loop filter is denoted as e_n and the output as U_n, then (see Fig. 1)

$$U_n = K_1 \sum_{i=0}^{n} e_i \tag{1}$$

or by adding $K_1 e_{n+1}$ to both sides we obtain

$$U_{n+1} = U_n + K_1 e_{n+1} \tag{2}$$

[1] The parameter k is set so that this is true, and $M = 4$ in the present design (see Fig. 1).

Taking z-transforms we obtain the z-transform of $\{U_n\}$ in terms of the z-transform of $\{e_n\}$

$$U(Z) = \frac{E(Z)\,K_I}{1 - Z^{-1}} \tag{3}$$

where

$$E(Z) = z\{e_n\} = \sum_{n=0}^{\infty} e_n Z^{-n} \tag{4}$$

$$U(Z) = z\{U_n\} = \sum_{n=0}^{\infty} U_n Z^{-n} \tag{5}$$

The proportional term, when z-transformed, remains unaltered so that

$$F(Z) = K_L + \frac{K_I}{1 - Z^{-1}} \tag{6}$$

Next we need the z-transform of the product of the zero order hold ($H'(S)$) and the $VCO(K_{VCO}/S)$ which we denote by

$$z\left\{H'(S)\,\frac{K_{VCO}}{S}\right\} = B(Z)$$

Taking z-transforms we have

$$B(Z) = z\left\{\frac{1 - e^{-ST_M}}{S^2}\right\} K_{VCO} \tag{7}$$

or

$$B(Z) = \frac{K_{VCO}\,T_M}{Z - 1} \tag{8}$$

In order to get the closed loop transfer function (and letting $\theta(Z)$ be the transform of $\theta(t)$ etc.), we write the z transform of the oscillator output phase estimates as

$$\hat{\Theta}(Z) = \left(\frac{K_{VCO}T_M}{(Z - 1)}\right) GF(Z)\,\Phi(Z) \tag{9}$$

Since the phase error $\phi(t)$ has transform $\Phi(Z)$, and the phase estimate $\hat{\theta}(t)$ has transform $\hat{\Theta}$, we have

$$\Phi(Z) = \Theta(Z) - \hat{\Theta}(Z) \tag{10}$$

Now clearly

$$\hat{\Theta}(Z) = \frac{K_{VCO}\,T_M}{(Z - 1)} GF(Z)\,(\Theta(Z) - \hat{\Theta}(Z)) \tag{11}$$

where

$$\hat{\Theta}(Z) = z\{\hat{\theta}(t)\},\ \Phi(Z) = z\{\phi(t)\},\ \Theta(Z) = z\{\theta(t)\} \tag{12}$$

and where G is the signal gain of the Costas loop. Solving for $\hat{\Theta}(Z)$, we have

$$\hat{\Theta}(Z) = \left[\frac{GK_{VCO}\,T_M\,F(Z)}{(Z - 1) + K_{VCO}\,GT_M\,F(Z)}\right]\Theta(Z) \tag{13}$$

Therefore, the closed loop transfer function in the Z variable is

$$H(Z) = \frac{GK_{VCO}\,T_M\,F(Z)}{(Z - 1) + GK_{VCO}\,T_M\,F(Z)} \tag{14}$$

For our case of a hard-limited, in-phase channel Costas loop, the loop gain, G, is proportional to the signal gain through the limiter times the signal voltage itself. The limiter signal gain depends upon the SNR into the limiter.

Rearranging Eq. (14), we obtain

$$H(Z) = \frac{\dfrac{GK_{VCO}\,T_M}{(Z - 1)}\,F(Z)}{1 + \dfrac{GK_{VCO}\,T_M}{Z - 1}\,F(Z)} \tag{15}$$

Since the stability of the loop depends on the closed loop poles of $H(Z)$, we consider the denominator of $H(Z)$, which we denote by $DH(Z)$.

$$DH(Z) = 1 + \frac{GK_{VCO}\,T_M}{Z - 1}\,F(Z) \tag{16}$$

Using Eq. (6) in Eq. (16) we obtain

$$DII(Z) = 1 + \frac{GK_L K_{VCO} T_M}{Z - 1} + \frac{GK_I T_M K_{VCO} Z}{(Z-1)^2} \quad (17)$$

Setting $DII(Z) = 0$ produces

$$Z^2 + (a + b - 2) Z + (1 - a) = 0 \quad (18)$$

where

$$a = GK_L K_{VCO} T_M \quad (19)$$

$$b = GK_I K_{VCO} T_M \quad (20)$$

We apply the Jury stability criterion (Ref. 1) to Eqs. (18) to (20) to determine if the loop is stable. The Jury stability criterion is based on the coefficients of $DII(Z)$. Specifically for digital first and second order loops, we have

(1) First order loop: if

$$DII(Z) = a_1 Z + a_0 = 0 \, , a_1 > 0 \quad (21)$$

and

$$\left| \frac{a_0}{a_1} \right| < 1 \quad (22)$$

then the system is stable.

(2) Second order loop: If

$$DII(Z) = a_2 Z^2 + a_1 Z + a_0 = 0 \, , \, a_2 > 0 \quad (23)$$

and

$$\begin{aligned} &\text{(I)} \quad a_2 + a_1 + a_0 > 0 \\ &\text{(II)} \quad a_2 - a_1 + a_0 < 0 \\ &\text{(III)} \quad a_0 - a_2 < 0 \end{aligned} \quad (24)$$

then the system is stable.

Use of condition (I) of (2) in Eq. (18) results in

$$1 + a + b - 2 + 1 - a = b > 0 \quad (25)$$

From condition II of (2) we have

$$1 + 2 - a - b + 1 - a = 4 - 2a - b > 0 \quad (26)$$

or

$$4 - GK_{VCO} T_M (2K_L + K_I) > 0 \quad (27)$$

The present design calls for

$$\frac{K_I}{K_L} = 2^{-8} = 0.00391 \quad (28)$$

so that for stability we must have

$$GK_{VCO} K_L T_M < 1.9961 \cong 2 \quad (29)$$

The third condition is met trivially, i.e.,

$$1 - a - 1 = -a < 0 \quad (30)$$

which is true since

$$-GK_L K_{VCO} T_M < 0 \quad (31)$$

We conclude from Jury's stability criterion that for loop stability we require $GK_{VCO} K_L T_M < 2$. At threshold conditions, it has been shown that $G_0 K_{VCO} K_L T_4 = 3.9046 \times 10^{-3}$ which is much less than 2.

As a double check on the stability result (Eq. 29) and also as a way of determining gain margin, we consider the root-locus plot for this system. To utilize the root locus we consider the open loop transfer function given by

$$OL(Z) = GF(Z) = \left| IF'(S) \frac{K_{VCO}}{S} \right|$$

or

$$OL(Z) = \frac{GK_L K_{VCO} T_M}{(Z-1)} + \frac{GK_I T_M K_{VCO} Z}{(Z-1)^2} \quad (32)$$

Using the notation of Eqs. (19) and (20) we have

$$OL(Z) = \frac{a}{Z-1} + \frac{bZ}{(Z-1)^2} \tag{33}$$

or

$$OL(Z) = \frac{(a+b)\left(Z - \frac{a}{(a+b)}\right)}{(Z-1)^2} \tag{34}$$

Using the methods of the root locus (Ref. 2), which apply to the Z plane as well as the S plane, we know that the locus starts at the poles of $OL(Z)$ with zero gain ($a + b = 0$), and terminates on the zeros for unbounded gain ($a + b = \infty$). Further, the locus exists at any point along the real axis where an odd number of poles plus zeros is found to the right of the point. Using the above facts and the remaining rules of root locus construction yields the root locus of our digital Costas loop, as shown in Fig. 3.

Since system instability occurs when the root locus goes onto or outside of the unit circle, it is necessary to find the value of "gain" ($a + b$) such that the locus just crosses the unit circle at the point $Re(Z) = -1$ and $Im(Z) = 0$. Since the "gain" is given by zero and pole distances we obtain

$$a + b = \frac{|-2|^2}{\left|-1 - \frac{a}{(a+b)}\right|} \tag{35}$$

Equation (35) yields

$$2a + b = 4 \tag{36}$$

or

$$a + \frac{b}{2} = 2 \tag{37}$$

For stability, therefore, the locus must be inside the unit circle, so we require

$$\left(a + \frac{b}{2}\right) < 2 \tag{38}$$

This condition is precisely the same as that derived from Jury's stability criterion (Eq. (26)).

We conclude, then, that for stability

$$GK_L K_{VCO} T_M < 2 \tag{39}$$

III. Gain Margin

Now we shall determine the gain margin of the loop, that is, how many dB increase in signal level is needed to just make the system unstable. To determine the gain margin we must compute the range in G which is the product of the AGC output signal voltage A and the gain through the limiter α, which depends on the limiter input SNR (SNR_i), i.e.

$$G = \alpha A, \quad \alpha = \alpha(SNR_i) \tag{40}$$

We do this by considering the widest pre-AGC filter case (53.4 MHz = B) in which data rates vary from 4 MSPS to 32 MSPS. First we determine the range of the signal component *rms* voltage A out of the AGC. Consider the noncoherent AGC model as shown in Fig. 4. Denote the input noise power by N_0B and the input signal power at threshold by S_0. Further, denote the gain of the AGC at threshold by g_0, and the total output power by P_T. Then we have

$$g_0 (N_0B + S_0) = P_T \tag{41}$$

or

$$g_0 = \left(\frac{P_T}{N_0B + S_0}\right) \tag{42}$$

At a higher input signal level, S_1, we have

$$g_1 (N_0B + S_1) = P_T \tag{43}$$

or

$$g_1 = \left(\frac{P_T}{N_0B + S_1}\right) \tag{44}$$

where g_1 is the AGC gain when the input signal power is S_1.

The output signal power component for each case is

$$P_0 = S_0 g_0 \tag{45}$$

$$P_1 = S_1 g_1 \tag{46}$$

Hence, the dynamic range of the output signal power is given by

$$\frac{P_1}{P_0} = \frac{g_1 S_1}{g_0 S_0} = \frac{N_0 B + S_0}{N_0 B + S_1} \frac{S_1}{S_0} \tag{47}$$

or

$$\frac{P_1}{P_0} = \left[\frac{1}{\frac{N_0 B}{S_1} + 1}\right]\left[1 + \frac{N_0 B}{S_0}\right] \tag{48}$$

Then, when the final SNR is very large, Eq. (48) approaches

$$\frac{P_1}{P_0} = SNR_0^{-1} + 1 \tag{49}$$

where SNR_0 is the input SNR at threshold, i.e.,

$$SNR_0 = \frac{S_0}{N_0 B} \tag{50}$$

Now the direct component loop gain $GK_V K_L T_M$ increases by the ratio $\alpha_1 r/\alpha_0$ where (α_1/α_0) is the ratio of limiter suppression factors. The suppression factor is given by

$$\alpha \cong \text{erf}\left(\sqrt{\frac{E_s}{N_o}}\right) \tag{51}$$

where

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-y^2} dy \tag{52}$$

The signal voltage ratio into the loop (out of the AGC) is given by

$$\frac{A_1}{A_0} = \frac{\sqrt{g_1 S_1}}{\sqrt{g_0 S_0}} = \frac{\sqrt{P_1}}{\sqrt{P_0}} = r \tag{53}$$

At the lowest data rates (4 MSPS) in which the 53.4 MHz bandpass filter is used and at the lowest value of E_s/N_o (-4 dB), we find that the SNR_o in 53.4 MHz, is given by

$$SNR_o = \frac{E_s}{N_o} \frac{R_s}{B} = -15.1 \text{ dB} \tag{54}$$

The limiter suppression factor is equal to

$$\alpha_0 = \text{erf}(\sqrt{0.398}) = 0.627 \tag{55}$$

At the maximum data rate (32 MSPS) and the maximum value of E_s/N_o we find that the SNR in 53.4 MHz is

$$SNR_1 = \frac{E_s}{N_o} \frac{R_s}{B} = 9.8 \text{ dB} \tag{56}$$

and the corresponding limiter value is equal to

$$\alpha_1 = \text{erf}(\sqrt{15.8}) \cong 1.0 \tag{57}$$

Therefore the direct component loop gain at the maximum data rate and the maximum value of E_s/N_o, assuming that it is set to threshold at the lowest data rate (4 MSPS) and lowest value of E_s/N_o (-4 dB), is given by

$$\frac{\alpha_1}{\alpha_0} G_0 K_L K_V T_4 = 3.48 \times 10^{-3} \tag{58}$$

where we have used Eqs. (48), (53), (55), (57) and the fact that $G_0 K_L K_V T_4 = 3.904 \times 10^{-3}$ at threshold. We conclude that the gain margin (GM) is

$$GM = 20 \log\left(\frac{2}{3.48 \times 10^{-3}}\right) = 35.2 \text{ dB} \tag{59}$$

when $M = 4$. It, therefore, is clear that the loop is quite stable.

IV. Conclusion

In the present digital Costas loop design with $M = 4$, there is about 35 dB of gain margin. Further refinement in the model will be discussed in a later report.

References

1. S. C. Gupta, *Transform and State Variable Methods in Linear Systems*, John Wiley & Sons, New York, 1966.
2. C. J. Savant, *Basic Feedback Control System Design*, Chapter 4, McGraw-Hill Book Company Inc., New York, 1958.

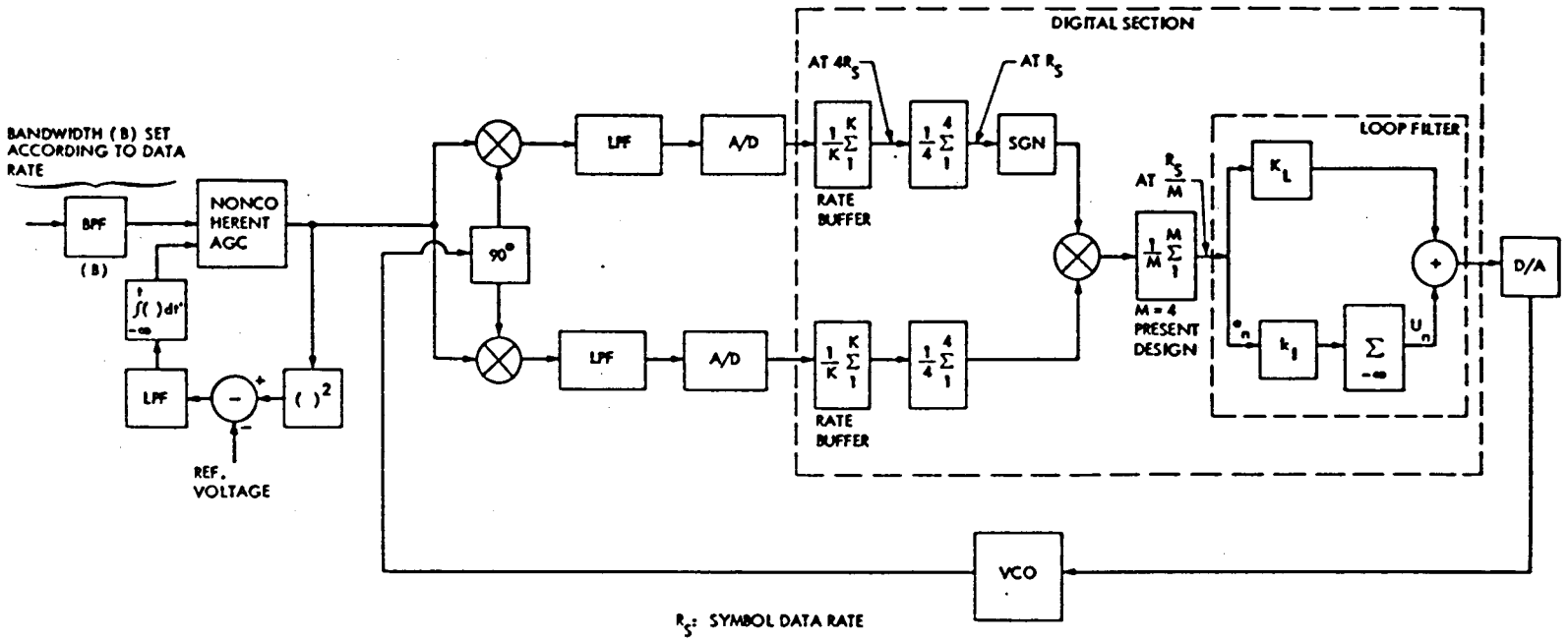
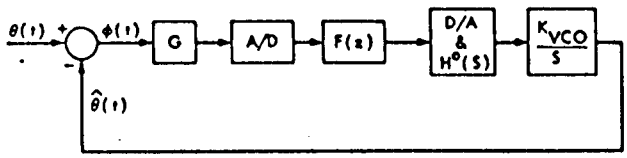


Fig. 1. Model of current multimegabit carrier mode (Costas loop) in tracking



D/A: DIGITAL TO ANALOG CONVERTER
G: LOOP GAIN
$H^{\circ}(S)$: ZERO ORDER HOLD

Fig. 2. Equivalent linear phase lock loop model

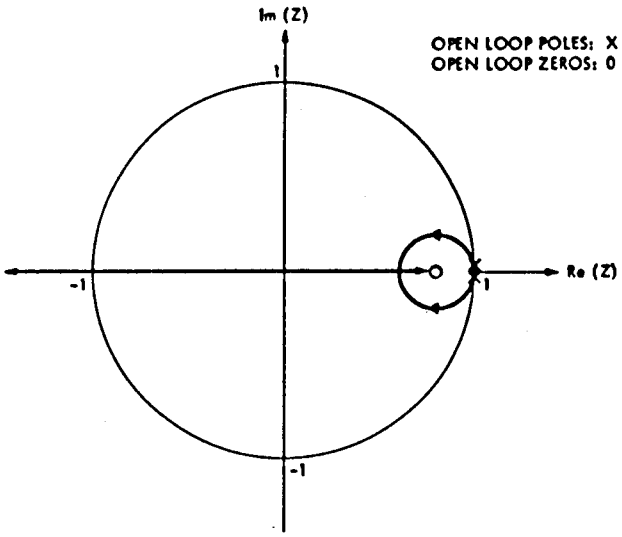
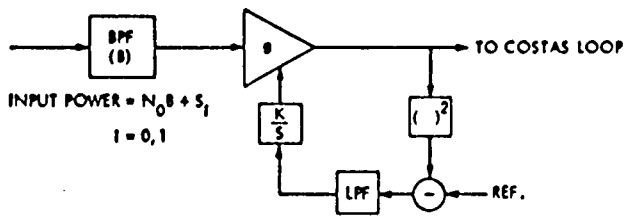


Fig. 3. Root locus of multimegabit digital Costas loop (second order)



A = OUTPUT SIGNAL VOLTAGE = $\sqrt{P}$
$gS_i = P_i$ = OUTPUT SIGNAL POWER
P_T = TOTAL OUTPUT POWER
B = SELECTED ACCORDING TO DATA RATE

Fig. 4. Noncoherent AGC model for determining dynamic range