Polyimide and BeO Mini Port Card Performance Comparison for CDF Run IIb

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***Abstract*-- The new silicon detector design for CDF relies on advanced packaging solutions in order to attain the strict small size and low mass requirements dictated by the experiment's physics program. The silicon strip detector at CDF is composed of overlaying silicon sensors in the form of a barrel around the colliding beam. The electronic instrumentation (sensors, readout and transceiver chips) is assembled into the staves of this barrel. In this paper we describe the development of the mini port card (MPC). The MPC is located at one of the ends of the stave, and it is responsible for signal translation and repetition from the readout chips to and from the data acquisition system (DAQ). The MPC's development has taken two approaches that use different technologies. One of the approaches uses BeO as the board substrate (BeO-MPC), while the other approach uses a hybrid rigid-flexible polyimide substrate (Poly-MPC). We present test results of pre-production parts, each one assembled with a different MPC packaging technology. Complete thermal and electrical characterization of the MPC is shown, and the advantages and disadvantages of both technologies, as well as their influence in the overall system performance, are presented.**

I. Introduction

The silicon strip detector at CDF [1] is composed of overlaying silicon sensors in the form of a barrel around the colliding beam (Fig. 1). The electronic instrumentation (sensors [2], transceiver [3] and readout [4] chips) is assembled into the staves of this barrel (Fig. 2). The mini port card (MPC) is assembled on the end of the carbon fiber structure of the stave (as shown in Fig. 3 and Fig. 4), and three flex circuits are attached to it: the data and high voltage (Data/HV) pigtail, the low voltage (LV) pigtail, and the wing. The Data/HV pigtail is an 8-bit data and 16-bit control low voltage differential signaling (LVDS) standard interface of the stave to the data acquisition (DAQ) system. This flex circuit also brings six high voltage signals (up to 500V) to bias the silicon sensors in the stave individually. The LV pigtail brings 13 low voltage signals (2.5V) to the 24 readout chips on a stave and for the five transceiver (TX) chips on the MPC. Since both sides of the stave are instrumented, a flex circuit (wing) is attached to one edge of the MPC, and folded around the carbon fiber structure for the connection to the readout chips on the bottom side of the stave. In this configuration the readout chips on top and bottom of the stave are connected to the same MPC.

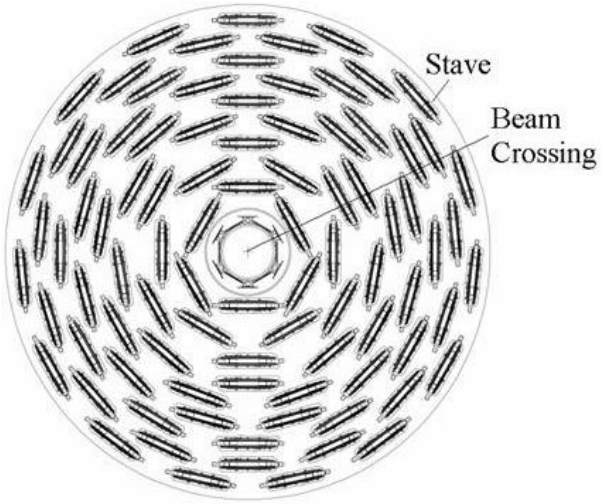

Fig. 1. Cross section of the silicon detector barrel

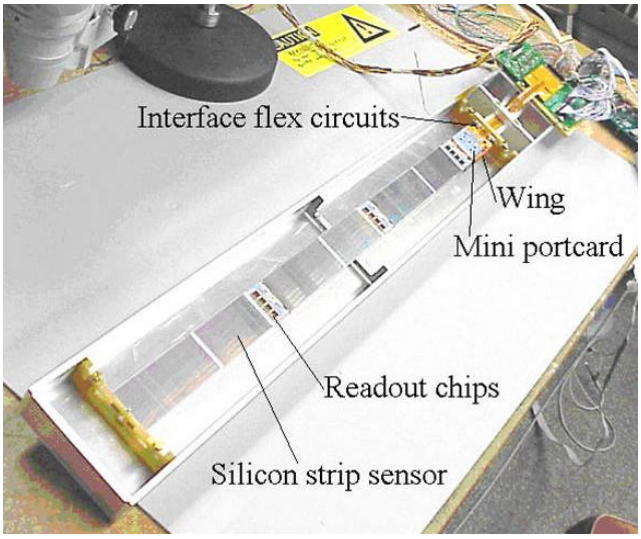

Fig. 2. Stave of the silicon strip detector barrel

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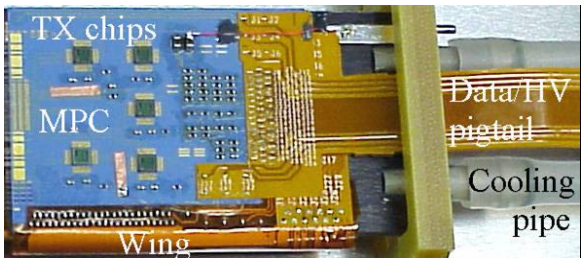

Fig. 3. Top of stave, MPC region

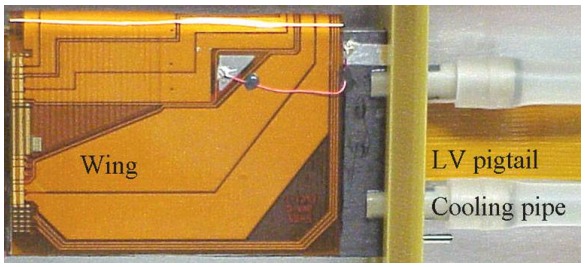

Fig. 4. Bottom of stave, MPC region

II. BEO-MPC

In the BeO-MPC design 157 solder pads attach three flex circuits (Data/HV pigtail, LV pigtail, and wing) to the MPC. Fig. 5 shows a picture of the BeO-MPC assembled on a test card. The wing flex circuit in the picture is not folded. A detail of the solder pad region is shown in Fig. 6. The BeO-MPC has 6 metal layers on top and bottom of the BeO substrate. The total thickness of this 2" by 1.55" board is 750µm.

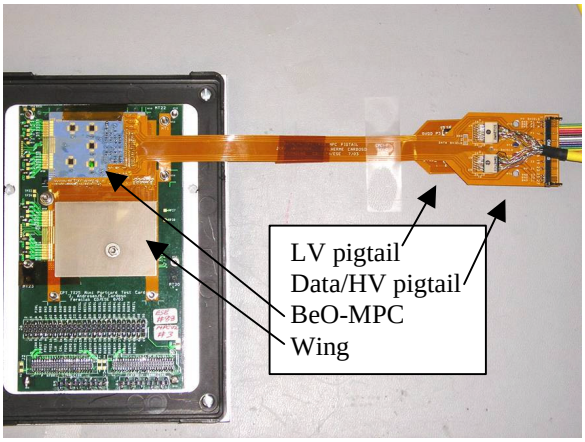

Fig. 5. BeO-MPC assembled on test card

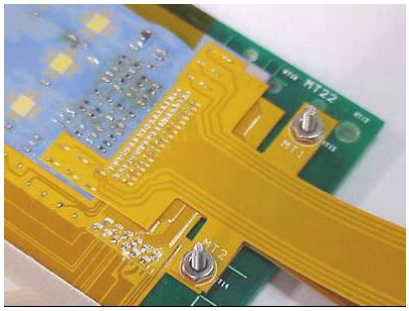

Fig. 6. Solder pad region, BeO-MPC

A. *Electrical Performance*

The MPC is responsible for repeating data and control signals between the DAQ system and the readout chips. Therefore it's important that the MPC produces signals with good electrical integrity. If the impedance between the MPC and the other parts of the system is not well matched, signal reflections may cause error at the receivers of the readout chips. For this reason, the BeO-MPC was produced with a controlled differential characteristic impedance of 100Ω (which agree with the measurements). The dielectric constant of the BeO substrate is 5 (er @ 60 Hz), and the dielectric strength is 100kV/mm. The gold traces have width and spacing of 75µm. Fig. 7 shows the electrical integrity of a signal in the BeO-MPC, with rise and fall times of about 4ns and 5ns. The signal integrity is excellent, allowing reliable and consistent data and control transmission.

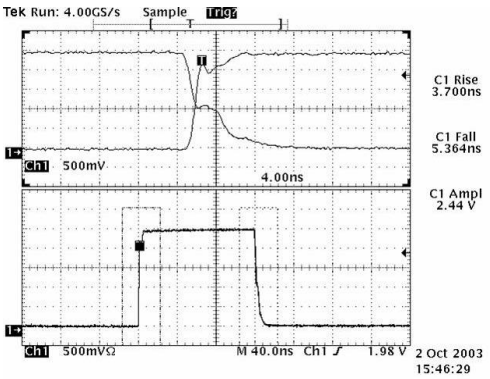

Fig. 7. Electrical signal integrity, BeO-MPC

Another important characteristic to be observed in this system is the pedestal and noise distribution of the readout chips. For more details on this test refer to [5]. The goal of the MPC design is to minimize changes in readout chips' performance that may happen due to timing variations on the control signals. Fig. 8 shows the pedestal and noise distribution of four readout chips (512 channels) connected to a BeO-MPC. The performance of the readout chips with and without the BeO-MPC show almost no variation, which implies that the electrical performance of the BeO-MPC complies with the requirements of the readout chip.

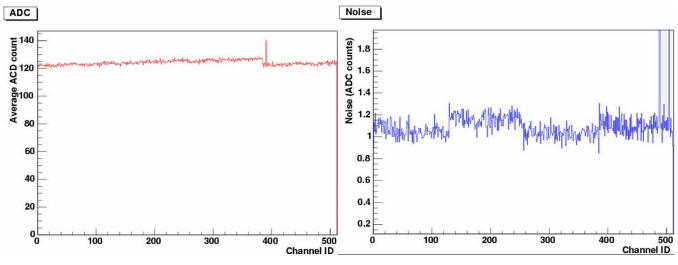

Fig. 8. Pedestal (left) and noise (right) distribution, four readout chips (512 channels), BeO-MPC

B. *Mechanical Performance*

The MPC is assembled at the end of the stave, on top of the same carbon fiber structure that cools down sensors and readout chips on the stave. Since five transceiver chips are mounted on the MPC (each one dissipating about 500mW), it's important that the cooling structure is able to sink most of the heat generated by the MPC. Finite element analysis was performed on the BeO-MPC design, and the temperature profile on top and bottom of the MPC are shown in Fig. 9. This analysis was performed with four transceiver chips on the MPC, but a latter review of the design included another transceiver chip.

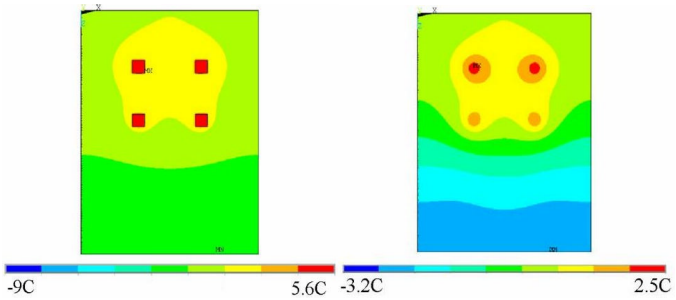

Fig. 9. BeO-MPC thermal dissipation simulation, top (left) and bottom (right) layers

This analysis showed that in order to the BeO-MPC to operate at a temperature that would not disturb the other pieces of the system, the transceiver chips would have to be mounted on a thermal dissipation pad in the BeO-MPC (Fig. 10).

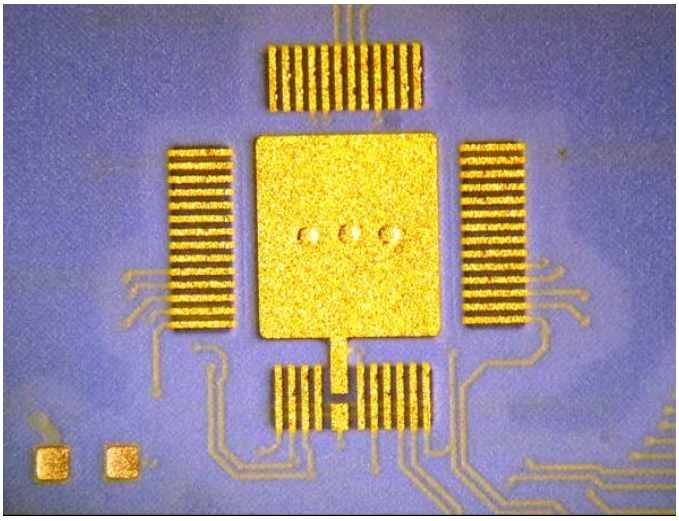

Fig. 10. Thermal dissipation pad, BeO-MPC

Fig. 11 shows an infrared picture of the BeO-MPC during normal operation. The temperature profiles in the picture are very close to the simulation. The temperature gradient of around 14°C also coincides with the simulated values.

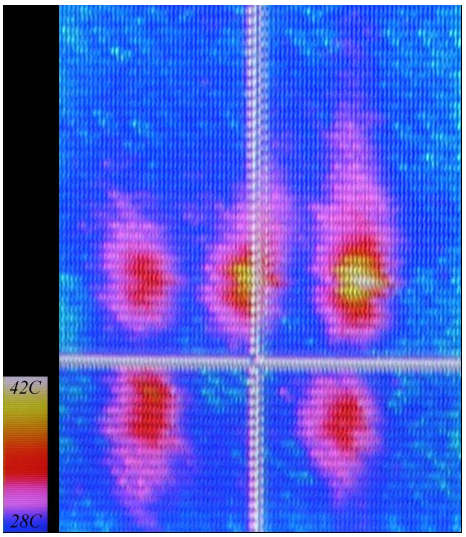

Fig. 11. Infrared picture of the BeO-MPC during normal operation

III. POLYIMIDE MPC

The Poly-MPC design brings considerable simplification to the MPC assembly, since it allows two of the pigtails (Data/HV and wing) to be integrated into the layout of the MPC as a thin film rigid and flexible substrate. Only the LV pigtail is soldered to the Poly-MPC. The substrate is rigid in the MPC, wing and connectors region, and flexible in the pigtail and folding locations. A picture of the Poly-MPC assembled on to a test card is shown in Fig. 12, while Fig. 13 shows a detail of the Poly-MPC in the transition between rigid and flexible circuit (wing). The integration of the two pigtails in the MPC reduces the number of solder pads from 157 in the BeO-MPC to 32 in the Poly-MPC. The Poly-MPC is also assembled on the end of the carbon fiber structure of the stave, in the same location as the BeO-MPC. The Poly-MPC has 6 metal layers over the polyimide substrate (Pyralux AP from DuPont). The 2" by 1.55" board in the rigid part is 750µm thick.

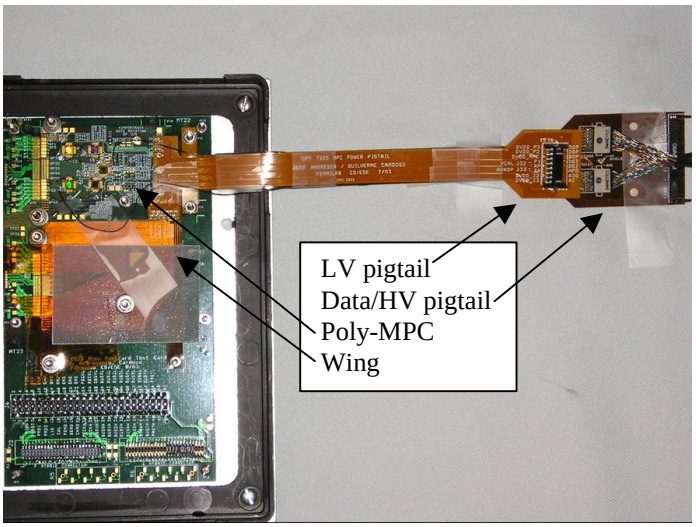

Fig. 12. Poly-MPC assembled on test card

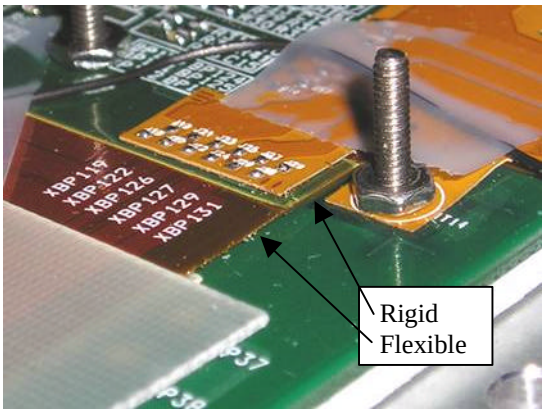

Fig. 13. Poly-MPC detail, rigid to flexible circuit transition

A. *Electrical Performance*

The dielectric constant of the Poly-MPC is 3.8 (er @ 60 Hz), and the dielectric strength is 16kV/mm. The board has copper traces with width and spacing of 100µm. The characteristic impedance of the differential traces is around 100Ω. The signal electrical integrity of the Poly-MPC is shown in Fig. 14. The rise and fall times are 4 ns and 7 ns, which is very close to the performance of the BeO-MPC. The pedestal and noise distributions of four readout chips are shown in Fig. 15. The readout chip characterization results show that the Poly-MPC doesn't change the performance of the readout chips.

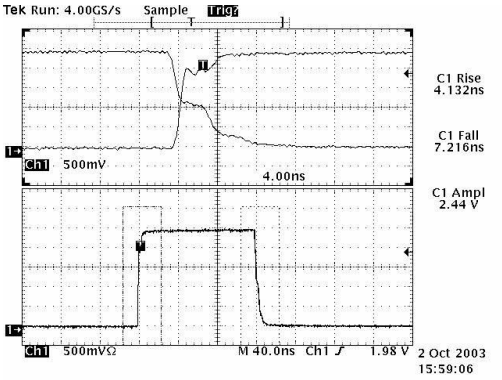

Fig. 14. Electrical signal integrity, Poly-MPC

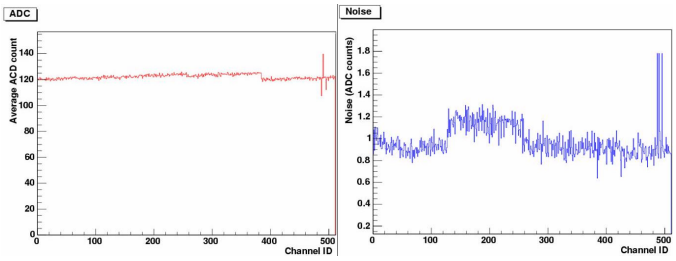

Fig. 15. Pedestal (left) and noise (right) distribution, four readout chips (512 channels), Poly-MPC

B. *Mechanical Performance*

Similar to the BeO-MPC, the Poly-MPC also has five transceiver chips dissipating 500mW each. Although the Poly-MPC simplifies the assembly and design of the MPC (two board layouts instead of four), the BeO substrate has the advantage of being a better heat conductor. The finite element analysis performed in the Poly-MPC design showed that the transceiver chips can operate at a reasonable temperature (maximum of 13°C) if nine thermal vias are placed under the chips (Fig. 16). Fig. 17 shows a picture of the thermal dissipation pad, where the transceiver chips are assembled.

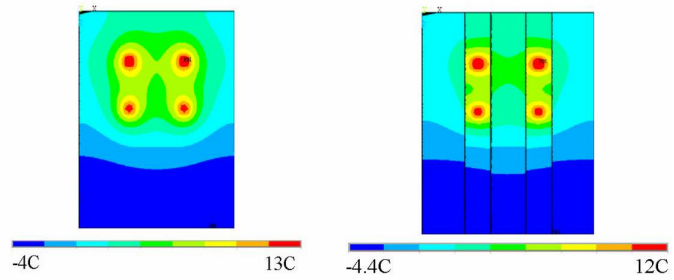

Fig. 16. Poly-MPC thermal dissipation simulation, top (left) and bottom (right) layers

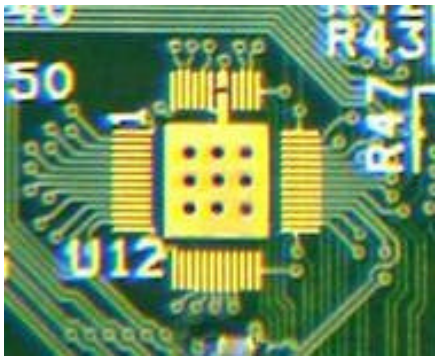

Fig. 17. Thermal dissipation pad, Poly-MPC

A strip of copper was laid out at the bottom of the MPC (which is in contact with the stave cooling channel) in order to improve the heat distribution of the transceiver chips. Fig. 18 shows an x-ray of the thermal dissipation pad. The heat dissipation strip on the bottom layer of the Poly-MPC is visible in the figure. Fig. 19 shows an infrared picture of the Poly-MPC during normal operation. The picture shows that the heat is dissipated vertically to the bottom of the board using the copper cooling strips.

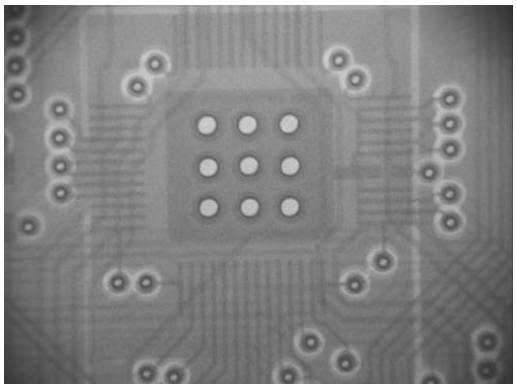

Fig. 18. X-ray of the Poly-MPC thermal dissipation pad

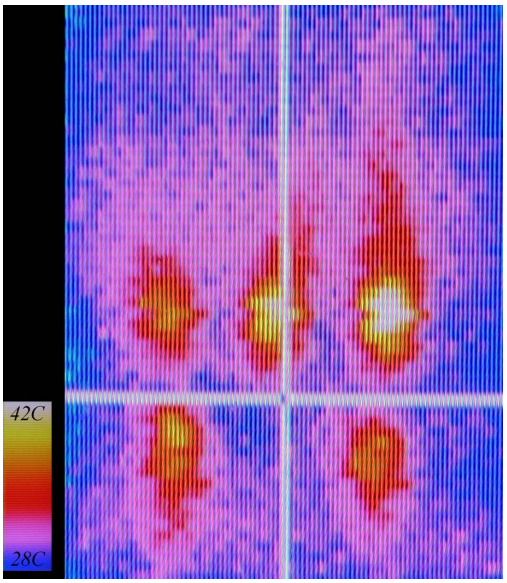

Fig. 19. Infrared picture of the Poly-MPC during normal operation

IV. Conclusions

The electrical and mechanical performance of both MPC designs are comparable. Fig. 20 shows the pedestal and noise distributions of both MPC designs. The BeO substrate has been preferred in the past due to its thermal dissipation characteristics. This study has shown that appropriate design changes could be made to the Poly-MPC design so that it complies with the thermal requirements of the project.

The polyimide rigid/flex technology is attractive, since it allows embedding the design of two flex circuits (wing and Data/HV pigtail) into the MPC design. Reducing the number of board designs not only saves layout time, but it also reduces problems caused by board misalignments.

More studies are being performed on the Poly-MPC thermal and radiation hardness performance. So far the Poly-MPC seems to be an attractive replacement for the BeO-MPC. A conclusion will only be possible once these studies are completed. Table 1 shows a summary of the results presented in this paper.

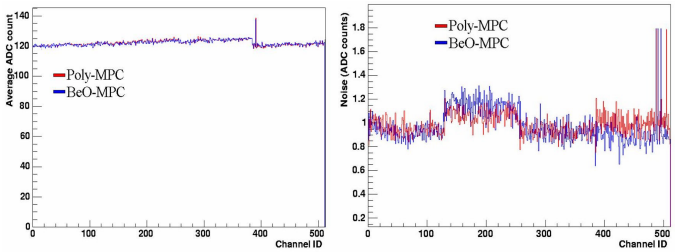

Fig. 20. Pedestal (left) and noise (right) distribution, four readout chips (512 channels), Poly-MPC and BeO-MPC

V. Acknowledgments

We thank Dick Wernersbach and Jim Smith (Printed Circuits, INC.), Chris Stringer, Joe Occhipinti, and John Maki (Zentrix Technologies, INC.) for the technical support they provided in the development of this work.

VI. References

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[4] B. Krieger, et al., "SVX4: A New Deep Submicron Readout IC for the Tevatron," to be published in the *Proceedings of the 2003 IEEE Nuclear Science Symposium*, Portland, October 12-24, 2003.

[5] R.-S. Lu, et al., "Stave Design and Testing of SVXIIb of CDF at Fermilab," to be published in the *Proceedings of the 2003 IEEE Nuclear Science Symposium*, Portland, October 12-24, 2003.

Table 1. Summary of results

Parameter:	BeO-MPC	Poly-MPC
Number of signal layers	6	6 (rigid), 2 (flexible)
Substrate:		
▪ Thermal resistivity (ρ = W/mK)	250	0.16
▪ Radiation length X_0 (mm)	143	286
▪ Dielectric constant (ε_r @ 60 Hz)	5	3.8
▪ Dielectric strength (V/mm x 10^3)	100	16
Signal layers:		
▪ Material	Gold	Copper
▪ Radiation length X_0 (mm)	3.4	14.3
▪ Conductivity σ $(\Omega.\text{meter})^{-1}$	4.10 x 10^7	5.81 x 10^7
▪ Relative Permeability, k	1	1
▪ Thickness (μm)	10	17
▪ Traces width/spacing (μm)	75/75	100/100
Price (each, for 25 parts purchased, in US$)	1,500	770
Safety procedures required	Handling training required	No training required
Turnaround time (weeks)	10-12	2
Number of boards in the MPC system	4 (MPC, wing, data/HV and LV pigtails)	2 (MPC and LV pigtail)