Virtex-5 Rocket IO GTP Transceiver Radiation Test Report (preliminary)

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Outline

- Test Goals
- Test Setup
- Test Methodology
- Test Results
- Test Setup and Methodology 2
- Test Results 2
- Observations
- Proposed Test Enhancements
- Future Test Plans

Test Goals

- **Measure x-section of Gigabit Transceiver low-Power (GTP) using Aurora protocol**
  - GTP is fixed silicon
  - Aurora is implemented in programmable logic
- **Measure x-section of just GTP**
  - To help Xilinx design ‘harder’ GTP for future SIRF chips
- **Understand failure modes of GTP using Aurora protocol**
- **Understand recovery methods of GTP using Aurora protocol**

Test Setup

- **Connect two FPGA boards together with a serial link**
  - Functional monitor (funcmon) FPGA board
    - XC2VP7 FPGA
    - Generate test frames (pseudo-random pattern of data), transmit frames to DUT, receive frames back from DUT, check received test frames
  - Design under test (DUT) FPGA board
    - XC5VLX50T FPGA (XC5VLX50T;FFG1136CNU0641;DD17147A;1C-ES; S/N 1)
    - Receive frames from funcmon, transmit frames back to funcmon (simple loopback)
- **Serial link parameters**
  - 2.5 Gbps line rate
  - 8B/10B encoding
    - Effective line rate: 2.0 Gbps
- **The serial link uses the Aurora protocol**
  - Open (free) *very lightweight* standard created by Xilinx
  - Used for point-to-point links
  - Can achieve over 99% efficiency
    - Our setup has ~98.67% efficiency
    - Effective line rate: 1.97 Gbps

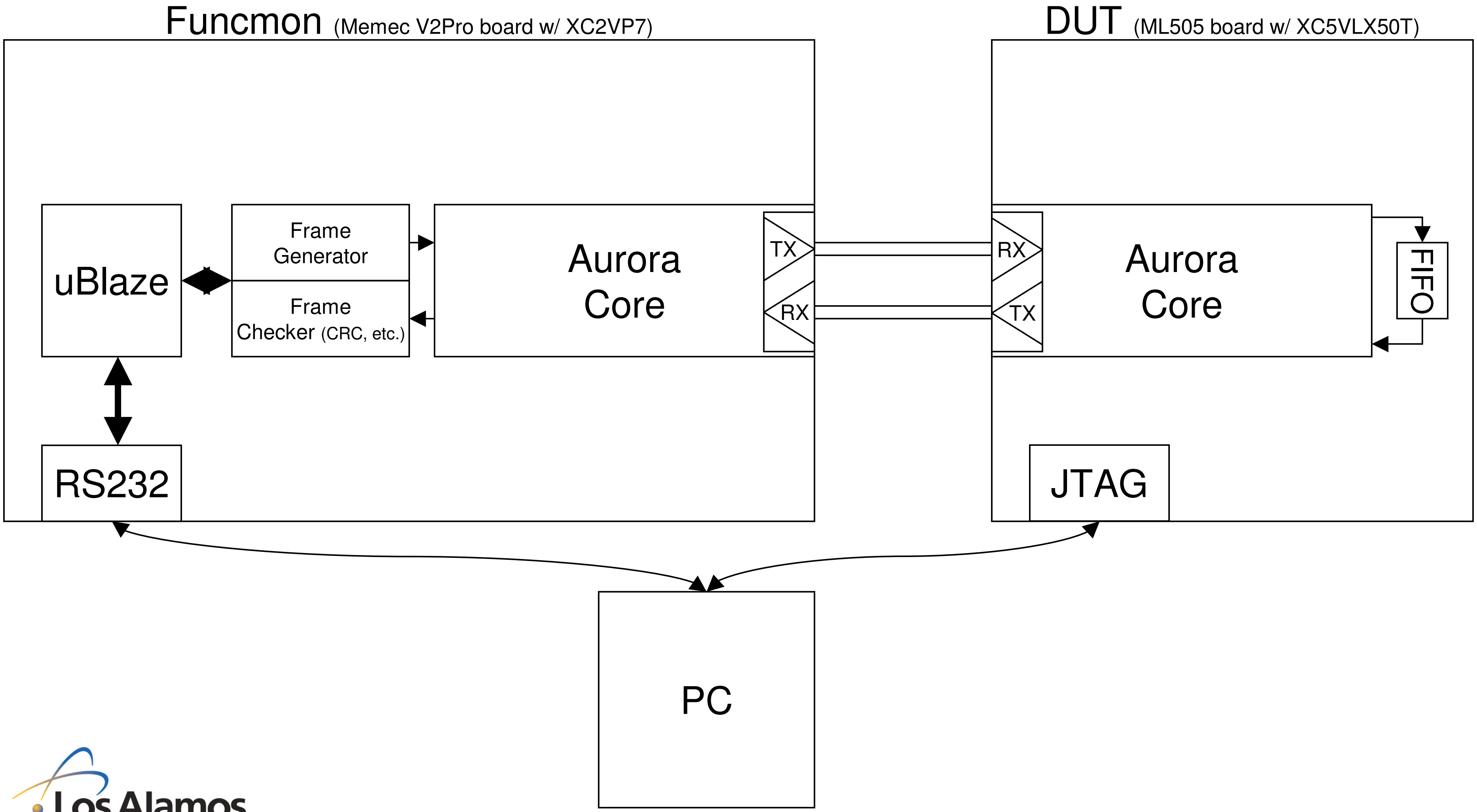
Test Setup: Frame Composition

16 bits	16 bits	*n* x 16 bits	16 bits
Frame #	Num 16-bit words *n*	Payload	CRC

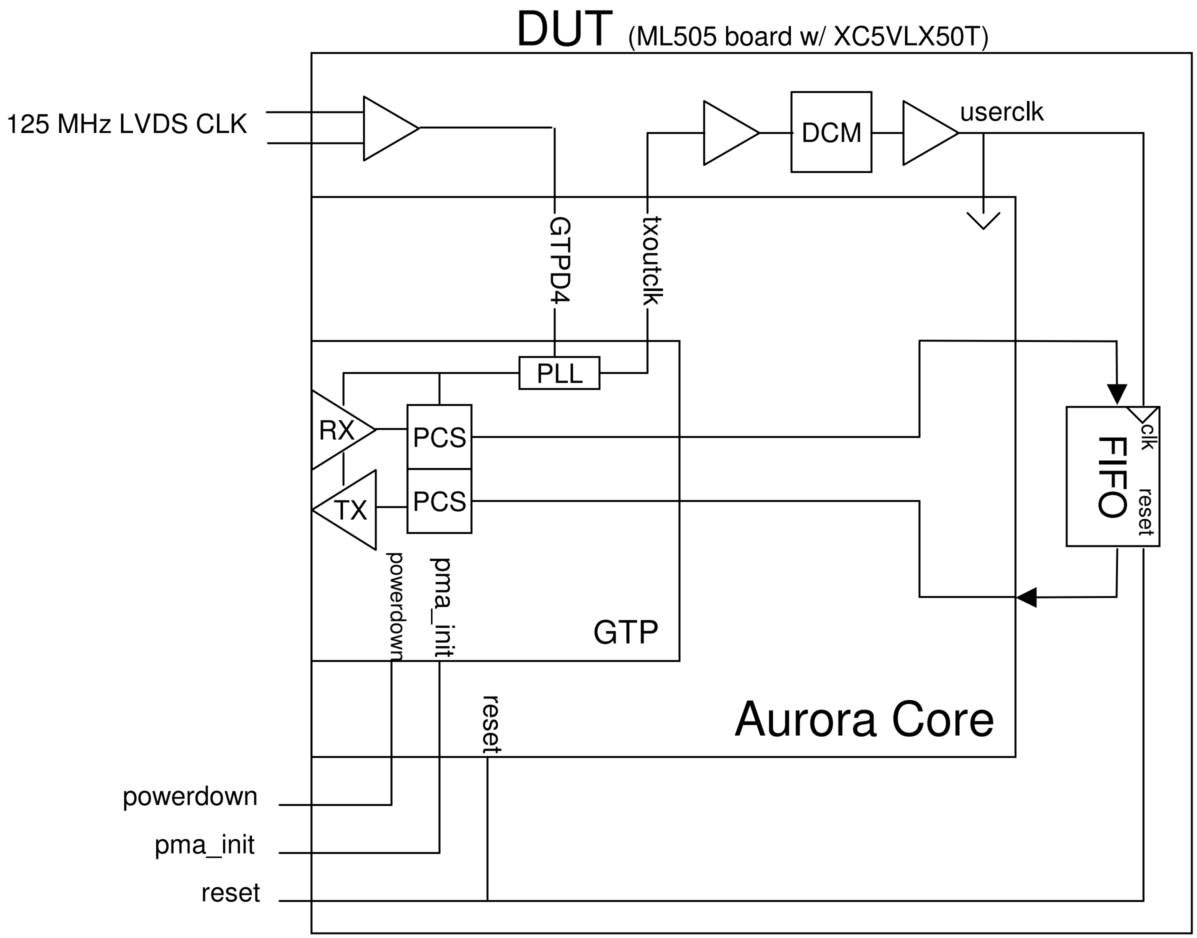
Notes:

- Frame payload is random data generated by an LFSR
- *n*=510

Test Setup: Block Diagram


Funcmon (Memec V2Pro board w/ XC2VP7)
DUT (ML505 board w/ XC5VLX50T)
uBlaze
Frame Generator
Frame Checker (CRC, etc.)
Aurora Core
TX
RX
RX
TX
Aurora Core
FIFO
RS232
JTAG
PC

Test Setup: DUT Reset and Clock Architecture



Notes:

- PCS = Physical Coding Sublayer (8b/10b encoder/decoder, PLL, TX and RX buffers)
- Serializer and Deserializer not shown

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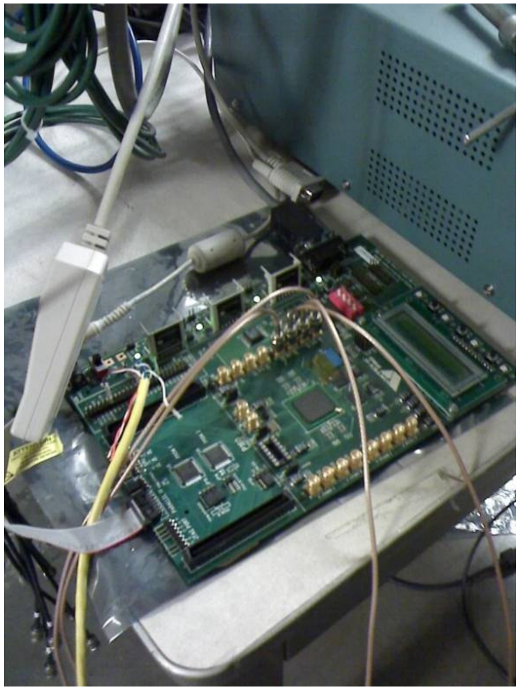
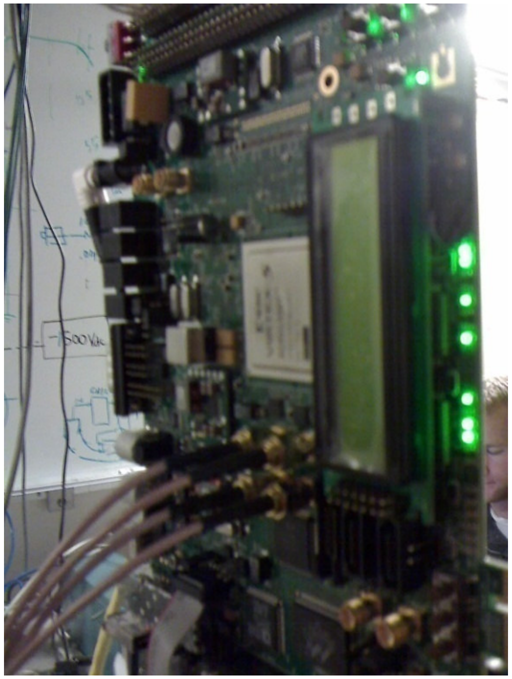
Test Setup: Pictures



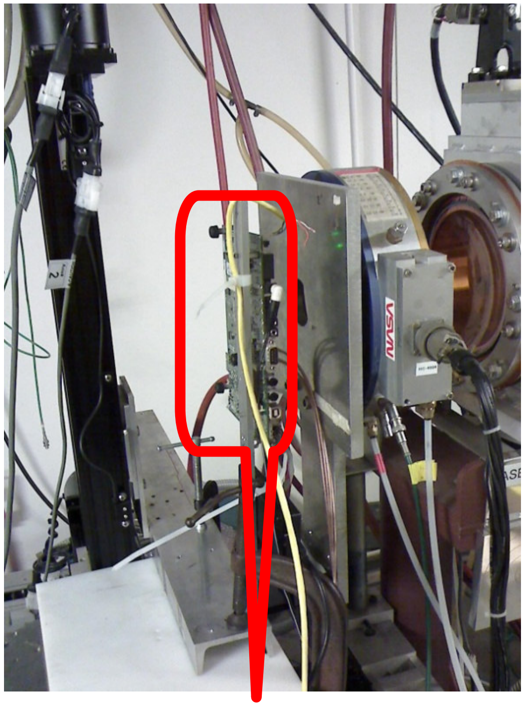
Funcmon board

(Memec V2Pro board w/ XC2VP7)



DUT board

(ML505 board w/ XC5VLX50T)



DUT board in front of beam

Test Setup: Cyclotron

- **Lawrence Berkeley National Laboratory 88-inch Cyclotron**
  - November 1st 2007
  - Helium heavy ions (alpha particles)
    - 32 MeV/amu (128 MeV)
    - Testing in air
    - .075 LET
  - Average flux: 1.95 x 10^7 particles/s/cm^2
- **Indiana University Cyclotron Facility**
  - December 4th and 5th 2007 (just postponed to January 9th and 10th 2008)
  - Protons
    - 63 MeV?

Test Methodology

1. Apply fluence to DUT until failure

- Failure =
  - Hard error
    - RX/TX buffer overflow/underflow
    - Bad control character
    - Too many soft errors
  - Soft error
    - Invalid 8B/10B code
    - Disparity error
    - No data in frame
  - Frame error
    - Truncated frame
    - Invalid control character
  - Lane or channel down
  - Data stops flowing
  - CRC error
  - Missing frame

2. Attempt to recover link

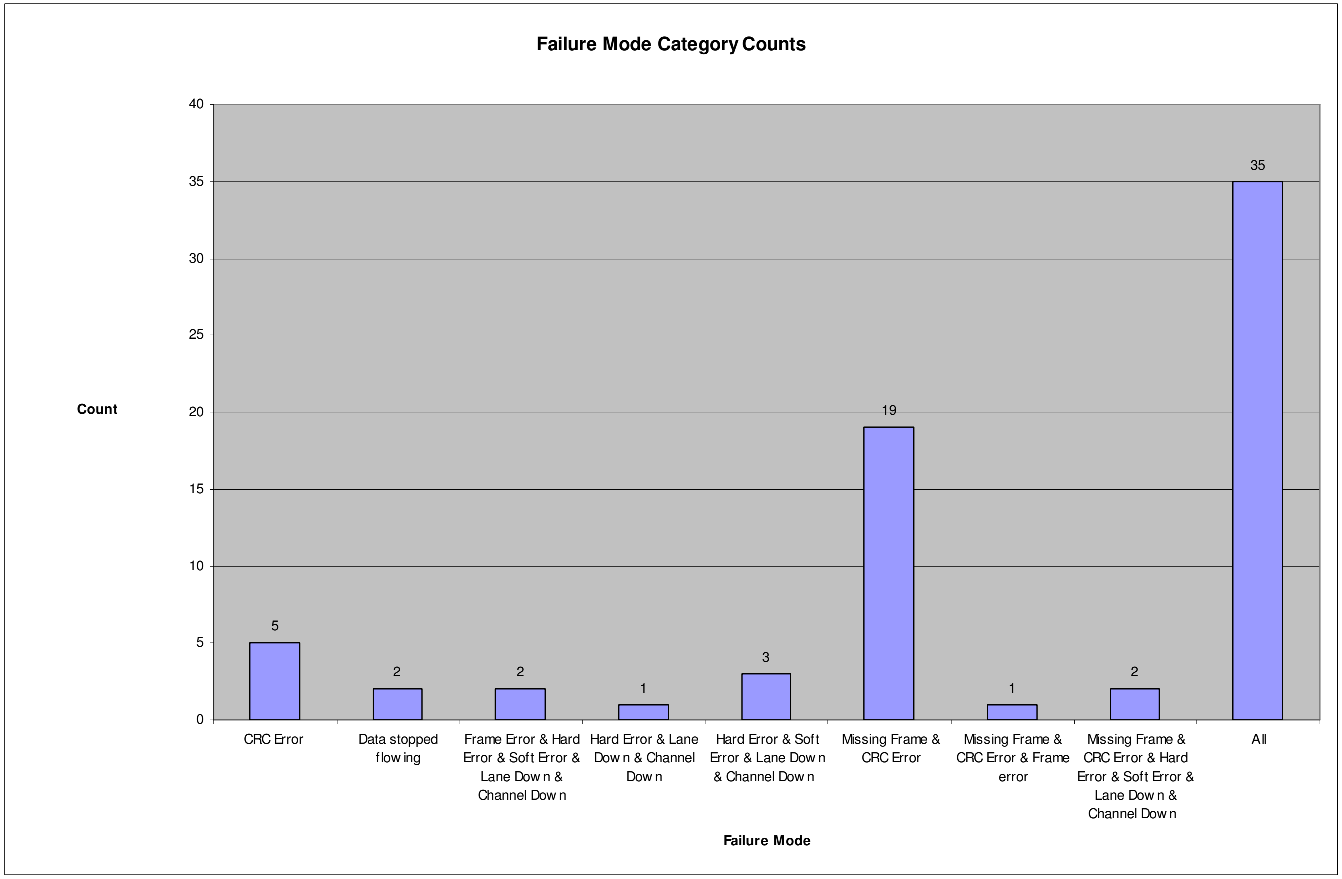
- Steps

a. Reset DUT
b. Reset GTP
c. Power-cycle GTP
d. Scrub DUT
e. Reset DUT
f. Reset GTP
g. Power-cycle GTP
h. Reconfigure DUT
i. Power-cycle DUT
j. Reset funcmon

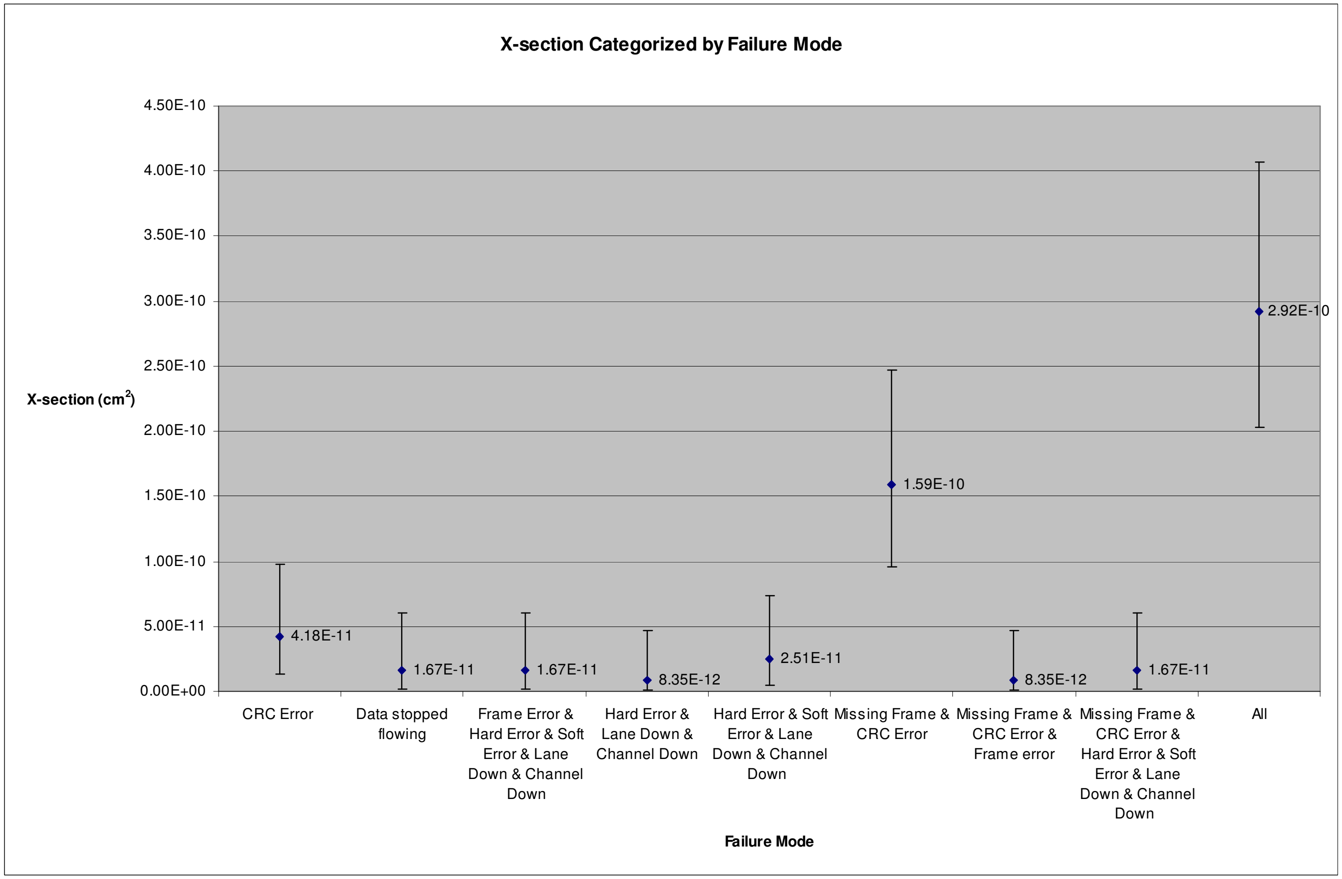
Test Results: Failure Modes & Recovery Methods

- **We found eight unique failure signatures**
  1. CRC error
  2. Data stopped flowing
  3. Frame error & hard error & soft error & lane down & channel down
  4. Hard error & lane down & channel down
  5. Hard error & soft error & lane down & channel down
  6. Missing frame & CRC error
  7. Missing frame & CRC error & frame error
  8. Missing frame & CRC error & hard error & soft error & lane down & channel down
- **Five successful recovery methods**
  1. DUT reset
  2. Scrub
  3. Scrub and reset
  4. Self-recovery
  5. Funcmon reset
- **GTP reset and GTP power-cycle never successfully recovered the link**
- **A full DUT reconfigure or a DUT power-cycle was never required for recovery**
- **There was not a one-to-one relationship between failure mode and recovery method**

Test Results: Failure Mode Category Counts

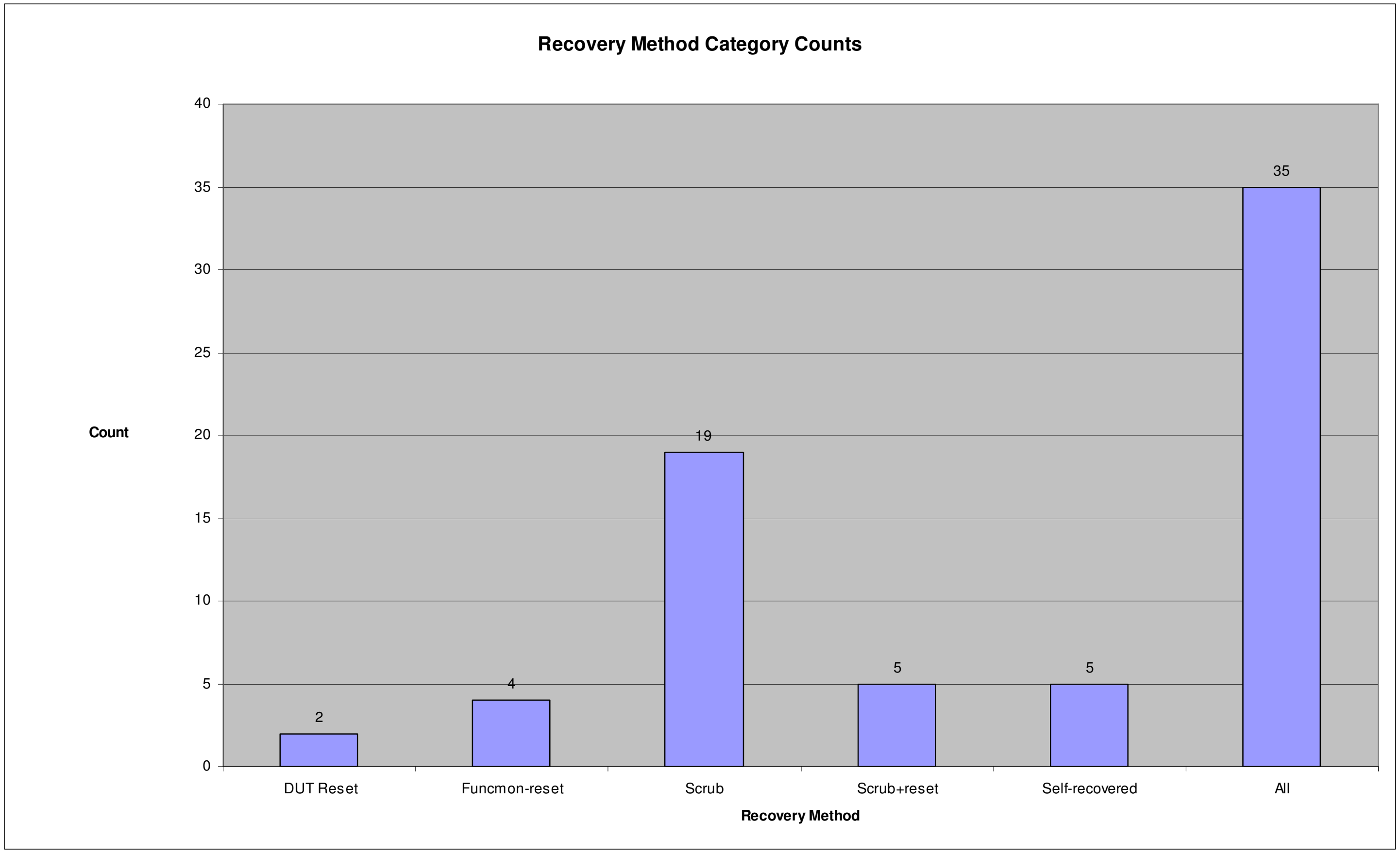


Test Results: X-section categorized by Failure Mode

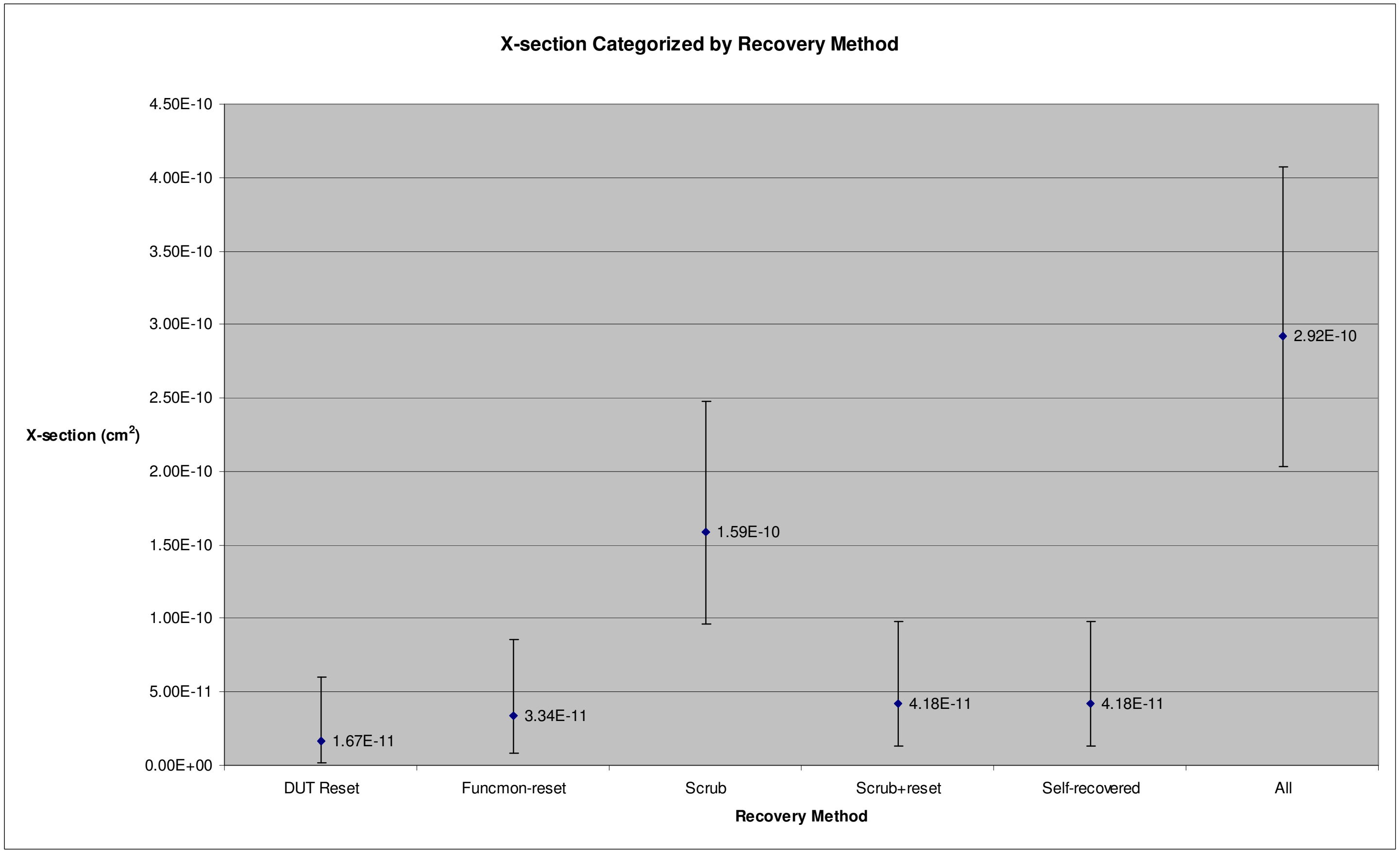


See slide 25 for the equation used to calculate the cross section.
Error bars are +/- two standard deviations based on a Poisson distribution. See slides 26 & 27.

Test Results: Recovery Method Category Counts



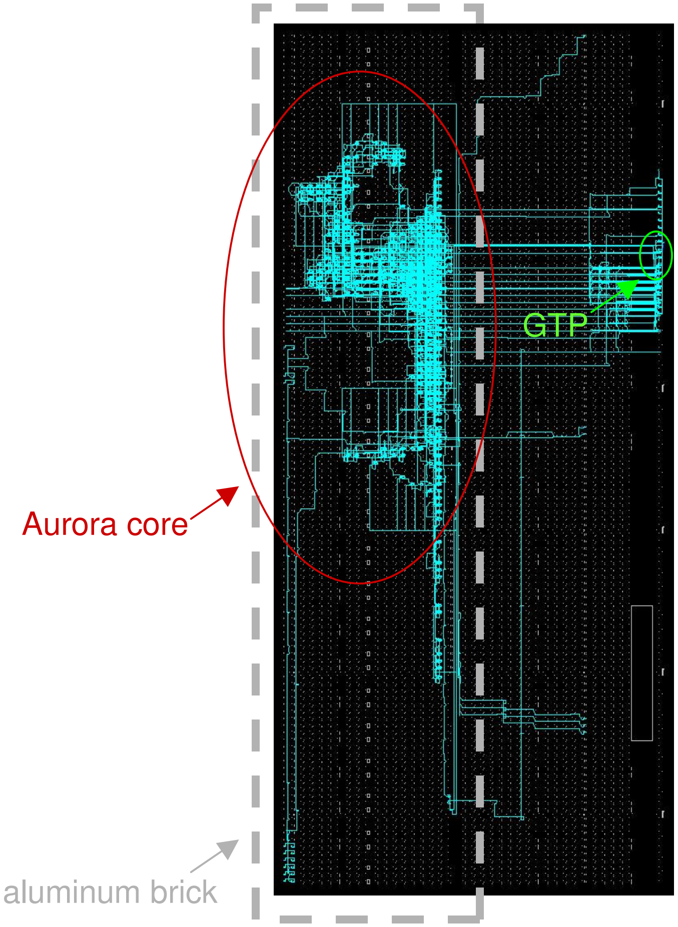
Test Results: X-section Categorized by Recovery Method



See slide 25 for the equation used to calculate the cross section.
Error bars are +/- two standard deviations based on a Poisson distribution. See slides 26 & 27.

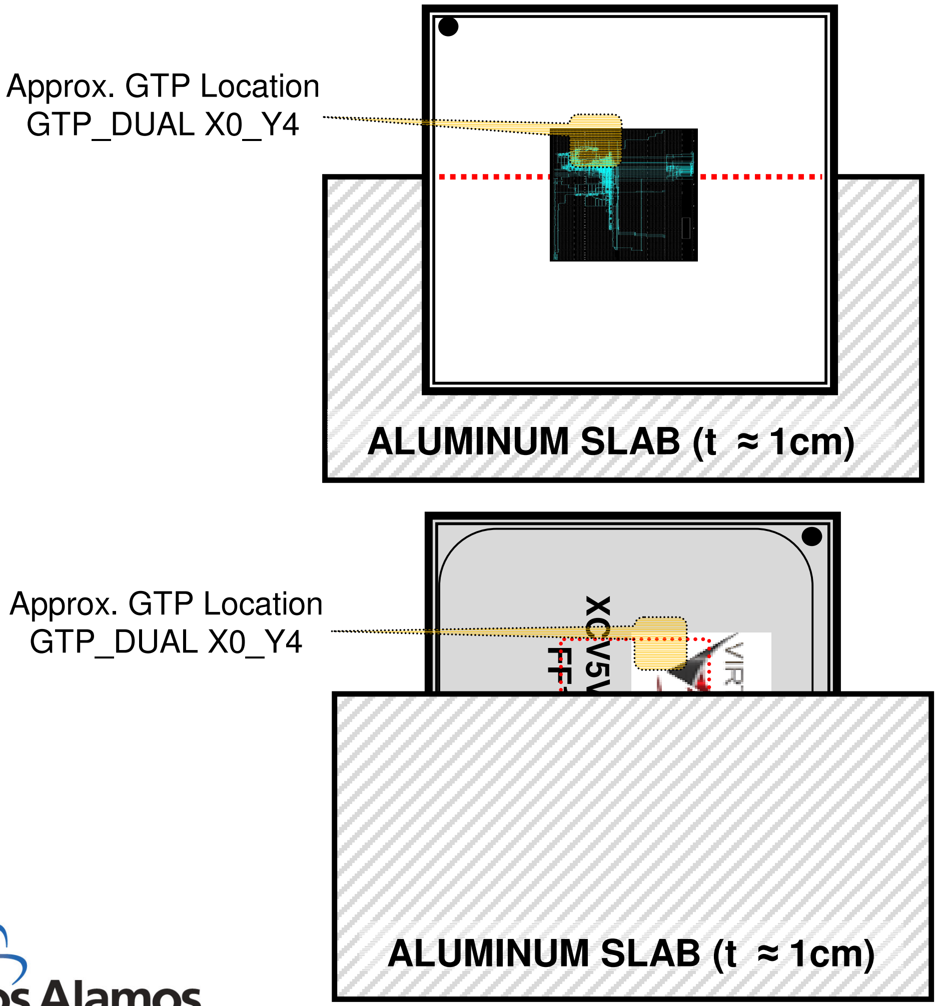
Test Setup and Methodology 2: Covered DUT

- To isolate the GTP we ‘floor-planned’ the Aurora core so it was placed on the half of the FPGA opposite from the GTP (see fpga_editor screenshot)
- We covered the Aurora core part of the FPGA die with an aluminum brick
- The test methodology remained the same
- Based on configuration bit x-section change (64% smaller x-section covered than uncovered) we covered approx. 2/3 of the die
- We only had time to gather data for two events with this test setup – we will do more testing at a later date



Screenshot of DUT placement and routing (back view)

Test Setup and Methodology 2: Covered DUT Block Diagram



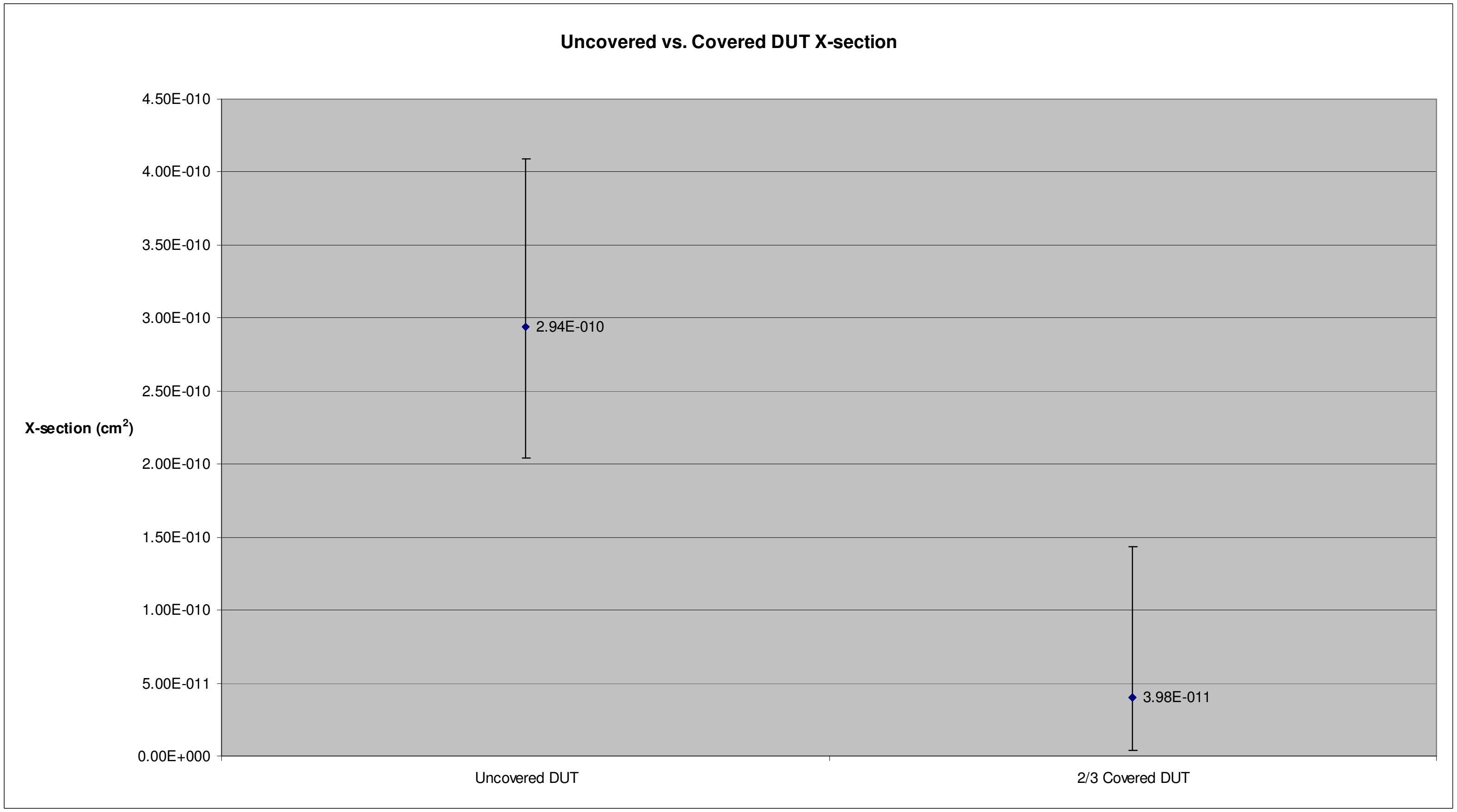
Back View

Front View

Test Results 2

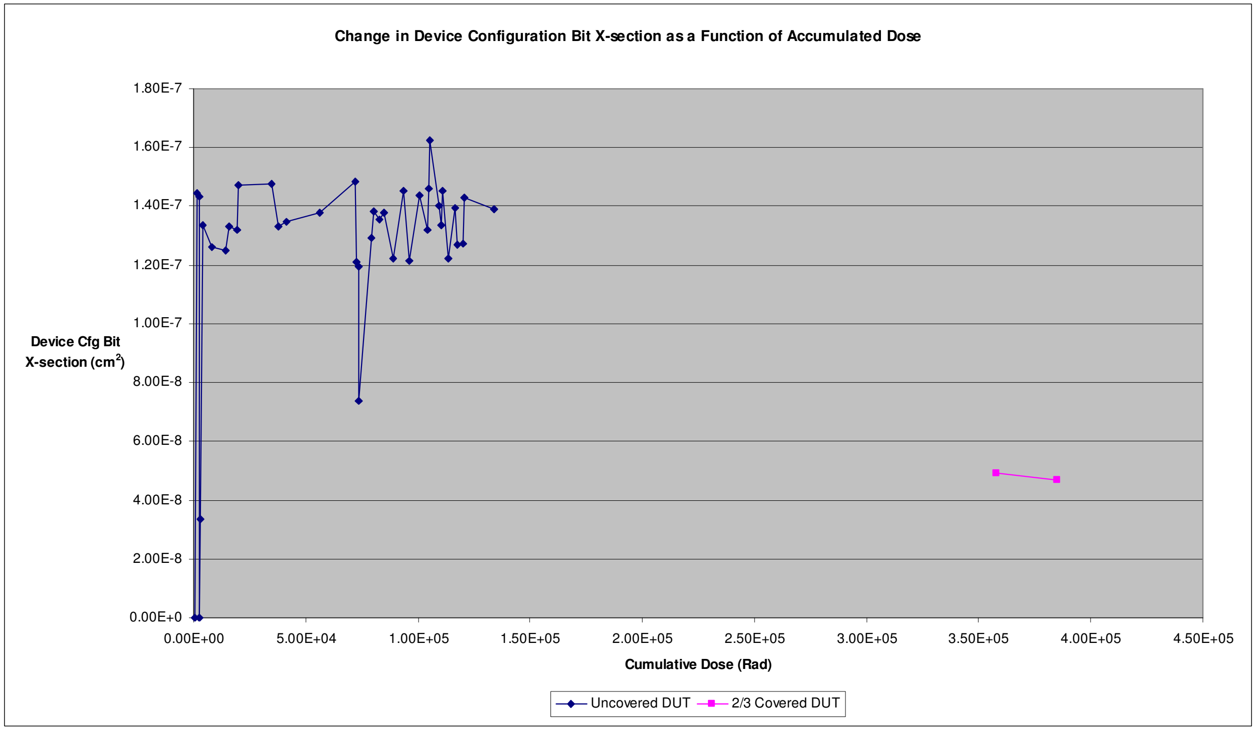
- **We only had enough time to collect data on two events**
- **Both events had the same failure mode and recovery method**
  - Failure Mode = CRC Error
  - Recovery Method = Self-recovered

Test Results 2: Uncovered vs. Covered DUT X-section



See slide 25 for the equation used to calculate the cross section.
Error bars are +/- two standard deviations based on a Poisson distribution. See slides 26 & 27.

Test Results: Dose



- 385 KRad total dose
- For a specific DUT coverage the device configuration bit x-section did not vary significantly as dose accumulated

Observations

- **GTP x-section *appears* to be an order of magnitude smaller than Aurora x-section**
  - In other words the Aurora logic dominates the x-section, not the GTP itself
  - More testing needed with the DUT partially covered
- **The primary failure mode is CRC error + missing frame**
  - Data gets corrupted more often than the entire link fails
  - It is also interesting to note that sometimes the other end of the link needs to be reset in order to get data flowing again (hypothesis: clock recovery circuit lost clock)
- **The primary recovery method is a configuration scrub**
  - A system that uses configuration scrubbing can significantly improve availability
  - A system that uses scrubbing and asserts reset every time failure is detected can improve availability even more
  - A full DUT reconfigure or a DUT power-cycle was never required for recovery
- **There was not a one-to-one relationship between failure mode and recovery method**

Proposed Test Enhancements

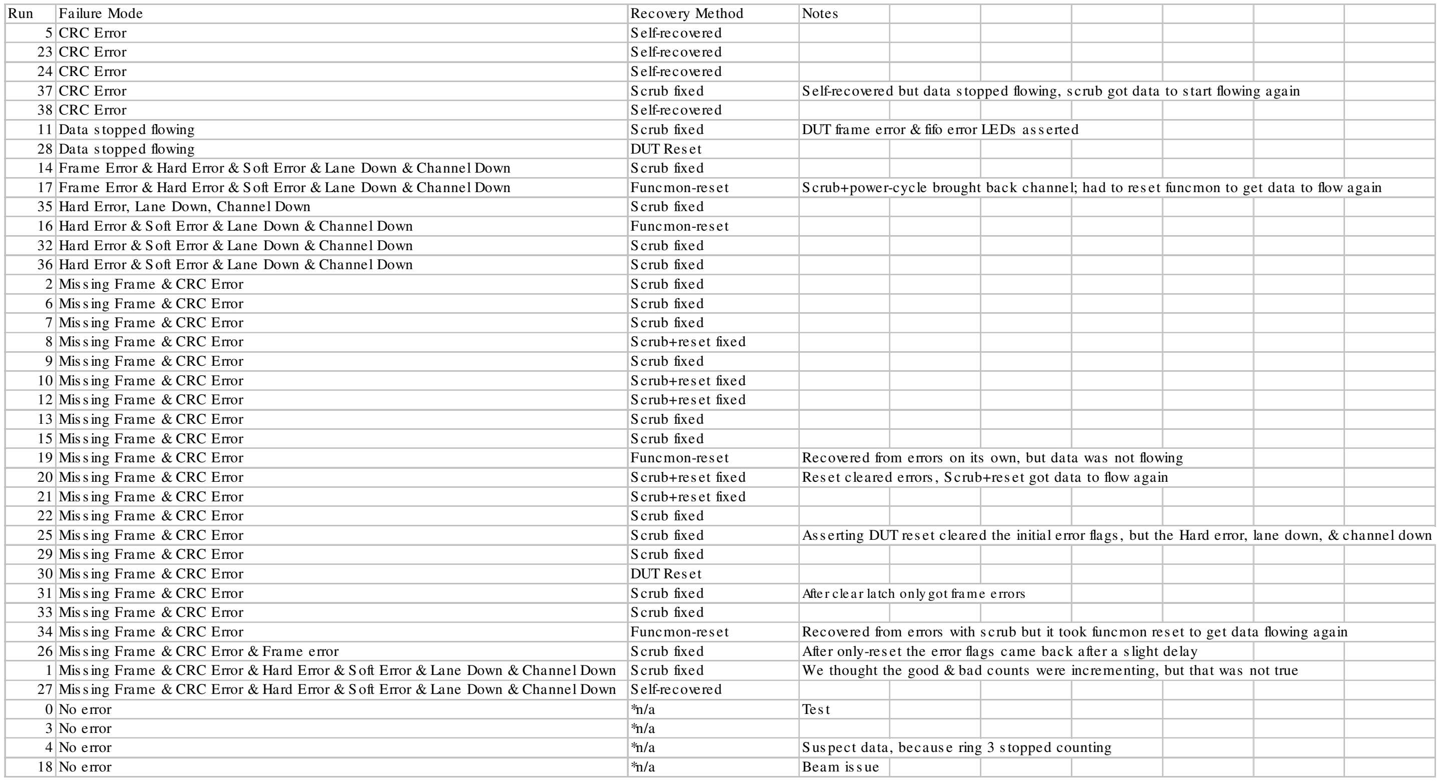
- **Current test setup**
  - Add heartbeat monitor
  - Add software timestamps
  - Separate the funcmon and DUT power supply controls
  - Integrate the various SW (term, iMPACT scripts, power supply control)
- **Port setup to Xilinx Radiation Test Consortium (XRTC) test fixture**
  - Build Virtex-5 LX50T daughter-card
  - Test using continuous scrubbing

Future Test Plans

- Protons on December 4th and 5th at Indiana University Cyclotron Facility
- Other trips TBD
- Test GTP using PCI Express protocol

Backup Slides

Data Results: Breakdown by Failure Mode



Run	Failure Mode	Recovery Method	Notes
5	CRC Error	Self-recovered	
23	CRC Error	Self-recovered	
24	CRC Error	Self-recovered	
37	CRC Error	Scrub fixed	Self-recovered but data stopped flowing, scrub got data to start flowing again
38	CRC Error	Self-recovered	
11	Data stopped flowing	Scrub fixed	DUT frame error & fifo error LEDs asserted
28	Data stopped flowing	DUT Reset	
14	Frame Error & Hard Error & Soft Error & Lane Down & Channel Down	Scrub fixed	
17	Frame Error & Hard Error & Soft Error & Lane Down & Channel Down	Funcmon-reset	Scrub+power-cycle brought back channel; had to reset funcmon to get data to flow again
35	Hard Error, Lane Down, Channel Down	Scrub fixed	
16	Hard Error & Soft Error & Lane Down & Channel Down	Funcmon-reset	
32	Hard Error & Soft Error & Lane Down & Channel Down	Scrub fixed	
36	Hard Error & Soft Error & Lane Down & Channel Down	Scrub fixed	
2	Missing Frame & CRC Error	Scrub fixed	
6	Missing Frame & CRC Error	Scrub fixed	
7	Missing Frame & CRC Error	Scrub fixed	
8	Missing Frame & CRC Error	Scrub+reset fixed	
9	Missing Frame & CRC Error	Scrub fixed	
10	Missing Frame & CRC Error	Scrub+reset fixed	
12	Missing Frame & CRC Error	Scrub+reset fixed	
13	Missing Frame & CRC Error	Scrub fixed	
15	Missing Frame & CRC Error	Scrub fixed	
19	Missing Frame & CRC Error	Funcmon-reset	Recovered from errors on its own, but data was not flowing
20	Missing Frame & CRC Error	Scrub+reset fixed	Reset cleared errors, Scrub+reset got data to flow again
21	Missing Frame & CRC Error	Scrub+reset fixed	
22	Missing Frame & CRC Error	Scrub fixed	
25	Missing Frame & CRC Error	Scrub fixed	Asserting DUT reset cleared the initial error flags, but the Hard error, lane down, & channel down
29	Missing Frame & CRC Error	Scrub fixed	
30	Missing Frame & CRC Error	DUT Reset	
31	Missing Frame & CRC Error	Scrub fixed	After clear latch only got frame errors
33	Missing Frame & CRC Error	Scrub fixed	
34	Missing Frame & CRC Error	Funcmon-reset	Recovered from errors with scrub but it took funcmon reset to get data flowing again
26	Missing Frame & CRC Error & Frame error	Scrub fixed	After only-reset the error flags came back after a slight delay
1	Missing Frame & CRC Error & Hard Error & Soft Error & Lane Down & Channel Down	Scrub fixed	We thought the good & bad counts were incrementing, but that was not true
27	Missing Frame & CRC Error & Hard Error & Soft Error & Lane Down & Channel Down	Self-recovered	
0	No error	*n/a	Test
3	No error	*n/a	
4	No error	*n/a	Suspect data, because ring 3 stopped counting
18	No error	*n/a	Beam issue

Cross Section Calculation Equation

- **The total cross section σ was calculated as the total number of failure events divided by the total fluence for all runs**
- **The cross section σ_c for a particular category *c* was calculated as the total number of events for that category divided by the total fluence for all runs**

$$\sigma = \frac{\#events}{\sum_{i}^{n} fluence_i}$$

$$\sigma = \text{cross section}$$

$$i = \text{run number}$$

$$n = \text{total num runs}$$

e.g.

$$\sigma = \frac{35}{\sum_{i}^{39} fluence_i}$$

$$= \frac{35}{1.2 \times 10^{11}}$$

$$= 2.94 \times 10^{-10}$$

Error Bars Calculation (source: Swift, 2006)

- We assumed a Poisson distribution
- To capture 95% of the range of the real cross section σ we plotted the error bars +/- two standard deviations
- For data sets with more than 100 events the standard deviation can be approximated as the square root of the number of events
- Since our data set has less than 100 events we had to use the 95% confidence table (see pTable on next slide) from "The Concept of Confidence or Fiducial Limits Applied to the Poisson Frequency Distribution" by W. E. Ricker, Journal of the American Statistical Association, v 32, (1937) pp. 349-386.
- Pseudo-Excel equations…

$$\mathrm{Count}_1 = \mathrm{IF}((\#\mathrm{events} > 50), \#\mathrm{events} - 2 * \mathrm{SQRT}(\#\mathrm{events}), \mathrm{VLOOKUP}(\#\mathrm{events}, \mathrm{pTable}, 2))$$

$$\mathrm{Err}_1 = \mathrm{ABS}(\mathrm{Count}_1/\mathrm{fluence}) - \sigma_{\mathrm{mean}}$$

$$\mathrm{Count}_2 = \mathrm{IF}((\#\mathrm{events} > 50), \#\mathrm{events} + 2 * \mathrm{SQRT}(\#\mathrm{events}), \mathrm{VLOOKUP}(\#\mathrm{events}, \mathrm{pTable}, 3))$$

$$\mathrm{Err}_2 = \mathrm{ABS}(\mathrm{Count}_2/\mathrm{fluence}) - \sigma_{\mathrm{mean}}$$

Suggested Error Bars for 95% (source: Swicker, 1937)

pTable

	95% Limits	
N	lower	upper
0	0.0	3.7
1	0.1	5.6
2	0.2	7.2
3	0.6	8.8
4	1.0	10.2
5	1.6	11.7
6	2.2	13.1
7	2.8	14.4
8	3.4	15.8
9	4.0	17.1
10	4.7	18.4
11	5.4	19.7
12	6.2	21.0
13	6.9	22.3
14	7.7	23.5
15	8.4	24.8
16	9.4	26.0
17	9.9	27.2
18	10.7	28.4
19	11.5	29.6
20	12.2	30.8
21	13.0	32.0
22	13.8	33.2
23	14.6	34.4
24	15.4	35.6
25	16.2	36.8
26	17.0	38.0
27	17.8	39.2
28	18.6	40.4
29	19.4	41.6
30	20.2	42.8
31	21.0	44.0
32	21.8	45.1
33	22.7	46.3
34	23.5	47.5
35	24.3	48.7
36	25.1	49.8
37	26.0	51.0
38	26.8	52.2
39	27.7	53.3
40	28.6	54.5
41	29.4	55.6
42	30.3	56.8
43	31.1	57.9
44	32.0	59.0
45	32.8	60.2
46	33.6	61.3
47	34.5	62.5
48	35.3	63.6
49	36.1	64.8
50	37.0	65.9

Efficiency Calculation Equation

$$E = 100 \frac{n}{n + 4 + 0.5 + [\frac{w}{2} - 1] + \frac{12(n+o)}{9{,}988} + o + i}$$

Where:

E = The average efficiency (as a percentage) of a specified PDU

n = Number of user data bytes

4 = The overhead of SCP + ECP (start of frame + end of frame)

0.5 = The average PAD overhead

w = Interface width (e.g. 1 byte, 2 bytes, 4 bytes)

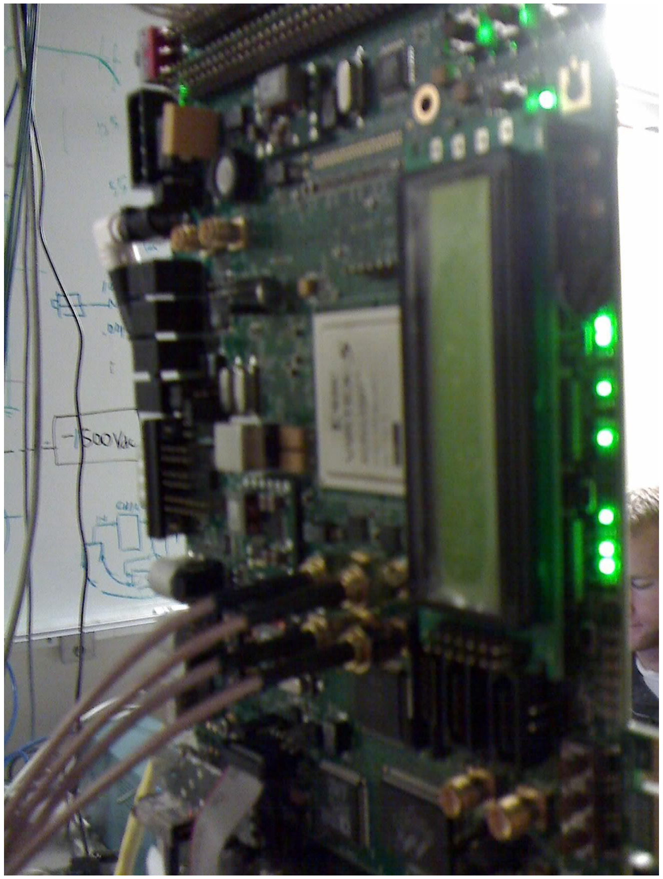
o = Frame overhead bytes (specific to our implementation)

12(n + o)/9,998 = Clock correction overhead

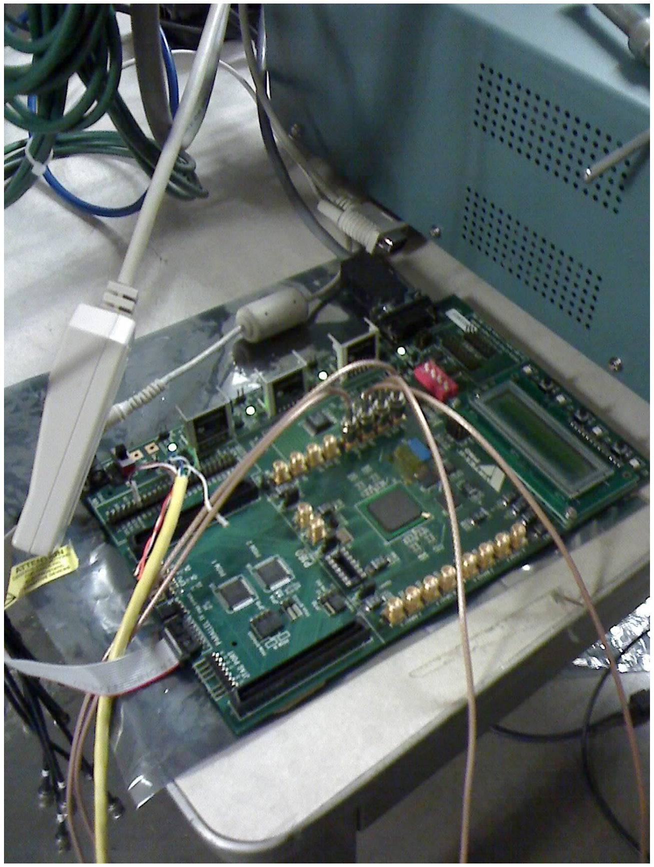
i = Idle transmission bytes (specific to our implementation)

Adapted from: Xilinx LogiCORE Aurora v2.7 User Guide; UG061 (v2.7) May 17, 2007; page 44

Test Setup: Picture



DUT (ML505 board w/XC5VLX50T)



Funcmon (Memec V2Pro board w/XC2VP7)