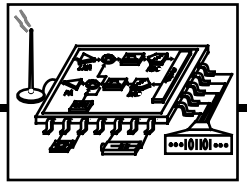
A Multi-Standard Monolithic CMOS RF Transceiver

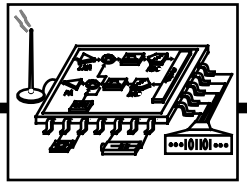
Thomas Cho, Jacques Rudell, Jeff Ou,
Todd Weigandt, Sekhar Narayanaswami,
Srenik Mehta, George Chien,
Carrol Barrett, Francesco Brianti*,
and Prof. Paul Gray.

University of California, Berkeley
***SGS Thomson**

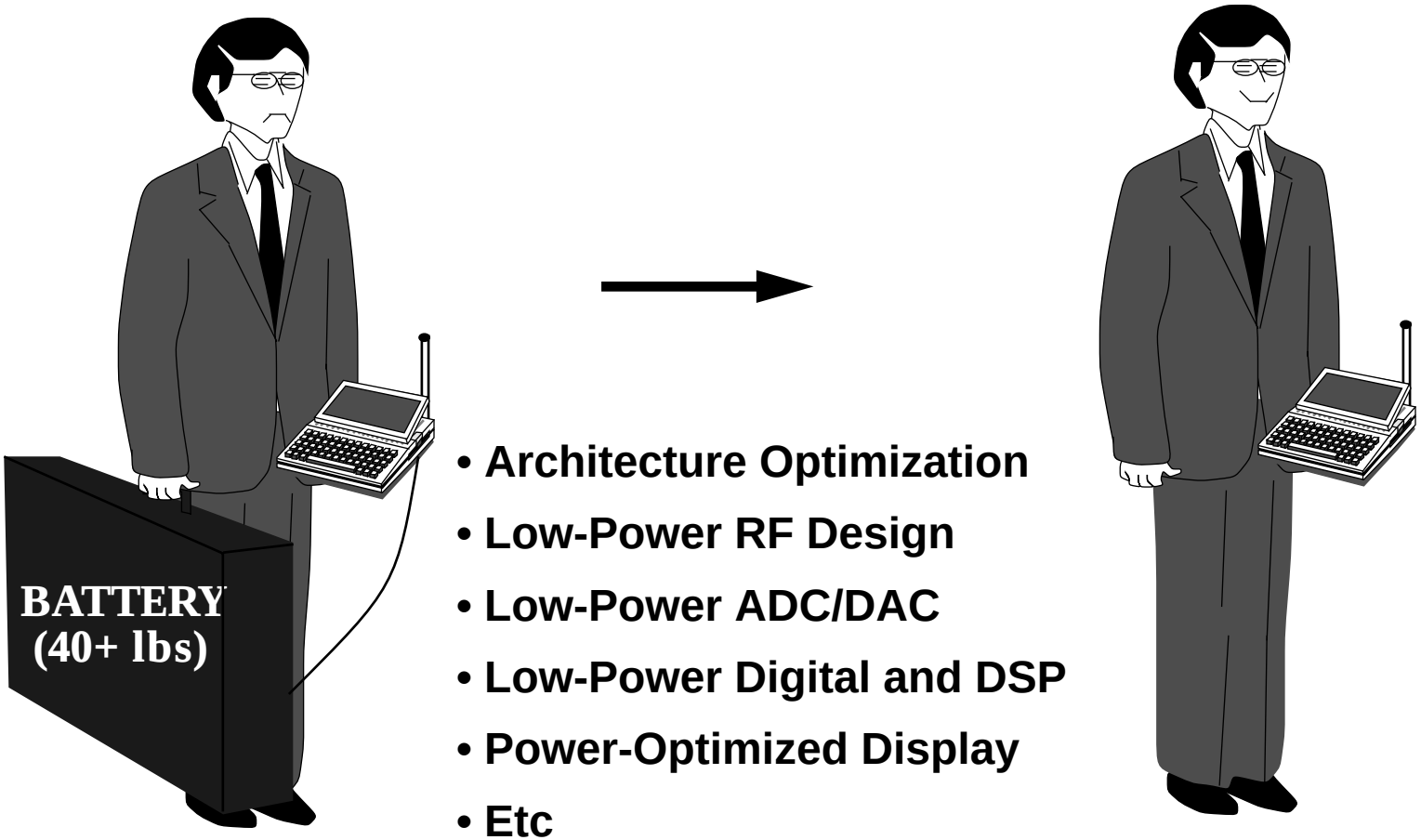


Outline

- Background/Motivation
- A monolithic CMOS RF transceiver
- Design considerations
- Key building blocks
- Future plan

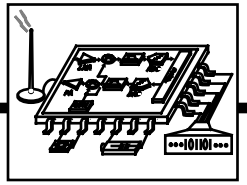


Low Power Terminal Design



- **Architecture Optimization**
- **Low-Power RF Design**
- **Low-Power ADC/DAC**
- **Low-Power Digital and DSP**
- **Power-Optimized Display**
- **Etc**

Next Step:
Multi-Standard, Adaptive Modes of Communication



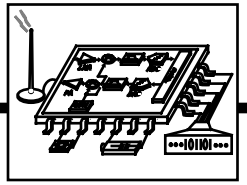
Overall Objective

Single RF Modem with interface capability to:

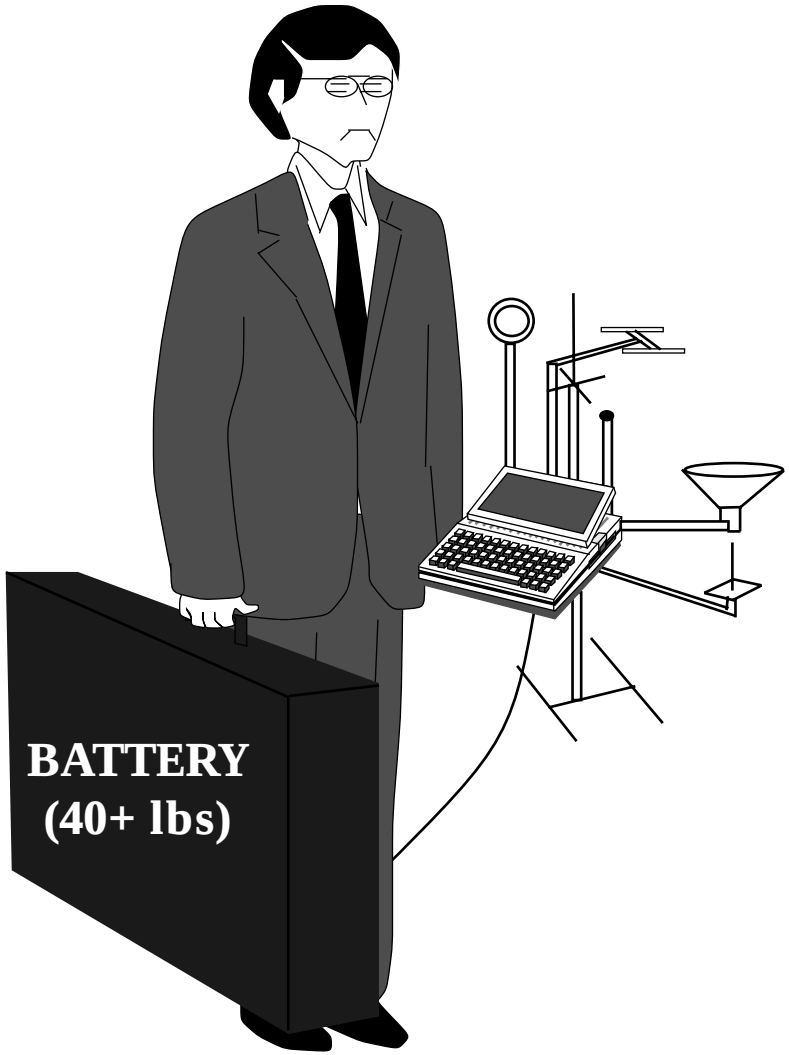
- **Public Cellular Network**
- **Cordless Phones/PBXs**
- **Wireless LANs**
- **Other emerging PCS Systems**

Focus of this research:

- **What are the important technical problems from the perspective of the RF modem design?**



Adaptive, Multistandard RF Modems



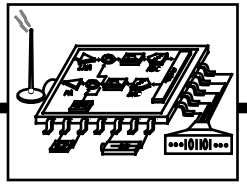
Motivation

Design Goal:

- Radio transceiver for personal communications.

Design Objectives:

- Low power consumption
- Low cost implementation
- Multi-Standard capability



Research Goals

- **Single-chip implementation**

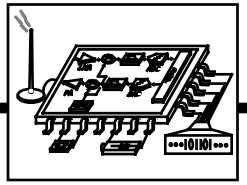
  Integrate both RF & Baseband circuits on the same chip

  Eliminate off-chip high frequency signal paths to reduce off-chip components for low power, low cost & smaller form factors
  (ext. LC-tank, ext. IF BPF, ..)

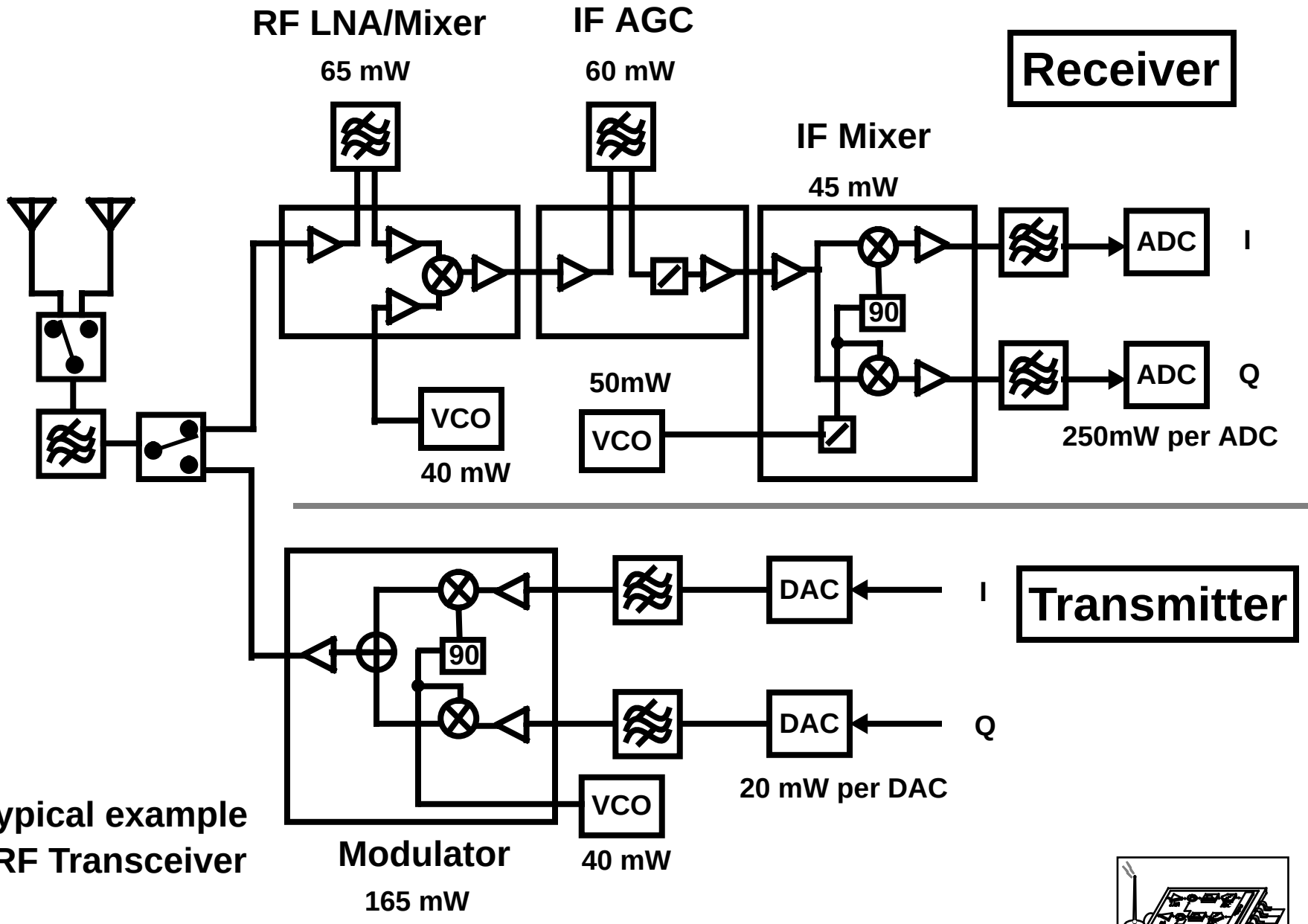
  Baseband digital signal processing for programmable multistandard capability

- **CMOS technology**

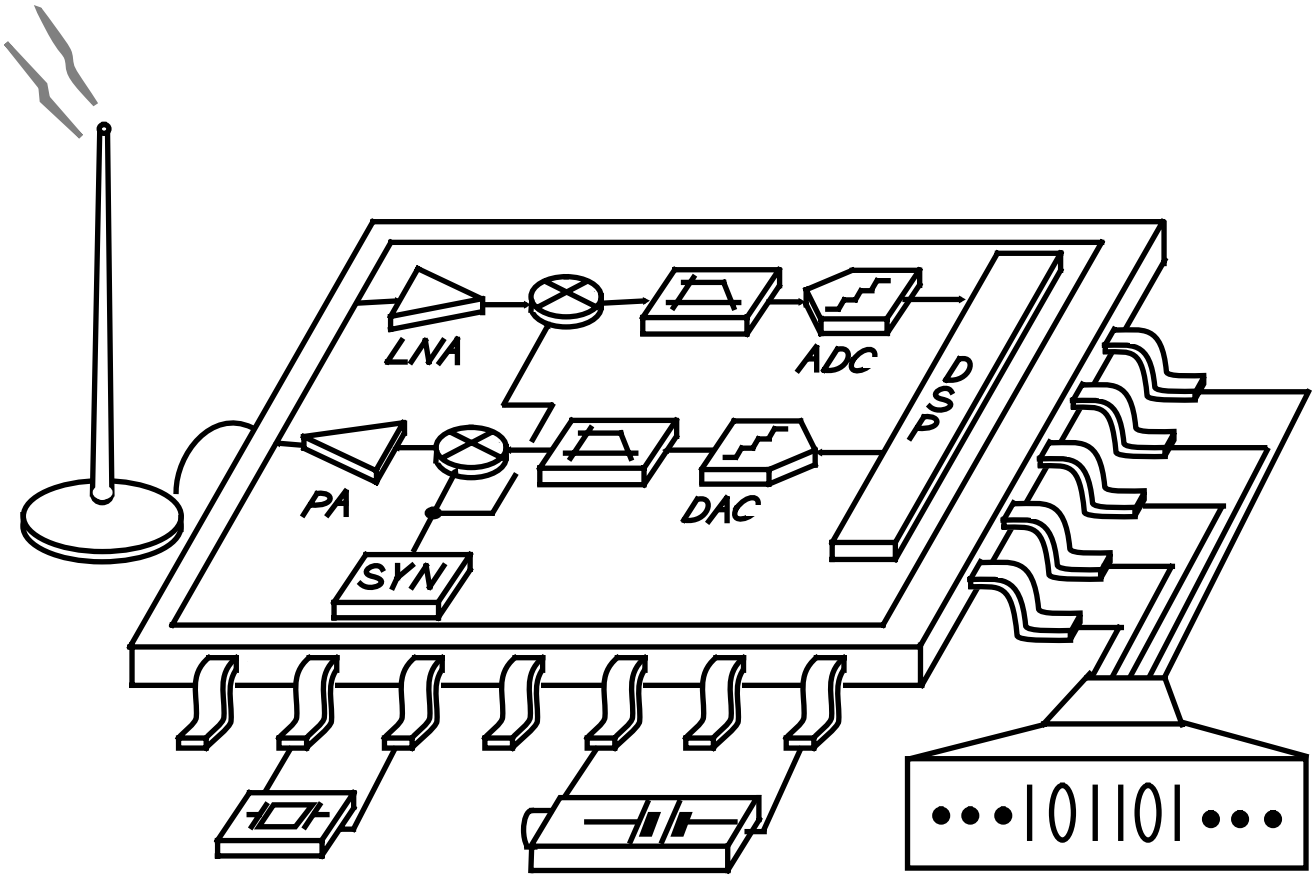
  High integration and low cost



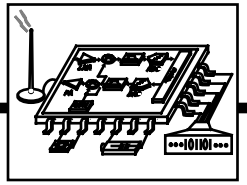
Conventional Approach



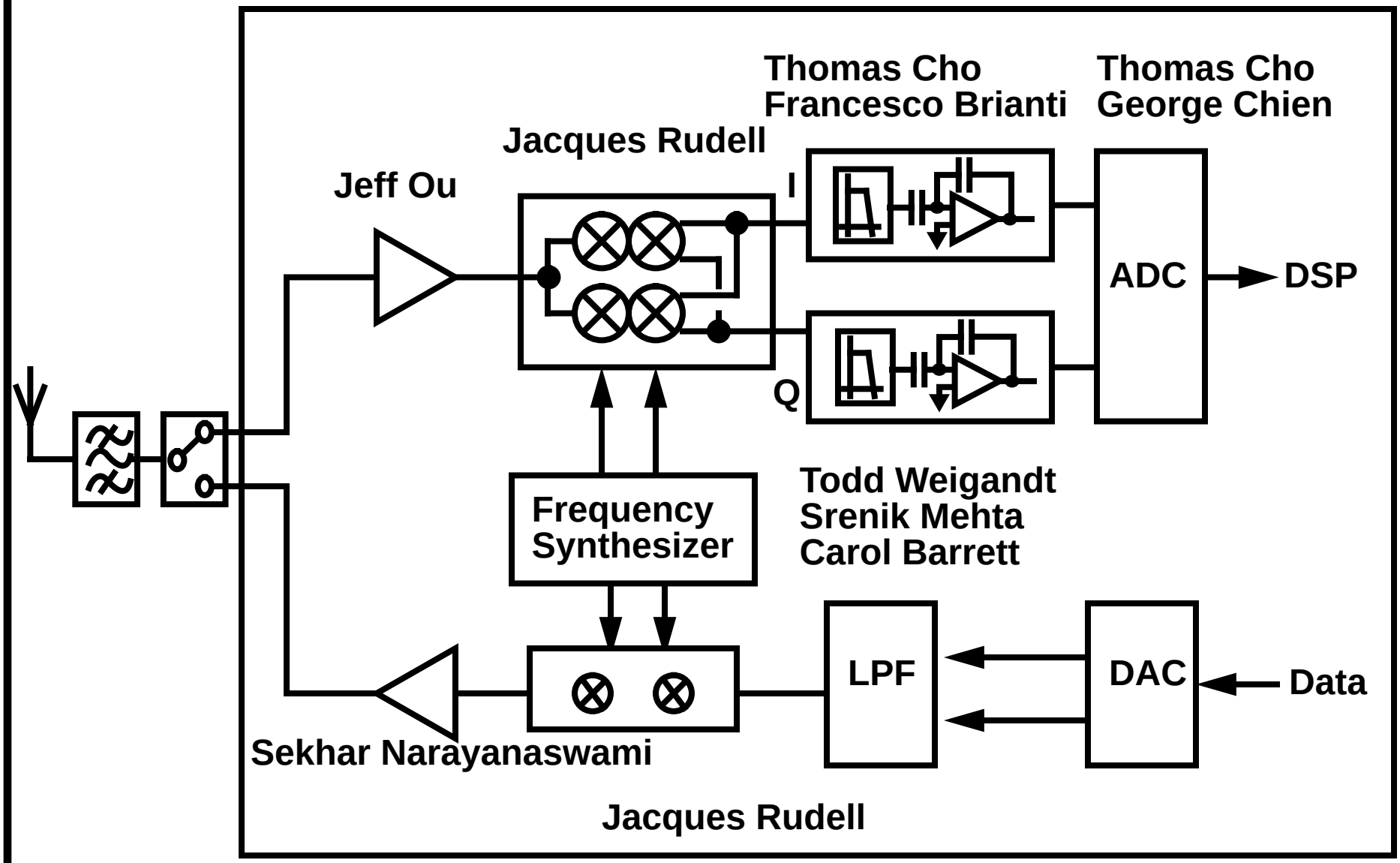
Our Approach



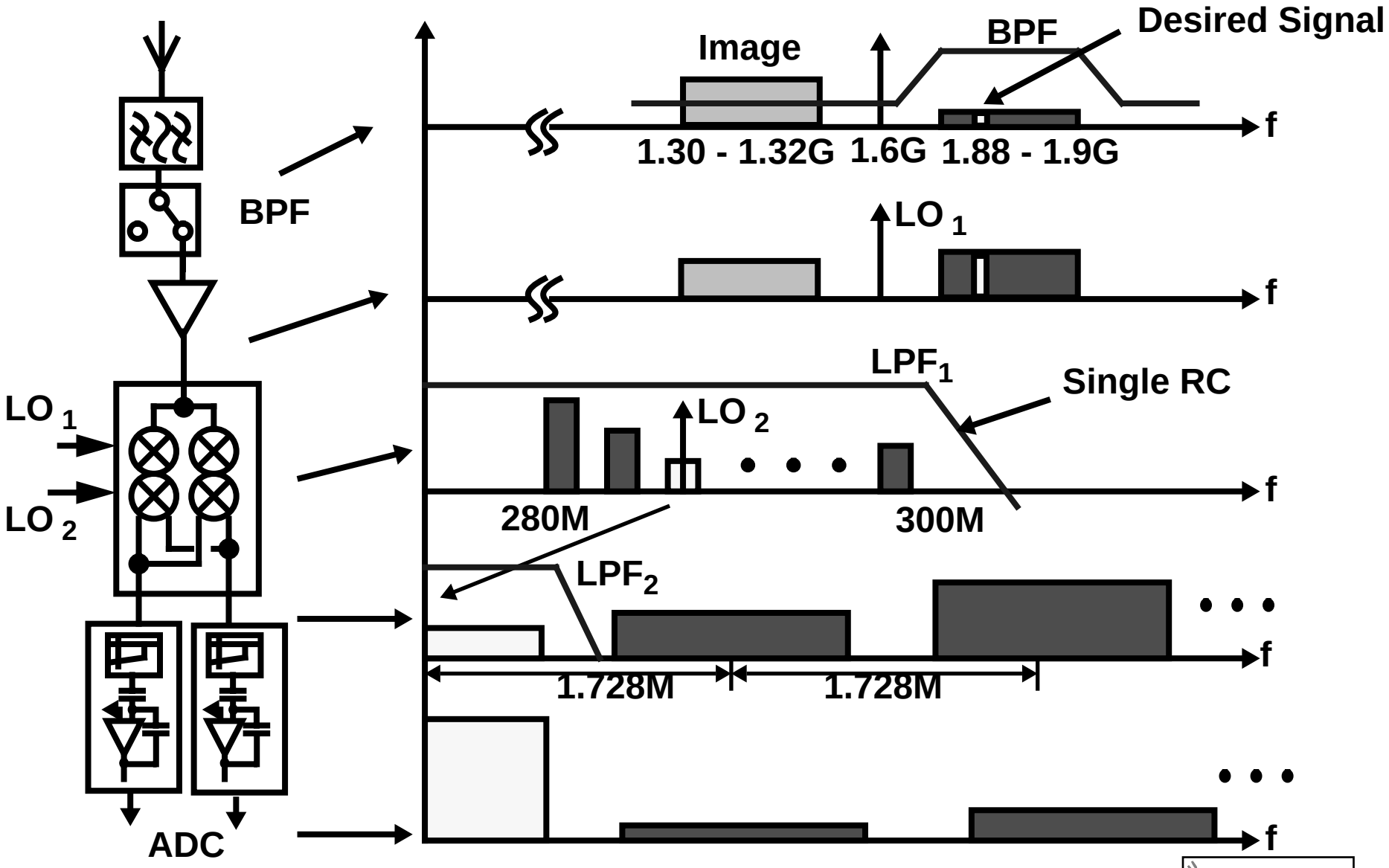
- **Using DECT standard as a vehicle to study various problems/issues**



A Quasi-Direct Conversion Approach

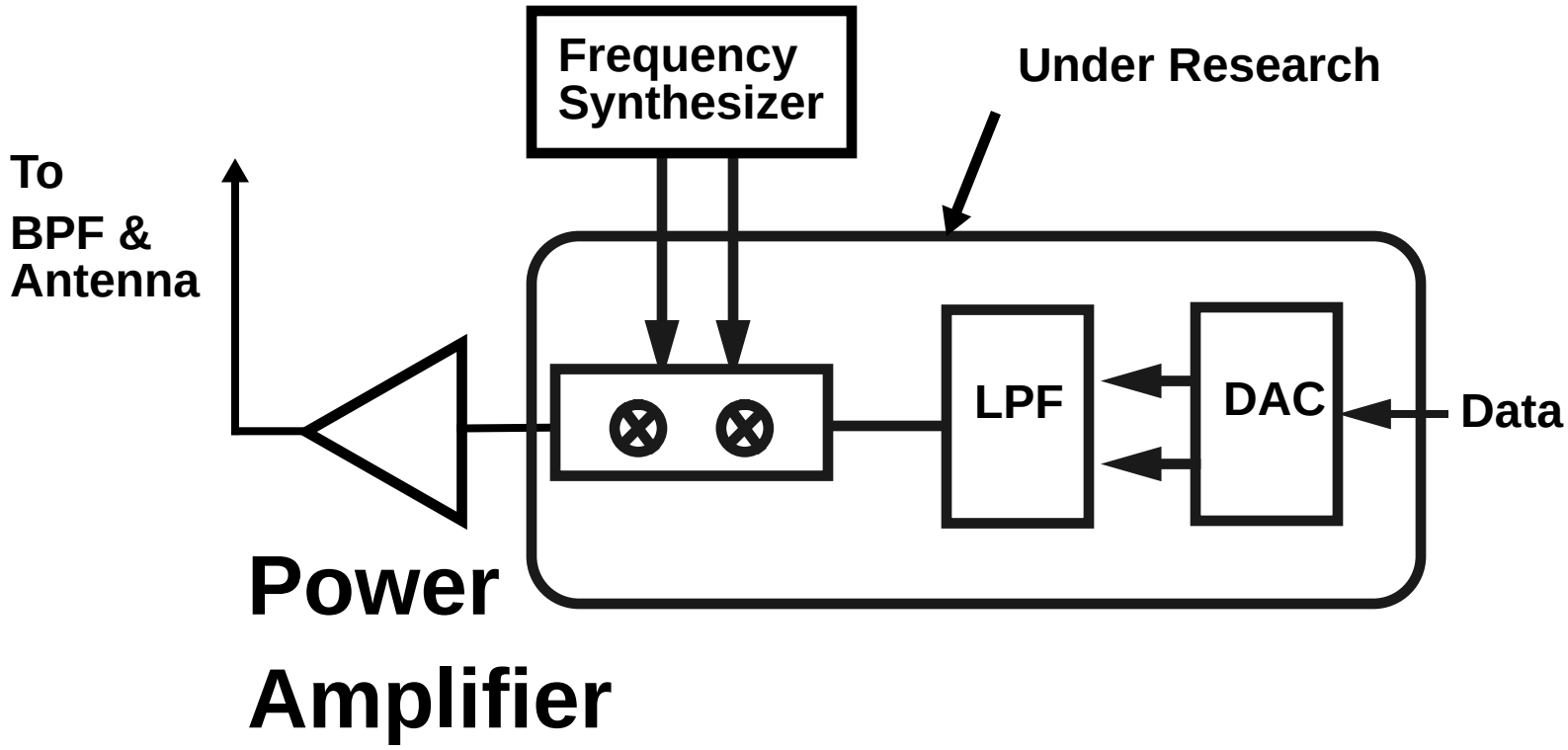


Receiver Path (DECT)



Transmitter Path (DECT)

- Power Amplifier(PA) design is near completion.
- Transmitter architecture still in early research phase



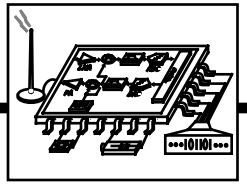
What's different?

A Quasi-Direct Conversion Receiver

- **No external IF BPF**
  => Little or No IF Filtering
  => Selective filtering at Baseband

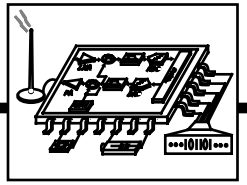
- **Two Local Osc. freq's.**
  LO_1 : a fixed freq. osc
  LO_2 : a tuned osc to the desired channel

  => Elimination of carrier feedthrough compared to direct conversion arch.
  => Relaxed phase noise requirement on LO_2 (tuned osc).

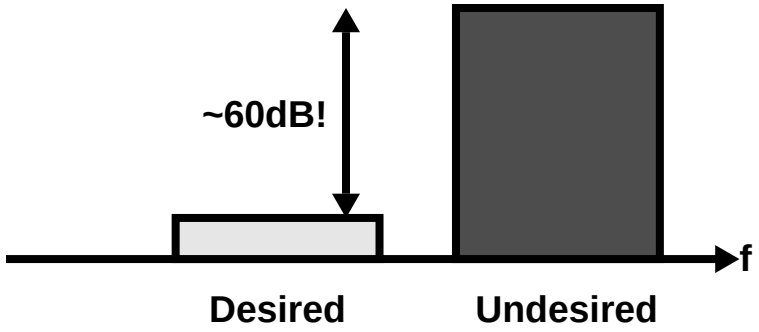


Design Challenges

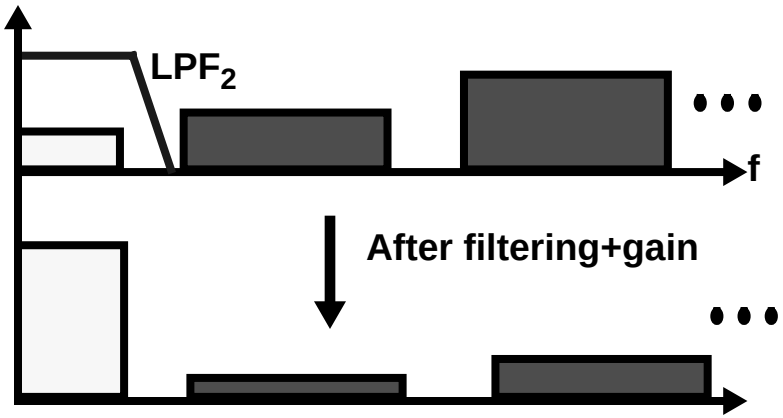
- **System:**
  - **Data recovery in the presence of strong interferers and noise w/o ext. IF filters!**
  - **Image-Reject Mixer required**
  - **Low phase noise osc w/o ext. high-Q LC tank**
- **Circuit:**
  - **CMOS design**
  - **Power efficient circuit topologies**
  - **Low voltage design: 3.3V**



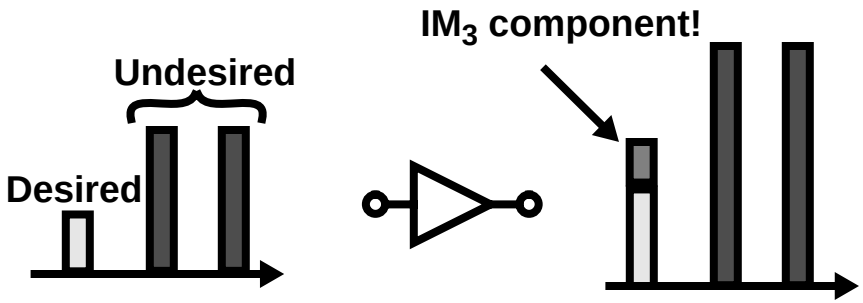
Design Considerations (I): System



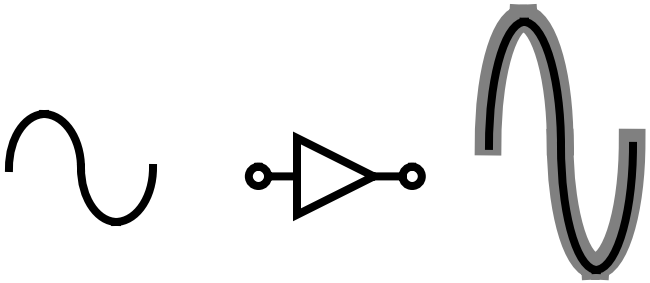
Proper signal level control along the receiver signal path



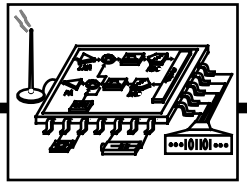
Baseband channel select filter/gain design



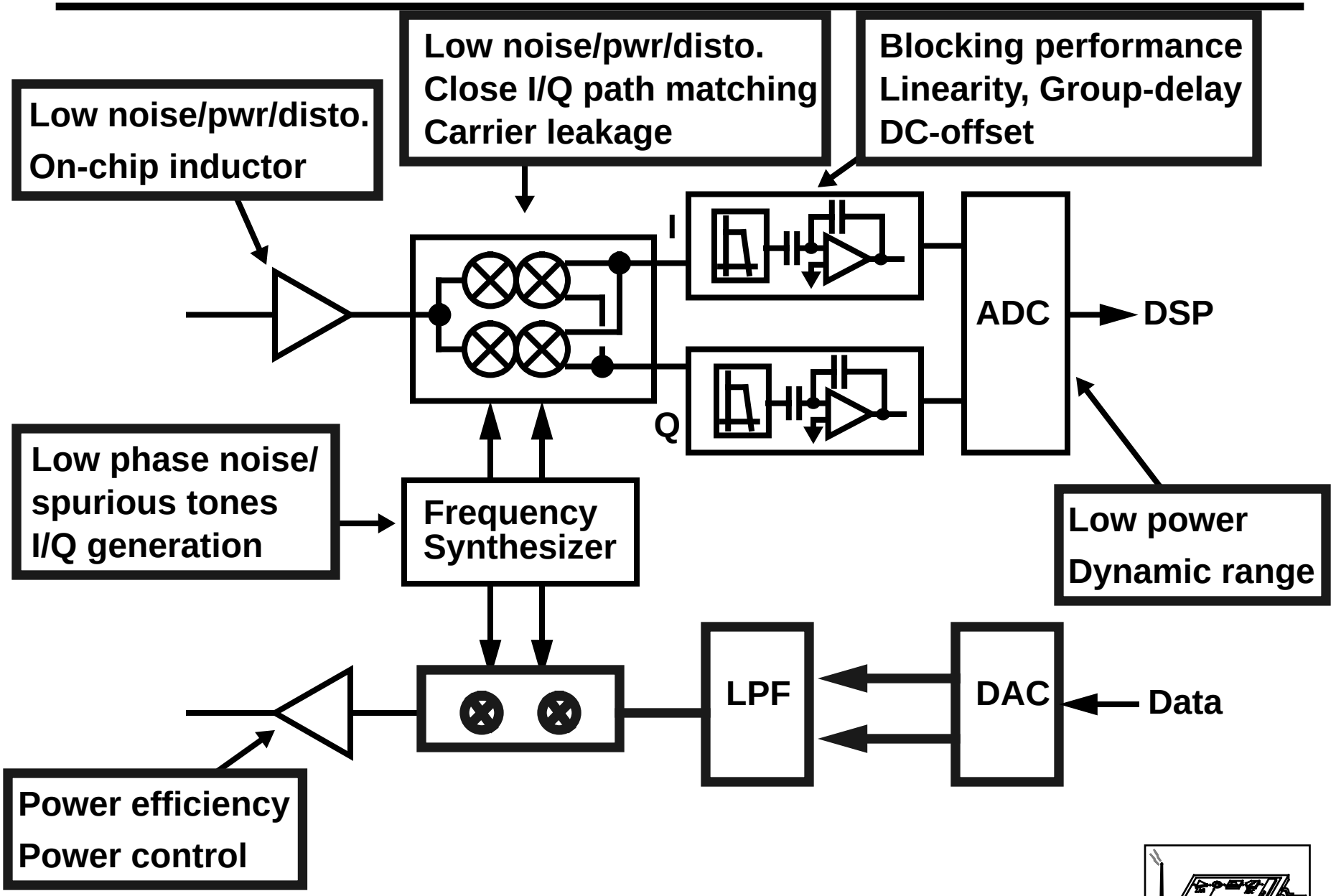
Distortion performance: Intermodulation(IM_3)



Noise performance: Power vs. noise

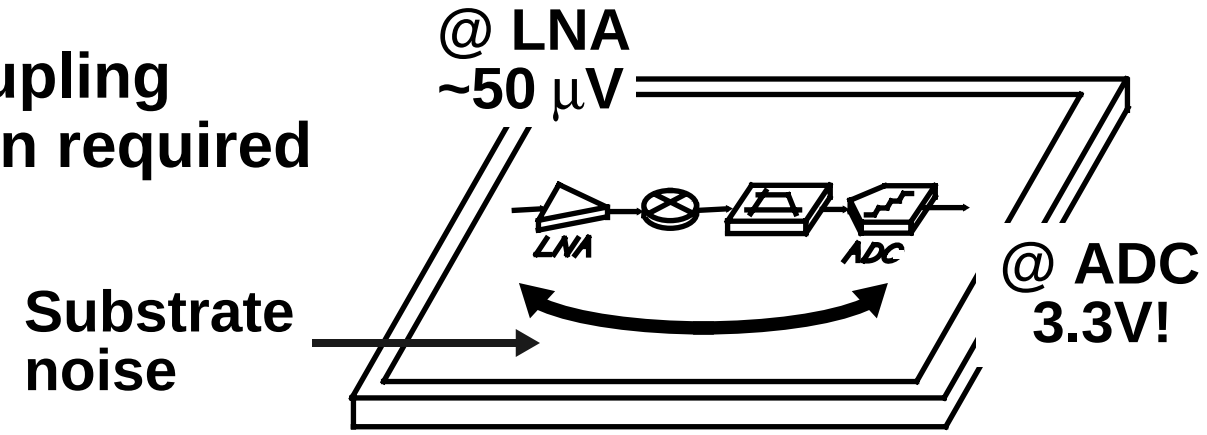


Design Considerations (II):Block

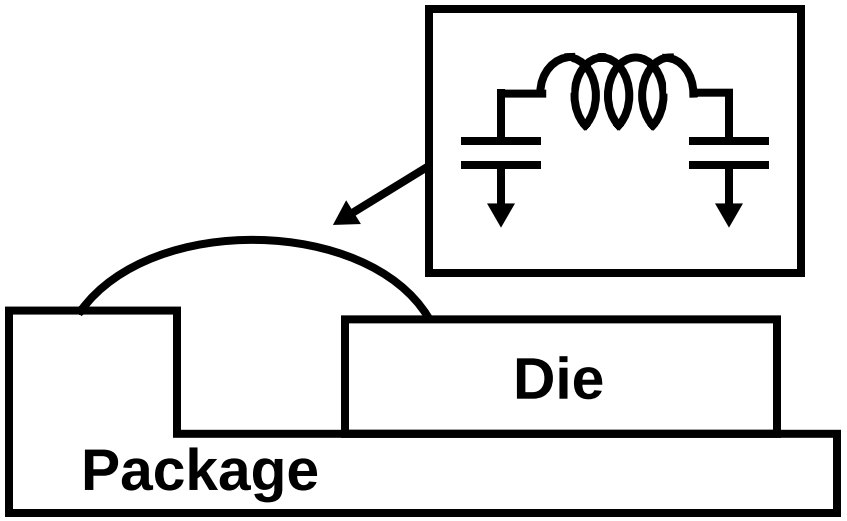


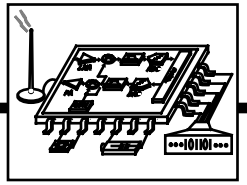
Design Considerations (III): Others

- **Substrate noise coupling**
  - **Noise isolation required**



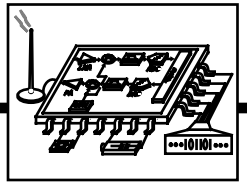
- **Package modelling**
  - **Bond wire modelling for LNA & PA's I/O impedance matching**





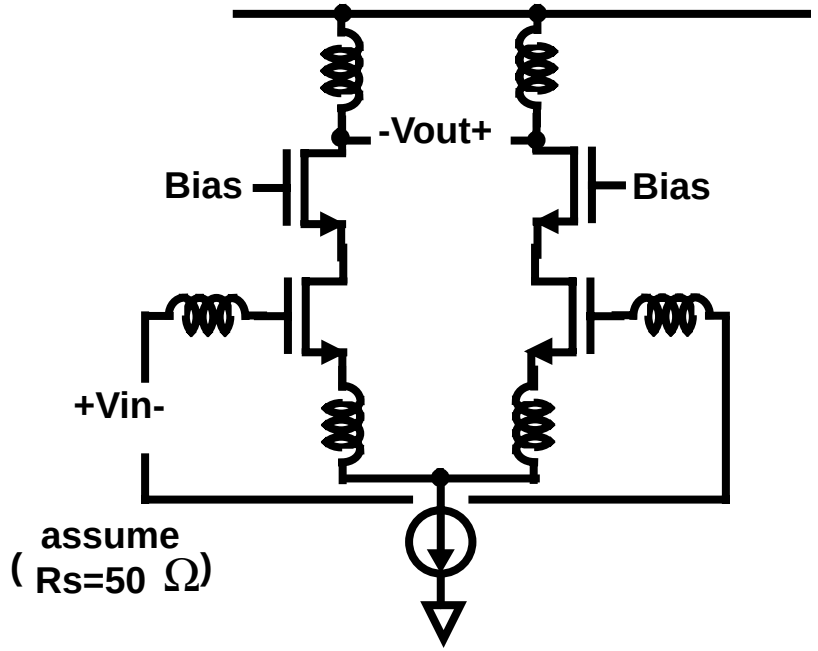
Key Building Blocks

- **LNA : Jeff Ou**
- **Image-Reject Mixer : Jacques Rudell**
- **Freq. Synthesizer : Todd Weigandt, Srenik Mehta, Carol Barrett**
- **Baseband Filter /Gain : Thomas Cho, Francesco Brianti**
- **A/D Convertert : Thomas Cho, George Chien**
- **PA : Sekhar Narayanaswami**



RF Low Noise Amplifier

- A single-stage differential-mode amplifier
- On-chip spiral inductors for input impedance matching and output load tuning
- Critical Issues: Modelling of spiral inductors, Package modelling..



Noise Figure: 2.1 dB

Gain: 20dB @1.9GHz

IP3: -2 dBm (input)

Power: 20mW @3V

Tech: 0.6 μm CMOS

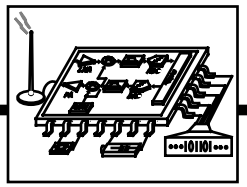
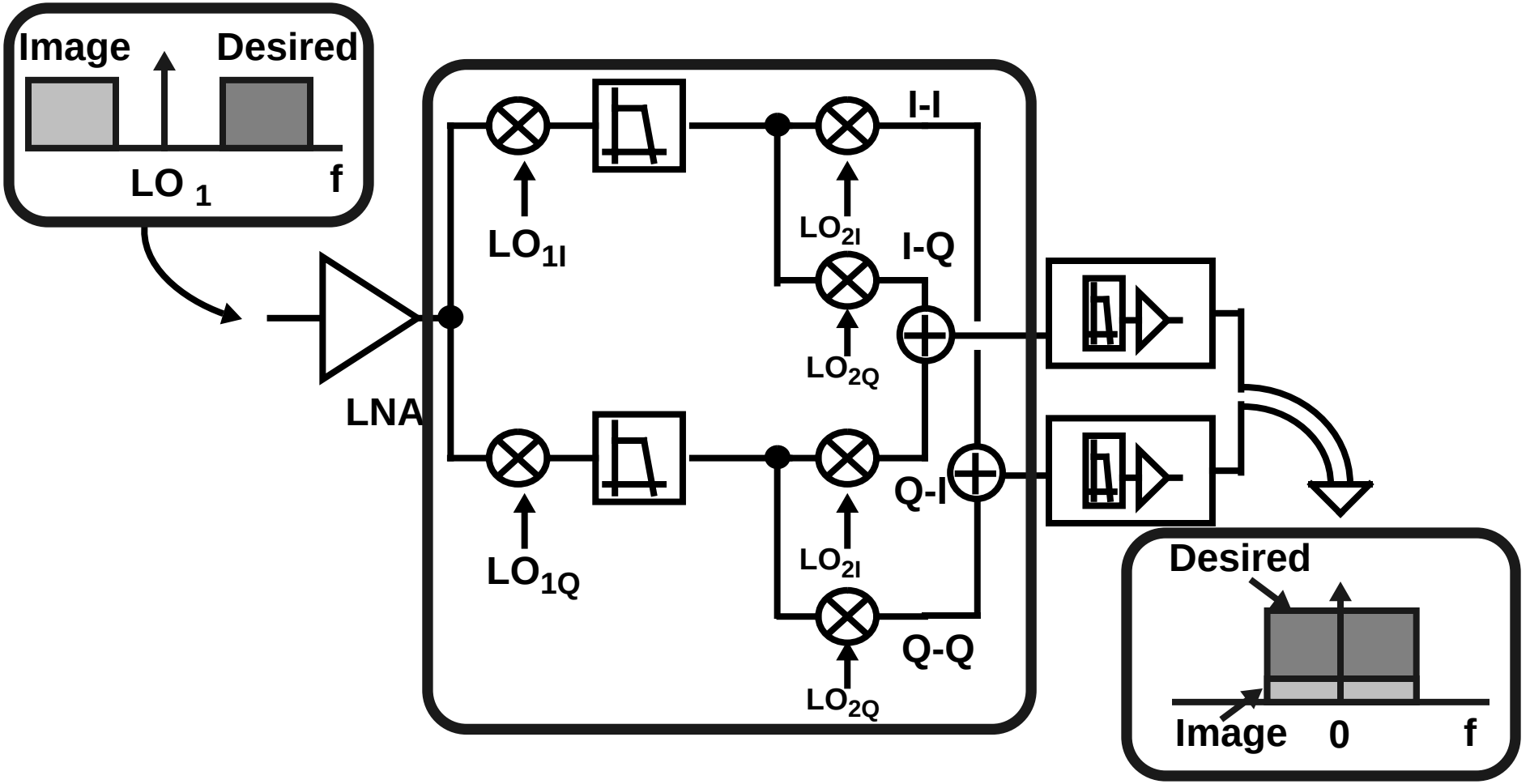


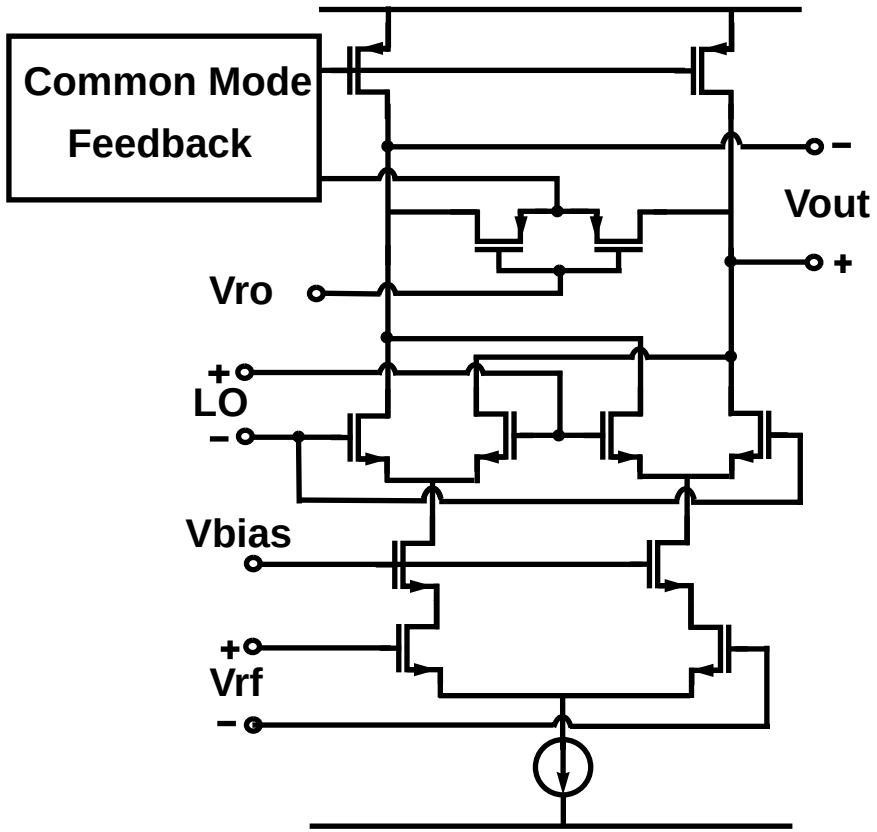
Image-Reject Mixer



- **Extra 35dB of image rejection required due to insufficient image rejection from RF BPF**

Image Reject Mixer Cell

- Gilbert Cell Based Topology.
- Variable Gain via Vro.
- Cascode stage to isolate input stage from the Local Osc.



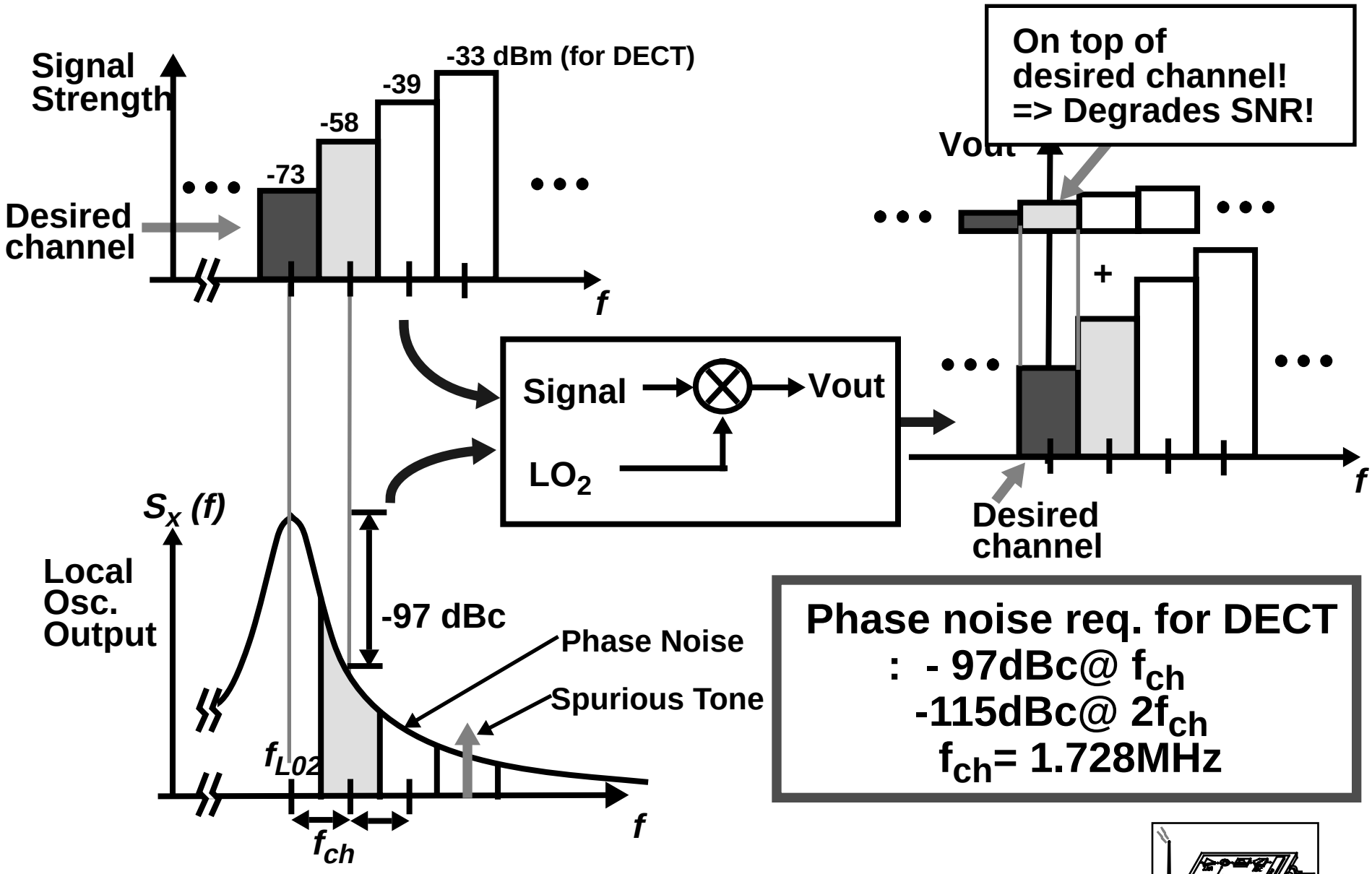
IP_3 : 10dBm.

Variable Gain : 10dB ~ 35dB

Image-Rejection: ~35dB

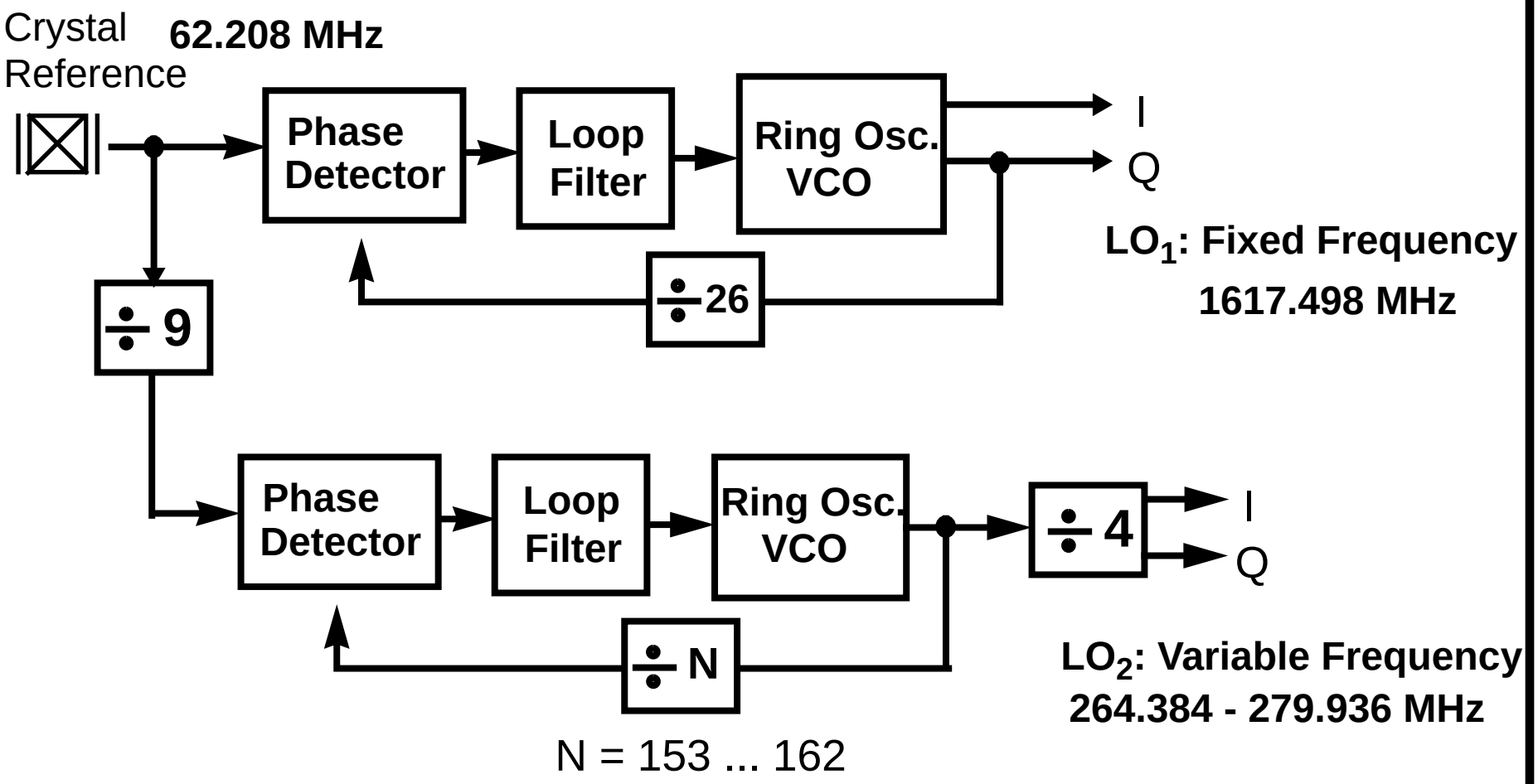
Total Power : 40mW

Freq. Synthesizer(I): Phase Noise Req.



Phase noise req. for DECT
: - 97dBc@ f_{ch}
-115dBc@ $2f_{ch}$
f_{ch}= 1.728MHz

Freq. Synthesizer(II): for DECT

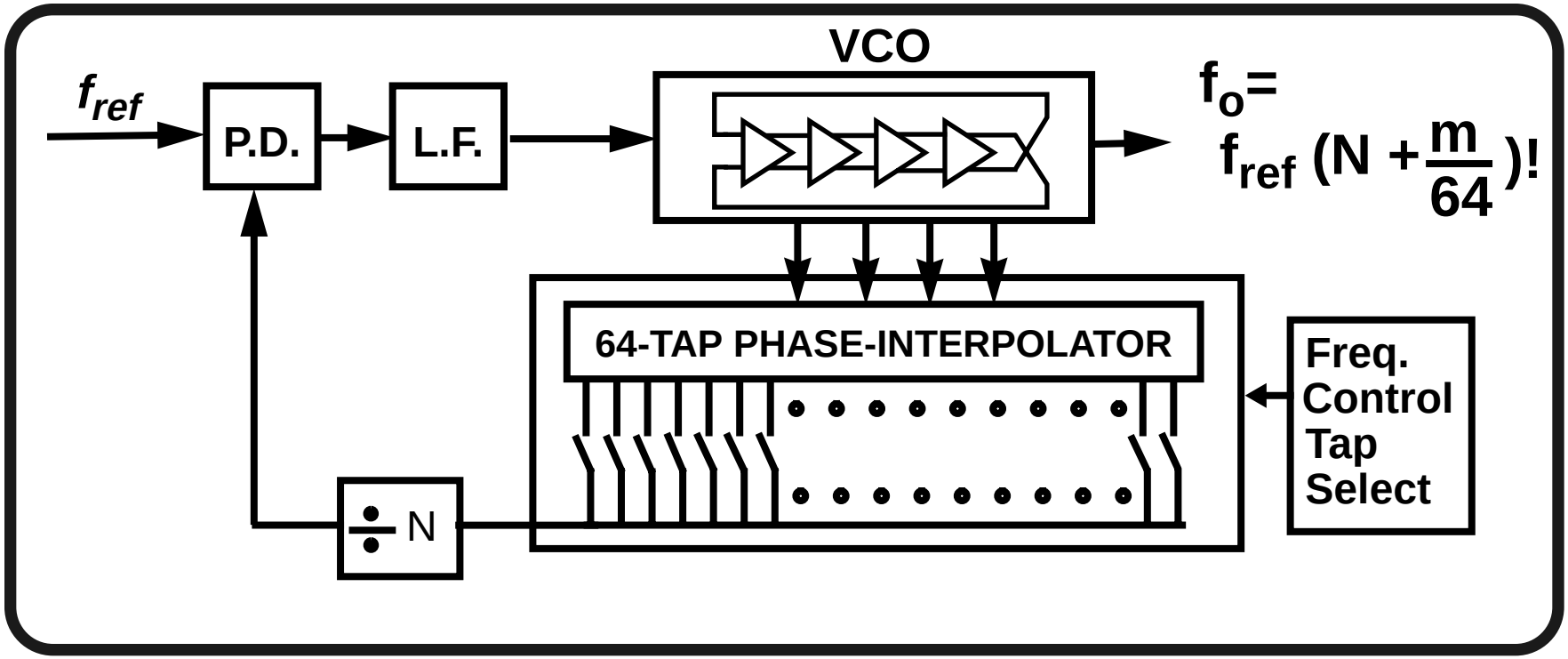


DECT Channel Spacing = 1.728 MHz

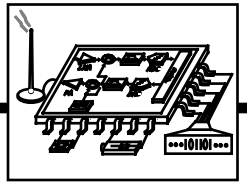
Freq. Synthesizer(III): for Multistandard

Channel Spacing : **DECT** **1.728 MHz**

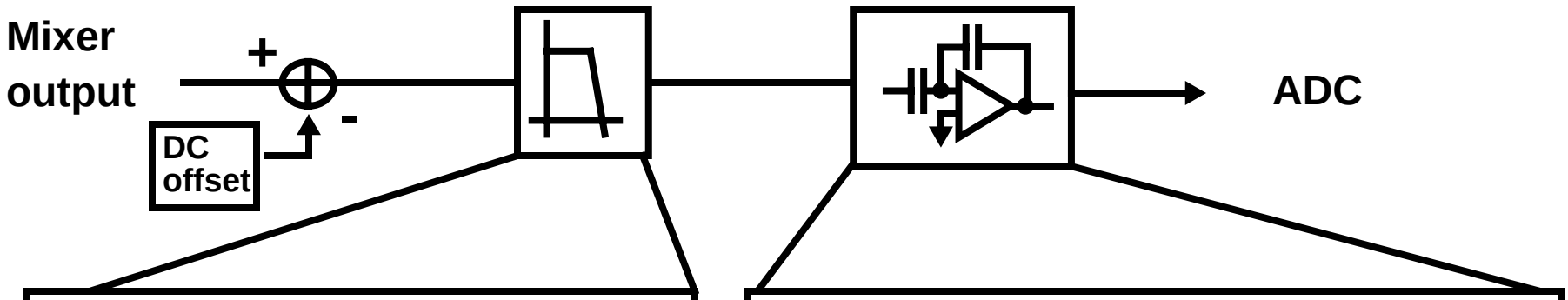
Other Standards (FDMA) **10 KHz, 30 KHz, 200 KHz**



- ***PHASE INTERPOLATED FREQ. SYNTHESIZER*** **for finer channel spacings while maintaining high ref. freq. and high PLL bandwidth.**



Baseband Filter/Gain Stage



- **Anti-aliasing Filter:**

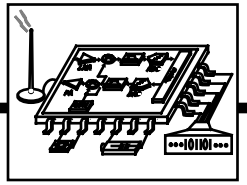
Sallen-Key continuous-time LPF

- Out-of-DECT-Band signal rejection
- BW= ~2MHz
- ~ 4-5th order
- DC offset correction

- **Channel Selection Filter:**

Switched capacitor sampled-data LPF + Gain

- Adjacent channel rejection
- constant group delay
- BW = ~ $f_{data}/2$
- 6th order(fs=18x) + 3rd order Phase eq.

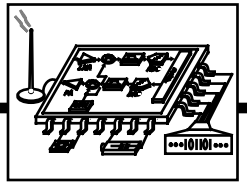


A/D Converter

A 10-bit 20MS/s 35mW Pipeline ADC*

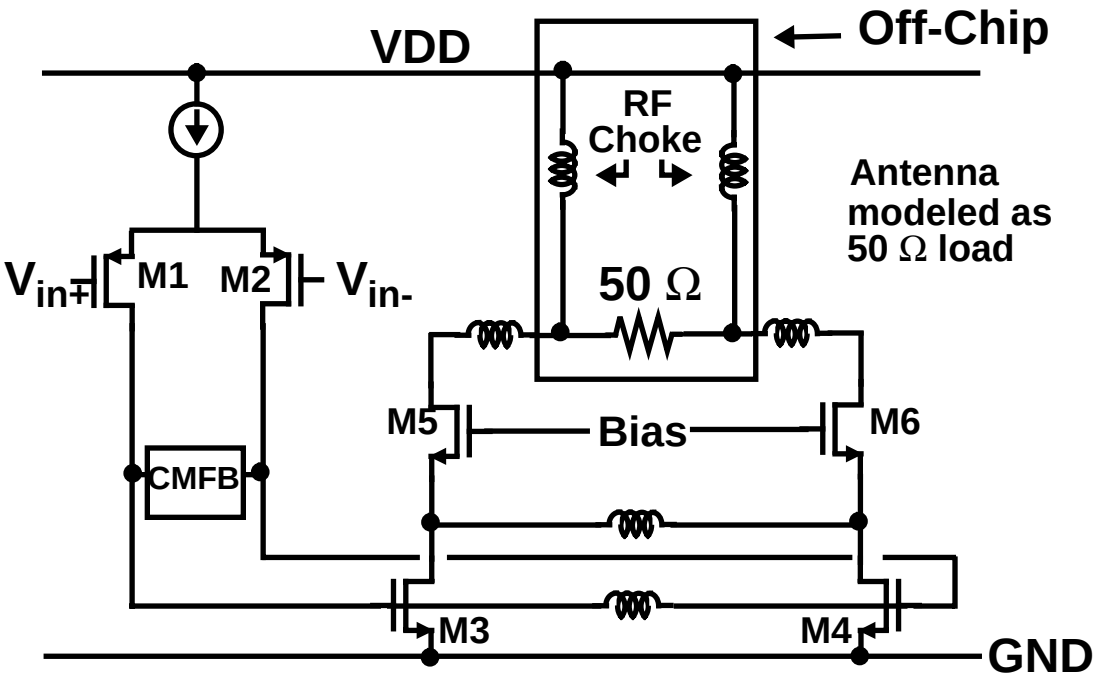
The Next Generation of 10 bit 20MS/s CMOS ADC		
Tech	1.2μm	0.6 or 0.8 μm
Vdd	3.3V	3.3V
Active Area	3.2x3.3 mm^2	~1.5x1.5 mm^2
Power	35mW @ 20MS/s	~10mW @ 20MS/s

*:T. Cho & P. Gray
@CICC 94, San Diego



RF Power Amplifier

- A two-stage differential-mode amplifier
- On-chip spiral inductors for tuning out gate capacitance and output impedance matching
- Require power control

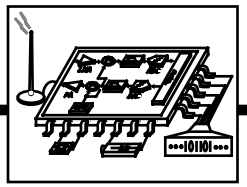


Output Power:

250mW@1.9GHz

Efficiency: > 30%

Tech: 0.6 μm CMOS



Future Plan

- **Tape out 1st version : Spring, 1995**

  - **Individual blocks**
  - **The whole receiver channel**

- **Testing/Evaluation : Summer, 1995**

- **Tape out 2nd version : Winter, 1995**

  - **Both receiver/transmitter channels**