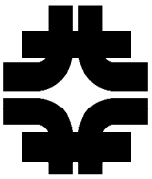

Fermi National Accelerator Laboratory

Silicon Strip Detector

TEN BITS DIFFERENTIAL TRANSCEIVER (0.25μm)

Document # ESE-SVX-020502

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1. GENERAL INFORMATION

The ten bits transceiver chip is being fabricated at Mosis using the TSMC 0.25 micros Cmos process. The die size is 2.52mm x 2.88mm. Figure 1 shows the configuration of the chip. It shows ten bits transceiver on the left hand side and shows just one bit transceiver gate on the right hand side. It contains both transmitter and receiver units. Each differential transceiver gate is formed by two units:

a) One is transmitter, with differential inputs B and B* and differential outputs A and A* or one can choose single ended output A. The outputs can be tri-state using the control line ESA for single ended output or EDA for differential outputs.
b) Other is a differential receiver, with inputs A and A* and differential outputs B and B*. The output of the receiver can be tri-state using the control line EDB.

In this document, the word "transmitter" is referring to transmitter unit of the transceiver and "receiver" is referring to the receiver unit of the transceiver. The transceiver chip has capability to take Low Current Differential Signals (LCDS) which defines the characteristics of the differential signals in the A 0 – A9 and A0* - A9* line of the transmitter and receiver. The receiver responds to differential input voltage from 200 mV to supply voltage. The output is able to drive a 50 pF load and a 500 ohm load to ground.

The transceiver is composed of ten transceiver gates controllable by enable control lines EDA, ESA, and EDB which enable differential transmitter A, single ended transmitter A, and differential transmitter B, respectively. Table 1 shows the truth table of the enable control lines.

The VBB signal is a reference voltage used to transform the differential inputs into single ended inputs. The signal VBB is an internal voltage divider, which is set to about 1.4 volt.

Table 2 shows the truth table of the current control line. The output current can be controlled by signals OCA and OCB. One can program the current to be 4 mA, 8 mA, 12 mA, or 16 mA by selecting OCA and OCB signals.

		Operation
EDA	High	Enables differential driver A
	Low	High Z differential driver A
ESA	High	Enables s.e. driver A
	Low	High Z s.e. driver A
EDB	High	High Z differential driver B
	Low	Enables differential driver B

Table 1 – Truth Table for Enable Control Lines

OCA	OCB	Output Current
0	0	4 mA
0	1	8 mA
1	0	12 mA
1	1	16 mA

Table 2. Truth Table for the Current Control Line

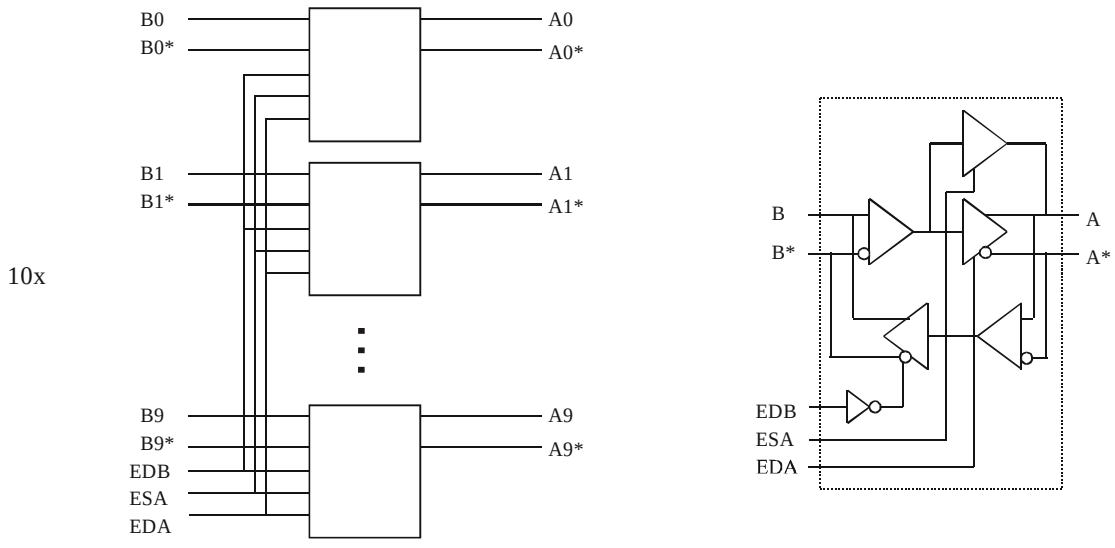
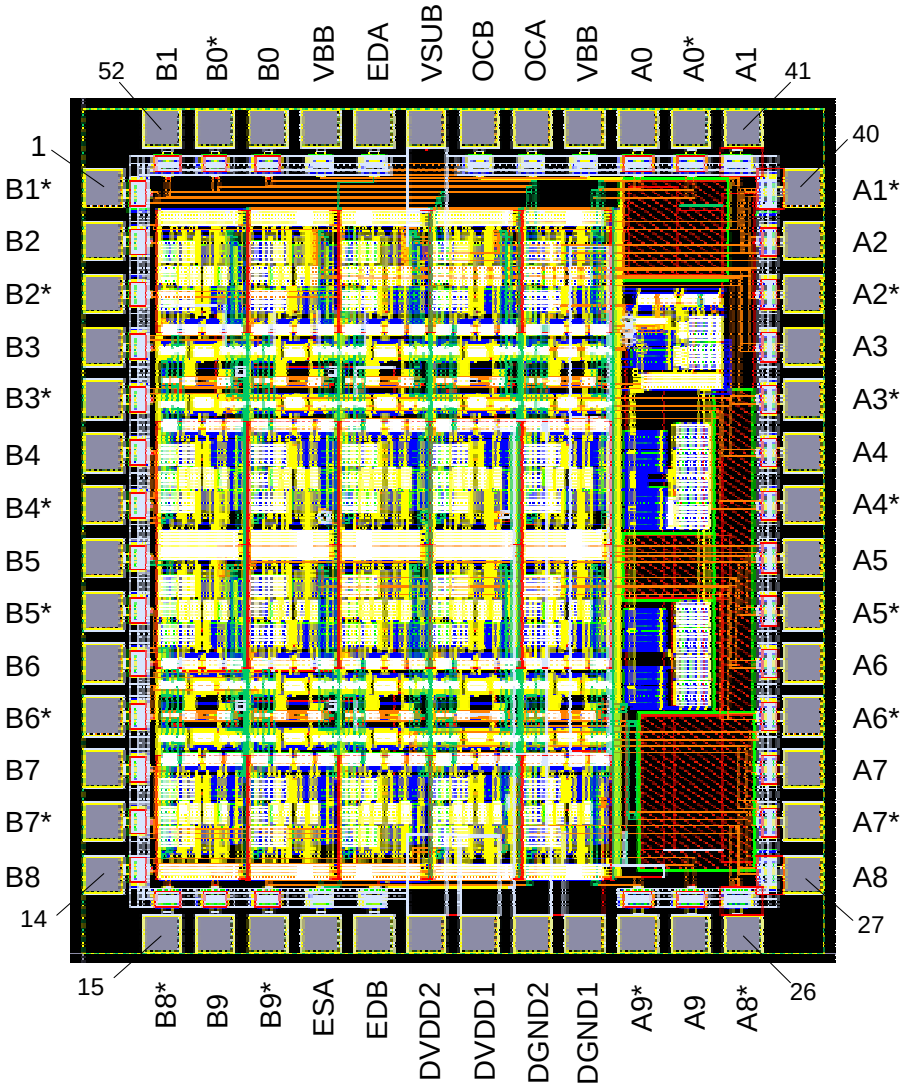


Figure 1 – Transceiver Chip

Transceiver Chip Pinout

(Drawing **NOT** to Scale)



Transceiver die size: 2.52mm x 2.88mm
Die bond pad size: 135 micrometers x 135 micrometers
Die bond pad pitch: 180 micrometers
Supply Voltages: 2.25V - 2.75V
Max. Supply Voltage: 2.75V

Pad Number	Pad Name	Description
1	B1*	Complement bit 1 differential input to transmitter/output from receiver
2	B2	Bit 2 differential input to transmitter/output from receiver
3	B2*	Complement bit 2 differential input to transmitter/output from receiver
4	B3	Bit 3 differential input to transmitter/output from receiver
5	B3*	Complement bit 3 differential input to transmitter/output from receiver
6	B4	Bit 4 differential input to transmitter/output from receiver
7	B4*	Complement bit 4 differential input to transmitter/output from receiver
8	B5	Bit 5 differential input to transmitter/output from receiver
9	B5*	Complement bit 5 differential input to transmitter/output from receiver
10	B6	Bit 6 differential input to transmitter/output from receiver
11	B6*	Complement bit 6 differential input to transmitter/output from receiver
12	B7	Bit 7 differential input to transmitter/output from receiver
13	B7*	Complement bit 7 differential input to transmitter/output from receiver
14	B8	Bit 8 differential input to transmitter/output from receiver
15	B8*	Complement bit 8 differential input to transmitter/output from receiver
16	B9	Bit 9 differential input to transmitter/output from receiver
17	B9*	Complement bit 9 differential input to transmitter/output from receiver
18	ESA	Enable single ended drivers A
19	EDB	Enable differential drivers B
20	DVDD2	Drivers 2.5V power supply
21	DVDD1	Drivers 2.5V power supply
22	DGND2	Drivers ground
23	DGND1	Drivers ground
24	A9*	Complement bit 9 differential transmitter and receiver function and output from s.e. transmitter
25	A9	Bit 9 differential output from transmitter/input to receiver
26	A8*	Complement bit 8 differential transmitter and receiver function and output from s.e. transmitter
27	A8	Bit 8 differential output from transmitter/input to receiver
28	A7*	Complement bit 7 differential transmitter and receiver function and output from s.e. transmitter
29	A7	Bit 7 differential output from transmitter/input to receiver
30	A6*	Complement bit 6 differential transmitter and receiver function and output from s.e. transmitter
31	A6	Bit 6 differential output from transmitter/input to receiver
32	A5*	Complement bit 5 differential transmitter and receiver function and output from s.e. transmitter
33	A5	Bit 5 differential output from transmitter/input to receiver
34	A4*	Complement bit 4 differential transmitter and receiver function and output from s.e. transmitter
35	A4	Bit 4 differential output from transmitter/input to receiver
36	A3*	Complement bit 3 differential transmitter and receiver function and output from s.e. transmitter

37	A3	Bit 3 differential output from transmitter/input to receiver
38	A2*	Complement bit 2 differential transmitter and receiver function and output from s.e. transmitter
39	A2	Bit 2 differential output from transmitter/input to receiver
40	A1*	Complement bit 1 differential transmitter and receiver function and output from s.e. transmitter
41	A1	Bit 1 differential output from transmitter/input to receiver
42	A0*	Complement bit 0 differential transmitter and receiver function and output from s.e. transmitter
43	A0	Bit 0 differential output from transmitter/input to receiver
44	VBB	Reference voltage 1.25V
45	OCA	Programmable resistors to adjust the differential output current of the Differential transmitter. They are internally pulled up.
46	OCB	
47	VSUB	Substrate voltage (ground)
48	EDA	Enable differential drivers A
49	VBB	Reference voltage 1.25V
50	B0	Bit 0 differential input to transmitter/output from receiver
51	B0*	Complement bit 0 differential input to transmitter/output from receiver
52	B1	Bit 1 differential input to transmitter/output from receiver

Table 3 – Transceiver Pad Description

2. CHIP SPECIFICATIONS

General:	
Bonding pad pitch:	180 μm
Pad size:	130x130 μm^2
Overall length (pad to pad):	~2.52mm
Overall width (pad to pad):	~2.88mm
Supply voltages:	2.25-2.75
Maximum supply voltage:	2.75V
Output Differential Driver:	
Current source range:	4mA to 17.5mA (2 bit adjust)
Rise and fall times:	>2ns and <4ns with nominal load
Common mode:	VDD/2 nominal with T termination
Load capability:	to be simulated with the model of the circuit
Output data skew:	>1ns between any two bus lines
Output data symmetry:	The differential signals should be as symmetric as possible, such that the cross happens at 50% of the voltage swing. See fig. **Error! Reference source not found.**
Single Ended Output Driver:	
Output current (sink and source):	25mA

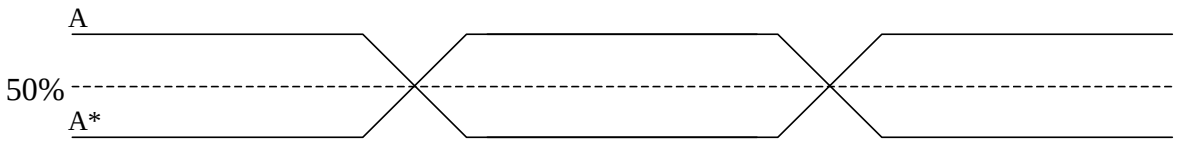
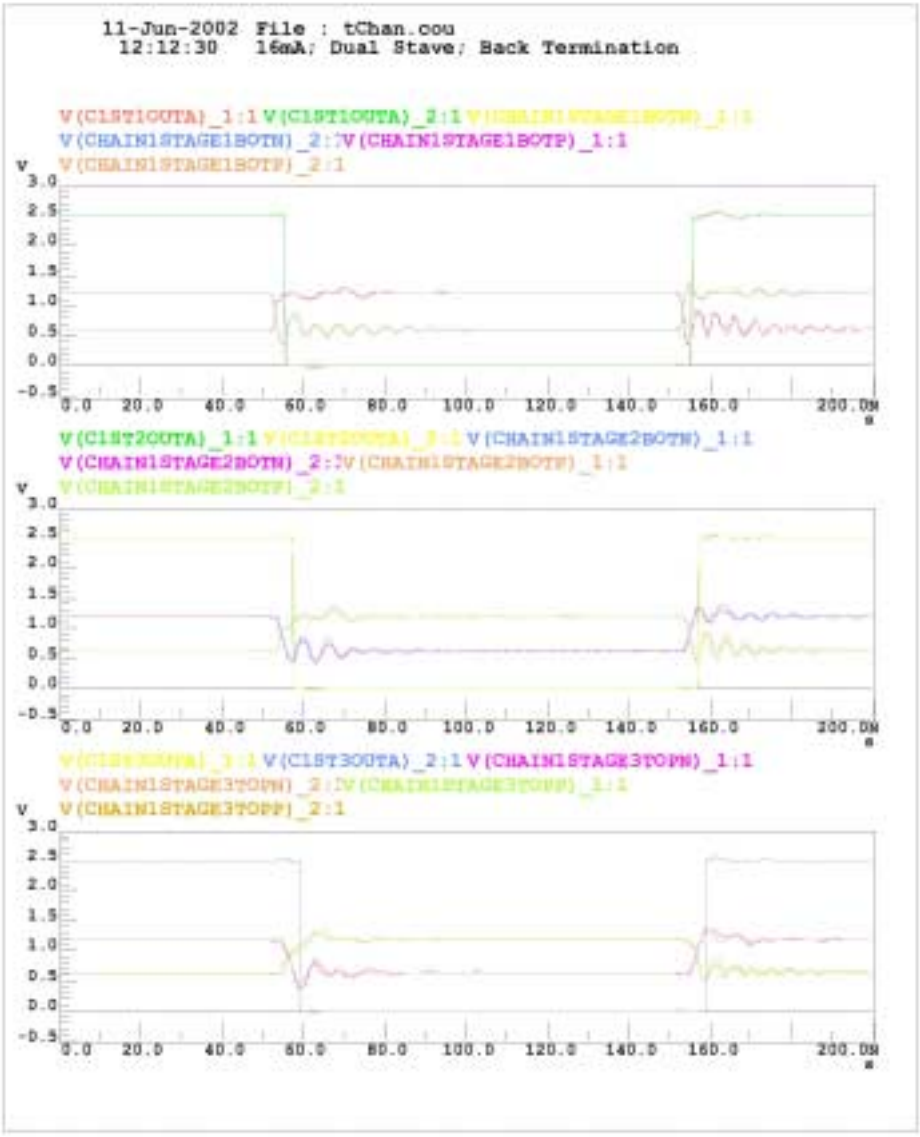
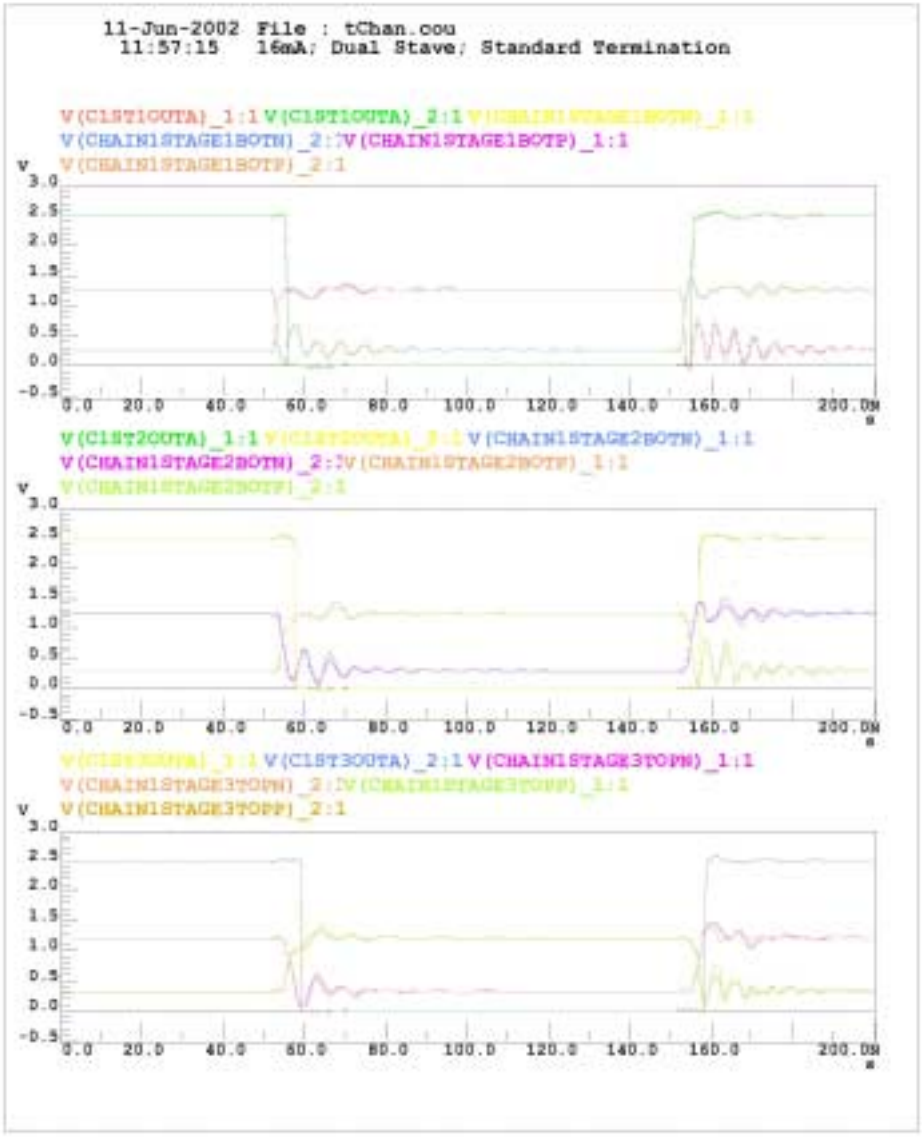


Figure 2

3. SIMULATIONS


11-Jun-2002 File : tChan.cou
12:12:30 16mA; Dual Stave; Back Termination
V(C1ST1OUTA)_1:1 V(C1ST1OUTA)_2:1
V(CHAIN1STAGE1BOTN)_2:?V(CHAIN1STAGE1BOTP)_1:1
V(CHAIN1STAGE1BOTP)_2:1
V
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0.0 20.0 40.0 60.0 80.0 100.0 120.0 140.0 160.0 200.0n
s
V(C1ST2OUTA)_1:1
V(CHAIN1STAGE2BOTN)_2:?V(CHAIN1STAGE2BOTP)_1:1
V
V(C1ST3OUTA)_2:1 V(CHAIN1STAGE3TOPN)_1:1
V(CHAIN1STAGE3TOPN)_2:?V(CHAIN1STAGE3TOPP)_1:1
V(CHAIN1STAGE3TOPP)_2:1
V


11-Jun-2002 File : tChan.cou
11:57:15 16mA; Dual Stave; Standard Termination
V(C1ST1OUTA)_1:1 V(C1ST1OUTA)_2:1
V(CHAIN1STAGE1BOTN)_2:?V(CHAIN1STAGE1BOTP)_1:1
V(CHAIN1STAGE1BOTP)_2:1
V
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0.0 20.0 40.0 60.0 80.0 100.0 120.0 140.0 160.0 200.0n
s
V(C1ST2OUTA)_1:1 V(CHAIN1STAGE2BOTN)_1:1
V(CHAIN1STAGE2BOTN)_2:?V(CHAIN1STAGE2BOTP)_1:1
V(CHAIN1STAGE2BOTP)_2:1
V
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0.0 20.0 40.0 60.0 80.0 100.0 120.0 140.0 160.0 200.0n
s
V(C1ST3OUTA)_2:1 V(CHAIN1STAGE3TOPN)_1:1
V(CHAIN1STAGE3TOPN)_2:?V(CHAIN1STAGE3TOPP)_1:1
V(CHAIN1STAGE3TOPP)_2:1
V
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0.0 20.0 40.0 60.0 80.0 100.0 120.0 140.0 160.0 200.0n
s